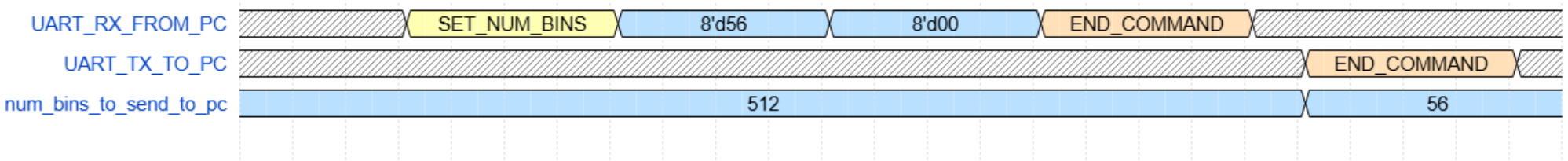
UART TRANSFER HANDSHAKE PROTOCOL

COMMAND	BITS	PURPOSE
END_COMMAND	1111_1111	To end the command/ data transfer to/ from FPGA.
START_HISTOGRAM	0000_0010	To start the histogram capture process on the FPGA.
STOP_HISTOGRAM	0000_0011	To stop the histogram capture process on the FPGA.
CLEAR_RESULTS	0000_0100	To clear the histogram data on the FPGA.
START_UPLOAD	0000_0101	To start the histogram data transfer from FPGA to PC for the requested settings.
SET_BASE_ADDRESS	0000_0110	To set the starting address for data upload to the PC.
SET_NUM_BINS	0000_0111	To set the number of bins for data upload to the PC.

Configure Settings

Number of bins can vary from [1 – 512]. Since 10 bits are required to configure the number of bins to all the values in this range, 2 UART byte transfers are needed. The format is:

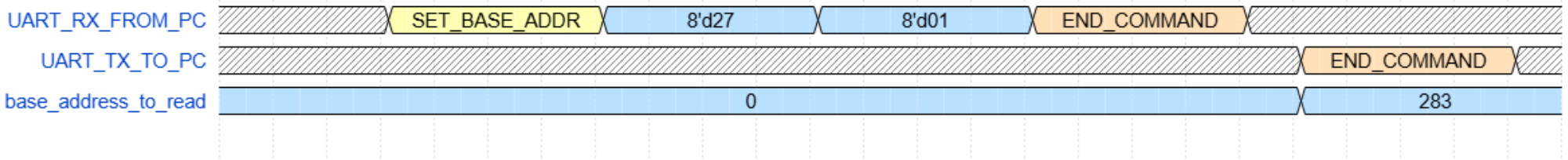
<SET_NUM_BINS> | <BYTE_LSB[7:0]> | <BYTE_MSB[15:8]> | <END_COMMAND>



Example timing diagram: To set “number of bins to read” to 56.

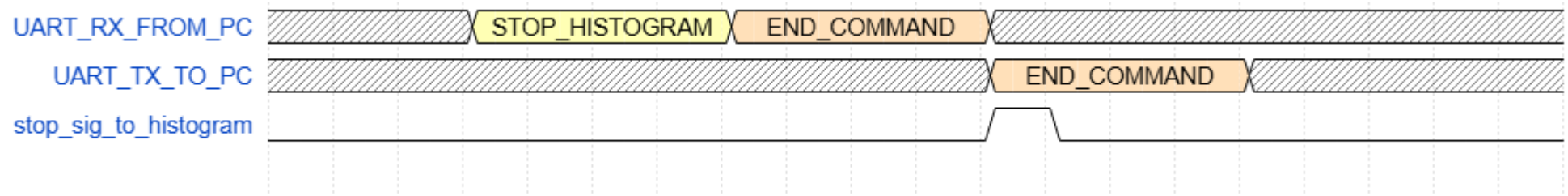
Histogram start address can vary from [0 – 511]. Since 9 bits are required to configure the address to all the values in this range, 2 UART byte transfers are needed. The format is:

<SET_BASE_ADDR> | <ADDR_BYTE_LSB[7:0]> | < ADDR_BYTE_MSB[15:8]> | <END_COMMAND>



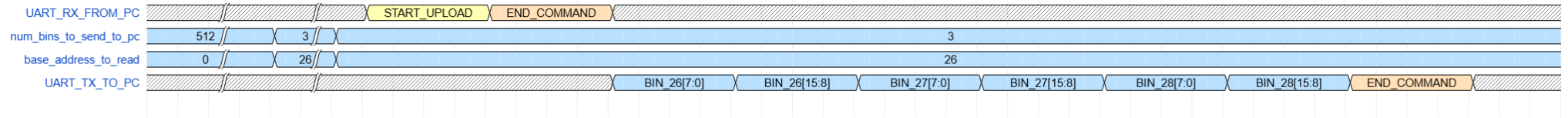
Example timing diagram: To set “starting bin address” to 283. The 2 bytes are 00011011 (8’d27) and 00000001 (8’d01).

Trigger Control Signals



Example timing diagram: To set “stop histogram control signal” to true. This stops the histogram computation process on the FPGA.

Start Histogram Data Capture



Example timing diagram: To start the data transfer of histogram data from the FPGA to the PC. Other points to note:

1. Configure any settings prior to sending the command (for ex: number of bins to read, starting bin address).
2. The FPGA responds back in the format:

<BIN_0_BYTE_LSB> | <BIN_0_BYTE_MSB> | <BIN_1_BYTE_LSB> | <BIN_1_BYTE_MSB> | … | <END_COMMAND>