Design and implementation of Half Subtractor

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Abstract

This reference paper proposes the design of a half subtractor.Subtractor Is a digital circuit that performs subtraction of two numbers. It has two inputs and two outputs. This circuit is employed to subtract two single bit binary numbers A and B.In many computers and other kinds of device processors, subtractors are used in ALU operations and are also frequently used in other parts of the processor.Depending upon the application of the device or upon the purpose of the application to be performed, the inputs to the circuit device may vary from two to 3. We could possibly use a Half-Subtractor if there are two inputs while for 3 inputs, a Full-Subtractor may be used.

1. Reference circuit Details

The 1-bit half subtractor accepts two binary inputs A and B and produces the output D(difference) and Bo(borrow).CMOS logic consists of one pullup and pulldown network .The pullup network consists of pmos whereas the pull down network consists of nmos. The circuit has mainly an inverter for obtaining the inverted input and an AND gate which is used to design the borrow and an XOR gate is used to generate the difference output.

The AND gate is implemented using CMOS design with 2 pmos in series and two nmos in parallel.Similarly the XOR gate is also realized using CMOS design with four pmos and four n-mos transistors in the pullup and pull down network respectively.

The proposed design can have four possible combinations of inputs and corresponding four outputs of difference and borrow respectively.The input combinations are 00,01.10 and 11 .The borrow output is only high when A is 0 and B is logic 1.The output of the difference is same as the output of the Xor gate.

2. Reference Circuit

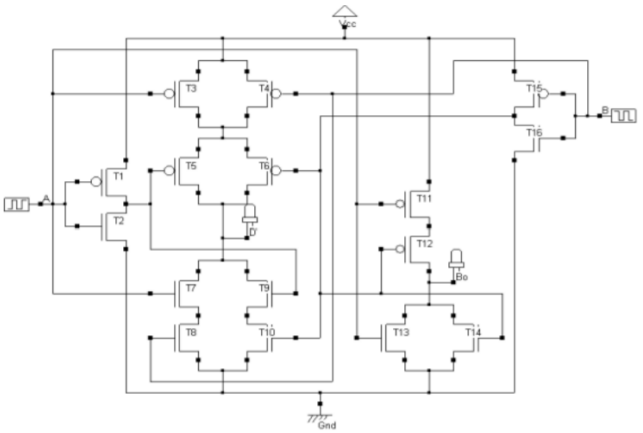

Fig-1: Half subtractor schematic (Referred from Reference Paper [1])

3. Reference Circuit Waveforms

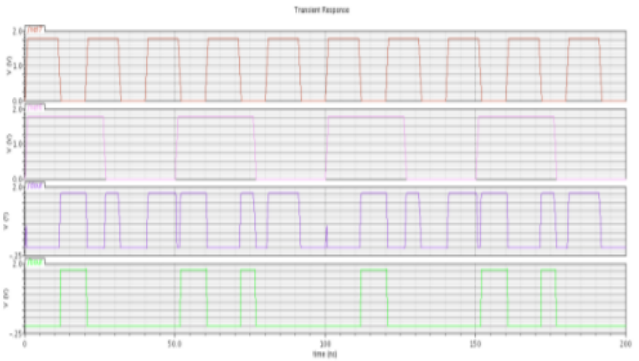

Fig-2: Simulation result of half subtractor (Referred from Reference paper [2])

References

[1] Tanvi Sood,Rajesh Mehra(2013) Design of a low power half subtractor using 90um cmos technology .IOSR Journal of VLSI and Signal Processing.https://www.iosrjournals.org/iosr-jvlsi/papers/vol2-issue3/H0235156

[2] Monikashree T.S, Divya A, Kithara V, Nithya Shree S,Area efficient Full Subtractor design using CMOS Technology.ITSI Transactions on Electrical and Electronics Engineering (ITSI-TEEE)