

VISVESVARAYA TECHNOLOGICAL UNIVERSITY

Jnana Sangama, Machhe, Belgaum-590018, Karnataka.



A Dissertation Report on

**DESIGN AND VERIFICATION OF DDR SDRAM MEMORY
CONTROLLER USING SYSTEMVERILOG FOR HIGHER COVERAGE**

Submitted in partial fulfillment of the requirement for the award of the degree of

**MASTER OF TECHNOLOGY
in
VLSI DESIGN AND EMBEDDED SYSTEMS**

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CERTIFICATE

This is to certify that the project work entitled “**Design and Verification of DDR SDRAM Memory Controller Using SystemVerilog For Higher Coverage**” has been successfully carried out by **Mr. Pavan Kumar M P.** bearing the USN: **1BG17LVS05** a bonafide student of BNM Institute of Technology, Bengaluru in partial fulfillment for the **Master of Technology in VLSI Design and Embedded Systems** of the **Visvesvaraya Technological University, Belagavi** during the year **2018-2019**. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the project report deposited at the department library. The project report has been approved as it satisfies the academic requirements in respect to project work prescribed for the said Degree.

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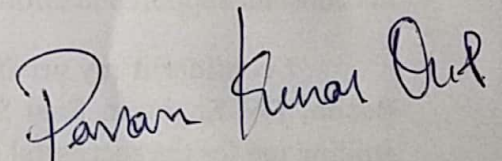
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DECLARATION

I, the undersigned solemnly declare that the report of the project "**Design and Verification DDR SDRAM memory controller using SystemVerilog for higher coverage**" is based on my work carried out during the course study under the supervision of **Dr. Subodh Kumar Panda**, Associate professor, Department of ECE, BNM Institute of Technology, Bangalore and the industry guide **Mr. Shaik Chand Basha**, DV Engineer, **SION Semiconductor Pvt. Ltd**, 3rd Floor, P.N. Plaza, Lane Beside Staples, Munnekolala Main Road, SGR Dental College Rd, Chandra Layout, Marathahalli, Bengaluru, Karnataka 560037. I assert that the statements made and conclusions drawn are an outcome of the project. I further declare that, to the best of my knowledge and belief, that this report does not contain any work which has been submitted for the award of the degree or any other degree in this university or any other university.



PAVAN KUMAR M P

ACKNOWLEDGEMENT

On successful completion of this project, I would like to place on record my sincere thanks and gratitude to the concerned people, whose suggestions and words of encouragement has been valuable.

I would like to express my heartfelt gratitude to **B.N.M. Institute of Technology**, for giving me the opportunity to pursue Degree in Master of Technology. I take this opportunity to thank **Prof. T. J. Rama Murthy**, Director, BNMIT, **Prof. Eishwar M. Mannay**, Dean, BNMIT and **Dr. Krishnamurthy G. N**, Principal, BNMIT for their support and encouragement to pursue this project.

I would like to thank **Dr. P. A. Vijaya**, Professor and Head, Dept. of Electronics and Communication Engineering, for her support and encouragement.

I would like to thank PG co-coordinator **Dr. Yasha Jyothi M. Shirur**, Professor, Dept. of Electronics and Communication Engineering, for her support and encouragement.

I would like to thank my guide **Dr. Subodh Kumar Panda**, Associate Professor, Dept. of Electronics and Communication Engineering, who has been the source of inspiration throughout my project work and has provided me guidance and valuable suggestions at every stage of my project work.

Finally, I am grateful to all the teaching and non-teaching staff of Department of Electronics and Communication for their help in the successful completion of my project. Last but not the least I would like to extend sincere gratitude to my parents and all my friends who were a constant support throughout my project work.

PAVAN KUMAR M P

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ABSTRACT

Synchronous Dynamic Random-Access Memory (SDRAM) has become a mainstream memory of choice in any design due to its speed, burst access and pipeline features. For high end applications processors, the interface to the SDRAM is supported by the processor's built-in peripheral module. However, for other applications, the system designer must design a memory controller to provide proper commands for SDRAM initialization, read/write accesses and memory refresh. DDR SDRAM uses double data rate architecture to achieve high-speed data transfers. DDR SDRAM (referred to as DDR1) transfers data on both the rising and falling edge of the clock. The proposed DDR controller is interface between the DDR memory and processor. The DDR is designed using Verilog HDL, functional verification carried out using Modelsim 6.4b and Xilinx ISE 9.2 synthesizer used for synthesis. Functional coverage is carried out using SystemVerilog, QuestaSim tool. Random combinational patterns are applied to the memory banks and it will cover all the combinations. In this proposed work, it is mainly focused on getting higher coverage, which may result in 100% coverage using Questasim tool.

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