Pavan Kumar M P

Location: International Dormitory, NSYSU, Kaohsiung Taiwan, 80424
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RESEARCH INTEREST

Machine Learning, Transfer Learning Algorithms, Unsupervised Domain Adaptation, SF-UDA, Predictive Maintenance, RTL Design and Verification.

EDUCATION (Ph.D. Ongoing)

National Sun- Yat-Sen University, Kaohsiung, Taiwan (*Ongoing*) 2020/10 – 2024/06
Ph.D., Computer Science Engineering, GPA: 3.71/4.3 Advisor: Prof. Kun-Chih Chen

BNM Institute of Technology, Bangalore, India 2017/08 – 2019/08
Master of Technology., VLSI Design, GPA: 8.9/10 Advisor: Prof. Subodh Kumar
Thesis: Design and verification of DDR SDRAM memory controller for higher coverage

Visvesvaraya Technological University, India 2012/08 – 2016/08
Bachelor of Engineering., Electronics and Communication, GPA: 8/10

INDUSTRIAL EXPERIENCES

國家高速網路與計算中心 (NCHC) 2023/09/01 -2024/05/07
Research Intern, Tainan, Taiwan
During my internship at NCHC, I am focusing on the development of Physics Informed Neural Networks (PINNs), with the objective of establishing a user-friendly computing platform for PINN applications.

Sierra Circuits Ind Pvt Ltd 2016/10 -2020/10
PCB Tech Engineer, Bangalore, India
I worked in an American-based PCB manufacturing company. My Responsibilities include 1) Printed circuit board specification analysis; 2) Providing the PCB information to the clients; 3) Cooperation with the design team for manufacturing capabilities.

Sion Semiconductors Pvt Ltd 2018/10 – 2019/04
SoC Design Verification Engineer Intern, Bangalore, India *Supervisor: Chand Basha*
I worked on the DDR SDRAM memory controller design and verification. Verilog-based coding for design and system Verilog coding for verification and for higher coverage.

PUBLICATIONS

Journal/Transaction papers:

1. **P. Kumar Mp,** Z. -J. Gao and K. -C. Chen, "Time Series-Based Sensor Selection and Lightweight Neural Architecture Search for RUL Estimation in Future Industry 4.0," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 13, no. 2, pp. 514-523, June 2023, doi: 10.1109/JETCAS.2023.3248642. **(**link**)**
2. **Pavan Kumar MP**, Jing-Wen Liang, and Kun-Chih (Jimmy) Chen, "Neural Network-based Anomaly Detection Architecture for Industry Motor System", IEEE TIM, 2024 (Submitted)
3. **Pavan Kumar MP** and Kun-Chih (Jimmy) Chen, "Mitigating Negative Transfer Learning In Source-Free Unsupervised Domain Adaptation for Rotating Machinery Fault Diagnosis", IEEE TIM, 2024 (Submitted)

Conference Papers:

1. **P. Kumar M.P**. and S. K. Panda, "Design and Verification of DDR SDRAM Memory Controller Using SystemVerilog For Higher Coverage," 2019 International Conference on Intelligent Computing and Control Systems (ICCS), Madurai, India,2019, pp.689-694,doi:10.1109/ICCS45141.2019.9065407. (link)
2. **M. Pavan Kumar**, C. -J. Tang and K. -C. J. Chen, "Composite Fault Diagnosis of Rotating Machinery With Collaborative Learning," 2022 International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, 2022, pp. 1-4, doi: 10.1109/VLSI-DAT54769.2022.9768050. (link)

3. **Pavan Kumar MP** and Kun-Chih (Jimmy) Chen, "Bearing Fault Diagnosis by Using Exponential Power Entropy and a Decision Threshold for Artificial Neural Network," Proc. 2022 VLSI Design/CAD Symposium, Aug. 2022.
4. **P. K. MP** and K. -C. Jimmy Chen, "NN-based Bearing Fault Diagnosis Using Exponential Power Entropy and a Decision Threshold," 2023 IEEE International Conference on Omni-layer Intelligent Systems (COINS), Berlin, Germany, 2023, pp. 1-5, doi: 10.1109/COINS57856.2023.10189273. **(**link**)**
5. **P. K. MP** and K. -C. J. Chen, "Mitigate the Negative TL using Adaptive Thresholding for Fault Diagnosis," 2023 IEEE International Conference on Omni-layer Intelligent Systems (COINS), Berlin, Germany, 2023, pp. 1-6, doi: 10.1109/COINS57856.2023.10189313. (link)
6. **Pavan Kumar MP,** Zhe-Xiang Tu, and Kun-Chih (Jimmy) Chen, "Fine-Tuned Based Transfer Learning with Temporal Attention and Physics-Informed Loss," to be appeared in IEEE International Conference on Artificial Intelligence Circuits and Systems (IEEE AICAS'24), Apr. 2024.

PERSONAL

Skills: *Python, C, Verilog, SystemVerilog*
Hobbies: *Motorcycle Racing, Gym, LinkedIn.*