Pavan Umesh

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EDUCATION

Northeastern University, Boston, MA. **GPA- 3.77** May 2025
Master of Science in Electrical and Computer Engineering
Coursework: Analog IC Design, Computer Architecture, VLSI Design, Semiconductor Packaging, Micro and Nanofabrication, Solid State Devices, Wireless Sensor Networks and IoT.

SJC Institute of Technology, Bengaluru, KA, India. **CGPA: - 8.02/10** June 2023
Bachelor's degree in Electronics & Communication Engineering
Coursework: Embedded Systems, Real-time Systems, Digital Signal Processing, electrical systems, Semiconductor device physics, VLSI fundamentals.

SKILLS

Programming language: C++, TCL, Python, Verilog, VHDL, Bash. **OS**:- Windows, Linux.

Software: Cadence Allegro, Virtuoso, Tempus, Comsol, LabVIEW, Xilinx Vivado, Arduino,Git, TCAD, HSpice.

Laboratory Instruments:- Oscilloscope, Network Analyzer, Function generator, Multimeter.

PROFESSIONAL EXPERIENCE

Graduate Teaching Assistant, **Northeastern University,** Boston, MA, USA Sept 2024 - Present
- Facilitated courses on electronic materials and electromechanical systems, emphasizing experimental setups and material characterization. Created engaging course materials to support student learning.
- Conducted problem-solving sessions and hands-on lab exercises to reinforce theoretical concepts.

Intern, **Infonex Technologies,** Mysore, KA, India. July – Dec 2022
- Designing Circuit of Automated circuit testing setups, boosting efficiency by 30% with LabVIEW and NI hardware, Optimized EV battery production lines, reducing cycle times by 20% and defects by 15%.
- Improved scalability and reliability in testing processes for high-volume manufacturing.

Intern, **Nano-Technology Lab, VTU Research Center,** Muddenahalli, India**.** Jan – June 2022
- Characterized 10+ materials samples using XRD and SEM, enhancing battery efficiency by 12%.
- Improved material sustainability and performance by 10% through rigorous testing and optimization.

PROJECTS

Design and implementation of a Low Dropout Regulator, Northeastern University. Feb 2025
- Developed and generated low noise, high PSRR LDO in Cadence Virtuoso with dropout voltage of 70mV.
- Analyzed the circuit for LDO performance and reliability parameters using ADE L simulations.

Design of 16-bit Multiplier, Northeastern University. Jan 2025
- Implemented a 16-bit multiplier circuit in cadence virtuoso, achieving functionality and efficiency.
- Analyzed power, area, and performance, achieving a low-power multiplier with high propagation delay.

STA on Rocket core, Northeastern University. Dec 2024
- Resolved setup and hold violations with Tempus, reducing path delay by 15% and improving slack by 20%.
- Performed MMMC analysis, optimizing critical paths through buffer insertion, reducing power by 10%.

Dynamic Scheduling Optimization in gem5, Northeastern University. Sept-Nov 2024
- Implemented multi-instruction commitment and aggressive speculative execution to enhance performance.
- Improved instruction-level parallelism, reducing pipeline stalls and optimizing cache efficiency. Achieved a 50% reduction in simulated time through benchmark analysis.

741 Operational Amplifier, Northeastern University. Sept – Dec 2024
- Designed 741 OPamp using BJT, simulated it, carried out DC and small signal circuit analysis in Virtuoso.
- Plotted gain and phase, calculated and compared frequency response and rejection ratios parameters.

SOT-MRAM, Northeastern University. Jan – March 2023
- Researched SOT-MRAM and its advantage over other RAMs to minimize the size and power consumption.
- Researched RAM functionality, analyzed M-RAM drawbacks, and explored improvements.