



December - 2023

Programme : B.E / B.Tech
Course Code : CSA12
Course Name : Computer Architecture
Duration : 3 Hrs.

Max Marks: 100

Answer all the Questions

- 1/ Describe the primary functionalities of stacks and queues, and provide an (10) (CO1) (BL2) explanation for each operation
- 2/ Compare and contrast RISC and CISC architectures in terms of their design (10) (CO2) (BL2) philosophies and performance characteristics.
- 3/ Compare the benefits and challenges of using static and dynamic scheduling (10) (CO3) (BL2) techniques in superscalar processors.
- 4/ Describe in detail the architecture and features of a modern memory controller. (10) (CO4) (BL2)
- 5/ Describe the challenges of managing shared resources, such as buses and memory, (10) (CO5) (BL2) among multiple devices in a computer system.
- 6/ Conduct the multiplication of the numbers 0.00001 (in decimal) and 8192 (in (10) (CO1) (BL3) decimal) in floating-point arithmetic. Subsequently, denormalize the result based on the IEEE 754 double-precision format (64 bits), and illustrate all the intermediate steps.
- 7/ Describe the concept of pipelining in processor architecture and how it enhances (10) (CO2) (BL2) instruction throughput.
- 8/ Let's consider a pipeline with 5 phases having durations of 25, 35, 70, 60, and 90 (10) (CO3) (BL3) ns. Given the latch delay is 18 ns, calculate the following:
 - a) Pipeline cycle time
 - b) Non-pipeline execution time
 - c) Speed-up ratio
 - d) Pipeline time for 600 tasks
 - e) Sequential time for 600 tasks
 - f) Throughput(All questions carry equal marks)
- 9/ In a 2-way set associative cache memory unit with a capacity of 32 KB built using a (10) (CO4) (BL3) block size of 16 words, where each word is 64 bits long, and the physical address space size is 8 GB, determine the number of bits allocated for the TAG field.
- 10/ Consider a pipelined processor with a 5-stage pipeline (IF - Instruction Fetch, ID - (10) (CO5) (BL4)