


PAVITHRA. A

 8951681628

 pavithra.parandam@gmail.com

 github.com/pavithra7369

EDUCATION

CGPA - 8.5

PES University Electronic City Campus, Bengaluru
Bachelor of Technology in Electronics and Communication Engineering [2023-2025]

RELEVANT COURSEWORK

- Digital VLSI Design
- Linear Algebra
- Network Analysis and Synthesis
- Signals and Systems
- Linear Integrated Circuits
- Analog Circuit Design
- CADD
- RISC-V Architecture
- Machine Learning
- Computer Architecture
- Memory Design and Testing
- Low Power VLSI
- Verification of Digital Systems

PROJECTS

RTL to GDSII flow for Linear Feedback Shift Register (LFSR) | **Aug 2023 - Nov 2023**
iverilog, Yosys, Gtkwave, Magic, OpenLane

- Executed the RTL to GDSII flow for a Linear Feedback Shift Register (LFSR) using Icarus Verilog, Yosys, GTKWave, Magic, and OpenLane. Included RTL design and simulation, synthesis, physical design, and verification.

Layered Testbench for sequential and combinational circuits **Oct 2023 - Nov 2023**
| EDA Playground, System Verilog

- Wrote a layered testbench for JK Flipflop and half adder
- Testbench included transaction, generator, driver, environment, interface, monitor, and scoreboard

Single cycle RISC-V for R type instructions | Vivado, System **Oct 2023 - Dec 2023**
Verilog

- Implemented the processor's ISA and instruction decoding logic, ensuring compatibility with the RISC-V standard

Design of 6T SRAM cell (gpdk 180nm) | Cadence Virtuoso **Mar 2024 - Apr 2024**

- Designed 6T SRAM cells along with necessary peripherals for a 2x2 array to fulfill project specifications.

Low power optimization for level shifter (180nm) | Cadence **Mar 2024 - Apr 2024**
Virtuoso

- Implemented a 10T level shifter and calculated the average power, later optimized the circuit to reduce average power

TECHNICAL SKILLS

Languages: System Verilog, Verilog, C, ALP for RISC-V architecture, Python
Developer Tools: OpenLane, Quartus, Ripes, Cadence, Xilinx Vivado, EDA Playground, GitHub

CERTIFICATIONS

- Standard Cell Library design Workshop-24 | Cadence Virtuoso