Pavithra A

8951681628 | pavithra.parandam@gmail.com | LinkedIn | GitHub

EDUCATION

PES University Electronic City Campus **Bengaluru**
Bachelors of Electronics and Communications Engineering [2023-2025] CGPA - 8.27
Ramaiah Polytechnic **Bengaluru**
Diploma in electronics and communication[2019-2022] CGPA - 8.45

RELEVANT COURSEWORK

- Digital VLSI Design
- Analog Circuit Design
- Computer Architecture
- Linear Integrated Circuits
- Computer Aided Digital Design
- Machine Learning
- Digital Signal Processing
- Low Power VLSI
- Verification of Digital Systems
- RISC-V Architecture
- Memory Design & Testing

PROJECTS

Router 1X3 Design and Implementation | Verilog
- The design includes FIFO buffers, FSM control logic, and synchronizer modules to manage data routing between multiple output channels. **August-2024**

Implementation of Single-Cycle RISC-V processor | Verilog **May 2024**
- Constructed a single cycle RISC-V processor for RV32I base instruction set architecture

Low power optimization for level shifter (180nm) | Cadence Virtuoso **Apr 2024**
- Implemented a 10T level shifter and calculated the average power, later optimised the circuit to reduce average power

Design of a 6T-SRAM cell | Cadence Virtuoso **Apr 2024**
- Designed the cell along with peripherals to meet the required specifications
- Used the gpdk-180nm technology

RTL to GDSII flow for Linear Feedback Shift Register | Yosys, iVerilog, OpenLane, Gtkwave, Magic **Nov 2023**
- Performed RTL design and simulation, synthesis, physical design and verification

Layered Testbench for sequential and combinational circuits | EDA Playground, System Verilog **Nov 2023**
- Wrote a layered testbench for JK Flip Flop and half adder
- Testbench included transaction, generator, driver, environment, interface, monitor & scoreboard

TECHNICAL SKILLS

Coding Languages: Python, C, Verilog, System Verilog, ALP for RISC-V architecture
Tools: Cadence Virtuoso, Xilinx Vivado, EDA Playground, Quartus Prime Lite, OpenLane, Ripes

CERTIFICATIONS

Trainee at Maven Silicon **(June 2024 - February 2025)**
Standard cell library design workshop-2024 **Jan 2024**
- Designed standard cells for logic gates (NAND, NOR,AND)