Design and Construction of PCB Interface to Drive an Inverter and Open Loop Control of an Induction Motor

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Abstract—This report details on the design and construction of a PCB interface to drive a commercial power stage (Guasch Converter) which is used to drive the induction motor. The designed PCB provides interface between the programmed DSP control card (TMS320F28335) to control the switching of the inverter legs. The control strategy uses the Volts-Hertz open loop control. First the PCB interface is designed and fabricated and then tested in the lab. The control algorithm has been simulated and tested its working. Finally, the PCB is interfaced with the control card and the inverter to control the speed of the motor.

Keywords—open-loop control, Volts-Hertz, PCB Interface, Induction Motor, DSP, Inverter

I. INTRODUCTION

The main aim of this project is to carry out the PCB design and construction to interface a commercial power converter and the DSP control card and to perform the open loop Volt-Hertz control of an Induction motor. Motor drives are applicable in wide range of application. Understanding how to control the variables is important to work with them. For the same purpose, an interface PCB has been designed to interface the PCB to the power stage and to the control card. The power stage includes the three-phase diode rectifier, DC-link capacitor, and three leg IGBT inverter with gate drivers. Also, it comes with a Relay to control the Dc-link capacitor voltage. The three legs of the inverter are controlled using PWM techniques which will be supplied from the Texas Instrument's peripheral explorer kit. Besides the volts-Hertz control, the field oriented closed loop control (FOC) is another way to control motor drive. In this project, the open-loop V/f control is designed, simulated and implemented whereas the closed loop FOC control technique is designed and simulated.

II. CONTROL SYSTEM DESIGN

Open loop V/Hz and closed loop field-oriented control (FOC) are among some of the techniques used for controlling the Induction motor. The Volts-Hertz control method is commonly used to regulate the speed of induction motors for general-purpose applications due to its simplicity and low cost [1]. V/Hz performs the control while maintaining the ratio of voltage to frequency constant. The input frequency and the speed of the motor are related by the equation:

$$N = \frac{120f}{p} \tag{1}$$

Where, P is the number of motor poles, N and f are the input frequency and motor speed in RPM. The stator voltage at steady state is given by:

$$V_{-}s = R_{-}s I_{-}s + jw\lambda_{-}s \tag{2}$$

Where, w is the frequency, Rs is stator resistance, Is, Vs and \(\lambda \) are the stator current, voltage, and flux phasors, respectively. The motor's speed and the magnetic flux are affected by changing the stator voltage frequency. At low speed, higher magnetic field, there will be unnecessary excessive amount of heat in the motor. At high speed (high stator voltage frequency), the magnetic field weakens, resulting in lesser torque. The stator flux can be maintained by keeping the ratio of stator voltage and frequency constant. This also ensures torque generation remains constant independent of frequency. Volts/Hertz control assures constant flux by altering the voltage according to the frequency variation. From Equation 1, neglecting the voltage drop on the stator resistance, the constant proportionality between voltage and frequency is related by the following equation.

$$K = \frac{Voltage}{frequency} = \frac{V_{rated}}{2 * \pi * f_{rated}}$$
 (3)

The rated voltage $(400/\sqrt{3})$ and rated frequency (50 Hz) are taken from the nameplate of the motor. The voltage drop induced by the stator resistance is large at low speeds. The motor flux is directly affected by this decrement in voltage. Thus, to solve this issue, the stator voltage can be increased by booster Voltage to compensate for stator resistance losses. In Figure 1 below, Vb represents the booster voltage.

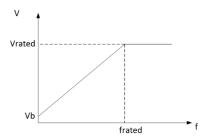


Fig. 1. Voltage and frequency relation

The open loop Volts/Hertz control scheme is as shown in Figure 2 below.

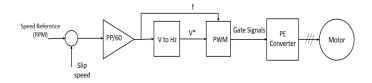


Fig. 2. Open-loop V/Hz control

The Field oriented control also designed to control the motor in closed loop. The motor parameters are estimated

using the nameplate data (when the motor is connected in delta). The calculated motor parameters are the summarized in the Table 1 below.

TABLE 1: MOTOR PARAMETERS

Motor parameters	Value
Stator Resistance (Rs)	12.56 Ohms
Stator Inductance (Ls)	1.10 H
Rotor resistance	12 Ohms
Magnetizing inductance (Lo)	1.03 H
No load current (Io)	1.23 A

The current and speed controllers are designed by considering the following two plant transfer functions.

$$G(s) = \frac{1}{SL_s + R_s} \tag{4}$$

$$H(S) = \frac{1}{SI_s + B} \tag{5}$$

Cascaded control is implemented and the bandwidth for the inner loop (current controller) is chosen 200 Hz and for the outer loop (speed controller), it is 20 Hz. Zero pole cancelation is applied where the integral gain tuned to cancel the zero and the proportional gain to keep the required bandwidth. The friction coefficient (B) is assumed zero.

$$C(s) = \frac{K_p \left(S + \frac{K_i}{K_p} \right)}{S} \tag{6}$$

The controller parameters for current and speed control are as shown in Table 2 below.

TABLE 2: CONTROLLER PARAMETERS

Controller pa	Value	
Current controller	Kp	115
	Ki	15782
Speed controller	KP	6.28
	Ki	0

III. HARDWARE IMPLEMENTATION

The approach for the interface design includes the design and construction of a printed circuit board to adapt the signals coming from the commercial power stage, interfacing to the TI microcontroller kit, and controlling the switching of the inverter to drive the Induction motor. Also, the DC-link voltage level of the power stage must be controlled autonomously to switch the relay ON and OFF. The DSP is used to control the switching of the power stage based on the open loop voltage to frequency control strategy to drive an Induction Motor.

The signal conditioning card will be able to adapt the 6 PWM signals from the microcontroller kit, boost them to the required voltage level (5V) using a buffer circuit and interface them to the power stack with a control switch. It also adapts two current sensor analogue signals, conditioned them to the

digital signals using filtering and conditioning stages. The anti-aliasing filter of 4 kHz cut-off frequency for the given sampling frequency of 10 kHz has been designed with the help of a Filter-Pro software tool. Also, it includes a DC-link voltage analogue sensor output and with the help of a comparator, switches the Relay to connect and disconnect the power stage which is very important for the protection of the circuit.

Texas Instrument's experimental control card TMS320F28335 is used as a DSP and the commercial MTL-CBI0010N12IXFA power stage from Guasch is used.

A. Power Stage

An internal schematic of the commercial power stage which includes the diode rectifier, DC link, IGBT drivers, sensors, and the three-phase inverter, is as shown in the Figure 3 below. This power stage module has control (J1) and sensor (J2) connector terminal which has DB-25 connector for each of them. In addition, it has power terminals (J3) and DC power supply auxiliary connector (J4).

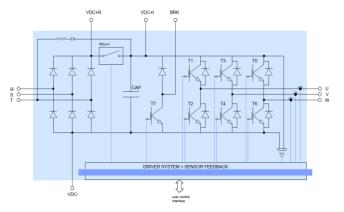


Fig. 3. Internal schematic of the commercial power stage

The designed PCB has 2 DB-25 connectors to connect to this power stage for control and the sensor. To supply different voltages to the PCB, it has a 6-port power terminal for +15V, -15V, +5V, +12V, +3.3V and the GND terminal.

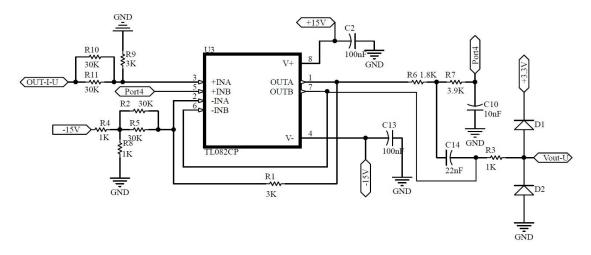
B. PCB Design

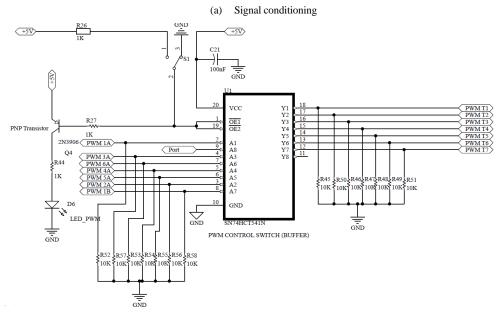
As already explained in the sections above, the aim of the PCB design and the construction is to adapt the signals between the Texas Instrument's control card used for control implementation and the commercial power stage which is used to drive the induction motor. The PCB has the ADC signal conditioning and filtering stage which are used for the closed loop control of the motor. The autonomous management of the DC-link voltage is done with the help of the relay circuit. Several LEDs are used to indicate different status about DC-link voltage, supply power, PWM signal, and to indicate the fault status. In addition, it contains a reset circuit to reset the power stack. The detailed explanation of each of the main functions are in the following.

1) Signal conditioning and filtering

The signal conditioning and filtering stage includes the use of an amplifier circuit one for each. The TL082 wide bandwidth dual JFET integrated circuit has two Op-Amps inbuilt. The two current sensors output are adapted considering the fact that, third current can be calculated automatically once other two are known (balance system). The current sensors output from the commercial converter are voltage signals ranging from -7.5V to 7.5V each

corresponding to -10 A to 10A currents. The DC-link voltage scale is between 0 to 7.5V for the actual voltage range of 0 to 750V.





b) Buffer circuit

Fig. 4. Schematic of the signal conditioning and Buffer Circuit

Now, with the signal adaptation block, we need to adapt these voltage signals to 0 to 3.0V to be able to use in the DSP card. Another important thing to consider in the signal adaptation stage is the filter. The anti-aliasing filter to filter out the noise signals (Sallen-Key LPF) is designed and constructed. The output signal is protected with two diodes which protects from the larger signals. Figure 4(a) shows the schematic of the signal adaptation stage, and the Figure 5 shows the input voltage signals and the output ADC filtered signal.



Fig. 5. Sensor Voltage and ADC Voltage

2) PWM Control

The PWM control signals from the DSP are passed through the buffer circuit designed as shown in Figure 4(b). The main task of the buffer circuit is to provide the more voltage than that of the controller i.e., it boosts the voltage level of the PWM signals from 3V to 5V and increases the current capability of the inverter. The logic voltage levels of

the commercial power stack (Guasch Converter) taken from the datasheet are as shown in Figure 6.

Description	symbol	notes/test conditions	min.	typ.	max.	units
Logic low input voltages (PWM & reset)	V _{IN,RESET}		-0.5		0.8	٧
Logic high input voltages (PWM & reset)	V _{IN,RESET}		2.0		5.5	٧
Logic high input voltages (relay)	V _{RELAY}			5		٧
Fault output current	I _{FAULT}				8	mΑ
Logic low input current (PWM & reset)	IN,RESET		-0.5	-0.4		mA
Logic high input current (relay)	IN,RELAY	V _{RELAY} = 5V			20	mΑ

Fig. 6. Driver characteristics of the commercial power stage [2]

The PWM logic is high or low which are given to the gate driver of the IGBT inverter of the power stack. A non-inverting buffer SN74HCT541N from Texas Instrument is used. If either output enables $(\overline{OE1} \text{ or } \overline{OE2})$ are high, input is high, all eight outputs are in the high-impedance state. A PWM switch to control these enable pins is used which controls the supply of PWM signals to the power stack. In addition, it has a LED to indicate the turn ON or OFF of the control switch. Several pull down resistors for each PWM input and output signals to the buffer are used to protect the circuit from any inconvenience that may occur and not to keep the output of the buffer floating when the PWM signals are switched OFF.

3) Fault & Relay control and Reset

Another important factor that we considered in our PCB design are the RELAY and FAULT control. The control connector from the power stage provides the seven different fault signals which are of the six different IGBT inverter switches and of a RELAY control switch. We need to control these fault signals, switch OFF the modulation signals and try to RESET the power stack when a fault occurs. A schematic view of the fault control circuit is as shown in the Figure 7. In addition, it has a fault control LED which indicates if there is a fault occurred. The TZ2 and TZ6 pins have been added to give the FAULT signals directly to the trip zone of the DSP which has been configured to cut-off the PWM signals in case of a fault.

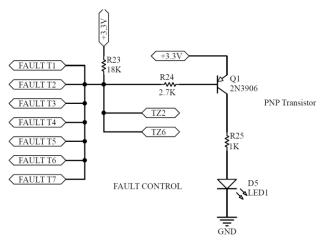


Fig. 7. Schematic of FAULT control circuit

A RESET circuit has been designed to RESET the power stack in case of a fault. From the datasheet of the power stack, the RESET has the falling edge signal. So, a push button is connected directly to the ground with one its terminal and another terminal is connected to the RESET pin which will give 0V when pressed. A schematic circuit is shown in Figure 8.

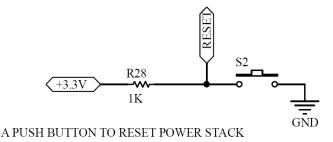


Fig. 8. Schematic of push button circuit to RESET the power stack

To control the DC-link voltage, a RELAY control circuit has been designed using a LM393 comparator which monitors the DC-link voltage. From the connection of the RELAY as shown in the Figure 9, when it is open, the DC- link capacitor is charged through the current limiting resistor and when it charges to 90 % (in theory) we close the RELAY for direct connection between the diode rectifier and the IGBT inverter to connect to the motor. Here we are closing the relay when the voltage is 67% of the maximum dc link capacitor voltage of 750V, which is given in the datasheet of the power stack. Since, initially capacitor draws more current to charge and if we don't pass it through the current limiting resistor, we may blow up everything.

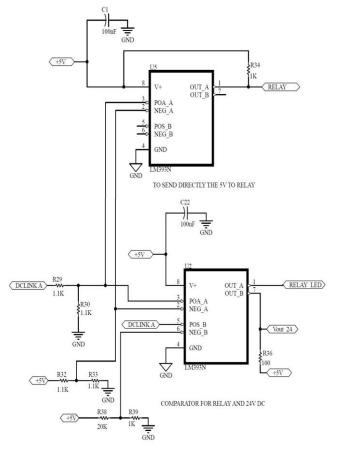


Fig. 9. Schematic of RELAY control circuit

From the driver characteristics of the power stack as shown in Figure 6 above, the RELAY operates with 5V so, we need to design the circuit to provide with the same voltage. To do so, two LM393N comparators, one to supply the direct 5V to the RELAY to turn ON in case the dc link capacitor reaches 500V and other to indicate both 24V and 500V status through two LEDs. The 24V LED status indicates the danger level of

the DC link capacitor. The dc link capacitor voltages measured from the power stack have been scaled down already inside the power stack by 100, so, 24V means 0.24V and 500 V means 5V.

The first comparator compares the DC link voltage, which has been scaled down further to 2.5V using a voltage divider, with the corresponding 2.5V and whenever the voltage is greater than 2.5V (corresponds to 500V), it sends 5V to the RELAY. The second comparator sends the signal to both RELAY LED and the LED for the 24V case.

4) LED circuit

Different LED circuits have been designed to indicate the various status during the operation. Some of the LEDs have been already mentioned in the subsections above, for example, for PWM and FAULT signal. The resistor values have been calculated based on the maximum diode current and the supply voltage. The schematic of various LED connection circuit is shown in Figure 10.

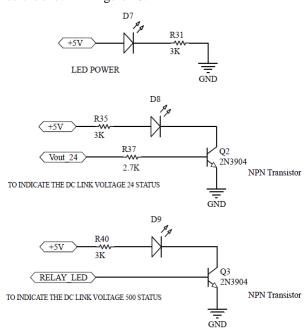


Fig. 10. Schematic of different LED circuits

LED power is used to indicate the supply connection of 5V. As already mentioned about the RELAY in the section above, we need to know the dc link voltage status. So, the LED 24V will indicate that we are in dangerous state, which means the DC link voltage passes 24V.In this case, the user should be cautious. And the LED 500V indicates that its safe to close the RELAY, which in-fact is being done automatically by directly sending the 5V signal to the converter.

Moreover, whenever there is a fault in any of the seven FAULT signals, a fault LED will turn on to inform that a FAULT has occurred. In this case, we turn off the PWM signals by turning OFF the PWM switch and we push the push-button to RESET the power converter to start working again. These seven FAULT signals have been merged as they are open collector signals.

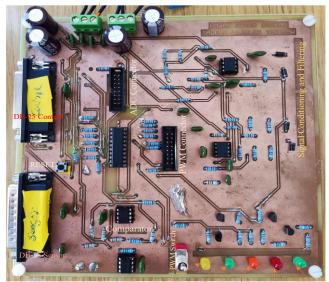
5) Final PCB

The top view of the final developed PCB is as shown in Figure 11. The PCB contains two major parts: control and measurement. The control part contains a DB-25 connector (control), Buffer circuit, Relay circuit, Reset circuit and 16-

pin PWM connector channel. The measurement part contains a DB-25 connector (sensor), Analogue conditioning and filtering circuit and 16-pin ADC connector channel. In addition, the power circuit contains a 6-pin power port to supply different voltages and a ground connection. The LED section contains five different LEDs each for PWM Signal, Relay Signal, Power Signal, 500V DC-link Signal, and the 24V DC-link signal.

The PCB has different test points with markings for the ease of verifying its working before testing with the commercial power converter and to verify the correct adaptation of the measurement signals. Both the DB-25 connectors, each for control and sensor, are arranged in such a way to be able to match them properly with the same pin arrangement with that of the Guasch Converter, which are connected with flat wires. The PWM and ADC connector pins are connected to the DSP via jumper cables (Flat-Wires).

Power Section



PWM LED 500V LED 24V LED Fault LED Power LED

Fig. 11. Final PCB interface design

IV. CONTROL SOFTWARE

The switches of the GUASCH inverter should be controlled accordingly to supply the motor with the required voltage supply. The PWM control modulation is applied to control the switching. The control programme is implemented by model-based programming using the C2000 Texas Instrument Toolbox and Simulink. The TMS320F28335 from Texas Instrument Shown in Figure 12 is utilized.

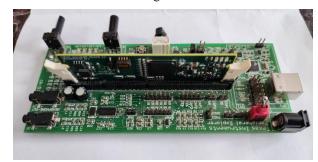


Fig. 12. Photo of TI TMS320F28335 Peripheral Explorer Kit

The GUASCH inverter has three legs with two IGBTs in each branch, thus, six gate signals are required. The Texas

Instruments Peripheral Explorer Kit has 12 PWM channels. For each branch of the inverter, ePWM2A and ePWM2B, ePWM3A and ePWM3B, and ePWM4A and ePWM4B are chosen where the A's are for the upper branch (T1, T3, and T5) and B's are for the lower branch (T2, T4 and T5) The speed reference is given by the potentiometer. The ADCINA0 of the DSP is a 12-bit module. So, to maintain the variation of the potentiometer from zero to maximum rated speed (1500 RPM), the gain multiplier is added as shown in Figure 13. The three-phase reference voltages are then generated using sine function, integrator, and phase shift. The reference signal should be normalized and then shifted up so the offset will be in the middle of the counter since the counter varies from zero to Time based period register (TBPRD) value (which is calculated using Equation 7) shows the implementation of control program in modelbased programming.

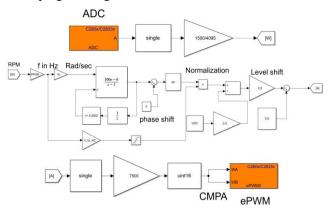


Fig. 13. The control program implementation in Simulink

The next task is configuring each Enhanced Pulse Width Modulator (*ePWM*). The carrier is set to be triangular as shown in Figure 14 (counting mode is Up-Down). The DSP board's system clock frequency is 150 *MHz*. The required frequency of PWM is 10 kHz (*TBCLK* = 1/10000*sec*). To directly use the microprocessor clock, the time-based clock pre-scaler divider (CLKDIV) and high-speed clock pre-scaler divider (HSPCLKDIV) are set to one. Then, TBPRD is calculated as:

$$TBPRD = \frac{T_{PWM}}{2 * T_{BCLK}} = 7500 \tag{7}$$

Configures the Event Manager of the C280x/C2833x DSP to generate ePWM waveforms.	
General ePWMA ePWMB Deadband unit Event Trigger PWM chopper control	Trip Zone unit
Allow use of 16 HRPWMs (for C28044) instead of 6 PWMs	
Module: ePWM2	
Timer period units: Clock cycles	
Specify timer period via: Specify via dialog	
Timer period: 7500	
Reload for time base period register (PRDLD): Counter equals to zero	
Counting mode: Up-Down	
Synchronization action: Disable	
☐ Specify software synchronization via input port (SWFSYNC)	
Synchronization output (SYNCO): Disable	
Time base clock (TBCLK) prescaler divider: 1	
High speed clock (HSPCLKDIV) prescaler divider: 1	

Fig. 14. Screenshot of the General ePWM configuration

Thus, the PWM works with the comparison of the reference signal and the triangle carrier which counts 7500 up and 7500 down. As shown in Figure 15 the PWM will be zero

when the reference (CMPA) crosses the triangle carrier during the up count and will be high when the reference (CMPA) crosses the carrier during down count (clear and set). The configuration is as presented in Figure 15.

General ← Finable ePV	ePWMA WM2A	ePWMB	Deadband unit	Event Trigger		
CMPA units: Clock cycles						
Specify CMPA via: Input port						
CMPA initial value: 0						
Reload for compare A Register (SHDWAMODE): Counter equals to zero						
Action when counter=ZERO: Do nothing						
Action when counter=period (PRD): Do nothing						
Action when counter=CMPA on up-count (CAU): Clear						
Action when counter=CMPA on down-count (CAD): Set						

Fig. 15. Screenshot of the ePWMA configuration

The gate signals of the same legs should be complimentary with a dead band. According to the information from the manufacturer [2], the driver system does not generate dead time between channels and thus, the dead time greater than $1 \mu s$ should be provided with the control signals between the two IGBTs from each branch. To be on the safe side, $2.5\mu sec$ dead time is chosen. Rising and failing age times (RED and FED) are calculated and configured in the dead-band unit.

$$ED = \frac{Dead \ tme}{TBCLk} = 2.5\mu sec * 150MHz$$

$$= 375$$
(8)

The PWM outputs of each branch were measured using oscilloscope and the deadtime, the frequency and duty are checked, and the results are as expected. Figure 16 shows the gate signals one of the three legs of the inverter.

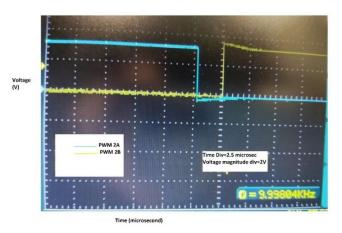


Fig. 16. PWM signal with 2.5 µs dead time

A. Control routine

The primary aim of the control program is to provide PWM signals to fire the GAUSCH inverter IGBTs using a volts-Hertz control approach. The potentiometer of the DSP board is used to give the speed command in rpm and the amplitude is limited to the maximum allowed speed. The position of the Knob determines the frequency and voltage amplitude while keeping the ratio constant (keep the flux

constant). The ePWM1A of the Peripheral Explorer Kit card is found defected, the voltage amplitude is below 3 V which could be problem for the buffer Thus, the ePWM2, ePWM3 and ePWM4 are utilized to deliver the gate signals. A dead time of 2.5 μs is guaranteed for PWM complementary signals. To set PWM signals to low state if the fault happened (the fault input from the GAUSCH is lowered), the trip zone could be implemented by enabling one-shot trip zone2/6. But the operation was not satisfactory. Therefore, the GPIO60 is set to read the fault input and provide the multiplication factor. The PWM will be lowered when there is fault unless GPIO60 input is one, hence, the normal operation continues.

The next control program implementation is closed loop current control in arbitrary reference angle. The current measurements are provided to the DSP board by the PCB board after the signals are being conditioned. Only two phases are measure and the third phase is calculated in the program considering power balance.

$$i_c = -(i_a + i_b) \tag{9}$$

ADCINA2, ADCINA3, and ADCINA4 reads the dc link measurement, current measurements of phase a and phase b respectively. The two potentiometers (VR1 and VR2) of the DSP board are used to deliver the arbitrary reference frame and the current magnitude. Based on the current command and measurement, the designed PI controller provides the voltage referenced in the arbitrary reference frame and then, then using, the reference angle set by potentiometer 2 (VR2) and 2/3 axis conversion, three phase reference voltages are obtained. Finally, the PWM signals generated in similar fashion as explained in V/Hz control scheme.

V. RESULTS

First, working of the designed control strategy is checked. For the maximum frequency of 50Hz, fundamental components of the PWM signals are as shown in Figure 17. In the figure, fundamental component of two PWM signals are shown. They have been filtered using the physical RC filter. By varying the frequency from the potentiometer of the DSP control card, the duty cycle of the PWM signals is varied and on doing so, the amplitude of the fundamental component changes, increases for increasing in frequency and vice-versa.

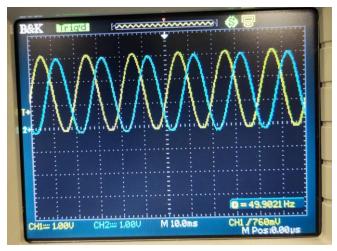


Fig. 17. Fundamental component of the controlled PWM signals

After the final designed PCB has been commissioned and verified that it's working, we finally tested it by connecting to the Guasch Converter and the DSP control card. The DSP control card is used to supply the PWM pulses for the IGBT inverter switching based on the V/f control strategy, where the magnitude and the frequency of the supply voltage can be varied using a potentiometer of the control card. When we vary the potentiometer knob from the control card, it varies the frequency from 0 Hz to 50Hz, which means the amplitude also varies to keep the v/f constant. The test setup is as shown in Figure 18.

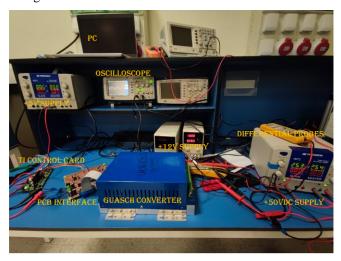


Fig. 18. Test Setup

The Guasch converter is first supplied with the constant 50V DC link volage directly from the DC voltage source. The modulating signals are fed and controlled from the microcontroller through the designed PCB interface. The output inverter voltage signal (Line-Line) from the Guasch Converter, when the motor is connected, is as shown in Figure 19. The figure shows both the actual line to line voltage (sampled at 125KS) and filtered (filtered through a low pass filter with the cut off frequency of 1 kHz) line to line voltage with motor load. By varying the frequency, we could verify that the voltage varies in accordance with the frequency to keep the ratio V/f constant.

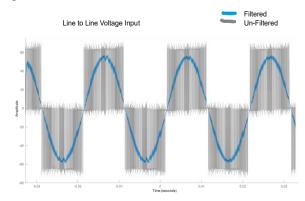


Fig. 19. Line to Line (U-V) voltage input to the motor

When the motor is connected from the Guasch Converter, the motor starts running and the speed of the motor could be controlled by varying the potentiometer knob of the control card, which represent the speed reference thus confirming the working of open loop control. The Figure 20 shows both the line to line (U-V) motor input voltage and motor input line current (one of the three phases) at maximum frequency of 50Hz. When reducing the speed reference, motor slows down as the input voltage reduces in magnitude. The current was

measure using a current probe which had settings of 100mV/1A and the current signals was magnified 10 times.

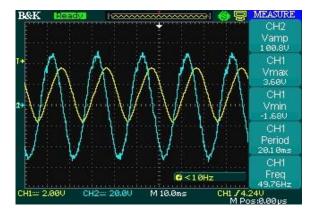


Fig. 20. Line to Line input voltage and Line current

The signal conditioning section is checked and verified it's working by giving the input voltage sinusoidal signal which varies from -7.5V to 7.5V. For the signal conditioning block, one difference amplifier (used to shift the voltage from 0V to 3V) and another operational amplifier for non-inverting filter are used. The output is the sinusoidal voltage signal from 0V to 3V in amplitude. The Figure 21 below shows the input voltage and output filtered voltage of the signal conditioning block. This confirms that the signal conditioning block from the PCB interface is working fine.

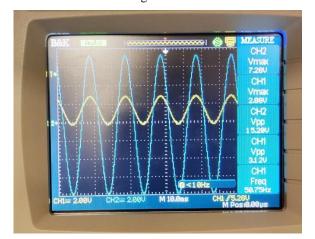


Fig. 21. Input and Output of Signal Conditioning and Filtering

VI. SHORTCOMINGS

In this section, various shortcomings or inconvenience occurred during the final testing of the designed interface and control are explained.

LED 24 V: The LED to indicate the 24V status was not working properly due to the transistor malfunctioning. To be sure that the DC-link voltage is safe to operate, we allowed few seconds for it to charge.

RELAY Voltage: For the measurement purpose, the RELAY output voltage from the comparator was connected to one of the pins of ADC connector using a voltage divider circuit to convert it from 5V to 3 V. Because of this, the output voltage supplied to the RELAY was less than 5V (it was

4.2V). We could get out of this problem by disconnecting the voltage divider circuit from the output RELAY port.

Footprints of PWM and ADC connector: Due to misunderstanding of the footprints of both PWM and ADC connector of the DSP microcontroller, they were different in the order of how we numbered them in our PCB footprint. This was overcome by using the separate jumper wires (not PWM and ADC adapters) to connect between the PCB and the microcontroller card.

TZ2 and **TZ6** of **DSP**: The both trip-zone of the DSP control card were not functioning properly when connected directly to the same TZ2 and TZ6 pins in the PCB when there is a fault. This was overcome by sending the TZ2 or TZ6 signal to the one of the GPIO pin of the control card and then programmed in the microcontroller itself to cut the modulation in case of a fault.

Closed Loop Current Control Implementation: The closed loop current control is simulated and verified it's working in MATLAB Simulink environment and PWM control strategy is programmed in DSP control card. One of the potentiometers of the DSP control card is used to vary the current reference while the other is used to vary the arbitrary reference angle. But due to time constraints and lack of motor speed measurement, the closed loop control testing of motor was not accomplished.

VII. CONCLUSION

This project verifies the working of motor speed control with open loop Volts-Hertz control strategy. For this purpose, a PCB interface has been designed and built to interface a commercial converter and the DSP control card. Several LEDs have been used to indicate the different status like PWM signals, Fault signals, Power and DC-link voltage. The DSP control card has been programmed in V/f control strategy to control the gate driver of IGBTs inverter. The output from the inverter has been fed to the motor. The speed of the motor has been successfully controlled by varying the speed reference from the control card. The motor parameters have been identified to design the controller parameters to simulate the closed loop control. The current sensor input signals from the converter have been conditioned and filtered to supply them to the DSP control card.

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