STES's

Sinhgad College of Engineering, Pune

Department of Electronics and Telecommunication Engineering

Subject – VLSI Design and Technology

BE E&TC 2019 Course

Question Bank

UNIT I

Design with HDL

1.	State and explain the program format of VHDL coding.	
2.	Explain different modelling styles in VHDL.	6M
3.	What is meant by concurrent and sequential statements in VHDL? Explain with examples.	7M
4.	Explain Generate statement in VHDL programming with the help of suitable example.	9M
5.	What is meant by synthesizable and non-synthesizable statement? Explain with example.	5M
6.	Explain different types of wait statements used in VHDL with suitable example.	9M
7.	Explain in detail: 1. Constants 2. Variable 3. Signals	6M
8.	What is difference between signal and variable.	
9.	Explain data objects with suitable examples.	5M
10.	Write VHDL code and test bench for D Flip flop using function for clock event.	
11.	Write VHDL code for half adder in behavioral, dataflow and structural modelling styles.	
12.	Write VHDL code for 8-bit SISO shift register by structural and behavioural modelling methods.	7M
13.	What is subprogram? Explore with suitable VHDL code.	5M
14.	What is function? Explain with suitable VHDL example.	5M
15.	Explain resolution function in VHDL.	5M
16.	Explain operator overloading in VHDL.	4M

17.	Explain procedure with example.	6M
18.	Compare function and procedure with suitable VHDL examples in detail.	9M
19.	What is need of package? Explain package declaration and package body with suitable VHDL example.	9M
20.	Write short note on configuration.	6M
21.	Explain different data types in VHDL.	6M
22.	What is need of attributes? Explain any three attributes in brief.	5M

UNIT II

Digital design and issues

1	Write a short note on metastability. Explain solution on it in detail.	8M
2	What is role of synchronizer in metastability problem? Explain any one synchronizer with timing diagram.	9M
3	List various encoding techniques of FSM. Design Mealy 110001 sequence detector and write VHDL code.	9M
4	Write VHDL code and test bench for 1011 Mealy sequence detector.	8M
5	Draw state diagram and write VHDL code for Traffic light controller.	14M
6	Explain clock skew with an example. How to minimize the effect of clock skew?	8M
7	Explain the terms: i) clock skew ii) clock jitter	4M
8	What is the reason for clock skew? Explain various clock distribution techniques.	5M
9	Explain positive and negative clock skew. Briefly explain the sources of clock skew.	6M
10	What are limitations of single phase clock? Explain with neat schematic. Two phase clock system in detail.	9M
11	What is the need of clock distribution? Explain techniques of clock distribution.	6M
12	Explain supply and ground bounce.	5M
13	Why should supply and ground bounce be taken care? How are these minimized?	5M

UNIT III

PLD Architectures and Applications

1	What is need of PLD? Explain technologies involved in detail	[8]
2	Enlist all the types of memory used in PLDs	[8]
3	Compare CPLD and FPGA	[6]
4	Compare PROM, PLA, PAL and CPLD	[8]
5	Explain in detail the synthesis in design flow	[5]
6	Draw and explain the architecture of CPLD	[8]
7	Explain features of CPLD.	[6]
8	Draw CPLD XC 9500 series architecture and explain in detail	[8]
9	Explain any four specifications of FPGA	[4]
10	Draw the architecture of FPGA and explain	[8]
11	What is the need of FPGA? List typical specifications of FPGA?	[8]
12	Draw and explain CLP structure of FPGA	[6]
13	Draw and explain the architecture of FPGA XC 4000 series	[6]
14	What is the difference between logic implemented in CPLD and that implemented in FPGA	[8]
15	Compare EPROM, PAL, CPLD, FPGA and ASIC	[8]
16	Explain FPGA synthesis and implementation	[6]

UNIT IV

DIGITAL CMOS CIRCUITS

1.	Explain CMOS inverter and transfer characteristics in detail.	[8]
2.	Explain with neat legends n-well CMOS layout design rules wrt i)maximum size ii)minimum spacing for a)n-well b)active area c)poly-1 d)metal-1	[8]
3.	Explain 1.Body effect 2.Transmission gate	[8]
4.	Design 4:1 MUX using transmission gates, compare this schematic with conventional design	[8]
5.	Design CMOS logic for Y=ABC+D	[8]
6.	Explain static and dynamic power dissipation. Derive an expression for power Delay product.	[8]
7.	Design CMOS logic for Y=A+BC+DE	[8]
8.	Explain static and dynamic power dissipation. What are main components which makes power dissipation in CMOS circuit.	[8]
9.	Prove that W/L ratio of PMOS to NMOS is approximately 2.	[6]
10.	Explain transmission gate and any one application of it in detail.	
11.	11.Write short note on RC Delay Model, Linear Delay Model, Parasitic Delay.	[6]
12.	12.Write a short note on CMOS Combo logic design	[8]
13.	.Explain in detail Non-ideal I-V effects	[8]
14.	What is technology scaling? Explain lateral and constant field scaling	[8]

UNIT V

1.	Draw the equivalent model of MOSFET and explain the parasitic in detail.	[8]
2.	Define figure of merit. Derive expression for it shows that switching speed requires high gm	[8]
3.	Explain channel length modulation and its performance.	[8]
4.	Explain DC characteristics of CS amplifier.	[8]
5.	List the parasitic and their typical values.	[7]
6.	What are the techniques to improve Rout of current source/sink? Explain cascade current source in detail.	[9]
7.	Explain current source and sink along with their limitations.	[8]
8.	Explain CMOS opamp in detail. Brief the concepts of active load, current mirror, and constant current source/p stage.	[8]
9.	How is frequency compensation done in CMOS opmap?	[6]
10.	With the help of schematic and necessary expression explain how MOSFET acts as diode and resister.	[10]
11.	Explain ASIC design flow in detail	[8]
12.	Explain following Design Issues i Antenna effect, ii Electro migration effect iii cross talk	[8]
13.	What is drain punch through? Explain with suitable diagram.	[8]
14.	Write a note on DRC	[8]
15.	Explain in detail latch up effect, latch up prevention techniques and comment on system level approach to avoid latch ups	[8]
16.	Draw circuit diagram of transmission gate and explain in detail	[8]
17.	Write in detail lambda rules with diagram	[10]
18.	Explain cross talk in detail	[8]
19.	Write in detail micron based design rules	[10]
20.	Write short note on Layout vs Schematic and Explain LVS checking process	[8]

UNIT VI

VLSI Testing and Analysis

1. What is the need of Design for testability? Explain in short different types of faults.
2. Explain TAP controller with its state diagram.
3. Write short notes on
   a) JTAG
   b) BIST
   c) Controllability and Observability
   d) Scan path-testing
4. Differentiate
   i) Testing Vs Verification.
   ii) White box Vs Black box testing.

5. Explain why model faults? Explain different fault models with schematics.

6. What is IEEE standard for boundary scan? Explain boundary scan architecture.

7. What do you mean by design for testability? How **it** can be categorized? Where it is useful?
8. Differentiate:
   i) White Box Vs Black Box testing.
   ii) Partial scan Vs Full scan.

9. What are objectives of boundary scan technique? Draw state diagram for TAP controller.

10. Explain why model faults? Explain different fault model with schematics

11. Explain DFT in detail. How it can be categorized? Where it is useful?