Amrutvahini College of Engineering, Sangamner
Department of Electronics & Telecommunication Engineering

Prelim Examination (2022 Semester- I)

Subject:VLSI Design & Technology **Marks:70**
Class: BE **Duration: 2.30 Hr.**

……

Instructions to the candidates:

(1) Answer Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6, Q. 7 or Q. 8.
(2) Draw neat diagrams wherever necessary.
(3) Figures to the right indicate full marks.

Que. No.		Question	CO	BT Level	Marks
Q1.	a)	Classify PLD.	CO3	2	[06]
	b)	Explore the PLD design flow.	CO3	2	[06]
	c)	Explain Complex PLD in detail.	CO3	2	[05]
		OR			
Q2.	a)	Draw CPLD architecture in detail, explain it in brief.	CO3	2	[06]
	b)	Compare CPLD and FPGA	CO3	4	[06]
	c)	Explain architecture of FPGA	CO3	2	[05]
Q3.	a)	Explain i)channel length modulation ii) body effect	CO4	2	[06]
	b)	What is technology scaling? what are its types.?	CO4	2	[06]
	c)	What is power delay product expression for it what is its significance?	CO4	2	[05]
		OR			
Q4.	a)	Explain the static and dynamic power dissipation.	CO4	2	[06]
	b)	Draw and explain working of Transmission Gate	CO4	2	[06]
	c)	Explain CMOS inverter circuit with neat diagram	CO4	2	[05]
Q5.	a)	Explain ASIC design flow in detail	CO5	2	[06]
	b)	Explain design issues like antenna effect and electro migration effect	CO5	2	[06]
	c)	Write a short note on layout versus (Vs) schematic and explain LVS checking process.	CO5	2	[06]
		OR			
Q6.	a)	Explain SPICE in detail	CO5	2	[06]
	b)	Explain AC and DC analysis of SPICE	CO5	2	[06]
	c)	Write a short note on SOC(system on chip)	CO5	2	[06]
Q7.	a)	What are types of fault explain each in brief	CO6	2	[06]
	b)	What is the need of DFT explain with suitable example	CO6	2	[06]
	c)	Explain partial scan and full scan	CO6		[06]
		OR			
Q8.	a)	Explain boundaries scan technique	CO6	2	[06]
	b)	Explain JTAG in detail with interface ports involved	CO6	2	[06]
	c)	Explain TAP controller with state diagram	CO6	2	[06]

CO3	Model digital circuit with HDL, simulate, synthesis and prototype in PLDs
CO4	Design CMOS circuits for specified applications.
CO5	Analyze various issues and constraints in design of an ASIC
CO6	Apply knowledge of testability in design and built in self-Test circuit.