Sinhgad Technical Education Society's

SMT. KASHIBAI NAVALE COLLEGE OF ENGINEERING

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Department of Electronics and Telecommunication Engineering

QUESTION BANK

SUBJECT: VLSI Design and Technology **CLASS: B.E. E & TC**

UNIT -I : HDL Design

1. **Explain Design flow of FPGA/VLSI**
2. **Define following**
   - **Entity**
   - **Architecture**
3. **Explain Libraries used in VHDL**
4. **Explain types of VHDL modeling techniques with example**
5. **Compare Signal and Variable**
6. **Compare Function and Procedure**
7. **Explain Data Objects in VHDL**
8. **What are the types of Data types in VHDL? explain.**
9. **What is Type statement ?explain its use**
10. **Explain Generate and Block statements**
11. **What are the different concurrent statements available in VHDL?**
12. **What are the different sequential statements available in VHDL?**
13. **Explain different Wait statements in VHDL**
14. **What is Process statement**
15. **Explain Concurrent and sequential execution in VHDL**
16. **Explain Package body and Package statement with example**
17. **What are the types of attributes available in VHDL explain with example**
18.
19. **What is sub program? Explore with suitable VHDL code.**
20. **Write VHDL code for 2:1 Mux in structural as well as behavioural modeling**

styles.

21. **Explain following**
    - **Simulation**
    - **Synthesis**
22. **Write VHDL code for Half Adder in structural as well as behavioral modeling styles.**
23. **Write VHDL code for Full Adder in structural as well as behavioral modeling styles.**
24. **Explain Hierarchical and flat designs**
25. **Write VHDL code for a sequence detector to detect a sequence of 100.**
26. **Write VHDL code for a D FF.**
27. **Write VHDL code for 4 bit counter.**
28. **Write VHDL code for a 2 bit comparator.**
29. **What is the test bench? Explain with an example**
30. **Write a VHDL code for 4 bit ALU**

UNIT - II :Digital Design and Issues

1. **What are the types of sequential machines explain with example.**
2. **Compare Mealy and Moore sequential machines.**
3. **Write a VHDL code to detect a sequence 11.**
4. **Explain Mealy sequential machine.**
5. **Define Clock skew and Clock Jitter**
6. **Write a short note on wire parasites**
7. **Write Short note on power distribution and power optimization?**
8. **Explain clock skew with an example. How to minimize the effect of clock skew?**
9. **Write short note on 1) EMI immune design 2) Clock Jitter 3) off chip connection.**
10. **What is supply and ground bounce?**
11. **Explain Power distribution techniques in brief?**
12. **Explain signal integrity issues, also explain the elimination techniques.**
13. **Explain input Pad design, output pad design and 3-state pad design in a chip.**
14. **What is floor planning? What cares are taken while floor planning.**
15. **Explain Noise Margin in detail.**
16. **Draw and explain I/O architecture?**
17. **What is meta-stability? Explain Sources of metstability. How to avoid metastability.**
18. **What is clock jitter? How to eliminate the clock jitter?**
19. **Explain clock skew and write in detail about positive and negative clock skew.**

Unit - III : PLD Architectures and Applications

1. **Write neat schematic explain the architectural building blocks of CPLD.**
2. **Differentiate CPLD and FPGA?**
3. **Explore Place & Rout (PAR) as well as timing verification w.r.t. CPLD/FPGA.**
4. **How does logic get implement in CPLD & FPGA? What is conceptual difference?**
5. **Explore the architecture of FPGA in detail.**
6. **What are the selection criteria of FPGA/ CPLD in the system? Explain with suitable example.**
7. **What do you mean by SRAM, Antifuse devices? What are their application.**
8. **Explore the term CLB, LC, LUT &IOB.**
9. **Explain Antifuse FPGA architecture?**
10. **Why FPGA called Field Programmable?**
11. **What are the merits of FPGA/CPLD over the logic implementing devices?**
12. **Explain the limitations of CPLD and FPGA?**
13. **Compare EPROM, PAL, CPLD and FPGA?**
14. **How the logic is implemented in FPGA ,explain with suitable example.**
15. **Draw CPLD XC9500 series at architecture and explain in detail.**
16. **Draw and explain the architecture of FPGA XC4000 series with neat diagram.**
17. **Draw and explain FPGA CLB architecture.**
18. **Explain in detail architecture of Macrocell in CPLD.**
19. **Explain any four important specifications of FPGA.**
20. **Explain any four features of FPGA.**