82335 SX
HIGH-INTEGRATION INTERFACE DEVICE FOR 386™ SX MICROPROCESSOR BASED PC-AT SYSTEMS

- **Operates with the 82230 and 82231 to Provide 100% IBM AT™ Compatibility**
- **Optimized for 16 MHz and 20 MHz 386™ SX Microprocessor Based PC-AT Systems**
- **Page Mode, Interleaved DRAM Controller**
- **Address Mapping/Shadow ROM Support**
- **387™ SX Numeric Coprocessor Synchronization Interface**
- **Parity Generation and Checking**
- **Low Power, High Speed CHMOS IV Technology**
- **Available in 132 Lead Plastic Quad Flat Pack**

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The Intel 82335 SX is a high integration interface device used together with the 82230/82231 to provide the most cost-effective and highest performance system design solution for AT-compatible 386 SX microprocessor based systems. The 82335 SX is plug compatible with the 82335.

The 82335 SX DRAM control feature is designed and optimized for the 16 MHz and 20 MHz 386 SX microprocessor bus architecture. The page mode, interleaved memory design allows 0 wait state performance on most memory accesses with 100 ns DRAM at 16 MHz or 80 ns DRAM at 20 MHz.

Several address mapping options are available to provide flexibility in the system memory size and configuration.

The 82335 SX also provides the necessary interface signals to allow the 387 SX numeric coprocessor to run in a PC/AT system. The 82335 SX with its intergrated parity generation and checking provides system designers with data integrity and reliability.

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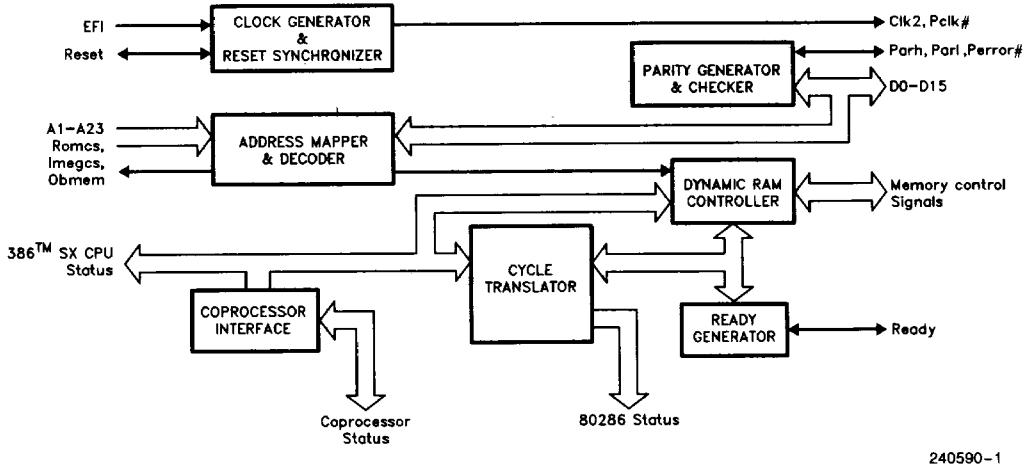

Figure 1.1. 82335 SX Internal Block Diagram

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1.0 PIN DESCRIPTION

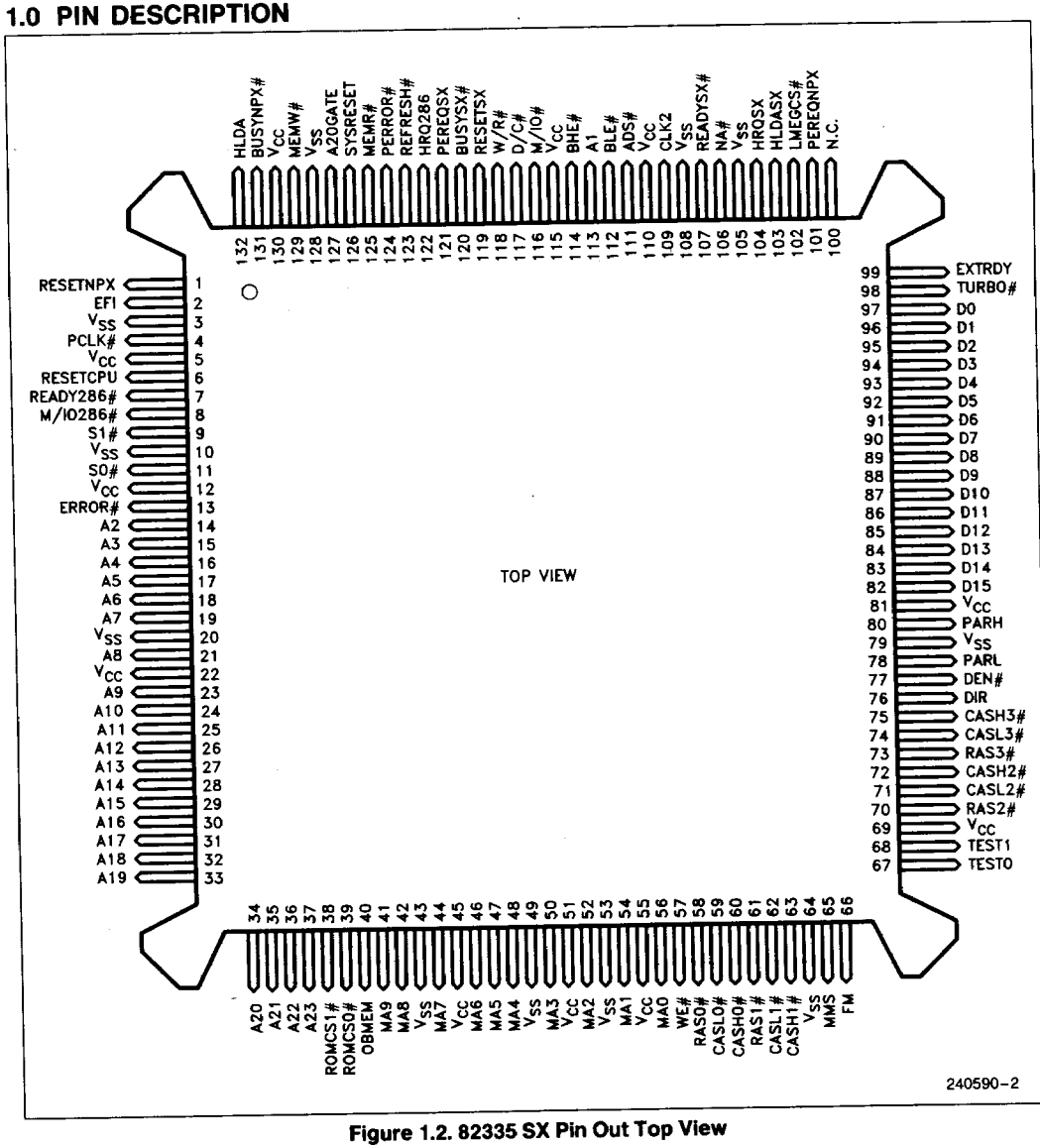


Figure 1.2. 82335 SX Pin Out Top View

Table 1.1. Alphabetical Pin Assignment

Address		Data		Control		Control		V_{CC}	V_{SS}
A1	113	D0	97	A20GATE	127	M/IO#	116	5	3
A2	14	D1	96	ADS#	111	M/IO286#	8	12	10
A3	15	D2	95	BHE#	114	NA#	106	22	20
A4	16	D3	94	BLE#	112	OBMEM	40	45	43
A5	17	D4	93	BUSYNPX#	131	PARH	80	51	49
A6	18	D5	92	BUSYSX#	120	PARL	78	55	53
A7	19	D6	91	CASH0	60	PCLK#	4	69	64
A8	21	D7	90	CASH1	63	PEREQNPX	101	81	79
A9	23	D8	89	CASH2	72	PEREQSX	121	110	105
A10	24	D9	88	CASH3	75	PERROR#	124	115	108
A11	25	D10	87	CASL0	59	RAS0#	58	130	128
A12	26	D11	86	CASL1	62	RAS1#	61		
A13	27	D12	85	CASL2	71	RAS2#	70		
A14	28	D13	84	CASL3	74	RAS3#	73		
A15	29	D14	83	CLK2	109	READY286#	7		
A16	30	D15	82	D/C#	117	N.C.	100		
A17	31			DEN#	77	READYSX#	107		
A18	32			DIR	76	REFRESH#	123		
A19	33			EFI	2	RESETCPU	6		
A20	34			ERROR#	13	RESETNPX	1		
A21	35			EXTRDY	99	RESETSX	119		
A22	36			FM	66	ROMCS0#	39		
A23	37			HLDA	132	ROMCS1#	38		
MA0	56			HLDASX	103	S0#	11		
MA1	54			HRQ286	122	S1#	9		
MA2	52			HRQSX	104	SYSRESET	126		
MA3	50			LMEGCS#	102	TEST0	67		
MA4	48			MEMR#	125	TEST1	68		
MA5	47			MEMW#	129	TURBO#	98		
MA6	46			MMS	65	WE#	57		
MA7	44					W/R#	118		
MA8	42								
MA9	41								

The 82335 SX is implemented in a 132-pin plastic flatpack package designed for direct surface mounting on component boards. The following is a description of the physical pin connections.

Table 1.2. Pin Description

Symbol	Pin No.	Type	Name and Function
A1–A23	14–19, 21, 23–37, 113	I*	**ADDRESS INPUTS:** These inputs are used to select the dynamic RAM address for a memory read or write operation.
A20GATE	127	I	**ADDRESS 20 GATE:** This active high input is used by the keyboard controller to force A20 low. When A20GATE is low, A20 is forced low internal to the 82335 SX during CPU memory cycles (not DMA or master). When A20GATE is high, A20 follows the CPU address input from the A20 pin.

NOTES:
*The following conventions are used in this table:
I = Input O = Output I/O = Input or Output
The symbol # following a signal name indicates that the signal is low active.

Table 1.2. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
ADS#	111	I	**ADDRESS STATUS:** This active low input indicates that a valid bus cycle definition and address (W/R#, M/IO#, D/C#, BLE#, BHE#, and A1–A23) is being driven by the 386™ SX microprocessor.
BHE#	114	I	**BYTE HIGH ENABLE:** This active low input indicates when data is being transferred on D8–D15.
BLE#	112	I	**BYTE LOW ENABLE:** This active low input indicates when data is being transferred on D0–D7.
BUSYNPX#	131	I	**BUSY NP:** This active low input is used by the 387™ SX coprocessor to indicate that it is busy. It is designed to be connected directly to BUSY# of the 387 SX. BUSYNPX# has a weak internal pullup resistor.
BUSYSX#	120	O	**BUSY SX:** This active low output indicates to the 386 SX CPU that the 387 SX is busy. It is designed to be connected directly to BUSY# of the 386 SX CPU.
CASH0# – CASH3#	60, 63, 72, 75	O	**COLUMN ADDRESS STROBE (HIGH BYTE):** These outputs are used by the high byte of the dynamic RAM array to latch the column address present on the MA0–MA9 pins. They can drive the dynamic RAM array directly and need no external drivers.
CASL0# – CASL3#	59, 62, 71, 74	O	**COLUMN ADDRESS STROBE (LOW BYTE):** These outputs are used by the low byte of the dynamic RAM array to latch the column address present on the MA0–MA9 pins. They can drive the dynamic RAM array directly and need no external drivers.
CLK2	109	O	**CLOCK2:** This output drives the 386 SX and 387 SX input clocks. It is generated by the External Frequency Input (EFI) and outputs the same frequency as EFI (32 MHz or 40 MHz).
D/C#	117	I	**DATA/CONTROL SELECT:** This input from the 386 SX is used to distinguish between data and control bus cycles.
DEN#	77	O	**DATA ENABLE:** This active low output is used by the data transceivers to enable the transfer of data between the dynamic RAM array and the local data bus.
DIR	76	O	**DIRECTION:** This signal is used to control the direction input of the data transceivers which connect the dynamic RAM array to the local data bus. When DIR is high, data is being written into memory.
D15–D0	82–97	I/O	**DATA BUS:** These inputs are used by the 82335 SX for parity generation and checking of data which is transferred between the local bus and the DRAM array. During initialization of the 82335 SX, they are used to write/read control words to/from the internal memory configuration registers.
EFI	2	I	**EXTERNAL FREQUENCY IN:** This input is driven by an external oscillator. It is used by the 82335 SX to generate the CLK2 and PCLK# output clocks. All internal 82335 SX logic is also driven by EFI. The EFI frequency is the same as the CLK2 (32 MHz or 40 MHz).
ERROR#	13	I	**ERROR:** This input indicates when a numeric coprocessor error has occurred. ERROR# is designed to be directly connected to the ERROR# output of the 387 SX and ERROR# input of the 82230. ERROR# has a weak pull-up resistor inside the 82335 SX.

Table 1.2. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
EXTRDY	99	I	**EXTERNAL READY:** This is an active high, level triggered input used to insert additional wait states into local memory bus cycles. Deactivation of EXTRDY during a local memory or numerics coprocessor access delays activation of the READYSX# output until EXTRDY is sampled active. Deactivation of EXTRDY will **block** (not delay) recognition of the READY286# input.
FM MMS	66 65	I I	FM and MMS are used to select DRAM operating modes. Refer to the DRAM controller section for available modes. These pins should be static after system reset.
HLDA	132	O	**HOLD ACKNOWLEDGE:** This output indicates the 386 SX has relinquished control of the local bus. It is asserted in response to activation of the HLDASX input from the 386 SX. It is designed to be connected to the 82231 HLDA input.
HLDASX	103	I	**HOLD ACKNOWLEDGE SX:** This input is asserted by the 386 SX in response to assertion of the 386 SX HOLD pin. It indicates that the processor has relinquished control of the local bus. It is designed to be connected to the 386 SX HLDA output.
HRQ286	122	I	**CPU HOLD REQUEST INPUT:** This active high input receives hold request signals for the 386 SX. It is designed to be driven by CPUHRQ from the 82231.
HRQSX	104	O	**CPU HOLD REQUEST OUTPUT:** This active high output drives the 386 SX HOLD input. It is the HRQ286 input with the trailing edge delayed.
LMEGCS#	102	O	**LOWER MEG CHIP SELECT:** This output is held low during local DRAM accesses made to the first megabyte of memory (000000H–0FFFFFH).
MA9–MA0	41, 42, 44, 46–48, 50, 52, 54, 56	O	**MULTIPLEXED ADDRESS:** These outputs are designed to provide the row and column addresses for CPU or DMA access, and row addresses for refresh access to the dynamic RAM array.
MEMR#	125	I	**MEMORY READ COMMAND:** This active low input is used to indicate when a DMA memory read cycle is being performed. It is designed to be connected directly to the —MEMR output of the 82230. MEMR# can be an asynchronous input.
MEMW#	129	I	**MEMORY WRITE COMMAND:** This active low input is used to indicate when a DMA memory write cycle is being performed. It is designed to be connected directly to the —MEMW output of the 82230. MEMW# can be an asynchronous input.
M/IO#	116	I	**MEMORY/IO SELECT:** This input from the 386 SX is used to distinguish between memory and I/O accesses.
M/IO286#	8	O	**MEMORY I/O SELECT 286:** This output emulates the M/IO# output of the 80286. It is used by the 82230/82231 and other system peripherals to distinguish memory access from I/O access. It is also used with the status output (S0, S1) to indicate halt/shutdown and interrupt acknowledge cycles.
NA#	106	O	**NEXT ADDRESS:** The NA# output is used to control the address pipelining of the 386 SX. It must be connected to the 386 SX NA# input. Consecutive local memory accesses are always pipelined after the first access.

Table 1.2. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
OBMEM	40	O	**ON-BOARD MEMORY:** This active high output indicates a local DRAM access is in progress.
PARH	80	I/O	**PARITY HIGH BYTE:** This three state input/output is used for the upper byte parity bit of data on the local bus (D8–D15). For memory write cycles, the 82335 SX outputs the internally generated parity bit to the DRAM array via the PARH pin. During a memory read, the 82335 SX uses the data received at PARH to validate the upper byte of data from the DRAM array.
PARL	78	I/O	**PARITY LOW BYTE:** This 3-state input/output is used for the lower byte parity bit of data on the local bus (D0–D7). Its function is identical to the PARH pin described above.
PCLK#	4	O	**PERIPHERAL CLOCK:** This clock signal is generated by dividing the EFI input by 2 in 16 MHz operation or by 2.5 in 20 MHz operation. It is designed to drive the X3 input of the 82230.
PEREQNPX	101	I	**PROCESSOR EXTENSION REQUEST NP:** This input is used by the 387 SX to indicate that it requires a data transfer. It is designed to be connected directly to PEREQ of the 387 SX.
PEREQSX	121	O	**PROCESSOR EXTENSION REQUEST SX:** This output to the 386 SX processor is used to request a data transfer to or from the numeric coprocessor. It is designed to be connected directly to PEREQ of the 386 SX.
PERROR#	124	O	**PARITY ERROR:** This active low output indicates that the 82335 SX has detected a parity error in either the upper or lower byte of data from the DRAM array. It is designed to drive the 82231 DPCK# input.
RAS0# – RAS3#	58, 61, 70, 73	O	**ROW ADDRESS STROBE:** These outputs are used by the dynamic RAM array to latch the row address present on the MA0–MA9 pins. The four outputs support up to a four-way interleaved dynamic RAM configuration with page-mode access. They drive the dynamic RAM array directly and need no external drivers.
READY286#	7	I	**READY 286:** This active low input is used to indicate the completion of system I/O or memory bus cycles. It is designed to be driven by the 82230 READY# pin.
N.C. (formerly READYNPX#)	100	I	**NO CONNECT:** This pin is not internally connected. The 82335 SX will generate READYSX# after 1 wait-state on all numerics coprocessor accesses if a coprocessor is present in the system.
READYSX#	107	O	**READY SX:** This active low output indicates the completion of the current bus cycle to the processor. It is a function of the internally generated ready signal for local memory, on-chip I/O, or coprocessor accesses, and the READY286#, EXTRDY, and TURBO# inputs.
REFRESH#	123	I	**REFRESH:** This active low input is used to notify the dynamic RAM controller that the dynamic RAM array requires refresh. It is designed to be driven by the 82231 –REFRESH output.
RESETCPU	6	I	**RESET CPU:** This high active input is used to generate the RESETSX output which resets the 386 SX CPU. It must be activated with SYSRESET during power-on reset. After power-on, activation of RESETCPU without SYSRESET will activate RESETSX without RESETNPX. RESETCPU is designed to be driven by the 82230 RES CPU output.

Table 1.2. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
RESETNPX	1	O	**RESET NPX:** This output is designed to drive the RESETIN pin of the 387 SX. It is activated only when SYSRESET and RESETCPU are both active.
RESETSX	119	O	**RESET SX:** This output is designed to drive the RESET pin of the 386 SX processor. It is a function of the SYSRESET and RESETCPU inputs.
ROMCS0# ROMCS1#	39 38	O	**ROM CHIP SELECT:** These outputs are used to support shadow RAM. They select the ROMs or EPROMs during system initialization. If ROM shadowing is selected, the ROMCS0–1 outputs are disabled and the ROM (EPROM) addresses are mapped into the DRAM physical address space by the 82335 SX.
S0# S1#	11 9	O	**BUS CYCLE STATUS:** The S0# and S1# outputs indicate the initiation of a system (non-local) bus cycle and, along with M/IO286#, define the type of bus cycle.
SYSRESET	126	I	**SYSTEM RESET:** This high active input is combined with RESETCPU to generate the RESETSX and RESETNPX outputs as well as synchronize the clock outputs. SYSRESET is designed to be driven by the 82230 + RESET output.
TEST0 TEST1	67 68	I	**TEST MODE:** These inputs are used for special test modes, and must be connected to V_{SS} during normal operation. TEST0 is a high active, level triggered input that disables all 82335 SX output buffers when active. The TEST1 input is reserved and must be connected to V_{SS}.
TURBO#	98	I	**TURBO MODE SELECT:** This active low input, when asserted, allows the 386 SX local bus to run with maximum performance. Deactivating the TURBO# input causes the 82335 SX READY generation logic to insert additional wait states into each bus cycle. In the non-turbo mode, 386 SX performance approximates 80286 bus efficiency.
V_{CC}	5, 12, 22, 45, 51, 55, 69, 81, 110, 115, 130	—	**POWER SUPPLY:** 11 V_{CC} pins total.
V_{SS}	3, 10, 20, 43, 49, 53, 64, 79, 105, 108, 128	—	**GROUND:** 11 V_{SS} pins total.
WE#	57	O	**WRITE ENABLE:** This output is used by the dynamic RAM array to enable input for a write operation. It is designed to drive two banks of DRAM with no additional buffering.
W/R#	118	I	**WRITE/READ SELECT:** This input from the 386 SX is used to distinguish between read and write cycles.

2.0 FUNCTIONAL DESCRIPTION

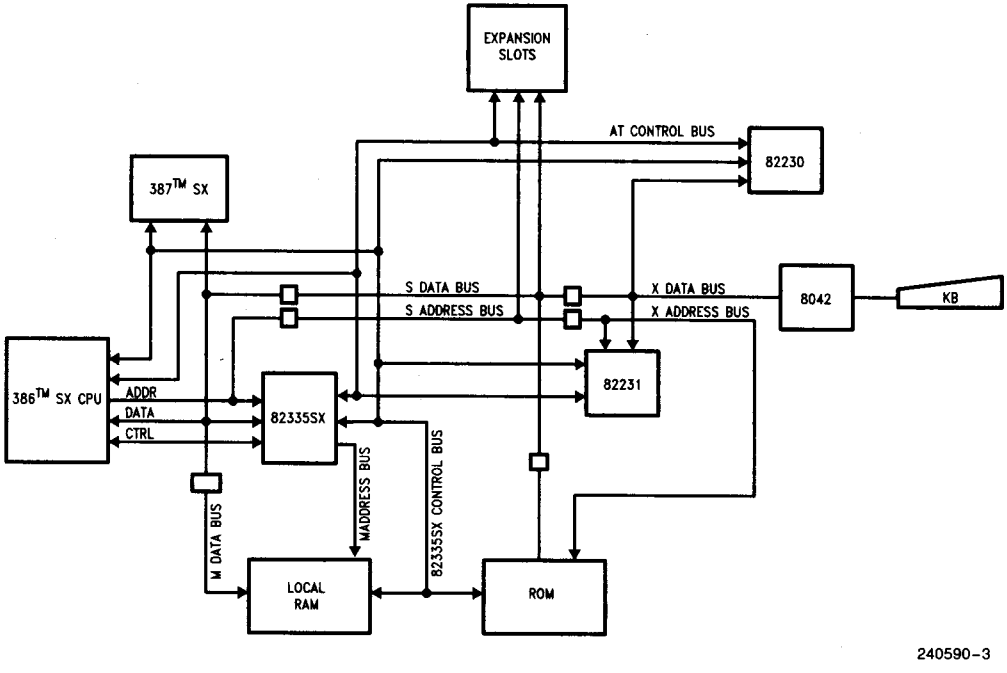
2.1 Introduction

The 82335 SX is a high-integration VLSI companion chip for the Intel 386 SX 32-bit microprocessor. It interfaces the 386 SX microprocessor to the 387 SX numeric coprocessor and to the 82230/82231 highly integrated peripherals to form an AT compatible system. The 82335 SX accomplishes this by converting 386 SX processor bus cycles to 80286 compatible cycles, generating necessary clock signals, and providing local dynamic memory control. Figure 2.1 shows a block diagram of this system.

The 82335 SX is composed of seven functional blocks:

1. DRAM Controller
2. Address Mapper/Decoder
3. Ready Generator
4. Bus Cycle Translator
5. Math Coprocessor Interface
6. Clock Generator/Reset Synchronizer
7. Parity Generator/Checker

Each functional block is described in the following sections.



NOTE:
To satisfy 82335 SX AC timing requirements, this configuration must use the 12 MHz 82230/82231.

Figure 2.1. 386™ SX CPU with 82335 SX System Block Diagram

2.2 DRAM Controller

2.2.1 INTRODUCTION

The 82335 SX dynamic RAM (DRAM) controller is designed and optimized for the Intel 386 SX Architecture. It keeps track of 386 SX CPU bus states and provides the necessary signals to address and refresh up to four 16-bit banks of 256K or 1M dynamic RAMs.

To optimize memory performance and flexibility, the DRAM controller has built in support for both paging and bank interleaving, and can be configured for several different modes of operation. These include four different memory modes to accommodate DRAM with different levels of performance: F1 and F4 are for either 100 ns (16 MHz) or 80 ns (20 MHz) fast page-mode DRAMs. WO1 and WO2 are for slower DRAMs. These modes are described in more detail in the DRAM mode configuration section.

In addition to the four memory modes available, the DRAM controller can be configured to operate in either turbo or non-turbo mode. The turbo mode allows the 386 SX microprocessor based system to run at peak efficiency, while the non-turbo mode allows it to approximate 80286 bus cycle timing for timing dependent software.

2.2.2 DRAM BANK CONFIGURATION

The local Dynamic RAM for the 386 SX/82335 SX system can be configured into one, two, or four 16-bit banks. Each 16-bit bank of memory is further divided into two 8-bit banks, low and high. Each 8-bit bank may contain one extra bit for parity.

Either 1 Mbyte or 256 Kbyte DRAM may be used. The same type of DRAM must be used in all banks installed. See Figure 2.2 for a block diagram of the 82335 SX to DRAM interface.

The exact memory configuration (DRAM size and number of banks installed) can be determined during system initialization through execution of a memory autoscan routine in the BIOS. Memory configuration information can then be programmed into the memory configuration register, roll compare registers, and address compare registers. See the address mapping/decoding section for details on register programming.

For local memory accesses the 82335 SX generates the DRAM control signals Row address strobe (RAS#), Column address strobe low and high (CASL# and CASH#), and Write enable (WE#), as well as the multiplexed row and column addresses (MA). Each bank has its own separate RAS#,

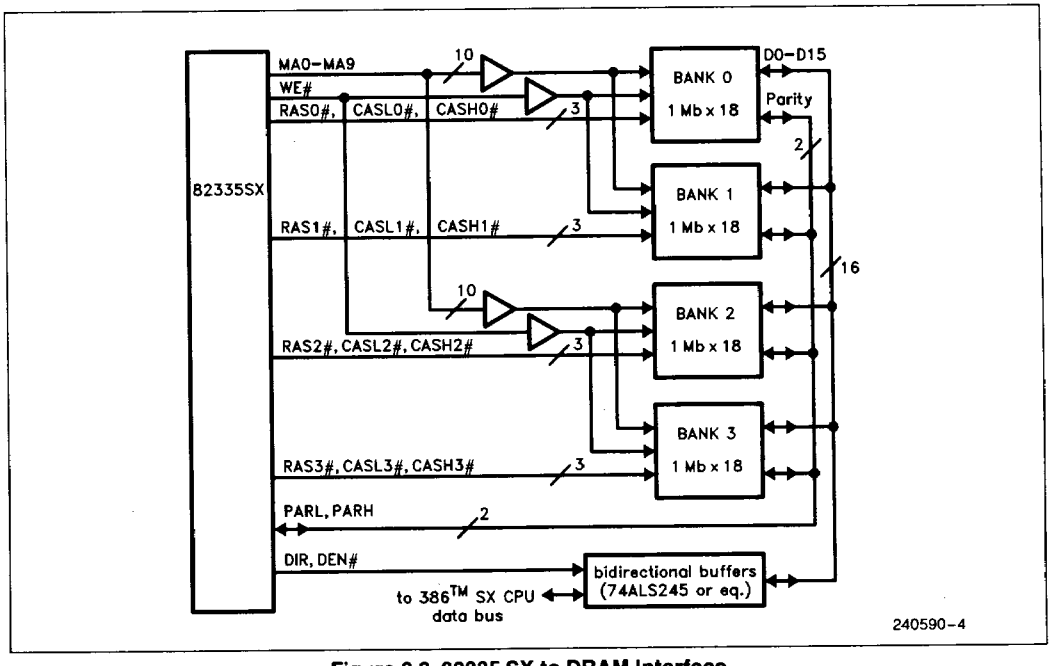


Figure 2.2. 82335 SX to DRAM Interface

Table 2.1. Address to Multiplexed Address Translation

Mode	DRAM Size	No. of Banks	Row Address										Column Address										Bank Select	
			MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	B1	B0
F1/F4	256K	1		A10	A11	A12	A18	A17	A16	A15	A14	A13		A9	A8	A7	A6	A5	A4	A3	A2	A1	0	0
F1/F4	256K	2		A19	A11	A12	A18	A17	A16	A15	A14	A13		A9	A8	A7	A6	A5	A4	A3	A2	A1	0	A10
F1/F4	256K	4		A19	A20	A12	A18	A17	A16	A15	A14	A13		A9	A8	A7	A6	A5	A4	A3	A2	A1	A11	A10
F1/F4	1M	1	A11	A19	A20	A12	A18	A17	A16	A15	A14	A13	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	0	0
F1/F4	1M	2	A21	A19	A20	A12	A18	A17	A16	A15	A14	A13	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	0	A11
F1/F4	1M	4	A21	A19	A20	A12	A18	A17	A16	A15	A14	A13	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A12	A11
WO1/WO2	256K	1		A10	A11	A12	A18	A17	A16	A15	A14	A13		A9	A8	A7	A6	A5	A4	A3	A2	A1	0	0
WO1/WO2	256K	2		A19	A11	A12	A18	A17	A16	A15	A14	A13		A9	A8	A7	A6	A5	A4	A3	A2	A10	0	A1
WO1/WO2	256K	4		A19	A20	A12	A18	A17	A16	A15	A14	A13		A9	A8	A7	A6	A5	A4	A3	A11	A10	A2	A1
WO1/WO2	1M	1	A11	A19	A20	A12	A18	A17	A16	A15	A14	A13	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	0	0
WO1/WO2	1M	2	A21	A19	A20	A12	A18	A17	A16	A15	A14	A13	A11	A9	A8	A7	A6	A5	A4	A3	A2	A10	0	A1
WO1/WO2	1M	4	A21	A19	A20	A22	A18	A17	A16	A15	A14	A13	A10	A9	A8	A7	A6	A5	A4	A3	A11	A10	A2	A1

NOTES:
1. When 256K DRAM is installed, the address output MA9 is not used.
2. During refresh the row addresses are internally generated by the 82335 SX and are not affected by the A1–A23 address inputs.
3. The bank select bits are interpreted as follows:

B1 B0 = 00 bank 0 selected
01 bank 1 selected
10 bank 2 selected
11 bank 3 selected

CASL#, and CASH# signals. The RAS#, CASL#, and CASH# outputs can directly drive the DRAM.

The WE# and Multiplexed Address lines are common to all banks. These outputs can directly drive approximately two banks of memory. If the capacitive loading on these outputs exceeds the maximum loadings defined in the AC timing specifications, then they will need to be buffered.

The multiplexed address outputs (MA0–MA9) are derived from the address inputs A1–A23 during local memory read or write operations. The way the 82335 SX translates the address inputs into row address, column address, and bank select bits depends upon several factors. These factors include DRAM size, number of banks installed, and mode of operation. Table 2.1 shows how the input addresses are translated.

2.2.3 PAGE-MODE DRAM OPERATION

Every DRAM access requires that the DRAM be provided with both a row address and a column address. A DRAM access requiring both a new row address and new column address has a long cycle time which requires at least one wait state. Figure 2.3 shows examples of DRAM cycles that require both new row and new column addresses.

The 82335 SX significantly improves bus performance by "paging" row addresses. Memory locations sharing the same row address are in the same "memory page". When successive memory accesses are in the same page (a page-hit memory access), only a new column address is required. This way, the row address strobe, RAS#, can be kept active, and each page-hit memory cycle only requires a new column address. This reduces the memory access time and allows most memory cycles to run at zero wait states. Figure 2.3 shows examples of both page-hit and page-miss cycles.

The effectiveness of page-mode operation in reducing wait states is dependent upon several factors. The most important factors are page location, page size, and page-mode cycle time. Page location and size are discussed below and page-mode cycle time is discussed in Section 2.2.4.

Page location is determined by the selection of address bits used for DRAM row addresses. To increase page-hits (zero wait state cycles), pages should be located such that successive memory accesses are in the same page. The 82335 SX generates row addresses from the higher order address bits. Since these bits are less likely to change than the lower order address bits, this increases the page-hit rate.

The page-hit rate can also be increased by increasing the page size. The page size for a single bank is 1 KByte if 256K DRAM chips are installed and 2 KByte if 1M DRAM chips are installed. The 82335 SX can keep a page of memory active in each bank. This can double the effective page size in a two bank configuration. A four bank configuration can effectively increase the page size by a factor of four. This increase in the active page size can significantly improve system performance. A memory access to an active page in a different bank (a page-hit-bank-miss) only requires a new column address, and therefore runs at zero wait states.

The 82335 SX keeps a memory page active for a particular bank by holding the RAS# signal active for that bank. The RAS# signal for a bank is activated by either an access to that particular bank or by a memory refresh.

RAS# deactivation can be caused by a number of events. In non-turbo mode RAS# is always deactivated at the end of each memory cycle. In turbo mode RAS# is deactivated by a page-miss memory cycle, RAS# timeout, or ending successive local memory accesses.

In addition to the RAS# deactivation events in turbo mode, F1 mode will also deactivate the RAS# signal for the previously accessed bank when a bank switch occurs.

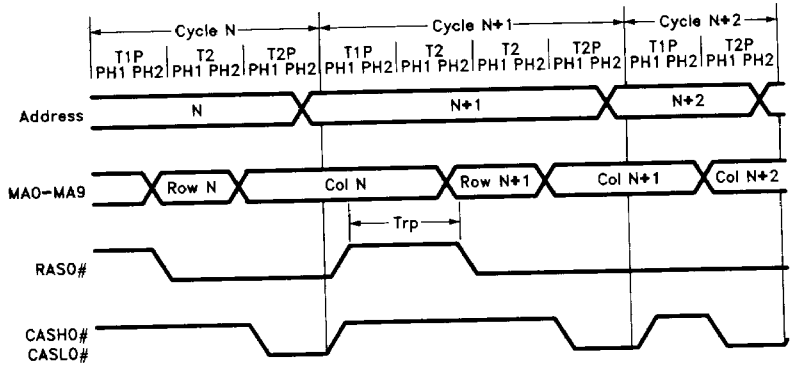
A page-miss memory cycle in modes F4, WO1, and WO2 will deactivate the RAS# signal only for the bank currently being accessed. Wait states are then inserted into the memory cycle to insure that the minimum RAS# precharge time required by the DRAM is satisfied.

RAS# deactivation can also be caused by a "RAS# timeout". Dynamic RAM chips have a limit on the maximum time that RAS# can be held active. The 82335 SX controls RAS# active time with four built-in watch-dog timers. Once timed-out, a RAS# signal will deactivate at the end of the current memory cycle. Each timer operates independently and guarantees a maximum RAS# active time of 10 μs.

RAS# signals that have been activated in mode F4, WO1, or WO2 and have not been timed-out, will remain active while successive local memory accesses are made. If the CPU executes a bus cycle other than a local memory cycle (i.e., I/O cycle, system memory cycle, etc.) or the CPU bus enters a hold or idle state, then all RAS# signals will deactivate. Table 2.2 summarizes RAS# activation.

Table 2.2. RAS# Activation

Mode	When	What
RAS# Activation		
All Modes	• A memory access is made to a bank. • A memory refresh is initiated.	RAS# for that bank is activated. All RAS# signals are activated.
RAS# De-Activation		
Non-Turbo	• End of each local memory cycle.	All RAS# are de-activated.
Turbo F4, Turbo WO1, Turbo WO2	• A page-miss occurs. • A RAS# timeout occurs. • Any cycle other than a local memory access.	RAS# is de-activated for that bank. RAS# is de-activated for that bank. All RAS# signals are de-activated.
Turbo F1	• A bank switch occurs. • A page-miss occurs. • A RAS# timeout occurs. • Any cycle other than a local memory access.	RAS# de-activates for the previous bank. RAS# is de-activated for that bank. RAS# is de-activated for that bank. All RAS# signals are de-activated.



NOTES:
1. New RAS# in cycle N requires one wait-state for row address latching.
2. Page-miss-bank-hit in cycle N+1. Two wait-states are required for RAS# precharge (T_{rp}).
3. Page-hit-bank-hit in cycle N+2 requires no wait-states.

Figure 2.3. 82335 SX Page Mode DRAM Cycles with New RAS#, Page Miss, and Page Hit Cycles in F1/F4 Modes

2.2.4 PAGE-MODE BANK INTERLEAVE OPERATION

Most fast page-mode DRAM have short cycle times which allow zero wait-state bus cycles on successive DRAM accesses. Slower DRAM, however, have longer cycle times which require wait-states to be inserted between successive accesses to the same memory bank. The 82335 SX allows most memory accesses to occur at zero wait-states, even for slow DRAM, by "interleaving" memory banks.

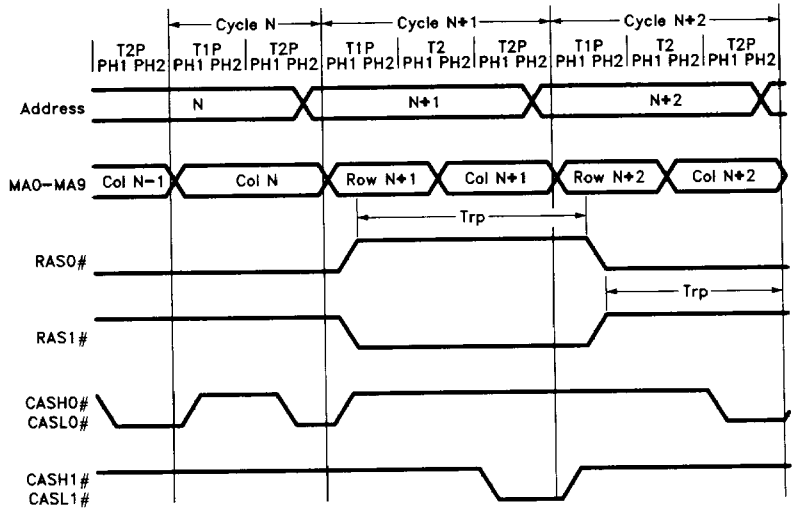
Interleaving refers to alternating bank accesses. Multi-bank configurations are always interleaved. In fast mode (F4/F1), banks are interleaved in pages. In slow mode (WO1/WO2), the lower address bit(s) are used to interleave banks by words (two bytes). Word interleaving alternates bank-hits for consecutive memory accesses thereby increasing the cycle time available to slow DRAM. This increases the number of zero wait-state page-hit-bank-miss cycles and improves system performance. Table 2.1 shows the address bits used for bank selection. An example of two bank interleaving in F1 mode is shown in Figure 2.4.

2.2.5 DRAM MODE CONFIGURATION

The 82335 SX can be configured to run in four different modes to operate with DRAM of various performance levels. This allows the system designer considerable flexibility. There are two modes (F1 and F4) for fast page mode DRAM and two modes (W01 and W02) for slower DRAM. The mode of operation is selectable by setting the input pins FM and MMS to the values shown in Table 2.3. Tables 2.3A and 2.3B show a summary of the different DRAM modes. A brief description of each mode follows.

F4: This is a high performance mode for fast 100 ns DRAM at 16 MHz or fast 80 ns DRAM at 20 MHz. The critical timing specifications that determine which DRAM can use this mode are listed in Tables 2.3A and 2.3B. Mode F4 allows up to four memory pages to be active simultaneously. This increases the page hit rate and allows more memory cycles to run at zero wait-states.

F1: This mode works with the same fast DRAM as mode F4. It differs from mode F4 in that only



NOTES:
1. DRAM access alternates between banks 0 and 1.
2. RAS precharge for bank 0 is hidden behind memory access of bank 1 and vice versa.

Figure 2.4. 82335 SX DRAM Cycle with Interleaved Memory in F1 Mode

one memory page can be kept active at a time. Activating only one page at a time reduces power consumption. Since only one page is kept active at a time, any bank-miss is also a page-miss which requires at least one wait-state.

WO1: Mode WO1 can be used with all 100 ns DRAM at 16 MHz or all 80 ns DRAM at 20 MHz. Slow page-mode DRAM that don't meet the critical specifications required for modes F4 and F1 can be used in mode WO1. This mode inserts one wait-state in page-hit-bank-hit cycles to allow the DRAM sufficient cycle time. At 20 MHz this mode also inserts one wait-state in page miss cycles to correspond to DRAM specifications. Up to four memory pages can be kept active simultaneously in this mode.

WO2: This mode allows inexpensive 120 ns DRAM to be used with the 82335 SX. It inserts additional wait-states in all cycles except page-hit-bank-miss cycles which run at zero wait-states. At 20 MHz there is no WO2 mode. At 20 MHz, if FM = 0, the 82335 SX will operate in WO1 mode regardless of the state of MMS. Up to four memory pages can be kept active simultaneously in this mode.

2.2.6 NON-TURBO MODE

Some programs written for 80286 based machines have software timing loops that are sensitive to processor speed. The 82335 SX non-turbo mode feature allows it to slow down local memory accesses to approximate 80286 bus timing.

The 82335 SX is put into non-turbo mode by driving the TURBO# input high (TURBO# > V_{IH}). The TURBO# input is then latched internally to synchronize it with DRAM accesses. It is latched on the falling edge of the 82335 SX HLDA output. This allows TURBO# to be an asynchronous input. Once the TURBO# input has been sampled high, a fixed number of bus states (six per memory cycle at 16 MHz or eight per memory cycle at 20 MHz) will be used for local memory accesses. The TURBO# input does not affect DMA cycle time. Figures 4.7A and 4.7B in the A.C. timing diagram section show examples of non-turbo mode read and write cycles.

2.2.7 REFRESH CYCLE

The 82335 SX controls DRAM refreshing in addition to controlling DRAM accesses. A DRAM refresh is initiated by asserting a hold request (HRQ286), receiving a hold acknowledge (HLDA), and then pulsing the REFRESH# input low. The 82335 SX then performs a "RAS only" refresh (no CAS# signals are generated). Once the refresh is completed (all banks have received a RAS# pulse), the REFRESH# and HRQ286 inputs can be deasserted. REFRESH# should not be asserted until the hold request has been acknowledged by the 82335 SX. Once asserted, the REFRESH# input must be held active for the minimum refresh period (see specification T83 in the A.C. specification section).

Table 2.3A. 16 MHz Summary of DRAM Modes

FM	MMS	Mode	Max Pages Active	Wait States				New RAS	DRAM Type	Critical DRAM Specifications
				Page Hit		Page Miss				
				Bank Hit	Bank Miss	Bank Hit	Bank Miss			
1	1	F4	4	0	0	2	2	1	100 ns Fast Page Mode	$t_{CAS} \leq 35$ ns $t_{CAC} \leq 35$ ns $t_{CP} \leq 20$ ns
1	0	F1	1	0	NA	2	1	1	100 ns Fast Page Mode	$t_{CAS} \leq 35$ ns $t_{CAC} \leq 35$ ns $t_{CP} \leq 20$ ns
0	1	W01	4	1	0	2	2	1	All 100 ns DRAM	
0	0	W02	4	2	0	3	3	2	120 ns DRAM	

Table 2.3B. 20 MHz Summary of DRAM Modes

FM	MMS	Mode	Max Pages Active	Wait States				New RAS	DRAM Type	Critical DRAM Specifications
				Page Hit		Page Miss				
				Bank Hit	Bank Miss	Bank Hit	Bank Miss			
1	1	F4	4	0	0	2	2	1	80 ns Fast Page Mode	$t_{CAC} \leq 30$ ns $t_{CP} \leq 20$ ns $t_{CAS} \leq 30$ ns $t_{RP} \leq 45$ ns $t_{AA} \leq 75$ ns $t_{RSH} \leq 30$ ns
1	0	F1	1	0	NA	2	1	1		
0	X	W01	4	1	0	3	3	2	All 80 ns DRAM and some 100 ns DRAM	$t_{RP} \leq 90$ ns $t_{CAS} \leq 50$ ns $t_{CP} \leq 40$ ns $t_{RSH} \leq 50$ ns

NOTES:
1. This table assumes the following input status: TURBO# $\leq V_{IL}$ max., EXTRDY $\geq V_{IH}$ min.
2. The first local memory access following an idle cycle or bus cycle other than a local memory access requires one extra wait-state to switch from non-pipelined to pipelined operation.
3. Definitions:

New RAS = The RAS# signal for a given bank transitions from an inactive to an active state.
Page hit = An access made to an active memory page.
Page miss = An access made to a memory page that is not currently active.
Bank hit = An access to the same memory bank accessed in the immediately preceding bus cycle.
Bank miss = An access to a memory bank that was not immediately preceded by an access to the same bank.
T_{CAS} = Column Address Strobe pulse width.
T_{CAC} = Column Address Strobe access time.
T_{CP} = Column Address Strobe precharge time.
T_{RP} = Row Address Strobe precharge time.
T_{AA} = Column Address access time.
T_{RSH} = Row Address Strobe hold time.

The 82335 SX generates its own refresh addresses. A ten bit refresh address counter within the 82335 SX is incremented by one at the beginning of every refresh. The refresh address appears on the address lines MA0–MA9 (MA0–MA8 if 256K DRAM are used) and is followed by RAS# activation. The address inputs A23:A1 are ignored during refresh.

During a refresh cycle, each bank of memory is refreshed when its RAS# signal activates. The 82335 SX staggers RAS# activation to reduce current surge during refresh. RAS# activation for each memory bank is separated by one PCLK# clock cycle and remains active for approximately two PCLK# cycles. All RAS# signals are activated during a refresh cycle if the REFRESH# input is held active long enough (see A.C. timing specification T83). If less than four memory banks are installed, the REFRESH# input may be de-activated after the installed banks have been refreshed. When the REFRESH# input is de-activated, any active RAS# signals will de-activate and the refresh cycle will be truncated. Figure 4.13 in the A.C. timing diagram section shows refresh timing.

2.3 Address Mapper/Decoder

2.3.1 INTRODUCTION

Several address mapping and decoding options are provided to improve performance and allow flexibility in the system memory size and configuration. These options include ROM/EPROM shadowing, mapping up to 512K addresses above the top of physical memory into physical addresses, and decoding input addresses to generate chip select signals. Selection of these options is done via programming of the configuration, roll compare, and address compare registers.

2.3.2 SHADOWING

Shadowing refers to copying data from slow memory devices like ROM and EPROM memories into RAM to speed up memory accesses. Since access to local RAM is much faster than ROM, this can improve BIOS performance considerably. The 82335 SX has built-in support for shadowing three different areas of memory: BIOS ROM, adapter ROM, and video RAM. Figure 2.5 shows the memory address ranges for each area. At least one megabyte of local memory must be installed to use the shadowing feature.

Shadowing can be done in two ways, each with different granularity. For 128 Kbyte granularity, shadowing can be selected for the BIOS ROM area (0E0000H–0FFFFFH), adapter ROM area (0C0000H–0DFFFFH), or video RAM area (0A0000H–0BFFFFH) by programming the configuration register bits ROMEN#, ENADP#, and ENV# respectively. If the configuration register bit for an area is cleared, then any access to an address in that area will be from ROM (or from system video RAM for the video area). If the configuration register bit for an area is set, then any access to that area will be from local memory. Each area can be shadowed independently. Note this matches 82335 shadowing exactly.

The second way has granularity of 32 Kbyte. The granularity is selected by programming the EXGRAN bit (bit 0) of the Granularity Enable register (I/O address 2CH). If EXGRAN = 0, then 128 Kbyte shadowing as discussed in the previous paragraph is used. The 82335 SX powers up with EXGRAN = 0. If EXGRAN = 1 then 32 Kbyte granularity is used.

If 32 Kbyte granularity is used, video RAM is shadowed the same way as in the 128 Kbyte granularity configuration. Shadowing of the BIOS and adaptor ROM areas is implemented in 32 Kbyte granularity by programming the Extended Granularity register (I/O address 2EH). Each bit in the register controls shadowing of one 32 Kbyte segment in the address range 0C0000H–0FFFFFH. The ENADP# and ROMEN# bits in the configuration register must be high if any 32 Kbyte segment in the respective address range needs to be shadowed. Section 2.3.4.4 and 2.3.4.5 contain more information on the Granularity Enable Register and the Extended Granularity Register respectively.

The BIOS ROM area FE0000H–FFFFFFH is addressable regardless of the shadow options selected. An access to an address in this region will always be from ROM.

When shadowing the BIOS ROM and adapter ROM, the ROM contents must be copied to the shadow RAM area. Since an access to one of these areas will access either the ROM *or* the RAM (not both), the following steps can be used to copy the ROM contents to the shadow area.

COPY BIOS ROM

a. Set configuration register to reflect correct DRAM size and number of banks installed, and clear the ROMEN# bit (enable BIOS ROM access).
b. Set address range compare registers to top of local memory (at least 1 MByte).
c. Copy contents of BIOS ROM to a temporary buffer in low memory (e.g., 040000h–05FFFFh).
d. Jump to code in temporary buffer to continue execution while enabling shadowing.
e. Set the ROMEN# bit in the configuration register to enable BIOS shadowing.

f. If 32 Kbyte granularity is desired
   1. Set EXGRAN = 1.
   2. Set the shadow bits in the Extended Granularity register that correspond to the address range desired for shadowing.
g. Copy contents of temporary buffer to BIOS shadow RAM area.
h. Jump back to high memory to execute code from BIOS shadow RAM area.
i. If 32 Kbyte granularity was selected, set the write-protect bits in the Extended Granularity register that correspond to the address range desired for write-protecting.

COPY ADAPTER ROM

a. Set configuration register to reflect correct DRAM size and number of banks installed, and clear the ENADP# bit (enable adapter ROM access).
b. Set address range compare registers to top of local memory (at least 1 MByte).
c. Copy contents of adapter ROM to a temporary buffer in low memory (e.g., 040000h–05FFFFh).
d. Set the ENADP# bit in the configuration register to enable adapter shadowing.
e. If 32 Kbyte granularity is desired
   1. Set EXGRAN = 1.
   2. Set the shadow bits in the Extended Granularity register that correspond to the address range desired for shadowing.
f. Copy contents of temporary buffer to adapter shadow RAM area.
g. If 32 Kbyte granularity was selected, set the write-protect bits in the Extended Granularity register that correspond to the address range desired for write-protecting.

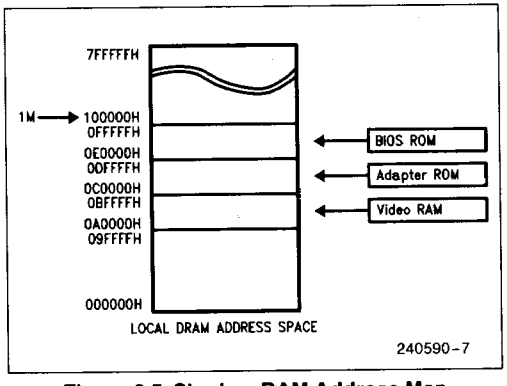


Figure 2.5. Shadow RAM Address Map

2.3.3 ROLL ADDRESS MAPPING

Roll address mapping is a method of utilizing DRAM memory space that may otherwise not be accessible. The memory space between 640K and 1M (0A0000h–0FFFFFh) is set aside for ROM and system video RAM in AT compatible systems. This space may also be associated with DRAM memory (e.g., one bank of 1M DRAM will reside at the physical address space 0K–2M). The "hidden" DRAM memory that resides in the same address space as the ROM and system video RAM can be either shadowed or it can be "rolled". Address rolling refers to re-mapping one address space to another.

The 82335 SX allows two memory address spaces to be defined; physical and logical. The physical address space corresponds to the amount of DRAM physically connected to the 82335 SX (e.g., one bank of 1M DRAM has the physical address space 0M–2M). The logical address space is the address range that the microprocessor sees as usable. The 82335 SX allows the logical address space to be larger than the physical address space. This is done by remapping logical addresses from above the physical address space (the "roll address" region) into the physical address space hidden by the ROM and video RAM areas. The physical memory between 512K and 640K may also be roll addressed when a 512K base memory is selected. Figure 2.6 illustrates address rolling from a logical to a physical address.

The amount of logical memory that can be rolled is dependent upon the amount of physical memory installed, the base memory selected and the shadow options selected. Up to 512K logical address space can be rolled into physical addresses in 128 Kbyte blocks. At least one megabyte of physical memory must be installed to utilize roll addressing.

Four physical DRAM areas can be utilized by roll addressing. These are called the BIOS ROM (0E0000h–0FFFFFh), ADAPTOR ROM (0C0000h–0DFFFFh), VIDEO RAM (0A0000h–0BFFFFh), and EXTRA (080000h–09FFFFh) areas. The BIOS ROM, ADAPTOR ROM, and VIDEO RAM areas can be selected for roll addressing if they are not selected for shadowing (configuration register bits ROMEN#, ENADP#, and ENV# = 0). The EXTRA area can be selected for roll addressing if a base memory of 512K is selected (memory configuration register bit S640 = 0). Each area can be selected independently of the others.

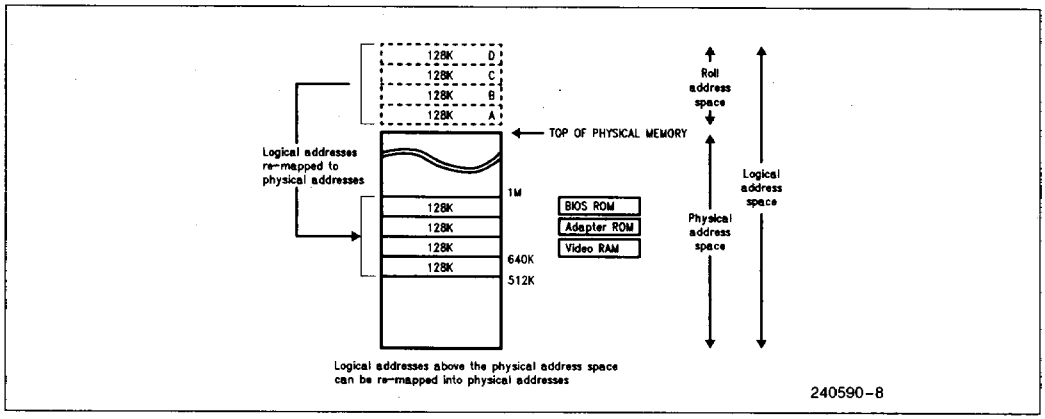
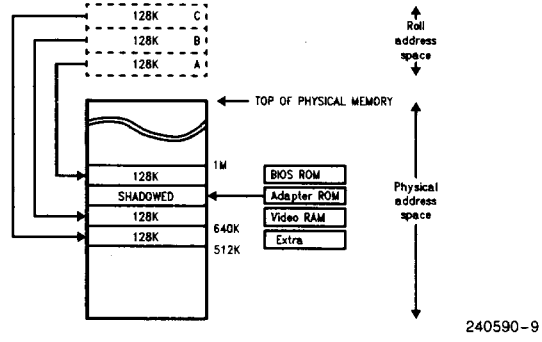


Figure 2,6. Roll Address Mapping Range

The number of DRAM areas selected for roll addressing determine the size of the roll address space. The address range for this roll address space is programmed via the roll compare registers. The roll address space must be programmed to start on a 512K boundary above the top of the physical address space. It can be programmed such that there is a gap between the physical memory connected to the 82335 SX and the roll address space (e.g., to accommodate add-in memory boards). See Section 2.3.4.2 for details on roll compare register programming.

Memory locations addressed in the roll address space do not map linearly into physical memory locations. Which roll address block maps to which physical memory block is controlled by the shadow and base memory options selected and the number of 128K byte blocks in the roll address space. Table 2.4 indicates how the roll address space maps into the physical address space for the various shadow and memory configurations available.

Figure 2.7 is an example illustrating how roll address blocks map into physical memory blocks.



EXAMPLE:
Assume:
- 512K base memory
- ADAPTOR ROM shadowed
- BIOS ROM and VIDEO RAM not shadowed
- 384K roll address space (3 blocks)

From Table 2.4, the following block mapping is found for this example:
Block A maps to BIOS area
Block B maps to VIDEO area
Block C maps to EXTRA area

Figure 2.7. Roll Address Block Mapping Example

Table 2.4. Roll Address Block Mapping

Blocks Not Shadowed	# of Blocks Rolled	Order of Logical Memory Blocks Rolled into Physical Memory Blocks			
		A	B	C	D
EXTRA	1	EXTRA			
VIDEO	1	VIDEO			
ADAPTER	1	ADAPTER			
BIOS	1	BIOS			
EXTRA, VIDEO	1	VIDEO			
	2	VIDEO	EXTRA		
EXTRA, ADAPTER	1	ADAPTER			
	2	ADAPTER	EXTRA		
EXTRA, BIOS	1	BIOS			
	2	BIOS	EXTRA		
VIDEO, ADAPTER	1	ADAPTER			
	2	ADAPTER	VIDEO		
ADAPTER, BIOS	1	BIOS			
	2	BIOS	ADAPTER		
VIDEO, BIOS	1	BIOS			
	2	BIOS	VIDEO		
EXTRA, VIDEO, ADAPTER	1	ADAPTER			
	2	ADAPTER	VIDEO		
	3	ADAPTER	VIDEO	EXTRA	
EXTRA, ADAPTER, BIOS	1	BIOS			
	2	BIOS	ADAPTER		
	3	BIOS	ADAPTER	EXTRA	
EXTRA, VIDEO, BIOS	1	BIOS			
	2	BIOS	VIDEO		
	3	BIOS	VIDEO	EXTRA	
VIDEO, ADAPTER, BIOS	1	BIOS			
	2	BIOS	VIDEO		
	3	BIOS	VIDEO	ADAPTER	
EXTRA, VIDEO, ADAPTER, BIOS	1	EXTRA			
	2	EXTRA	VIDEO		
	3	EXTRA	VIDEO	ADAPTER	
	4	EXTRA	VIDEO	ADAPTER	BIOS

LEGEND:
Physical Memory Block Addresses
BIOS AREA = 0E0000h–0FFFFFh
ADAPTER AREA = 0C0000h–0DFFFFh
VIDEO AREA = 0A0000h–0BFFFFh
EXTRA AREA = 080000h–09FFFFh

Logical Memory Block Order
Area A = lowest roll address memory block
Area D = highest roll address memory block

*Figure 2.6 illustrates logical memory block order

2.3.4 REGISTERS

There are seven registers in the 82335 SX that control the operation of the address mapping and DRAM control options. These registers are the configuration, roll compare (RC1 and RC2), address range compare (CC0 and CC1), granularity enable, and extended granularity registers. Each of these registers reside in the local I/O space of the 82335 SX and are read/writable until the LOCK bit has been set in the configuration register. The contents and purpose of each register are described in the following sections.

The 82335 SX contains a one-bit parity check enable register (PARCHEN). This register is a write only register and is not affected by the status of the LOCK bit in the configuration register. See the Parity Generator/Checker section for details on this register.

2.3.4.1 Memory Configuration Register

The memory configuration register resides at I/O location 22H upon system reset and is used to select a number of address mapping and DRAM control options. Upon reset, all bits in this register are set to zero. Figure 2.8 shows the bits used in the memory configuration register. The purpose of each bit is described in the following paragraphs.

ROMEN#: This bit is used to enable or disable shadowing of the BIOS ROM/EPROM in the address range 0E0000H–0FFFFFH. When this bit is cleared, BIOS ROM shadowing is disabled. A memory read in this range will access ROM by asserting ROMCS0# or ROMCS1# and by deactivating the OBMEM output. If BIOS ROM shadowing is disabled, this memory space can be accessed via roll addressing. See roll address mapping (Section 2.3.3) for details on address re-mapping.

Memory Configuration Register = I/O Address 22H

15	14–12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK		VRO	ENV#	ENADP#	ROMSIZE	INTERL			DSIZE	S640			ROMEN#

Bit Position	Name	Function
0	ROMEN#	0 = Enable BIOS ROM/EPROM Accesses (0E0000H–0FFFFFH) 1 = Disable BIOS ROM/EPROM Accesses, Shadow Enabled
3	S640	0 = Base Memory Size is 512K 1 = Base Memory Size is 640K
4	DSIZE	0 = 256K DRAM Installed 1 = 1 Mb DRAM Installed
7, 6	INTERL	00 = 1 Mem. Bank Installed (Note 1) 01 = 2 Mem. Bank Installed (Note 1) 10 = 2 Mem. Bank Installed (Note 1) 11 = 4 Mem. Bank Installed (Note 1)
8	ROMSIZE	0 = 256K ROM/EPROM 1 = 512K ROM/EPROM
9	ENADP#	0 = Enable Adaptor ROM/EPROM Accesses (0C0000H–0DFFFFH) 1 = Disable Adaptor ROM/EPROM Accesses, Shadow Enabled
10	ENV#	0 = Enable Video RAM Accesses (0A0000H–0BFFFFH) (Note 2) 1 = Disable Video RAM Accesses, Shadow Enabled
11	VRO	Video Read Only 0 = Video Area Read-Write (0A0000H–0BFFFFH) 1 = Video Area Read-Only
15	LOCK	0 = Enable all Configuration Register Accesses 1 = Disable all Configuration Register Accesses

NOTES:
1. When more than one bank of memory is installed, banks are always interleaved.
2. For AT compatible operation, Video RAM should be enabled (ENV# = 0).

Figure 2.8. Memory Configuration Register

When this bit is set, and EXGRAN and the extended granularity register is set appropriately, BIOS ROM shadowing is enabled and memory accesses to this address range are made from local DRAM. During shadow DRAM accesses, the OBMEM signal is asserted and the ROMCS0# and ROMCS1# signals are disabled.

S640: This bit selects the base memory size. When cleared, a base memory of 512K is selected. When set, a base memory of 640K is selected. If a base memory of 512K is selected, the address range 080000H–09FFFFH can be accessed via roll addressing. See roll address mapping (Section 2.3.3) for details on address re-mapping.

DSIZE: This bit is used to indicate the type of DRAM installed. When cleared, it indicates 256K DRAM and when set, it indicates 1M DRAM installed. DRAM sizes cannot be mixed. When 256K DRAM is installed, the multiplexed address line MA9 is not used.

INTERL: These two bits indicate the number of banks of memory installed. When more than one memory bank is installed, the banks are always interleaved. If the INTERL bits are set for one memory bank, RAS and CAS signals are generated for bank 0. If set to two bank operation, RAS and CAS signals are generated for banks 0 and 1. If set to four bank operation, RAS and CAS signals are generated for banks 0 and 1. The 82335 SX does not allow 3 way interleaving. Therefore if the INTERL bits are set to three, the 82335 SX will default to 2 bank operation, i.e., RAS and CAS will be generated for banks 0 and 1 only.

ROMSIZE: This bit indicates the size of the installed ROM/EPROM. When cleared, it indicates 256K bit ROM/EPROM and when set, it indicates 512K bit ROM/EPROM is installed. This bit also affects the ROMCS0# and ROMCS1# address decode ranges when ROM shadowing is disabled. See **Chip Select Signals** (Section 2.3.5) for further information.

ENADP#: This bit is used to enable or disable shadowing of the adapter ROM area. If cleared, adapter ROM shadowing is disabled and accesses to the memory range 0C0000H–0DFFFFH will be made from ROM. When this bit is set and EXGRAN and the extended granularity register is set appropriately, adapter ROM shadowing is enabled and memory accesses in this range will be from local DRAM. If adapter ROM shadowing is disabled, this memory space can be accessed via roll addressing. See roll address mapping (Section 2.3.3) for details on address re-mapping.

ENV#: This bit is used to enable or disable shadowing of the external video RAM. If cleared, video RAM shadowing is disabled and accesses to the memory range 0A0000H–0BFFFFH will be made to/from the system video RAM. If set, video RAM shadowing is enabled and memory accesses in this range will be to/from local DRAM. For AT compatible operation, video RAM shadowing should be disabled (ENV# = 0). If video RAM shadowing is disabled, this memory space can be accessed via roll addressing. See roll address mapping (Section 2.3.3) for details on address re-mapping.

VRO: This bit selects either read/write access or read only access from the video RAM area when shadowing is selected. When video RAM shadowing is enabled and this bit is set, the local video RAM area will be read only, otherwise it will be available for both read and write access.

LOCK: This bit enables or disables external access to the configuration, roll compare, granularity enable, extended granularity, and address range compare registers. When this bit is cleared the following conditions will exist:

- The configuration, roll compare, granularity enable, extended granularity, and address range compare registers will be read/writable at even I/O addresses from 22H–2EH
- The status outputs S0# and S1# will not be generated for these I/O addresses
- If EXGRAN = 0, the shadowing DRAM area will be available for both reading and writing
- If EXGRAN = 1, the write protect bits in the extended granularity register will determine which shadowing DRAM areas are read-only and which are read-writable
- If video RAM shadowing is selected, VRO# will determine if the video shadow area is read-only. Video RAM shadowing operates the same way in the 82335 SX as it does in the 82335.

When the LOCK bit is set, the following conditions will exist:

- The configuration, roll compare, granularity enable, extended granularity, and address range compare registers will not be accessible external to the 82335 SX
- The status outputs S0# and S1# will be generated for I/O addresses between 22H–2EH
- If BIOS or adapter ROM shadowing is selected and EXGRAN = 0, then the shadowed area(s) will read-only
- If EXGRAN = 1, the write protect bits in the extended granularity register will determine which shadowing DRAM areas are read-only and which are read-writable

- If video RAM shadowing is selected, VRO# will determine if the video shadow area is read-only. Video RAM shadowing operates the same way in the 82335 SX as it does in the 82335

Once the lock bit is set, the configuration, roll compare, address compare, granularity enable, and extended granularity registers can only be accessed again by resetting the system using the SYSRESET input. It is recommended that the LOCK bit be set after the 82335 SX is properly configured.

The lock bit does not affect the operations of I/O Ports 061H or 0F0H. Writing to these ports writes to both the 82335 SX and the 82230. Since this is an I/O write to the 82230, the 82230 is required to end the cycle by activating READY286#.

When writing to the 82335 SX registers, all bits are written over. Care should be taken to insure that all bits of the data to be written are set for the intended operation.

2.3.4.2 Roll Compare Registers

Two roll compare registers, RC1 and RC2, are used to re-map logical addresses to physical addresses. The input address for a memory access is compared with the roll address ranges programmed into the roll compare registers. If the input address is a logical address within the roll address area, the 82335 SX internally translates it to a physical address and outputs the translated address to the multiplexed address bus (MA0–MA9).

The size and location of the roll address area is programmable. The size of the roll address area can be 128K, 256K, 384K, or 512K bytes depending upon the shadow and base memory options programmed into the memory configuration register. Each memory block (BIOS, adapter, or video) that is not shadowed adds 128K to the memory available for roll addressing. If a base memory of 512K is selected, then another 128K block of memory is available for roll addressing.

The roll address area can be located anywhere above the physical memory and must start on a 512K boundary. The 82335 SX allows the roll address area to be discontinuous from the local memory address space. This allows system designers to accommodate external memory cards requiring hardware switch settings to work independently of address rolling options selected.

The roll address area must be programmed to be a single contiguous area. Each roll compare register can be programmed to decode a 128K, 256K, or 512K roll address space. If a 384K roll address space is desired, then one register can be programmed to decode a 256K address space and the other to decode an adjacent 128K address space. If a 128K, 256K, or 512K roll address area is desired, it can be programmed into one register and the other register can be disabled.

The size and location of the roll address area is set by programming three sections in each roll compare register. These sections are referred to as the "compare data", "address mask", and "compare enable" sections. Figure 2.9 shows the three parts of each roll compare register. Each of these roll compare register parts are described in the following paragraphs.

The compare data bits (C23–C17) are used to specify the starting address of the roll address area covered by that register. These bits should be programmed to match the address bits A23–A17 of the first address in the address space selected for that register. If only one roll compare register is used, the roll address space must start on a 512K boundary (C17 = C18 = 0). If two roll compare registers are used, then the first register must be programmed to start on a 512K boundary and the second register must be programmed to be contiguous with the first roll compare register. The examples at the end of this section illustrate roll compare register programming.

The address mask bits (M23–M17) are used to select the size of the roll address area covered by that register. For each mask bit that is set, the corresponding input address bit and compare data bit are compared for a match. If a mask bit is cleared, the corresponding input address bit and compare data bits are ignored. If all mask bits are set, the roll address area covered by that register will be 128 Kbytes. If mask bit M17 is cleared, the register will cover a 256 Kbyte roll address area. If both M17 and M18 are cleared, the register will cover a 512K byte roll address area.

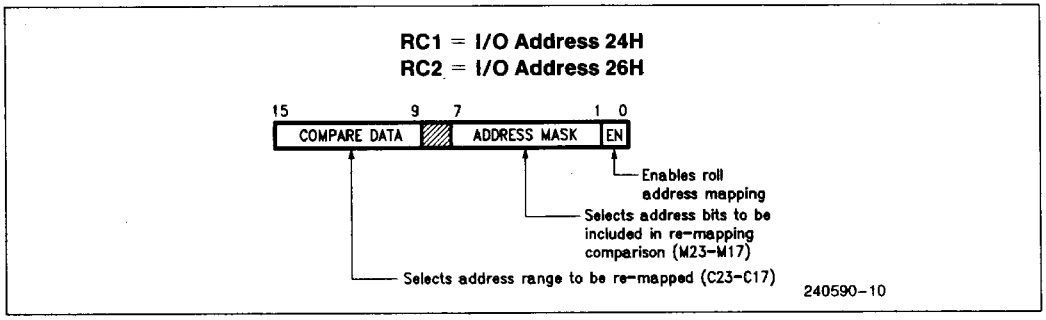


Figure 2.9. Bit Functions of the Roll Compare Registers

The compare enable bit (EN) enables roll address checking for that register. If EN is set, roll addressing is enabled for that register. If EN is cleared, roll addressing is disabled for that register and its address mask and compare data bits are ignored. Upon reset, both roll compare registers are disabled and the compare data and address mask bits are undefined.

The roll compare registers RC1 and RC2 are located at the I/O addresses 24H and 26H respectively. They can both be read and written to until the lock bit is set in the memory configuration register. Once the lock bit is set, these registers are not externally accesssible until the 82335 SX is reset by activating the SYSRESET input.

Example #1

— 4 Banks of 256K x 1 DRAM Installed

— S640 = 0, ROMEN# = 1, ENADP# = 0, ENV# = 0 (384K Roll-Over Avail.)

— Top of Physical Address Space = 1FFFFFH (2M)

— Roll Decode Range Selected = 380000-3DFFFF (384K)

Register	EN	C23-C17	M23-M17	Address Range
RC1	1	001110x	1111110	380000-3BFFFF (256K)
RC2	1	0011110	1111111	3C0000-3DFFFF (128K)

In this example, both roll compare registers are required to decode the 384K roll address area.

Example #2

— 2 Banks of 1M x 1 DRAM Installed

— S640 = 1, ROMEN# = 1, ENADP# = 0, ENV# = 0 (256K Roll-Over Avail.)

— Top of Physical Address Space = 3FFFFFH (4M)

— Roll Decode Range Selected = 600000H-63FFFFH (256K)

Register	EN	C23-C17	M23-M17	Address Range
RC1	1	011000x	1111110	600000H-63FFFFH (256K)
RC2	0	xxxxxxx	xxxxxxx	None

In this example, the 256K roll address area can be decoded with only one register. Therefore, the other register has been disabled.

2.3.4.3 Address Range Compare Registers

Two address compare registers, CC0 and CC1, are used to differentiate local memory accesses from system memory accesses (off-board memory). When a memory access is initiated, the input address is compared with the address range programmed into the address range compare registers. If the input address is within the local memory space, then the 82335 SX sets the OBMEM output high and initiates a local memory cycle. If the memory address input is outside the local memory address space, then the OBMEM output is cleared and the 286 style control signals S0#, S1#, and M/IO286# are output to initiate an off-board memory access.

If either of the roll compare registers (RC1 or RC2) are enabled, any address translation required is done before the input address is compared with the address ranges in address compare registers.

Both address range compare registers work identically. When an address comparison is made, the output of both registers is logically "ORed" together. Therefore, either register can be used for address range checking. The second address range com-

pare register was included for a feature that is not implemented. It is recommended that the unused register be disabled by clearing its compare enable bit (EN). The following paragraphs refer to the active address range compare register.

The address range compare register is designed to indicate the location and size of the local memory address space. This address space must start at address 000000H for proper DRAM addressing. The size of the local memory space is designed to be programmed into the address range compare register by the BIOS. For dynamic memory sizing, the BIOS could execute a memory autoscan routine that would determine the DRAM size being used and the number of banks installed. The size of the local memory address space could be calculated from this data and programmed into the address range compare register.

If an address space greater than 512K is programmed into the address range compare register, a memory access in the 080000H–0FFFFFH address range may not be considered a local memory access. This depends upon the base memory and shadow options selected in the memory configuration register. If a 512K base memory is selected (S640 = 0), then the address range 080000H–09FFFFH is considered non-local. If the BIOS (0E0000H–0FFFFFH), adapter (0C0000H–0DFFFFH), or video (0A0000H–0BFFFFH) areas are enabled (not shadowed), then each area not shadowed is considered non-local memory.

The size and location of the local memory address space is set by programming three sections in the address range compare register. These sections are referred to as the "compare data", "address mask", and "compare enable" sections. These sections work in a similar manner to the roll compare register sections. Figure 2.10 shows the three parts of the address compare register. Each of these address compare register parts are described in the following paragraphs.

The compare data bits (C23–C19) are used to specify the starting address of the local memory address space. These bits should all be programmed to zeroes to start the local memory address space at 000000H.

The address mask bits (M23–M19) are used to select the size of the local memory address space. For each mask bit that is set, the corresponding input address bit and compare data bit are compared for a match. If a mask bit is cleared, the corresponding input address bit and compare data bits are ignored. Table 2.5 shows how to program the compare data and address mask bits for all valid local memory configurations.

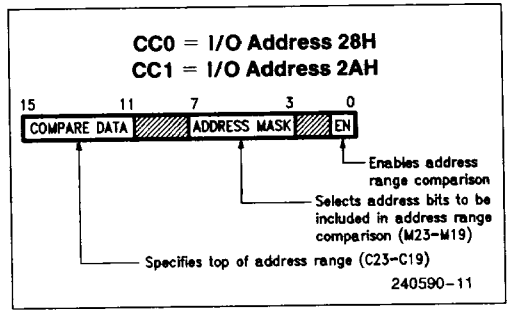


Figure 2.10. Bit Functions of the Address Range Compare Registers

Table 2.5. Address Range Compare Register Programming

Register	EN	C23–C19	M23–M19	Address Range
CC0	1	00000	11111	000000H–07FFFFH (512K)
CC0	1	0000X	11110	000000H–0FFFFFH (1M)
CC0	1	000XX	11100	000000H–1FFFFFH (2M)
CC0	1	00XXX	11000	000000H–3FFFFFH (4M)
CC0	1	0XXXX	10000	000000H–7FFFFFH (8M)

NOTES:
1. This table assumes register CC1 is disabled (EN = 0).
2. Register CC1 could be enabled over the above address ranges in place of register CC0.

The compare enable bit (EN) enables address range checking for that register. If EN is set, address range checking is enabled for that register. If EN is cleared, address range checking is disabled for that register and its address mask and compare data bits are ignored. If both address range compare registers are disabled, then all memory accesses will be non-local. Upon reset the CC0 register is enabled and programmed for a 512K local memory space, and the CC1 register is disabled.

The address compare registers CC0 and CC1 are located at the I/O addresses 28H and 2AH respectively. They are both read/writable until the lock bit is set in the memory configuration register. Once the lock bit is set, these registers are not externally accessable until the 82335 SX is reset by activating the SYSRESET input.

2.3.4.4 Granularity Enable Register

The Granularity Enable register is located at I/O location 2CH. This register is not in the 82335. It has two functions.

The EXGRAN bit (bit 0) enables extended granularity. If EXGRAN = 0, then the 82335 SX will shadow the same way the 82335 does with 128K granularity. The Extended Granularity Register will have no effect. EXGRAN = 0 upon powerup.

If EXGRAN = 1, then the 82335 will shadow and write-protect with 32 Kbyte granularity according to the Extended Granularity register.

The SPDSEL bit (bit 15) selects which speed the 82335 SX will run at. If SPDSEL = 0, the 82335 SX will assume a 32 MHz EFI (16 MHz operation). PCLK# will be a divide by 2 of EFI (see Figure 4.1A), DRAM control will correspond to Table 2.3A, and NON-TURBO mode accesses will take 6 T-states. If SPDSEL = 0 and EFI is 32 MHz, the A.C. Specifications will match the 16 MHz column in the A.C. Specifications Table. SPDSEL = 0 upon powerup.

If EFI = 40 MHz (20 MHz operation) SPDSEL should be set to 1 immediately by the BIOS. If SPDSEL = 1, PCLK# will be a divide by 2.5 of EFI (see Figure 4.1B) DRAM control will correspond to Table 2.3B, and NON-TURBO mode accesses will take 8 T-states. If SPDSEL = 1 and EFI is 40 MHz, the A.C. Specifications will match the 20 MHz column in the A.C. Specifications Table.

When writing to the SPDSEL bit, the PCLK output will change between a divide by 2 and a divide by 2.5 of EFI before the 82335 SX returns READYSX# to end the write cycle. Due to internal synchronization requirements there may be a delay of up to 20 wait states before READYSX# is activated to terminate the cycle.

When writing to the Granularity Enable register all other bits besides bits 0 and 15 should be set to zero. Once the LOCKbit is set, this register is not externally accessible until the 82335 SX is reset by activating the SYSRESET input.

1

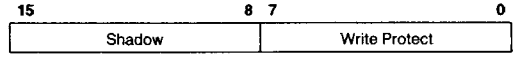
2.3.4.5 Extended Granularity Register

The Extended Granularity register is located at I/O address 2EH. This register is not in the 82335. Its function is to increase the granularity of shadowing and write-protect for the address range 0C0000H–0FFFFFH. EXGRAN must equal 1 for this register to have any effect on 82335 SX operation.

Shadowing can only occur if the corresponding bit in the configuration register is inactive. For example, ENADP# must be high (shadowing enabled) if any 32 Kbyte block in the adapter ROM space is to be shadowed. Similarly, if no 32 Kbyte block in the adapter ROM space is to be shadowed, then ENADP# should be low. ROMEN# works the same way. The function of each of the bits in the Extended granularity register is shown in Figure 2.10. Once the lock bit is set this register is not externally accessable until the 82335 SX is reset by activating the SYSRESET input. Note that the write-protect bits take effect immediately upon programming. They do not wait for the LOCK bit to be set to take effect.

When the extended granularity feature is used and BIOS is shadowed from ROM, it is recommended to shadow the entire BIOS from 0E0000h to 0FFFFFh. When only part of the BIOS ROM is shadowed with extended granularity, any unshadowed block between 0E0000h and 0FFFFFh will **not** be accessible to the CPU.

Extended Granularity Register = I/O Location 2EH



Bit Position	Name	Function
15	ROMEN7#	0 = Disable Shadow F8000H–FFFFFH 1 = Enable Shadow F8000H–FFFFFH
14	ROMEN6#	0 = Disable Shadow F0000H–F7FFFH 1 = Enable Shadow FF7FFFH
13	ROMEN5#	0 = Disable Shadow E8000H–EFFFFH 1 = Enable Shadow E8000H–EFFFFH
12	ROMEN4#	0 = Disable Shadow E0000H–E7FFFH 1 = Enable Shadow E0000H–E7FFFH
11	ROMEN3#	0 = Disable Shadow D8000H–DFFFFH 1 = Enable Shadow D8000H–DFFFFH
10	ROMEN2#	0 = Disable Shadow D0000H–D7FFFH 1 = Enable Shadow D0000H–D7FFFH
9	ROMEN1#	0 = Disable Shadow C8000H–CFFFFH 1 = Enable Shadow C8000H–CFFFFH
8	ROMEN0#	0 = Disable Shadow C0000H–C7FFFH 1 = Enable Shadow C0000H–C7FFFH
7	WRPRT7	Shadow RAM at F8000H–FFFFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
6	WRPRT6	Shadow RAM at F0000H–F7FFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
5	WRPRT5	Shadow RAM at E8000H–EFFFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
4	WRPRT4	Shadow RAM at E0000H–E7FFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
3	WRPRT3	Shadow RAM at D8000H–DFFFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
2	WRPRT2	Shadow RAM at D0000H–D7FFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
1	WRPRT1	Shadow RAM at C8000H–CFFFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)
0	WRPRT0	Shadow RAM at C0000H–C7FFFH in Read/Write Mode 0 = Read/Write (Default), 1 = Read Only (Write Protected)

Figure 2.11. Extended Granularity Register

2.3.5 CHIP SELECT SIGNALS

The address mapper/decoder uses the configuration, roll compare, and address range compare register contents along with input addresses to generate the following output signals:

ROMCS0# — ROM 0 Chip Select

ROMCS1# — ROM 1 Chip Select

LMEGCS — Lower Meg Chip Select

OBMEM — On-Board Memory Address Range

The ROM chip select signals are functions of the ROMSIZE and ROMEN# bits in the configuration register as well as the input address. If ROM shadowing is enabled (ROMEN# = 1), then the ROM chip select outputs will be disabled for the 0E0000H–0FFFFFH address range. The ROM chip select signals for the FE0000H–FFFFFFH address range are not affected by the shadowing options selected. If ROM shadowing is disabled or the input address is between FE0000H and FFFFFFH, then the ROM chip select outputs will be activated as follows:

If ROMSIZE = 0 (256K ROM)

ROMCS0# decodes the address ranges 0E0000H–0EFFFFH and FE0000H–FEFFFFH.

ROMCS1# decodes the address ranges 0F0000H–0FFFFFH and FF0000H—FFFFFFH.

If ROMSIZE = 1 (512K ROM)

ROMCS0# is inactive

ROMCS1# decodes the address ranges 0E0000H–0FFFFFH and FE0000H–FFFFFFH.

The lower meg chip select output (LMEGCS) is a function of both the input address and M/IO# inputs. It is activated whenever a memory address within the first megabyte of memory is decoded. It is inactive during I/O cycles.

The on-board memory output (OBMEM) is a function of the input address, M/IO#, address range comparators, roll comparators, and the bits ROMEN#, ROMSIZE, DSIZE, and S640 in the configuration register. It is used to differentiate local DRAM access from system RAM, ROM, or I/O accesses. OBMEM is active (high) during local DRAM accesses. If the M/IO# or address input signals are left floating, (during a refresh or DMA cycle for example) the OBMEM output will be undefined.

2.4 Ready Generator

Every 386 SX microprocessor bus cycle must be terminated by a ready signal to the processor. The 82335 SX generates this ready signal by translating external and internal ready inputs to a single ready output (READYSX#). The 82335 SX internally generates a ready signal for local DRAM cycles, on-chip I/O cycles, and numeric coprocessor cycles. For all other cycles (system I/O, system memory, etc.), the 82335 SX translates the ready input READY286# to the 386 SX compatible READYSX# output. The 82335 SX input EXTRDY# can be used to delay or mask the READYSX# output.

For on-chip I/O and local memory cycles, the internal ready generator in the 82335 SX determines the appropriate number of wait states to insert (if any), and activates the READYSX# output at the correct time. The READYSX# pulse can be delayed during local memory cycles by deactivating the EXTRDY input. If EXTRDY is sampled inactive, then the READYSX# output will be delayed until EXTRDY is sampled active. EXTRDY is sampled on the rising edge of CLK2 during phase 1 of each T2 and T2P state.

The external input READY286# is used to terminate all cycles other than local memory cycles, local I/O cycles, or numeric coprocessor cycles.

The READY286# input is designed to be driven by the 82230 READY# pin and is used to identify the completion of system bus cycles. If the READY286# input is sampled active during a system bus cycle and the EXTRDY input is high, the 82335 SX generates a READYSX# pulse. The READY286# input is sampled on the falling edge of PCLK# when an internal clock (half the frequency of PCLK#) is high. This synchronizes ready signals between the 82230/82231 and the 386 SX. The READY286# input is only sampled during system bus cycles.

The READYNPX# input is ignored by the 82335 SX. For Numeric Coprocessor cycles the 82335 SX will activate READYSX# after 1 wait-state. If no coprocessor is detected upon power up, the 82335 SX will not generate READYSX#, for numerics coprocessor cycles. If no coprocessor is present the 82335 SX will output S0# and S1# to the 82230/82231. The 82230/82231 will activate READY286# after completing a standard PC-AT numerics coprocessor cycle.

Deactivation of EXTRDY will delay READY SX# on numerics cycles the same way as it does on local DRAM cycles (if a coprocessor is present).

If EXTRDY is inactive (low) when the READY286# input is sampled, then no READYSX# pulse is generated. READY286# is **masked** (not delayed) if EXTRDY is low when sampled.

Setup and hold times for the READY286#, and EXTRDY inputs must be met to guarantee correct operation.

2.5 Bus Cycle Translator

The 82335 SX has a built in interface unit that translates 386 SX processor control signals to 80286 control signals. This bus cycle translator identifies the bus cycle being performed, monitors the CPU T-states, and outputs 80286-like bus control signals to the 82230/82231 and other components in a PC/AT system. It also receives 80286 control inputs and translates them into 386 SX processor compatible signals when required.

As the bus cycle translator monitors control inputs from both the 386 SX processor and the 82231, it determines what type of cycle is being requested. If one of the following cycles is being requested:

1. I/O Access
2. System Memory Access
3. Halt/Shutdown
4. Interrupt

then the bus tracker monitors the timing of the bus cycle and simultaneously outputs 80286-type bus control signals. The control signals output are S0#, S1#, and M/IO286#. The S0# and S1# outputs are not activated for local memory accesses, for numerics coprocessor accesses when a coprocessor is present or for accesses to the 82335 SX on-chip I/O (programming of the on-chip registers).

In addition to controlling status output to the 82230/82231, the bus cycle translator also controls the hold request (HRQSX) input to the 386 SX processor. A hold request signal coming from the 82230 (HRQ286) is translated into a 386 SX processor-compatible output and driven to the 386 SX processor. The 386 SX processor responds with a hold acknowledge (HLDASX) to the 82335 SX which then translates that to a HLDA output to the 82230/82231.

2.6 Math Coprocessor Interface

The 82335 SX provides interface signals between the 386 SX CPU and 387 SX numeric coprocessor to allow the 387 SX to function in a PC/AT environment with proper error handling. The 82335 SX can also identify 387 SX bus cycles and has built-in logic to automatically sense whether a 387 SX coprocessor is present in the system. Figure 2.12 shows a diagram of the coprocessor interface signals.

During coprocessor bus cycles, the 386 SX CPU initiates I/O accesses to addresses above 800000H. When a 387 SX is installed the 82335 SX recognizes these I/O accesses as coprocessor bus cycles and inhibits the status outputs S0# or S1#. If there is no 387 SX installed, the 82335 SX will activate the S0# and S1# status outputs when a coprocessor bus cycle is initiated.

The 82335 SX can detect the presence of a 387 SX coprocessor by sampling the ERROR# input during a system reset. The ERROR# input is sampled at the falling edge of the SYSRESET pulse. If ERROR# is sampled low, a 387 SX coprocessor is present. If ERROR# is sampled high, there is no coprocessor. The ERROR#, and BUSYNPX# inputs contain internal pull-up resistors to prevent false inputs when there is no coprocessor in the system.

If the 82335 SX does not detect a coprocessor in the system, the ERROR# and PEREQNPX inputs are ignored, and the PEREQSX and BUSYSX# outputs do not follow the PEREQNPX and BUSYNPX# inputs. If there is no coprocessor, the 82335 SX forces the PEREQSX output low. This insures that the 386 SX does not get any false processor extension requests. To prevent a 387 SX instruction from holding up the processor by waiting for the BUSYSX# signal to go inactive, the BUSYSX# output toggles high and low when there is no coprocessor. It toggles every time REFRESH# is activated.

If a coprocessor is present, the 82335 SX translates the BUSYNPX# and PEREQNPX inputs into BUSYSX# and PEREQSX outputs to the processor. During normal operation the BUSYNPX# and PEREQNPX signals are passed straight through to the BUSYSX# and PEREQSX outputs. There are two exceptions to this: during a system reset and when a numeric coprocessor error has occured.

During a system reset the BUSYSX# output is forced low to induce a processor self-test. The BUSYSX# output is deactivated on the falling edge of ADS# during the first bus cycle and follows the BUSYNPX# input thereafter.

When a numeric coprocessor error occurs, both the BUSYSX# and PEREQSX outputs are activated. Activation of the ERROR# input causes the current state of the BUSYSX# output to be latched and held. When the BUSYNPX# input deactivates, the PEREQSX output is activated. This holds processing on the 386 SX processor while completing the 387 SX coprocessor transfers. Both the BUSYSX# and PEREQSX outputs deactivate and return to normal

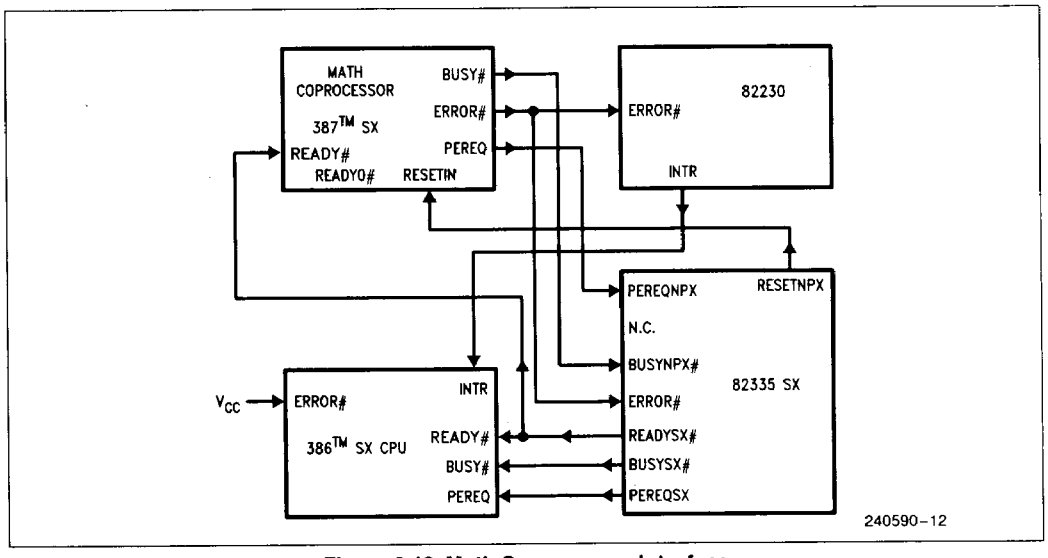


Figure 2.12. Math Coprocessor Interface

operation when an I/O write to address 0F0H is executed.

The 82335 SX handles unmasked overflow/underflow exceptions the same way PC/AT systems handle them. Both unmasked and masked overflow/underflow exceptions are treated like masked exceptions. If an error is triggered by an overflow/underflow exception, a value is written out to memory.

2.7 Clock Generator

The 82335 SX clock generator is used to synchronize the CPU, coprocessor, and peripherals by converting an input frequency into the system clock outputs CLK2 and PCLK#. The input frequency is obtained from an external oscillator connected to the 82335 EFI pin. A standard TTL oscillator can be used for this. This EFI input is internally buffered and output to the 386 SX processor and 387 SX coprocessor via the CLK2 output. It is also divided by 2 (16 MHz) or 2.5 (20 MHz) and output to the 82230/82231 using the PCLK# output.

Upon power-up both the CLK2 and PCLK# outputs are active. They are not phase synchronized, however, until after the falling edge of the RESETSX input. To synchronize the clocks, PCLK# is held high until the rising edge of CLK2. The second falling edge of PCLK# after this CLK2 edge will start a phase two clock cycle. Figure 4.2a shows the clock synchronization sequence. A CPU reset using only the RESETCPU input will not affect clock synchronization.

2.8 Reset Synchronizer

The 386 SX microprocessor requires a synchronous reset input to initialize the processor. The 82335 SX has a reset synchronizer that has two asynchronous reset inputs and generates synchronous reset signals to both the processor and numeric coprocessor. The two reset inputs to the 82335 SX (RESET CPU and SYSRESET) are used to initiate either a CPU reset or an entire system reset. The 82335 SX internal registers and output signals are initialized following a system reset. These internal registers are not affected by a processor reset.

The RESETCPU input is used to reset the processor only. This is frequently used to switch the processor from protected mode to real mode. When the RESETCPU input is activated, the 82335 SX synchronizes and activates the processor reset output (RESETSX). The RESETCPU input must be held active for at least 16 CLK2 cycles to guarantee a sufficient RESETSX pulse width to the processor. No other outputs or internal registers are affected by this reset. Figure 4.2b in the A.C. Timing Diagram Section shows processor reset timing.

The 82335 SX SYSRESET and RESETCPU inputs are used together to initiate a system wide reset and initialize the 82335 SX. When SYSRESET and RESETCPU are concurrently activated, both the processor reset (RESETSX) and coprocessor reset (RESETNPX) signals are activated. The 82335 SX internal registers and output signals are initialized to the values shown in Table 2.6.

Table 2.6. 82335 SX Initial State after System Reset

Internal Register Status			
Register	**I/O Address**	**Status**	**Bit Pattern**
Mem. Config.	22H	Shadow = Disabled Base Mem. = 512K DRAM Size = 256K Interleave = 1 Bank ROM Size = 256K VRO = Read/Write Lock = Unlocked	0000000000000000
RC1 RC2	24H 26H	Disabled Disabled	xxxxxxxxxxxxxxx0 xxxxxxxxxxxxxxx0
CC0 CC1	28H 2AH	Enabled 000000H–07FFFFH Disabled	00000xxx11111xx1 xxxxxxxxxxxxxx0
PARCHKEN	61H	Enabled	xxxxx0xx
Granularity Enable	2CH	EXGRAN = Disabled Speed = 16 MHz	0000000000000000
Extended Granularity	2EH	Disabled	0000000000000000

Output Pin Status		
Low	**High**	**Undefined**
BUSYSX# HLDA HRQSX PEREQSX OBMEM WE#	CASx# RASx# DEN# NA# PERROR# READYSX# ROMCSx# S0# S1#	LMEGCS# MA0–MA9 M/IO286# DIR

NOTE:
x in register bit pattern denotes undefined bit state.

When a system reset occurs, the 82335 SX forces the BUSYSX# output low to initiate a processor self-test. To guarantee correct processor self-test results, the SYSRESET and RESETCPU inputs must be held active for at least 80 CLK2 cycles. If the system designer chooses not to utilize the data returned by the processor self-test, the SYSRESET and RESETCPU input signals only need to be held active for 16 CLK2 cycles to guarantee correct system reset.

During a system reset the following sequence of events occurs:

- RESETSX and RESETNPX are activated.
- The DRAM control signals RASx#, CASx#, and DEN# are deactivated.
- BUSYSX# is held low to induce processor self-testing.
- The 82335 SX internal registers and output pins are initialized to the values shown in Table 2.6.
- The ERROR# input is sampled on the falling edge of SYSRESET to determine if a numeric coprocessor is present. If the ERROR# input is sampled low a coprocessor is present, otherwise there is no coprocessor.
- The PCLK# output is synchronized with the CLK2 output.
- RESETSX and RESETNPX are deactivated.

2.9 Parity Generator/Checker

The 82335 SX has a built-in parity generator and checker to maintain data integrity for the local memory. During local memory write or DMA write cycles the 82335 SX generates two parity outputs from the data inputs D0–D15. The 82335 SX calculates even parity for both the high byte and low byte and outputs the results on the parity high (PARH) and parity low (PARL) pins. During local memory read and DMA read cycles the 82335 SX compares the data (D0–D15) and parity (PARH and PARL) inputs and generates an error signal (PERROR#) if a parity error is detected. PARH and PARL are three-state input/output pins designed to directly drive the DRAM.

If a parity error is detected, the 82335 SX drives the PERROR# output low and latches it. PERROR# is cleared by either a system reset (SYSRESET pulsed high) or by disabling parity checking in the 82335 SX. The following paragraph details how to enable/disable parity checking.

Parity checking is enabled/disabled by a one bit parity check enable register (PARCHKEN). This register is located in bit 2 of the I/O address 61H. When programmed to "0", parity checking is enabled. When programmed to "1", parity checking is disabled and the PERROR# output is deactivated (PERROR# > V_{OH} min).

The PARCHKEN register is a write-only register. In a system that contains both an 82335 SX and 82231, a write to I/O port 61H will write to the parity registers in both chips. A read from I/O port 61H will read from the 82231 register. Care must be taken when writing to this register since the 82231 utilizes several other bits at I/O location 61H register to control other system functions.

2.10 General System Considerations

1. The RAS0#–RAS3#, CASH0#–CASH3#, and CASL0#–CASL3# output buffers are designed to directly drive the heavy capacitive loads of the dynamic RAM arrays. To keep the RAM driver outputs from ringing excessively in the system environment it is necessary to match the output impedance with the RAM array by using series resistors. Each application may have different impedance characteristics and may require different series resistance values. The series resistance values should be determined for each application.
2. If the capacitive loading on the MA0–MA9 outputs exceeds the maximum capacitive loading specification (see AC DRAM Timing Specifications), then buffering of the MA0–MA9 outputs is recommended. The MA0–MA9 outputs can directly drive approximately two banks of memory.
3. The NA# pin on the 82335 SX must be connected to NA# on the 386 SX processor.
4. If there is no DRAM installed in the physical address space 080000H–0FFFFFH, then shadowing and roll address mapping must be disabled.
5. When setting the LOCK bit in the configuration register, the entire contents of the configuration register must be written. Writing to a register in the 82335 SX will overwrite all bits in that register.

3.0 MECHANICAL DATA

3.1 Package Dimensions

The 82335 SX is available in a 132 lead plastic quad flat pack (PQFP) package. Table 3.1 and Figures 3.1–3.5 show the physical dimensions of this package.

Table 3.1. Intel Case Outline Dimensions for 132 Lead Plastic Quad Flat Pack 0.025 Inch Pitch

Symbol	Description	Inch		mm	
		Min	Max	Min	Max
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 REF		20.32 REF	
L1	Foot Length	0.020	0.030	0.51	0.76
Issue	IWS Preliminary 1/15/87				

Symbol List

Letter or Symbol	Description of Dimensions
A	Package Height: Distance from Seating Plane to Highest Point of Body
A1	Standoff: Distance from Seating Plane to Base Plane
D/E	Overall Package Dimension: Lead Tip to Lead Tip
D1/E1	Plastic Body Dimension
D2/E2	Bumper Distance
D3/E3	Footprint
L1	Foot Length

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane H located at the mold parting line and coincident with the bottom of the lead where lead exits plastic body.
3. Datums A B and D to be determined where center leads exit plastic body at datum plane H.
4. Controlling Dimension, Inch.
5. Dimensions D1, D2, E1, and E2 are measured at the mold parting line and do not include mold protrusion. Allowable mold protrusion is 0.18 mm (0.007 in) per side.
6. Pin 1 identifier is located within one of the two zones indicated.

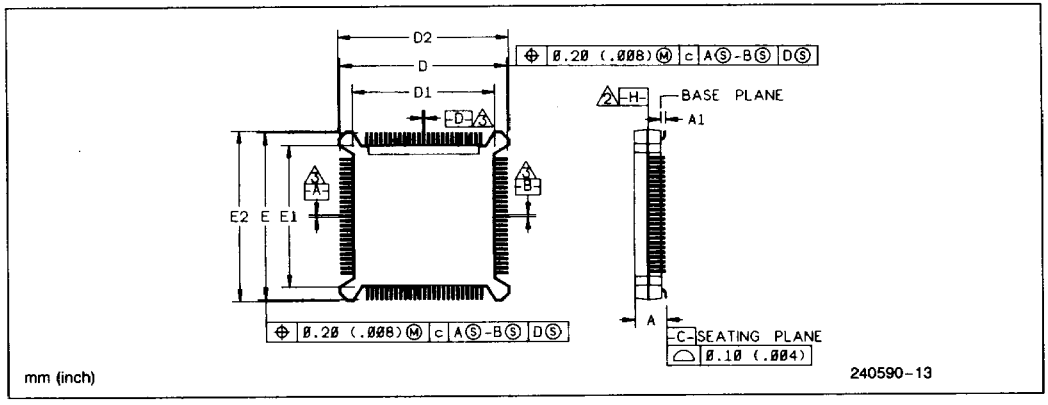


Figure 3.1. Principal Dimensions and Datums

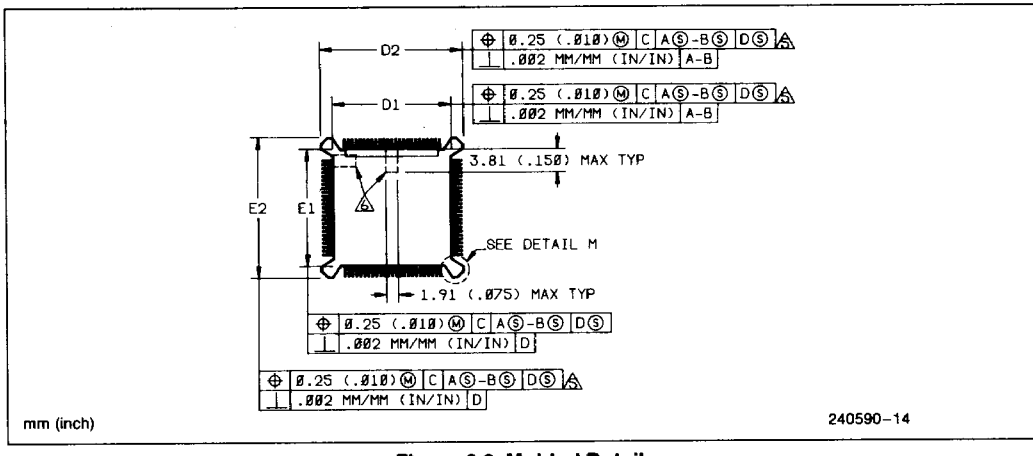


Figure 3.2. Molded Details

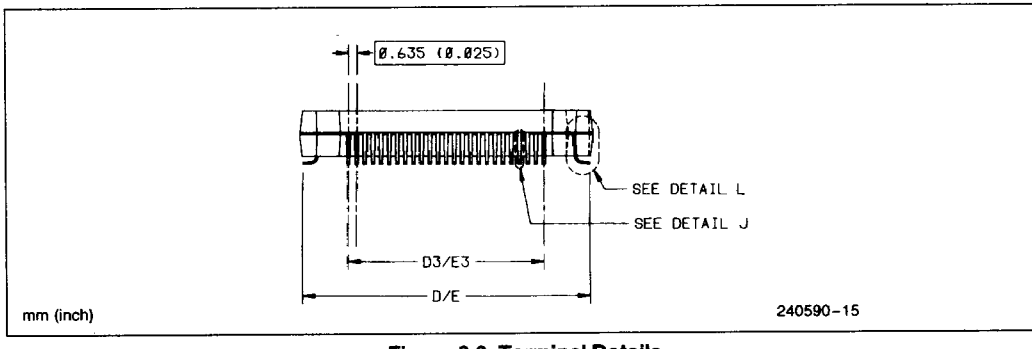


Figure 3.3. Terminal Details

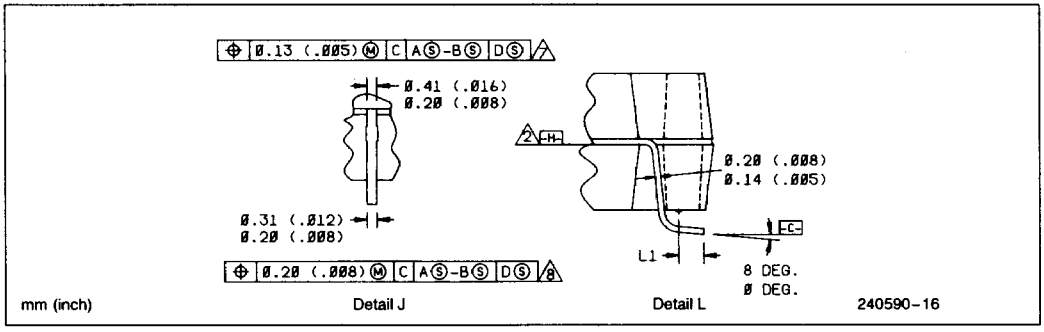


Figure 3.4. Typical Lead

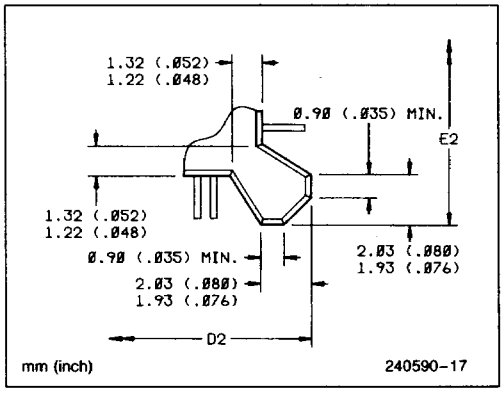


Figure 3.5. Detail M

3.2 Package Thermal Specifications

The 82335 SX is specified for operation when the case temperature is within the range of 0°C–85°C. The case temperature may be measured in any environment to determine whether the 82335 SX is within the specified range of operation. The case temperature should be measured at the center of the top surface opposite the pins. Table 3.2 shows the thermal resistance for this package.

Table 3.2. Thermal Resistances (°C/Watt)

θ Junction to Case	12
θ Junction to Ambient	40

4.0 ELECTRICAL DATA

4.1 Maximum Ratings

Table 4.1. Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	−65°C to +150°C
Case Temperature under Bias	−65°C to +110°C
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V
Voltage on Other Pins	−0.5V to V_{CC} + 0.5V

Table 4.1 is a stress rating only, and functional operation at the maximums is not guaranteed. Functional operating conditions are given in Section 4.2, D.C. Specifications and Section 4.3, A.C. Specifications.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the 82335 SX contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

1

4.2 D.C. Electrical Specifications

Functional Operating Range: V_{CC} = 4.5V to 5.5V, T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{ILC}	EFI Input Low Voltage	−0.3	0.8	V	(Note 1)
V_{IHC}	EFI Input High Voltage	2.4	V_{CC} + 0.3	V	
V_{OLC}	CLK2 Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OHC}	CLK2 Output High Voltage	V_{CC} − 0.8	V_{CC} + 0.3	V	I_{OH} = −1 mA
V_{OLP}	PCLK# Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OHP}	PCLK# Output High Voltage	V_{CC} − 0.5	V_{CC} + 0.3	V	I_{OH} = −1 mA
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −1 mA
I_{LI}	Input Leakage Current for All Pins except Group One		±15	μA	0 < V_{IN} < V_{CC} (Note 2)
I_{IL}	Input Sustaining Current for Group One Pins		−400	μA	V_{IL} = 0.45V, (Note 2)
I_{LO}	3-State Output Leakage Current		±15	μA	V_{OL} < V_{IN} < V_{CC}
I_{CC}	Supply Current		150	mA	(Note 3)
C_{IN}	Input Capacitance		10	pF	(Note 4)
C_{OUT}	Output or I/O Capacitance		12	pF	(Note 4)

NOTES:
1. The min value, −0.3, is not tested.
2. Group one = BUSYNPX#, ERROR#, M/IO#, and D/C#. All these inputs have internal pullup resistors.
3. CLK2 = 32 MHz or 40 MHz, maximum loading on DRAM address and control pins.
4. Not tested. These are guaranteed by design characterization.

4.3 A.C. Specifications

Unless otherwise specified, all timings are referenced at V = 1.5V, and all timing values are in nano-seconds, all voltages are in volts, and all output loadings are 50 pF.

A.C. Timings for Clocks

Symbol	Parameter	Figure	16 MHz		20 MHz		Units	Notes
			Min	Max	Min	Max		
	Operating Frequency			16		20	MHz	
T1	EFI Period	4.1	31	33	25	27		
T2	EFI High Time	4.1	12		11		ns	at 1.5V
T3	EFI Low Time	4.1	12		11		ns	at 1.5V
T4	EFI Fall Time	4.1		6		6	ns	2.4V to 0.4V (Note 1)
T5	EFI Rise Time	4.1		6		6	ns	0.4V to 2.4V (Note 1)
T6	CLK2 Period	4.1	31	33	25	27		
T7a	CLK2 High Time	4.1	9		8		ns	at 2V
T7b	CLK2 High Time	4.1	5		5		ns	at (V_{CC} − 0.8)
T8a	CLK2 Low Time	4.1	9		8		ns	at 2V
T8b	CLK2 Low Time	4.1	7		6		ns	at 0.8V
T9	CLK2 Fall Time	4.1		8		8	ns	(V_{CC} − 0.8) to 0.8 (Note 1)
T10	CLK2 Rise Time	4.1		8		8	ns	0.8 to (V_{CC} − 0.8) (Note 1)
T11	PCLK# Delay from CLK2	4.1		10		14		

Output Loadings: CLK2: 50 pF (20 MHz), 75 pF (16 MHz) Max
PCLK#: 75 pF Max

NOTE:
1. These are not tested. They are guaranteed by design characterization.

A.C. Timings for DRAM Controller Unit

Unless otherwise specified, all A.C. timings referenced to CLK2 refer to the CLK2 rising edge in phase one.

Symbol	Parameter	Figure	16 MHz		20 MHz		Unit	Notes
			Min	Max	Min	Max		
T12a	RAS# Active Delay from CLK2	4.3		62		50	ns	(Note 1)
T12b	RAS# Active Delay from CLK2			62		30	ns	(Note 2)
T13	RAS# Inactive Delay from CLK2	4.3	4		4		ns	
T14	Row Addr Setup to RAS# Active	4.3	15		15		ns	(Note 8)
T14a	Row Addr Setup to RAS# Active	4.3	2		2		ns	(Notes 9, 10)
T15	Row Addr Hold from RAS# Active	4.3	20		15		ns	(Note 8)
T15a	Row Addr Hold from RAS# Active	4.3	15		10		ns	(Notes 10, 12)
T16	RAS# Precharge Time	4.5	91		70		ns	(Note 1)
T16a	RAS# Precharge Time		91		91			(Note 2)
T17	Col Addr Setup to CAS# Active	4.3	7		15		ns	(Note 8)
T17a	Col Addr Setup to CAS# Active		0		2			(Notes 9, 10)
T18	Col Addr Hold from CAS# Active	4.3	25		20		ns	(Note 8)
T18a	Col Addr Hold from CAS# Active	4.3	23		18		ns	(Note 11)
T19a	CAS# Active Delay from CLK2	4.3		55		45	ns	(Note 3)
T19b	CAS# Active Delay from CLK2 (Read)	4.6		43		34	ns	(Note 2)
T19c	CAS# Active Delay from CLK2 (Write)	4.4	19	39	15	34	ns	(Note 4)

Maximum Output Loadings: WE#: 270 pF MA0–MA9: 240 pF RAS#: 120 pF CAS#: 75 pF

A.C. Timings for DRAM Controller Unit (Continued)

Unless otherwise specified, all A.C. timings referenced to CLK2 refer to the CLK2 rising edge in phase one.

Symbol	Parameter	Figure	16 MHz		20 MHz		Unit	Notes
			Min	Max	Min	Max		
T20	CAS# Inactive Delay from CLK2	4.3	6		6		ns	
T21a	CAS# Active Pulse Width	4.4	37		31		ns	(Note 1)
T21b	CAS# Active Pulse Width	4.6	62		50		ns	(Note 2)
T22a	CAS# Precharge Pulse Width	4.4	22		21		ns	(Note 1)
T22b	CAS# Precharge Pulse Width	4.6	50		40		ns	(Note 2)
T23a	RAS# Hold from CAS# Active	4.5	37		31		ns	(Note 1)
T23b	RAS# Hold from CAS# Active		62		50		ns	(Note 2)
T24	Read Data Setup before CLK2	4.4	11		9		ns	(Note 5)
T25	Read Data Hold from CAS# Inactive	4.4	2		2		ns	
T26	Write Data Delay from CLK2	4.4		9		6	ns	(Note 6)
T27	Write Data Hold after CLK2	4.4	0		0		ns	
T28	PARL/PARH Setup to CAS# Active	4.4	0		0		ns	
T29	PARL/PARH Hold from CAS# Active	4.4	28		20		ns	
T30	DEN# Active from CLK2	4.4	0	20	0	20	ns	
T31	DEN# Inactive from CLK2	4.4	6		6		ns	
T32	DIR Delay from CLK2	4.4	25	55	20	45	ns	
T33	WE# Setup to CAS# Active	4.6	5		5		ns	
T34	386 SX CPU Addr Setup to CLK2	4.3	26		23		ns	
T35a	Col Address Delay from CLK2	4.4		45		26	ns	(Note 8)
T35b	Col Address Delay from CLK2	4.4		55		35	ns	(Note 9)
T36	WE# Hold from CAS# Active (Write)	4.6	30		25		ns	
T37	WE# Hold from CAS# Inactive (Read)	4.6	0		0		ns	
T79	RAS# Active Delay from MEMx#	4.10		55		55	ns	(Note 7)
T80	RAS# Pulse Width	4.10	150		115		ns	(Note 7)
T81	CAS# Inactive from Memx#	4.10	9	40	7	40	ns	(Note 7)
T82	CAS# Active Delay from RAS# Active	4.10	55	100	45	100	ns	(Note 7)
T83a	Refresh Pulse Width (1 Memory Bank)	4.13	280		280		ns	
T83b	Refresh Pulse Width (2 Memory Bank)	4.13	310		310		ns	
T83c	Refresh Pulse Width (4 Memory Bank)	4.13	370		370		ns	
T84	DEN# Active to CAS# Active Delay	4.5	7		7		ns	

NOTES:
1. F1/F4 mode.
2. WO1/WO2 mode.
3. All F1/F4 cycles except page mode write.
4. F1/F4 page mode write cycles and WO1/WO2 mode write cycles.
5. For parity checker.
6. To guarantee PARL, PARH timings.
7. DMA/MASTER mode timings.
8. With C_{Load} = 50 pF.
9. With MA0–MA9 C_{Load} = 240 pF.
10. With RAS# C_{Load} = 120 pF.
11. With CAS# C_{Load} = 75 pF.
12. If MA0–MA12 use buffers, then minimum buffer delay must be added to T15a.

Other A.C. Timings

Unless otherwise specified, all A.C. timings referenced to CLK2 refer to the CLK2 rising edge in phase one. All references to PCLK# refer to the falling edge of PCLK#.

Symbol	Parameter	Figure	16 MHz		20 MHz		Units	Notes
			Min	Max	Min	Max		
T40a	W/R#, M/IO#, D/C#, ADS# Setup to CLK2	4.3	29		22		ns	
T40b	BLE#, BHE# Setup to CLK2	4.3	29		12		ns	
T41	RESETSX Valid before CLK2	4.2	13		12		ns	C_{Load} = 30 pF
T42	RESETSX Hold after CLK2	4.2	2		2		ns	C_{Load} = 30 pF
T43	READYSX# Valid before CLK2	4.11	31		24		ns	C_{Load} = 30 pF
T44	READYSX# Hold after CLK2	4.11	6		4		ns	C_{Load} = 30 pF
T45	NA# Valid before CLK2 ↑ Phase 2	4.3	11		7		ns	C_{Load} = 30 pF
T46	NA# Hold after CLK2 ↑ Phase 2	4.3	27		17		ns	C_{Load} = 30 pF
T47	HRQSX Valid before CLK2	4.12	28		17		ns	C_{Load} = 30 pF
T48	HRQSX Hold after CLK2	4.12	5		5		ns	C_{Load} = 30 pF
T49	RESETNPX Valid before CLK2	4.2a	13		12		ns	C_{Load} = 30 pF
T50	RESETNPX Hold after CLK2	4.2a	4		3		ns	C_{Load} = 30 pF
T57	READY286# Setup to PCLK#	4.11	50	90	45	90	ns	(Note 2)
T57a	READY286# Setup to PCLK#				35	75	ns	(Notes 2, 3)
T58	READY286# Hold from PCLK#	4.11	35		10		ns	
T59	SYSRESET, RESETCPU Setup to CLK2	4.2	20		18		ns	(Note 1)
T60	SYSRESET, RESETCPU Hold from CLK2	4.2	15		12		ns	(Note 1)
T61	A20GATE Setup to CLK2	4.12	40		30		ns	(Note 1)
T62	A20GATE Hold from CLK2	4.12	15		10		ns	(Note 1)
T63	HRQ286 Setup to PCLK#		25		25		ns	(Note 1)
T64	HRQ286 Hold from PCLK#		5		5		ns	(Note 1)
T65a	TURBO# Setup to HLDASX		15		15		ns	(Note 1)
T65b	TURBO# Hold from HLDASX		15		15		ns	(Note 1)
T66	MEMR#, MEMW#, Setup to CLK2	4.12	17		17		ns	(Note 1)
T66a	REFRESH# Setup to PCLK#		25		25		ns	(Note 1)
T67	MEMR#, MEMW#, Hold from CLK2	4.12	17		17		ns	(Note 1)
T67a	REFRESH# Hold from PCLK#		0		0		ns	(Note 1)
T68	EXTRDY Setup to CLK2	4.11	5		5		ns	
T69	EXTRDY Hold from CLK2	4.11	32		30		ns	

Other A.C. Timings

Unless otherwise specified, all A.C. timings referenced to CLK2 refer to the CLK2 rising edge in phase one. All references to PCLK# refer to the falling edge of PCLK#. (Continued)

Symbol	Parameter	Figure	16 MHz		20 MHz		ns	Notes
			Min	Max	Min	Max		
T70	M/IO286#, S0# and S1# Output Delay from PCLK#	4.8	0	15	0	15	ns	$C_{Load\ max}$ = 100 pF
T71	ROMCS#, LMEGCS# Output Delay from Valid Address	4.3		40		40	ns	C_{Load} = 50 pF
T72	OBMEM Output Delay from Valid Address	4.3		40		36	ns	$C_{Load\ max}$ = 50 pF
T73a	D0–D15 Output Valid before CLK2		30		30			
T73b	D0–D15 Hold after CLK2		6		6			
T74	PERROR# Output Delay from PCLK#	4.4		50		50	ns	C_{Load} = 50 pF
T75	HLDA Active Delay from HRQ286	4.10	92		92			
T76	HLDA Inactive Delay from HRQ286	4.10	185		185			

NOTES:
1. Asynchronous parameters, provided to assure recognition at a specific clock edge.
2. READY286# is only sampled when an internal 8 MHz clock is high. (See Figure 4.11)
3. This specification is valid only when EFI = 40 MHz and PCLK = 20 MHz before programming the SPDSEL bit.

4.4 A.C. Timing Diagrams

The following diagrams illustrate A.C. timing relations.

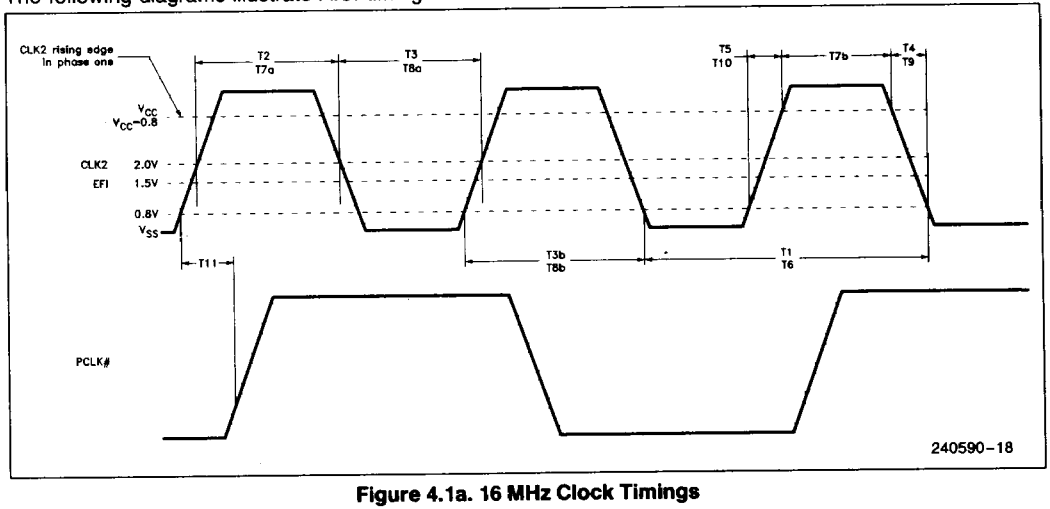


Figure 4.1a. 16 MHz Clock Timings

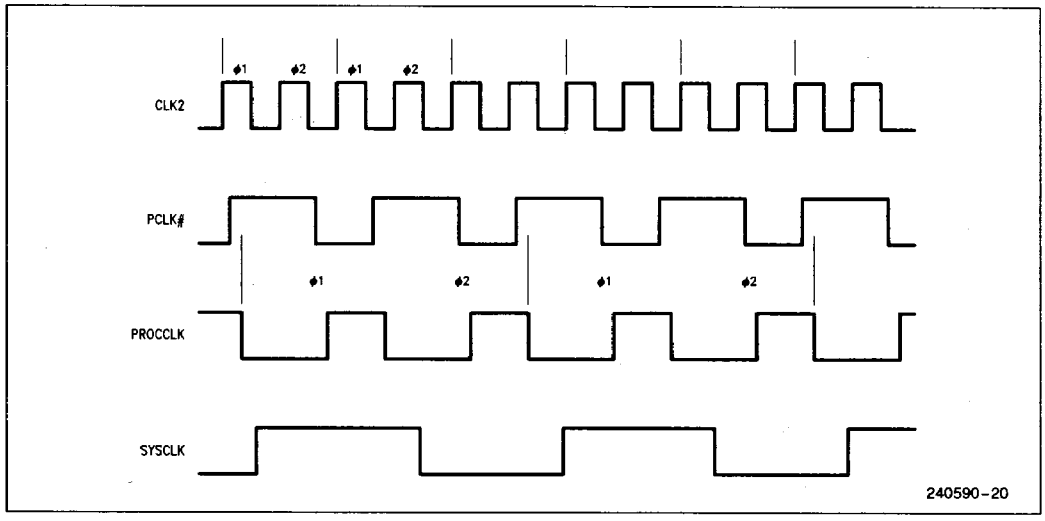


Figure 4.1b. 20 MHz Clock Timings

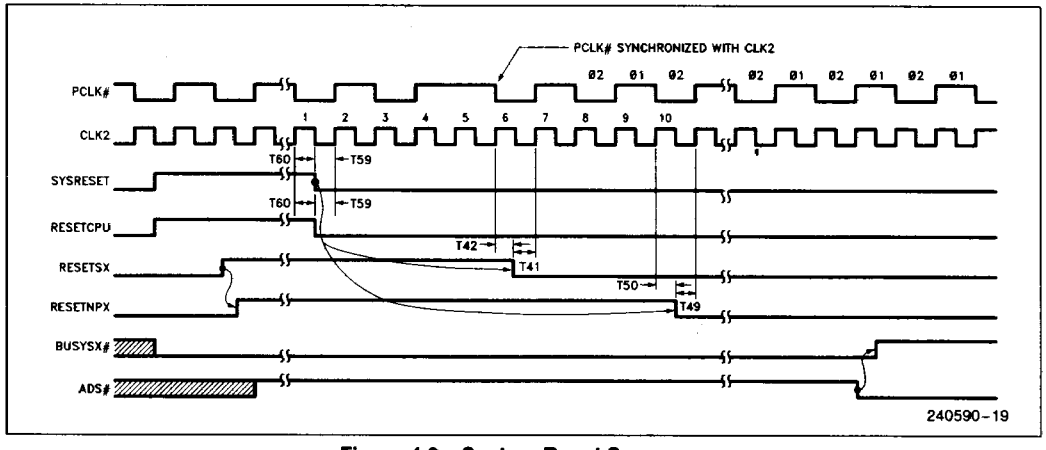
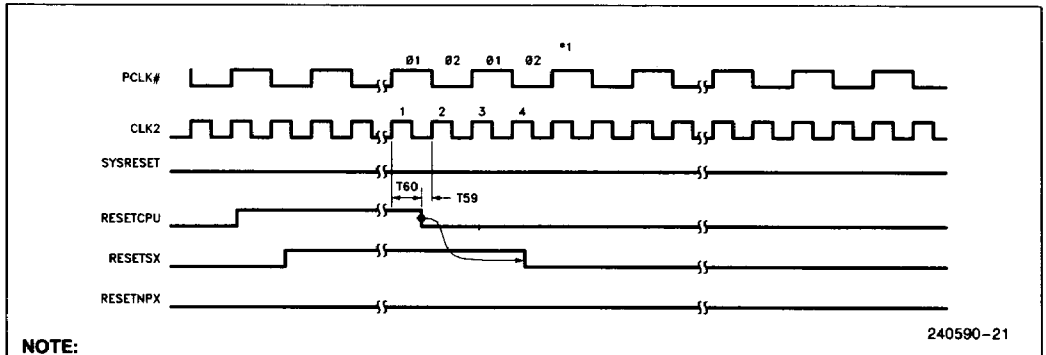


Figure 4.2a. System Reset Sequence



NOTE:
1. RESETSX will deactivate in phase 2 from 1 to 4 CLK2 cycles after the falling edge of RESETCPU.

Figure 4.2b. 16 MHz CPU Reset Sequence

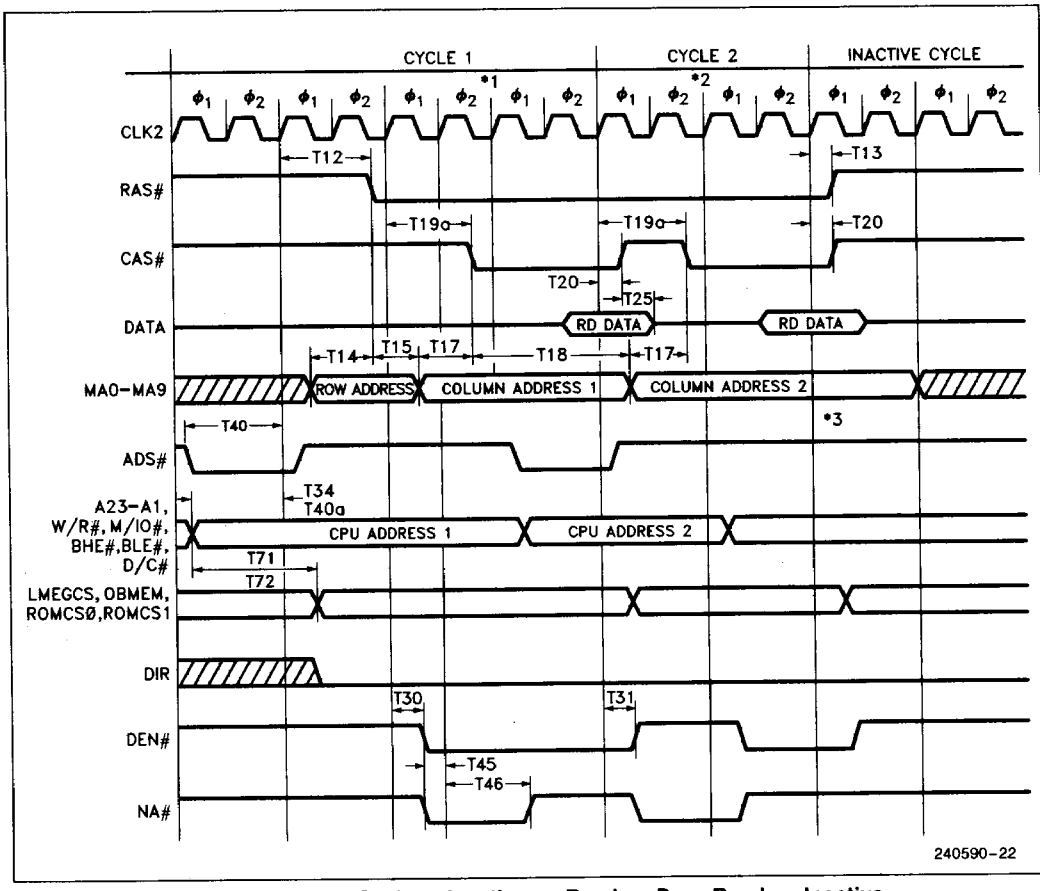


Figure 4.3. DRAM Cycles—Inactive . . . Read . . . Page Read . . . Inactive

NOTES:
1. Add 1 Wait State for W01 Mode.
2. Add 1 Wait State for W01 Mode, 2 Wait States for W02 Mode.
3. ADS# inactive at start of cycle deactivates RAS#.

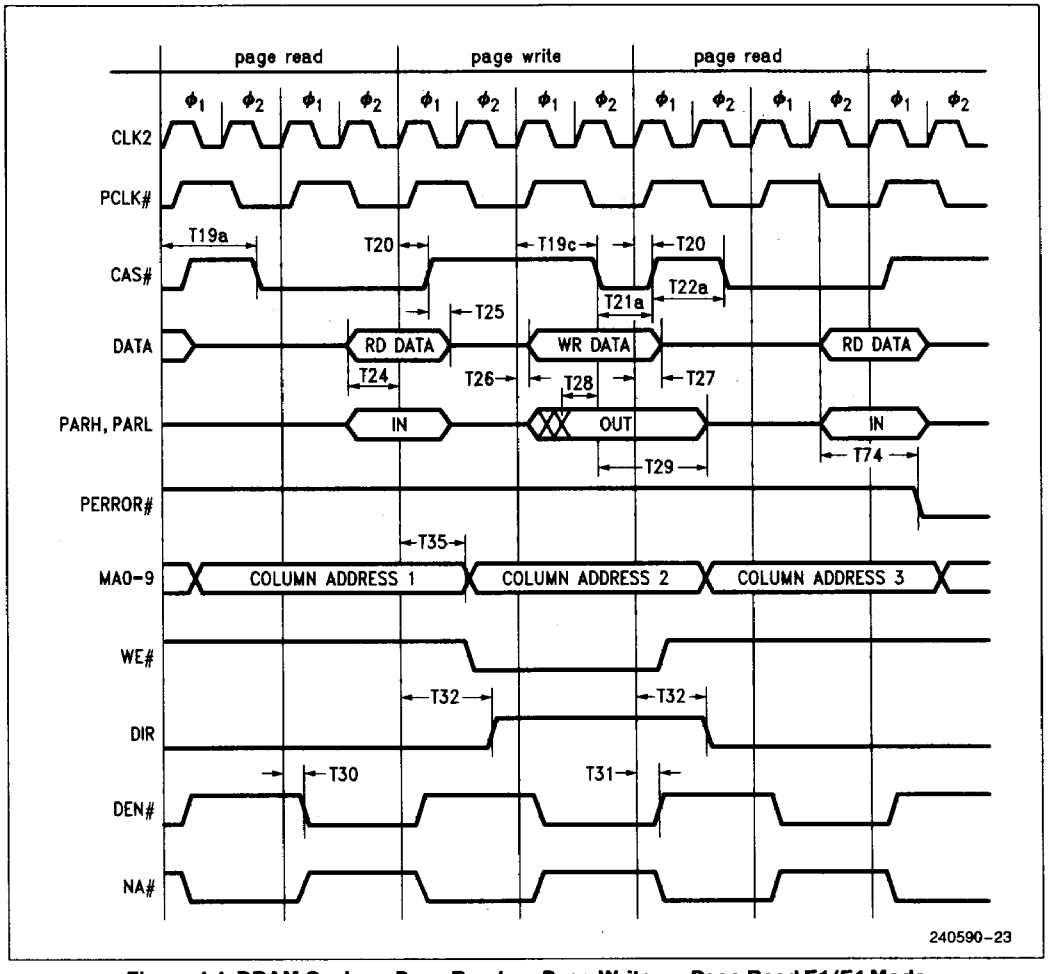


Figure 4.4. DRAM Cycles—Page Read . . . Page Write . . . Page Read F1/F4 Mode

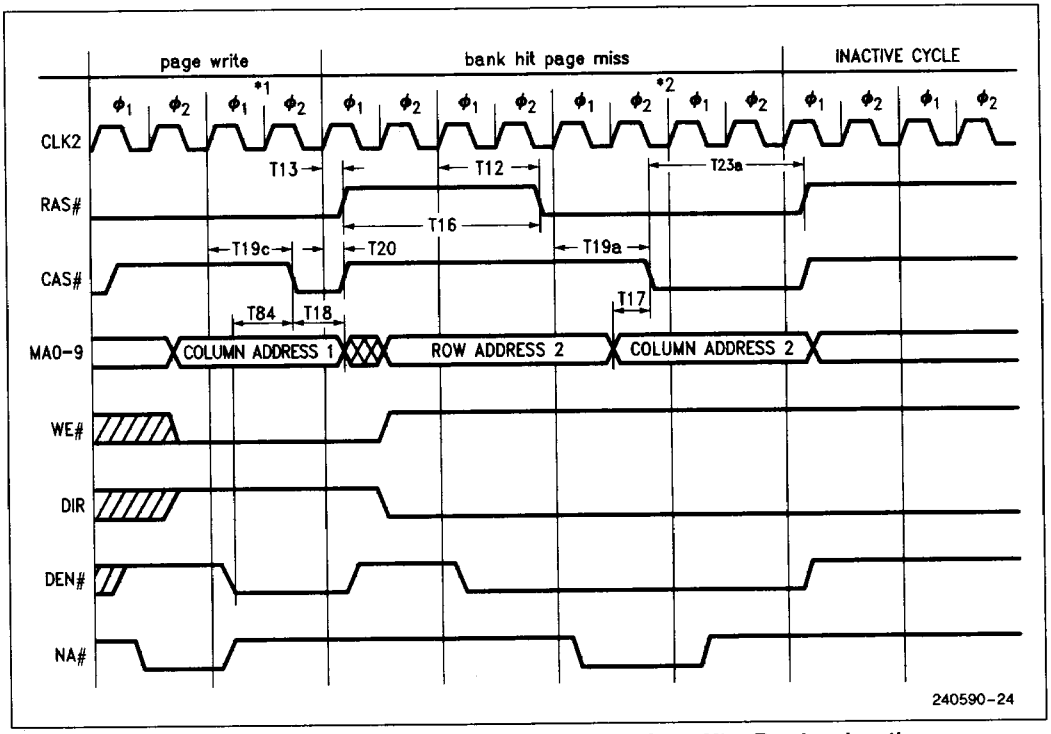


Figure 4.5. DRAM Cycles—Page Write . . . Bank-Hit-Page-Miss Read . . . Inactive

NOTES:
1. Add 1 Wait State for W01 Mode or 2 Wait States for W02 Mode.
2. Add 1 Wait State for W02 Mode.

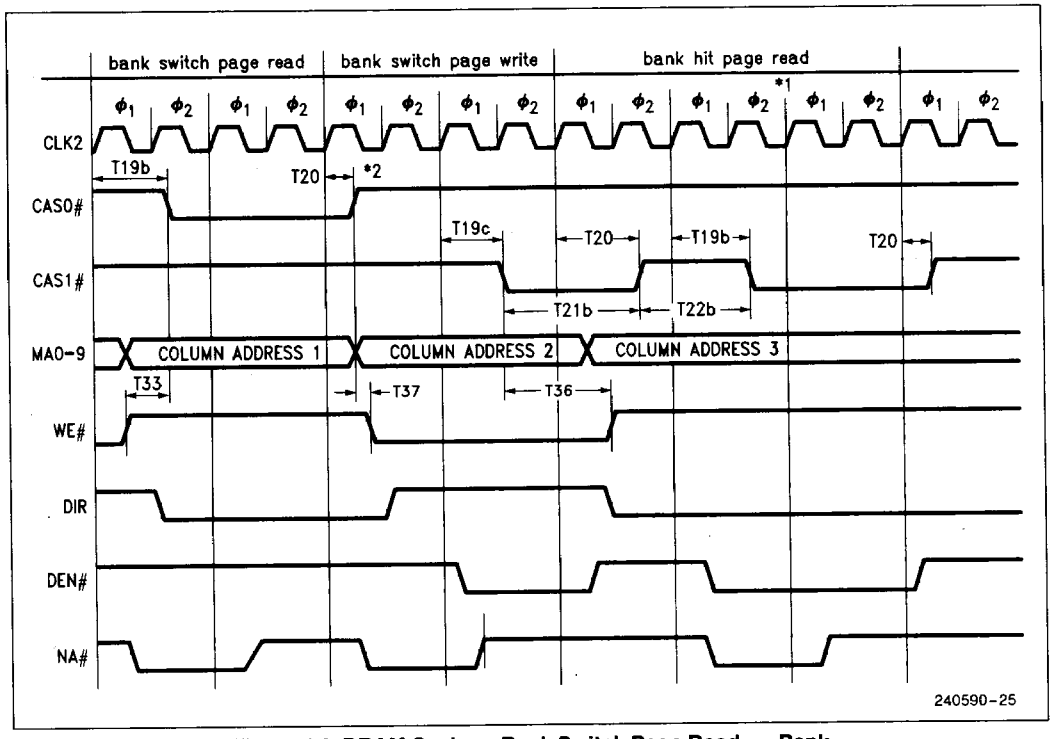


Figure 4.6. DRAM Cycles—Bank Switch Page Read . . . Bank Switch Page Write . . . Bank Hit Page Read for W01/W02 Mode

NOTES:
1. Add 1 Wait State for W02 Mode.
2. Following a read cycle, CAS# always de-activates before WE# activates. Following a write cycle, WE# may deactivate before CAS# de-activates.

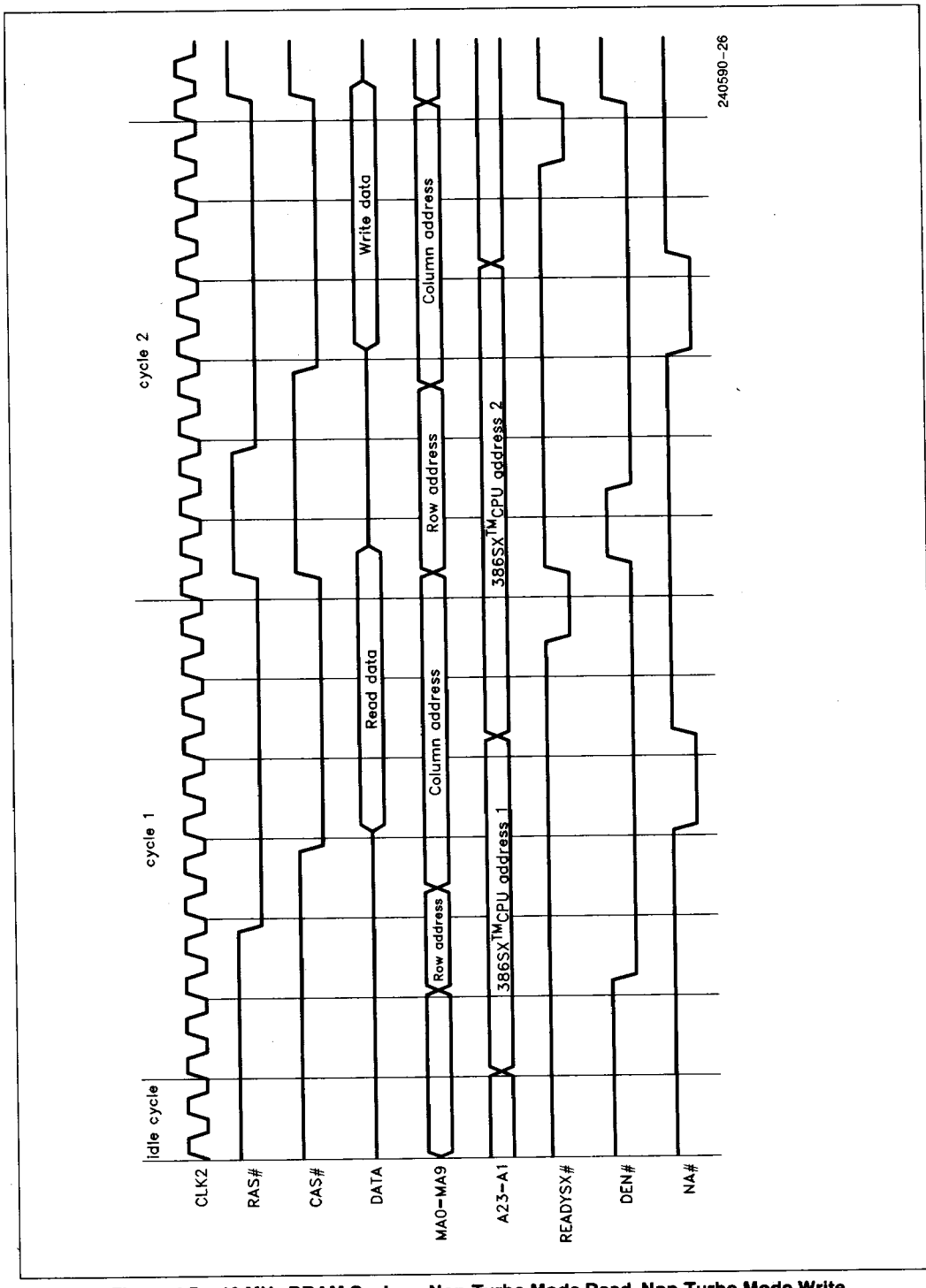
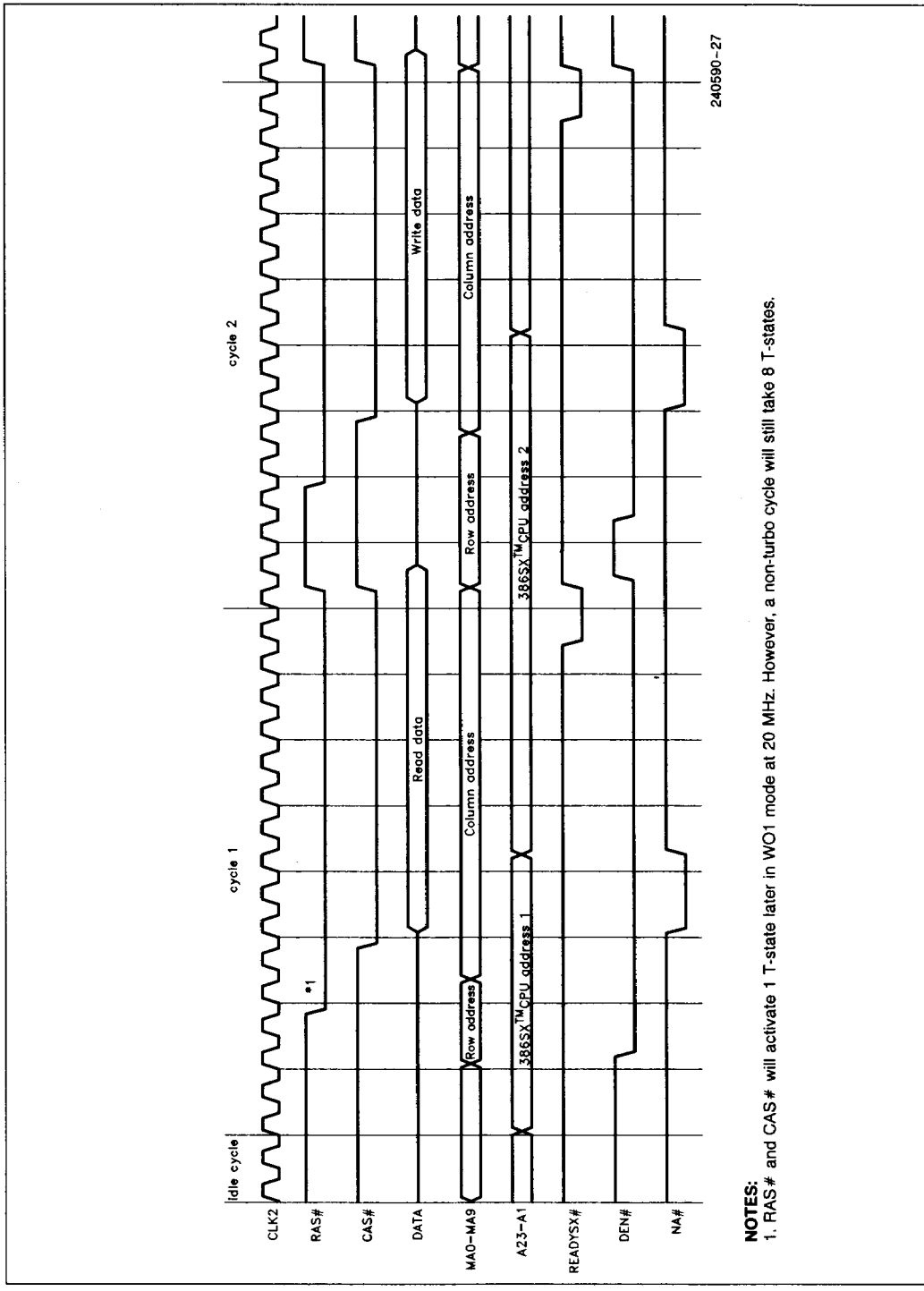


Figure 4.7a. 16 MHz DRAM Cycles—Non-Turbo Mode Read, Non-Turbo Mode Write



NOTES:
1. RAS# and CAS# will activate 1 T-state later in WO1 mode at 20 MHz. However, a non-turbo cycle will still take 8 T-states.

Figure 4.7b. 20 MHz DRAM Cycles—Non-Turbo Mode Read, Non-Turbo Mode Write

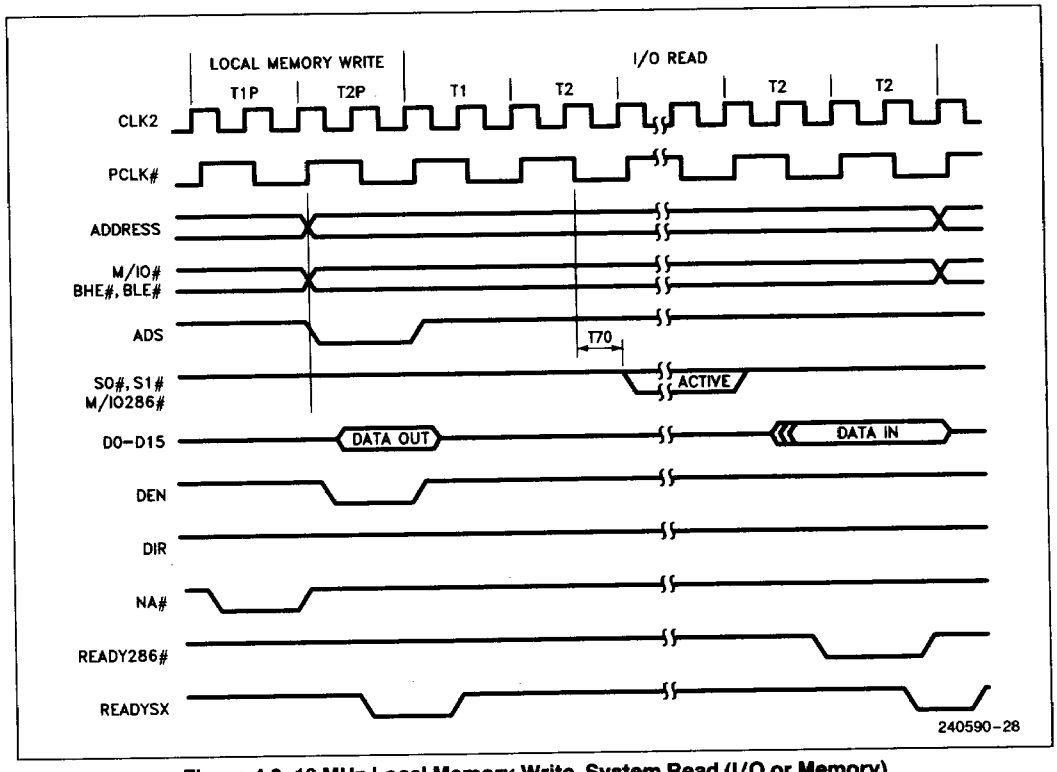


Figure 4.8. 16 MHz Local Memory Write, System Read (I/O or Memory)

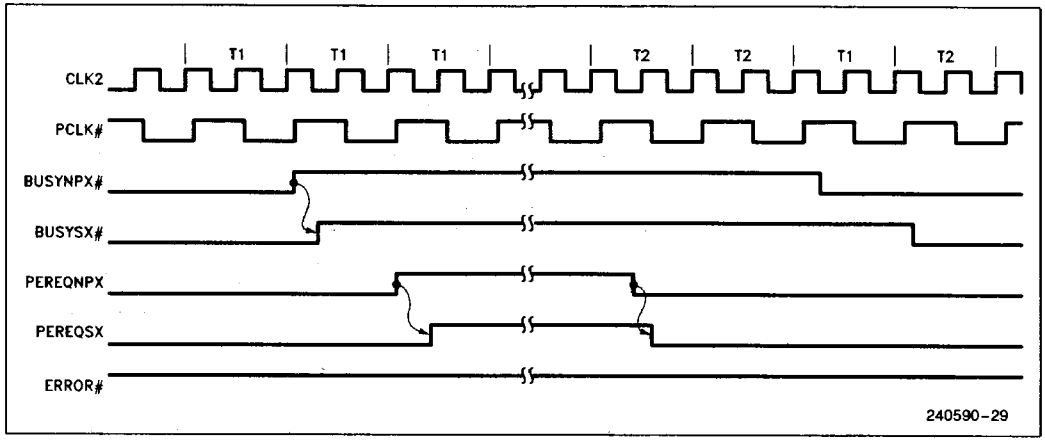


Figure 4.9a. Numeric Coprocessor Interface—No Error

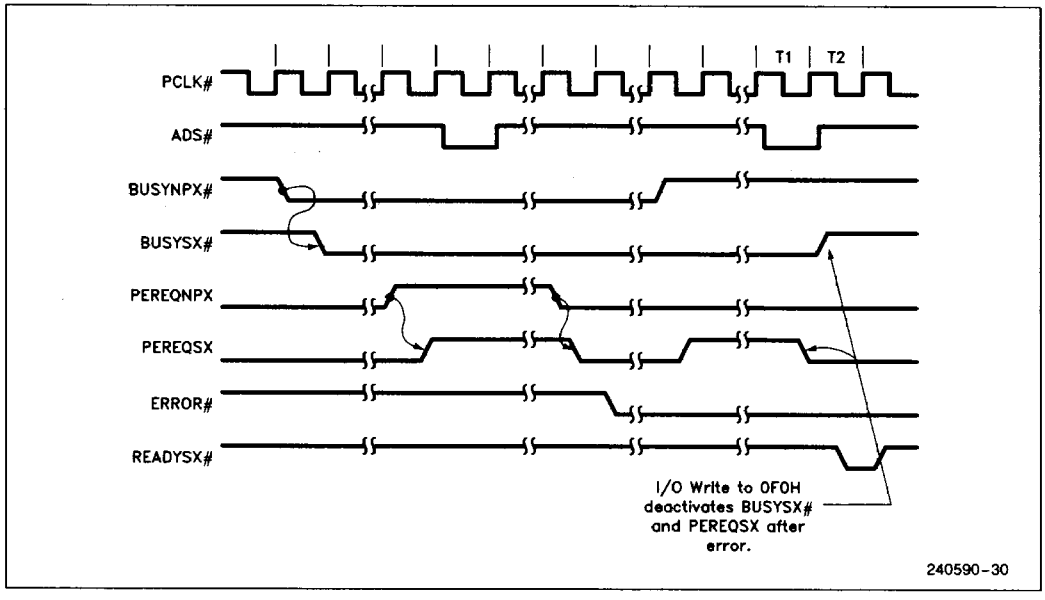


Figure 4.9b. Numeric Coprocessor Interface—with Error

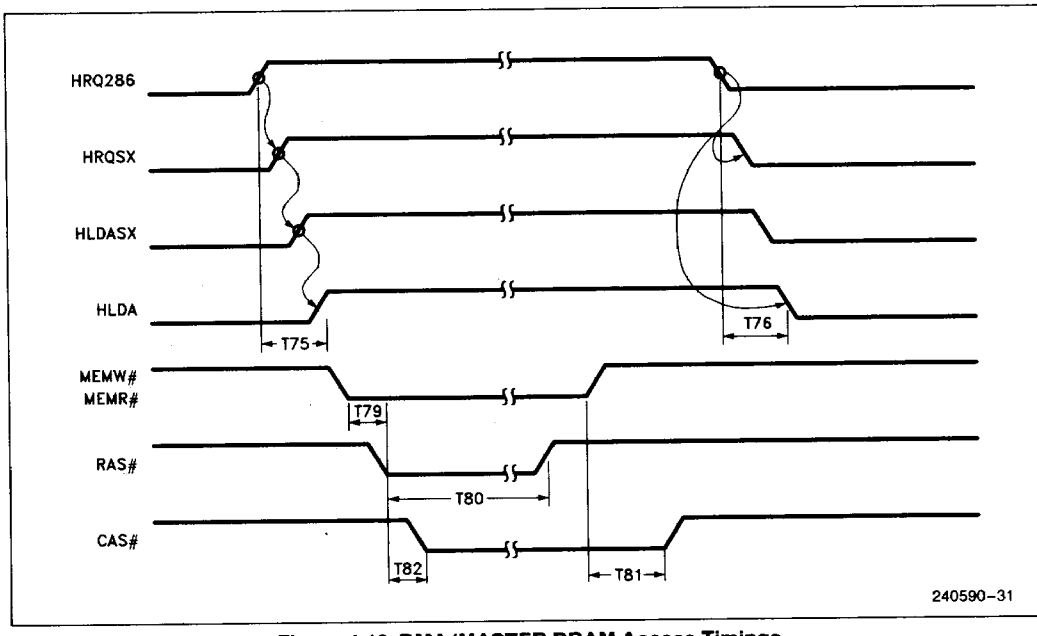
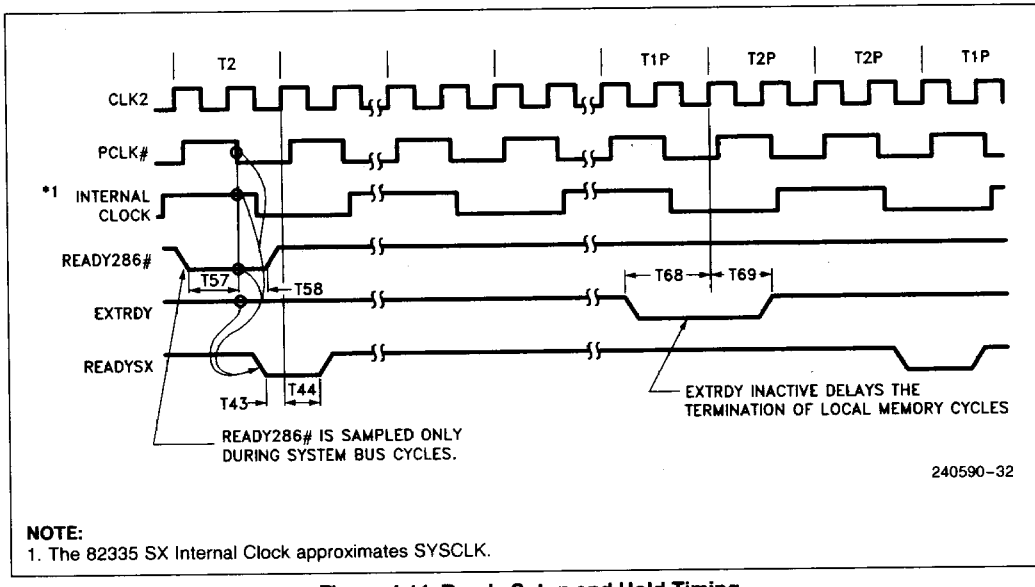


Figure 4.10. DMA/MASTER DRAM Access Timings



NOTE:
1. The 82335 SX Internal Clock approximates SYSCLK.

Figure 4.11. Ready Setup and Hold Timing

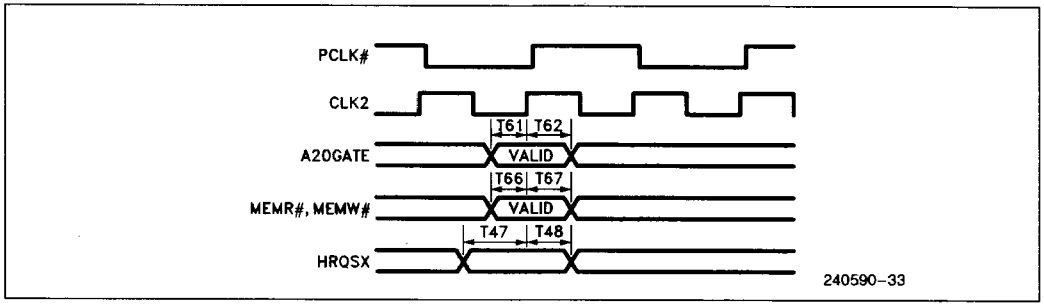


Figure 4.12. Misc. Setup and Hold Timings

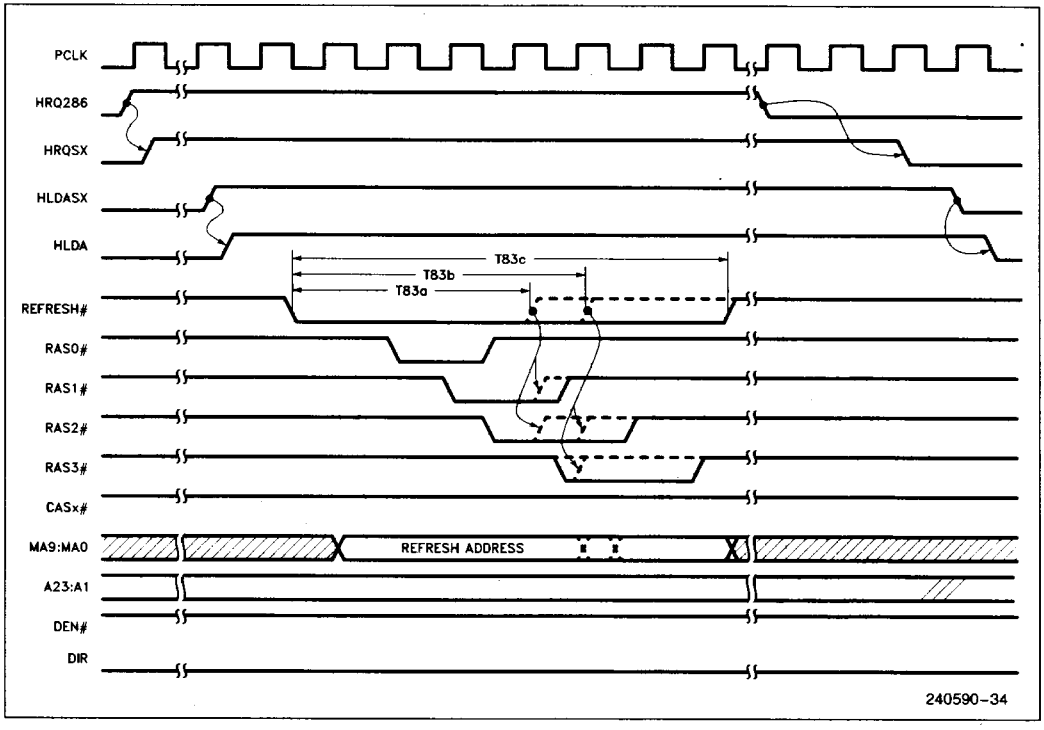


Figure 4.13. Refresh Timing

4.5 Capacitive Derating Curves

The capacitive derating curves for the various 82335 SX output buffers are shown in Figures 4.15 to 4.20. Each curve shows the output valid delay relative to a 50 pF nominal load. For A.C. Specifications that show a maximum capacitive load greater than 50 pF, the maximum value has been tested at 50 pF and derated to support the indicated capacitive load. The minimum values are all specified at 50 pF unless a capacitive load less than 50 pF is indicated. In which case the minimum value has been tested at 50 pF and derated to support the indicated capacitive load.

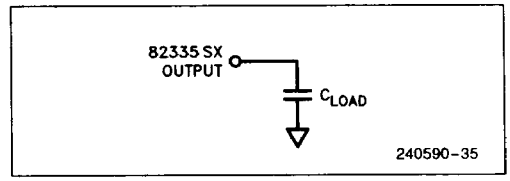


Figure 4.14. A.C. Test Loads

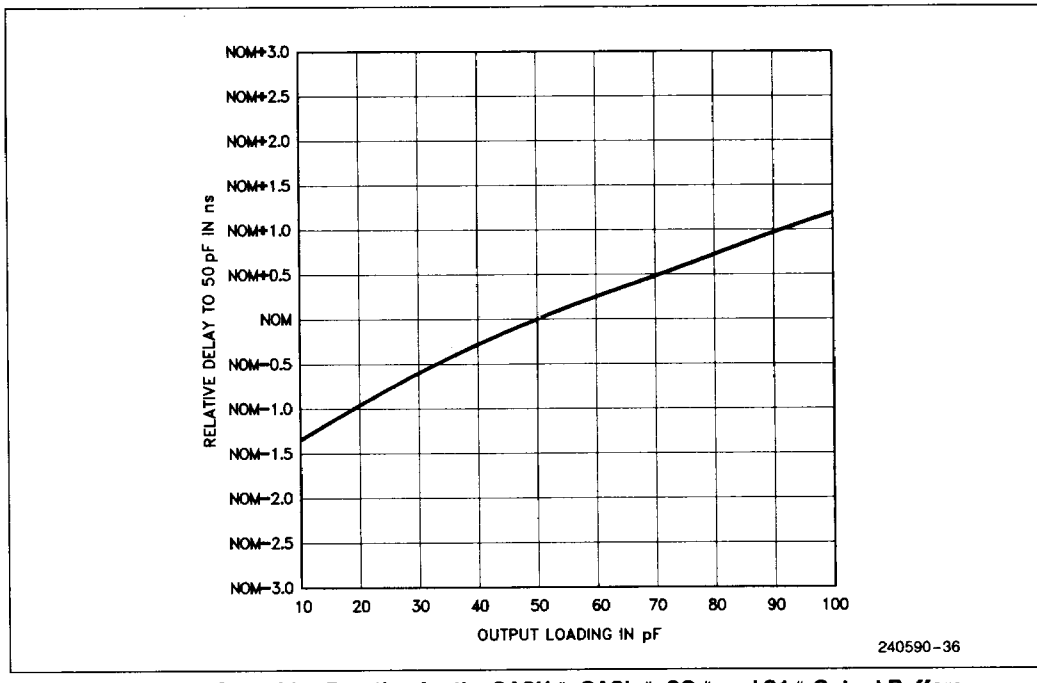


Figure 4.15. Capacitive Derating for the CASH#, CASL#, SO# and S1# Output Buffers

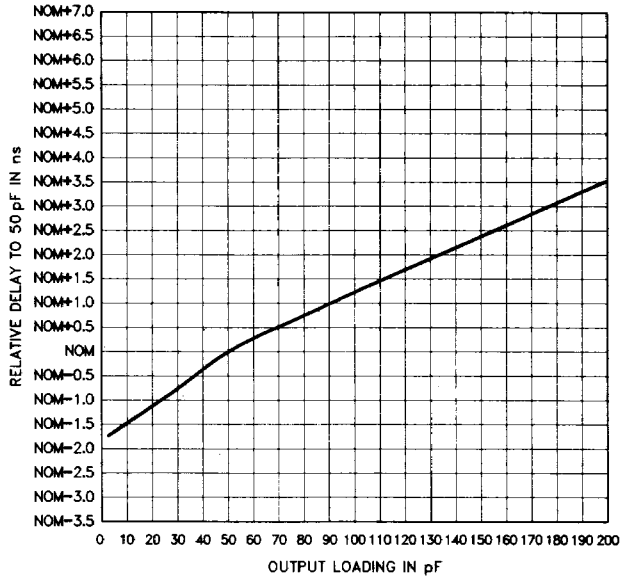


Figure 4.16. Capacitive Derating for the RAS0# –RAS3# Output Buffers

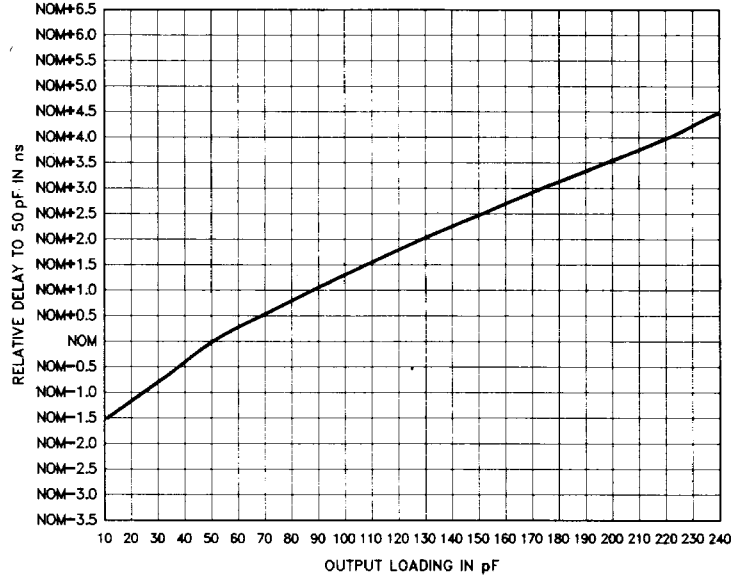


Figure 4.17. Capacitive Derating for the DEN#, DIR, MA0–MA9, WE#, OBMEM, ROMCS0#, ROMCS1#, MIO286#, HRQSX and LMEGCS# Output Buffers

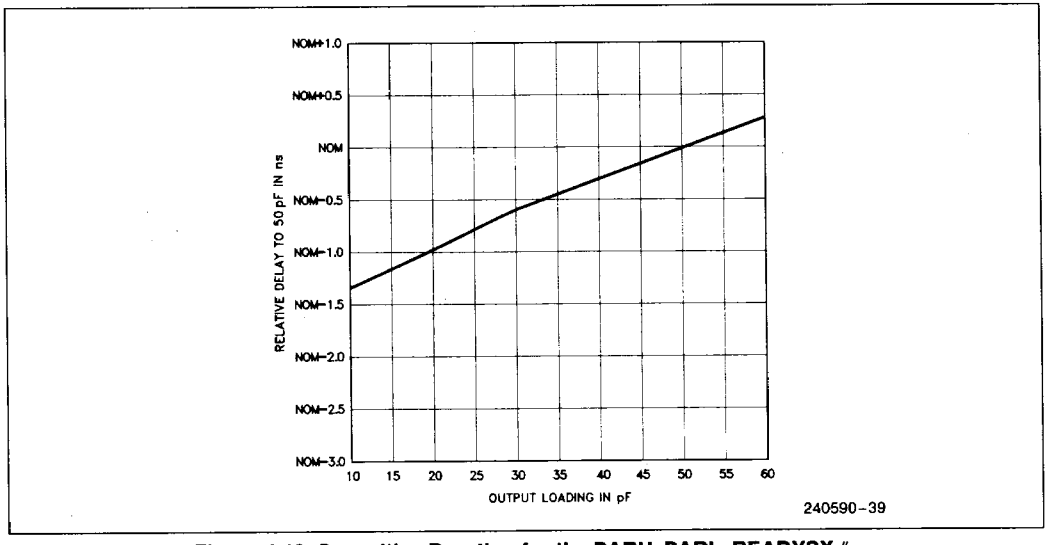


Figure 4.18. Capacitive Derating for the PARH, PARL, READYSX#, RESETSX, RESETNPX and NA# Output Buffers

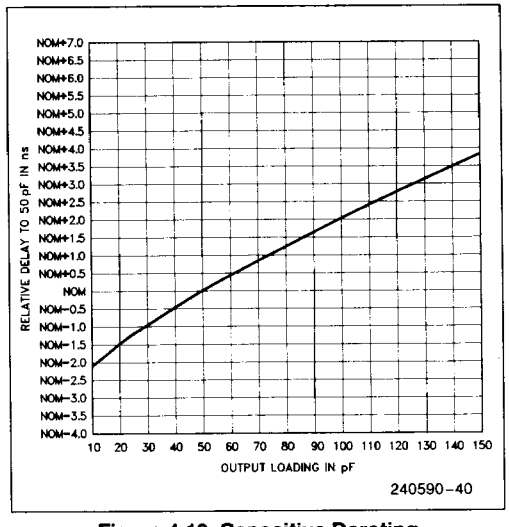


Figure 4.19. Capacitive Derating for the D0–D15 Output Buffers

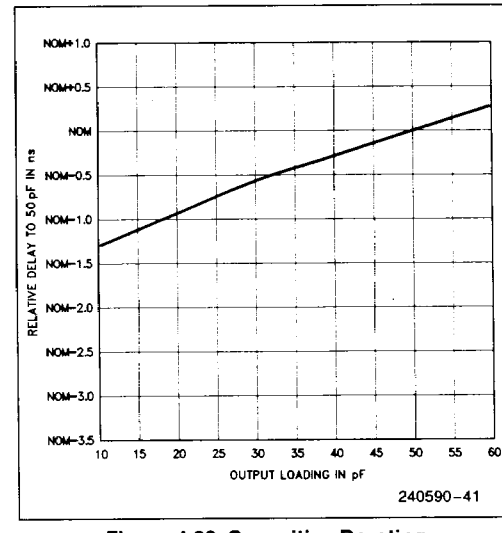


Figure 4.20. Capacitive Derating for the PCLK# Output Buffer

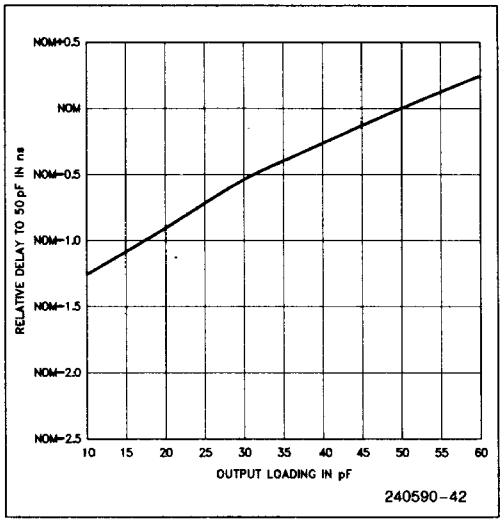


Figure 4.21. Capacitive Derating for the CLK2 Output Buffer

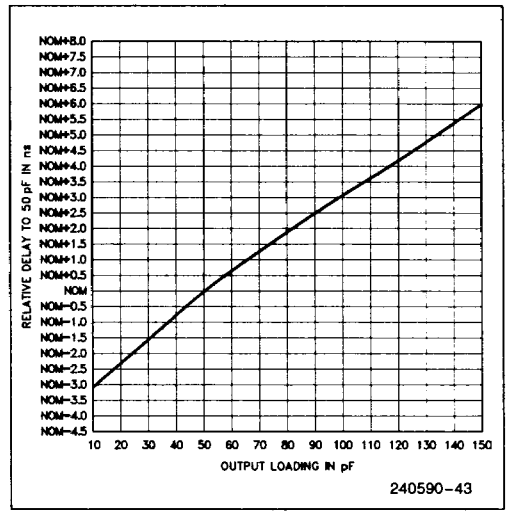


Figure 4.22. Capacitive Derating for the BUSYSX#, PEREQSX, PERROR#, HLDA Output Buffers

4.6 DIFFERENCES BETWEEN THE 82335 SX AND THE 82335

1. The 82335 SX can run at 16 MHz or 20 MHz. The 82335 can only run at 16 MHz.
   A. The 82335 SX has 16 MHz and 20 MHz A.C. Specifications. The 82335 has only 16 MHz A.C. Specifications.
   B. The 82335 SX DRAM modes are different at 20 MHz than 82335 DRAM modes. The 16 MHz 82335 SX DRAM modes are the same as the 82335.
   C. 82335 SX Non-turbo mode accesses take 8 T-states in 20 MHz operation. Non-turbo mode accesses take 6 T-states in both the 82335 and the 82335 SX in 16 MHz operation.
   D. PCLK# is a divide by 2.5 of EFI at 20 MHz, and a divide by 2 of EFI at 16 MHz in the 82335 SX. PCLK# is always a divide by 2 in the 82335 which only runs at 16 MHz.
2. The 82335 SX ignores READYNPX# (N.C.) and generates READYSX# after 1 wait-state for numerics coprocessor cycles if a coprocessor is present in the system. The 82335 uses READYNPX# to generate READYSX# on coprocessor cycles when a coprocessor is present.
3. The 82335 SX has separate output voltage specifications for PCLK#. The 82335 does not have separate output voltage specifications for PCLK#.
4. The 82335 SX has the Granularity Enable register. The 82335 does not.
5. The 82335 SX has the Extended Granularity register. The 82335 does not.
6. The 82335 SX can shadow and write-protect with 32 Kbyte or 128 Kbyte granularity. The 82335 can only shadow and write-protect in 128 Kbyte granularity.
7. The 82335 SX allows shadowing and write-protecting to be chosen independently of each other for the BIOS and adaptor ROM areas. The 82335 always write-protects shadowed areas.
8. 3-way interleaving is not possible with the 82335 SX. If the INTERLV bits in the 82335 SX are set for 3-banks, the DRAM controller will only access 2-banks. 3-way interleaving is possible with the 82335. If the INTERLV bits are set for 3-way interleaving in the 82335, the DRAM controller will access 3-banks but is not guaranteed to meet A.C. specifications. Correct DRAM operation is not guaranteed for 3-way interleaving in the 82335. Systems should not set the INTERLV bits in the 82335 for 3-banks.
9. PERROR# is latched until PARCHEN is cleared in the 82335 SX. PERROR# is not latched in the 82335.
10. TURBO is an asynchronous input in the 82335 SX. TURBO is not an asynchronous input in the 82335.
11. Only ROMCS1# is active for 512 Kbit ROM size operation in the 82335 SX. Only ROMCS0# is active for 512 Kbit ROM size operation in the 82335.
12. PCLK# is free-running during powerup in the 82335 SX. PCLK# is not active until SYSRESET is deactivated in the 82335.
13. RESET CPU will not be passed on to the 386 SX until HLDA is deactivated in the 82335 SX. RESETCPU will be passed on to the 386 SX during HLDA in the 82335. A SYSRESET combined with RESETCPU will always be passed through to the 386 SX by both the 82335 SX and the 82335.
14. The 82335 SX will only sample 386 SX bus cycle definition inputs when accompanied by ADS# active. The 82335 may sample 386 SX bus cycle definition inputs without ADS# active.
15. Some 16 MHz A.C. specifications are different in the 82335 SX than in the 82335, but the 82335 SX is upward compatible with the 82335.

The 82335 SX is plug compatible with the 82335

5.0 REVISION HISTORY

The following list represents key differences between this and the -001 version of the 82335SX data sheet. Please review this summary.

Front Sheet	CHMOS III has been changed to CHMOS IV.
Figure 2.1	This figure has been modified to include 82335SX device instead of 82335.
Table 2.3B	t_{AA} has been modified to be 75 ns maximum.
Section 2.3.4.5	A recommendation has been added to this section when using extended granularity feature. Please follow this recommendation.
Section 4.2	The V_{IHC} for the EFI has been changed to 2.4V minimum.
A.C. Timing	The following A.C. timings have been changed: T14a, T15, T16, T17, T17a, T18, T22b, T34, T42, T59 and T84. The following A.C. timings have been added: T15a, T18a. Notes 10, 11 and 12 have been added to A.C. timing for DRAM controller unit.
Figure 4.1a	The reference for EFI has been changed to 1.5V. T2 and T3 have replaced T2a for EFI high and EFI low values. T2b has been taken out.
Figure 4.3	T45 and T46 (NA# active and deactive edges) reference has been changed to the rising edge of CLK2 in phase two.
Figure 4.4	T21 label has been changed to T21a. T23a changed to T22a, and the extra T74 label has been removed.
Figure 4.6	T19a label has been changed to T19b and T23b has been changed to T22b.