Payal Mohapatra

Curriculum Vitae

PhD Student, Computer Engineering
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My Webpage
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Education

2021–present **PhD, Computer Engineering**, *Northwestern University*, Illinois, USA.
Machine Learning under data constraints, Human Centred AI

Advisor : Dr. Qi Zhu

CGPA : 4/4

2015–2017 : **Masters (*by research*), Electrical Engineering**, *Indian Institute of Technology Madras*, India.

CGPA : 9.31/10

2011–2015 : **Bachelor of Engineering, Electronics & Instrumentation**, *Madras Institute of Technology, Anna University*, India.

CGPA : 9.36/10

Publications

2022 Payal Mohapatra, Akash Pandey, Bashima Islam, and Qi Zhu. Speech disfluency detection with contextual representation and data distillation. In *Proceedings of the 1st ACM International Workshop on Intelligent Acoustic Systems and Applications*, pages 19–24, 2022.

2018 Payal Mohapatra, Preejith Sreeletha Premkumar, and Mohanasankar Sivaprakasam. A yellow–orange wavelength-based short-term heart rate variability measurement scheme for wrist-based wearables. *IEEE Transactions on Instrumentation and Measurement*, volume 67, pages 1091–1101. IEEE, 2018.

2017 Payal Mohapatra, SP Preejith, and Mohanasankar Sivaprakasam. A novel sensor for wrist based optical heart rate monitor. In *2017 IEEE international instrumentation and measurement technology conference (I2MTC)*, pages 1–6. IEEE, 2017.

Research Experience

Northwestern University

Jan,2022 – present ***Self Supervised Learning Methods to detect Speech Disfluency under Data Constraints***.
Develop a pipeline to use real-world unlabeled disfluency data from multiple domains to learn contextual representations for downstream tasks with a limited labeling budget. Presented preliminary results at the workshop on intelligent acoustics co-located with ACM MobiSys'22. Manuscript under submission for IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)'23

Collaborators: Dr. Bashima Islam (*Worcester Politecnic Institute*) Dr. Md Tamzeed Islam (*Amazon Lab126*) Dr. Qi Zhu (*Northwestern University*)

Nov,2021 – present ***Predictive Models for Human Fatigue - Operator 4.0***.
Develop sample-efficient machine learning methods to predict perceived fatigue levels from biophysical and locomotive sensor data collected from user studies at Northwestern University. Handle fine-grained, lossy, noisy, and missing long-range data from wearable sensors. Demonstrated a functional prototype on two factory floors with near-real-time data visualization and obtained user-feedback.

Collaborating Organisations: Northwestern University, John Deere, Boeing, MxD, University of Buffalo

Indian Institute of Technology Madras

July,2015 – Oct,2017 ***Wrist-based wearable device to measure heart rate under conditions of physical activity and Heart Rate Variability at stationary instants***.

Developed and designed a custom optical sensor board for optimum signal quality in users with varying skin-complexions. Developed motion-artifact rejection algorithm based on normalized least mean squared adaptive filtering for real-time processing and validated with an extensive user study. Studied the effect of pulse rate variability under different orthostatic loads.

Collaborators: Preejith SP (*Healthcare Technology Innovation Centre*) Dr. Mohanasankar Sivaprakasam (*Indian Institute of Technology Madras*)

Professional Experience

Analog Devices Incorporation

Experience as Design Verification engineer on multiple mixed-signal System on Chips(SoC)

March,2020 – Sept, 2021 ***Design Verification of Fast DSP in an Audio Noise Cancellation ASIC***.

Conducted end-to-end verification and developed reference models for a custom DSP used for biquad operations, audio peripherals like ADCs, DACs & asynchronous sample rate converters

Feb,2019 – Feb, 2020 ***Subsystem Verification of Scalable Ethernet Switch***.

Worked on time sensitive networking protocols and developed reference models for two of the five supported features by the SoC adhering to IEEE 802.1AS (time synchronization) and IEEE 802.1qbv (Scheduled Traffic). Employed verification strategy was selected for presentation at global intra-company conference in 2020. Chip successfully taped out in Feb 2020.

March,2018 – Dec, 2018 ***Block Level Verification of Beamforming Algorithm in Ultrasound Fingerprint Sensing ASIC***.

Developed an error injection mechanism to verify the calibration algorithm of transmitters and receivers in the signal datapath and worked on a synthetic aperture algorithm for beamforming. Demonstrated a system to detect occurrence of touch on the SoC at a company-wide workshop. Chip successfully taped out in Dec 2018.

Nov,2017 – March, 2018 ***Formal Digital Design verification***.

Developed mathematical theorems to describe system behavior without explicit modeling to prove/disprove properties with all possible stimuli using EDA tools.

Teaching Assistantship

Winter, 2017: **EE5400: Analog and Digital Circuits**, IIT Madras.

Fall, 2016: **EE5401: Measurements and Instrumentation**, IIT Madras.

Winter, 2016: **EE3006: Principles of Measurement**, IIT Madras.

Fellowships & Awards

2022 Travel grant of 1000 USD for MobiSys'22

2022 All inclusive grant to attend Computing Research Association Widening Participation (CRA-WP), Grad Cohort Workshop for Women

2021 Best research video award of 100 USD at Design Automation Conference Young Fellowship (DAC YF)

2021 Recipient of Design Automation Conference Young Fellowship (DAC YF)

2019 Spot Award at Analog Devices Inc.(ADI) acknowledging the contribution in scalable ethernet switch verification effort

- Awarded to less than 1% ADI employees globally.

2019 Global finalists and site (Bangalore) winners of Blockchain Innovation Challenge at ADI.

2018 Best Paper in all tracks in IEEE Conference WinTechCon

2017 Winner of Anveshan Design Challenge

- National level competition organised by Analog Devices Inc. annually.

2015-2017 Awarded Research Assistantship fellowship by Govt. of India

Computer skills

Programming Languages	Python, C++, Shell, Perl, LaTeX
Technologies	Pytorch, Tensorflow, Sklearn, Pandas, Seaborn, Librosa
Hardware Description Languages	Verilog, System Verilog, Universal Verification Methodology(UVM)
Tools	LabVIEW, Matlab, Spice Simulation & PCB Design, Xilinx Vivado