HEF4020B

14-stage binary counter Rev. 8 — 18 November 2011

Product data sheet

1. **General description**

The HEF4020B is a 14-stage binary counter with a clock input (CP), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (Q0, and Q3 to Q13). The counter advances on the HIGH to LOW transition of $\overline{\text{CP}}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. A feature of the device is its high speed (typ. 35 MHz at $V_{DD} = 15 \text{ V}$).

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to $V_{\text{DD}},\,V_{\text{SS}},$ or another input.

2. **Features and benefits**

- High speed operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

Ordering information 3.

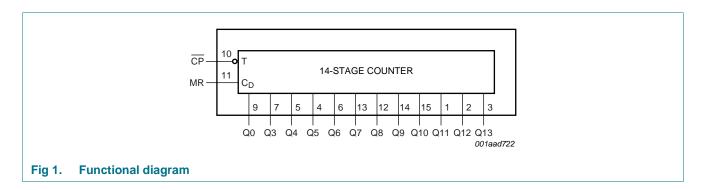
Table 1. **Ordering information**

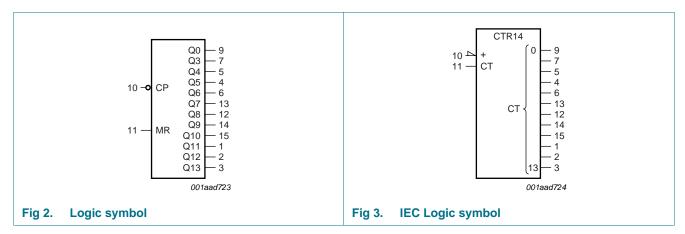
All types operate from -40 °C to +85 °C.

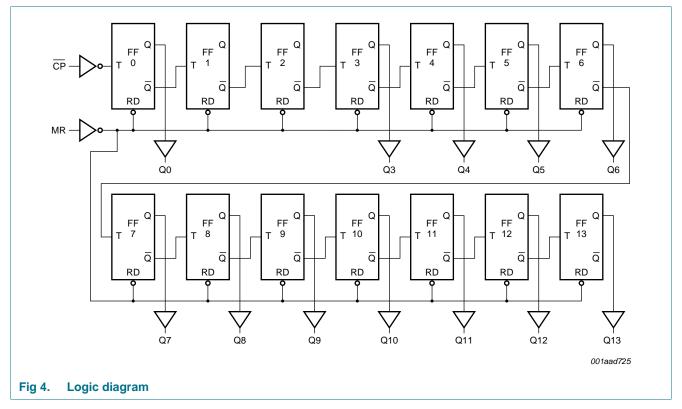
Type number	Package		
	Name	Description	Version
HEF4020BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4020BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



4. Functional diagram



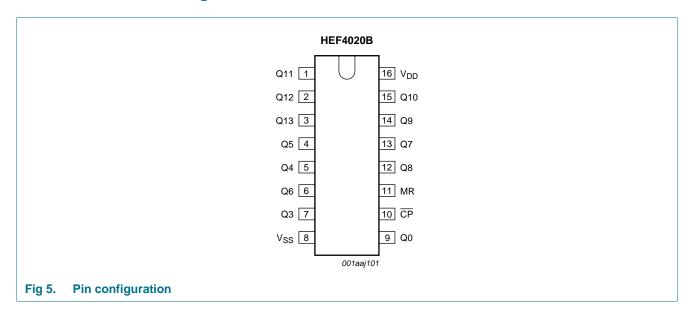




HEF4020B

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

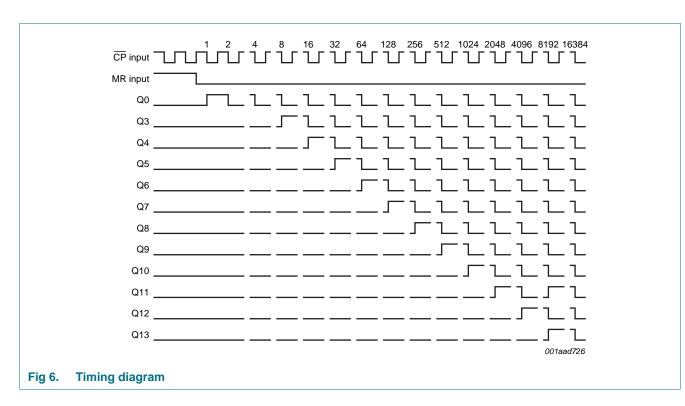
Symbol	Pin	Description
Q3 to Q13	7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	parallel output (Q3 to Q13)
V_{SS}	8	ground supply voltage
Q0	9	parallel output
CP	10	clock input (HIGH-to-LOW edge triggered)
MR	11	master reset input (active HIGH)
V_{DD}	16	supply voltage

6. Functional description

Table 3. Functional table[1]

Input	Output	
СР	MR	
\uparrow	L	no change
	L	count
X	Н	L

[1] $H = HIGH \text{ voltage level}; L = LOW \text{ voltage level}; X = don't care}; \uparrow = positive-going transition}; \downarrow = negative-going transition.$



7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_I < 05 \text{ V or } V_I > V_{DD} + 0.5 \text{ V}$	-	±10	mA
V_{I}	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T_{amb} -40 °C to +85 °C			
		DIP16 package	[1] _	750	mW
		SO16 package	[2] -	500	mW
Р	power dissipation	per output	-	100	mW

^[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

^[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 $^{\circ}\text{C}.$

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	$V_{DD} = 5 V$	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$ V; $V_{I} = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	-40 °C	T _{amb} = 25 °C		T _{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_{O} < 1 \mu A$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	$ I_{O} < 1 \mu A$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	$ I_{O} < 1 \mu A$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	$ I_{O} < 1 \mu A$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	$V_0 = 2.5 \text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mΑ
		$V_0 = 4.6 \text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mΑ
		$V_0 = 9.5 \text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mΑ
		$V_0 = 13.5 \text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mΑ
I _{OL}	LOW-level output current	$V_0 = 0.4 \ V$	5 V	0.52	-	0.44	-	0.36	-	mΑ
		$V_0 = 0.5 \text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mΑ
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mΑ
I _I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μΑ
I _{DD}	supply current	$I_O = 0 A$	5 V	-	20	-	20	-	150	μΑ
			10 V	-	40	-	40	-	300	μΑ
			15 V	-	80	-	80	-	600	μΑ
C _I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ °C}; \text{ for test circuit see } \frac{\text{Figure 8}}{\text{C}}.$

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	CP to Q0;	5 V	78 ns + $(0.55 \text{ ns/pF})C_L$	-	105	210	ns
p	propagation delay	see Figure 7	10 V	34 ns + (0.23 ns/pF)C _L	-	45	90	ns
			15 V	22 ns + (0.16 ns/pF)C _L	-	30	65	ns
		Qn to Qn + 1	5 V	53 ns + $(0.55 \text{ ns/pF})C_L$	-	80	160	ns
			10 V	19 ns + (0.23 ns/pF)C _L	-	30	60	ns
			15 V	12 ns + (0.16 ns/pF)C _L	-	20	40	ns
	MR to Qn;	5 V	153 ns + (0.55 ns/pF)C _L	-	180	360	ns	
		see Figure 7	10 V	79 ns + (0.23 ns/pF)C _L	-	90	180	ns
			15 V	62 ns + (0.16 ns/pF)C _L	-	70	140	ns
t _{PLH}	PLH LOW to HIGH propagation delay	CP to Q0;	5 V	78 ns + (0.55 ns/pF)C _L	-	105	210	ns
		see Figure 7	10 V	39 ns + (0.23 ns/pF)C _L	-	50	95	ns
		15 V	27 ns + (0.16 ns/pF)C _L	-	35	70	ns	
		Qn to Qn + 1	5 V	43 ns + (0.55 ns/pF)C _L	-	70	140	ns
			10 V	14 ns + (0.23 ns/pF)C _L	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C _L	-	20	40	ns
t _t	transition time	see <u>Figure 7</u>	5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _W	pulse width	CP = HIGH;	5 V		50	25	-	ns
		minimum width;	10 V		25	15	-	ns
		see Figure 7	15 V		20	10	-	ns
		MR = HIGH;	5 V		130	65	-	ns
		minimum width;	10 V		95	50	-	ns
		see Figure 7	15 V		90	45	-	ns
t _{rec}	recovery time	MR input;	5 V		115	60	-	ns
		see Figure 7	10 V		65	35	-	ns
			15 V		55	25	-	ns
f _{max}	maximum	see Figure 7	5 V		5	10	-	MHz
	frequency		10 V		13	25	-	MHz
			15 V		18	35	-	MHz

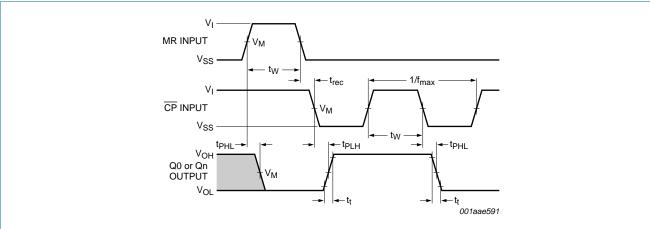
^[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

 P_D can be calculated from the formulas shown. $V_{SS} = 0 \ V$; $t_r = t_f \le 20 \ ns$; $T_{amb} = 25 \ ^{\circ}C$.

Symbol	Parameter	V _{DD}	Typical formula for P _D (μW)	where:
P_D	dynamic power	5 V	$P_D = 600 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
	dissipation	10 V	$P_D = 2800 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	fo = output frequency in MHz,
		15 V	$P_D = 8200 \times f_i + \Sigma (f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_0 \times C_L)$ = sum of the outputs.

11. Waveforms

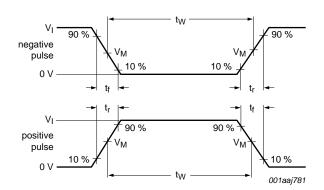


Measurement points are given in Table 9.

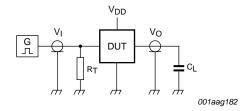
Fig 7. Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}



a. Input waveforms



b. Test circuit

Test data is given in <u>Table 10</u>.

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

 R_T = termination resistance should be equal to the output impedance Z_0 of the pulse generator.

Fig 8. Test circuit for measuring switching times

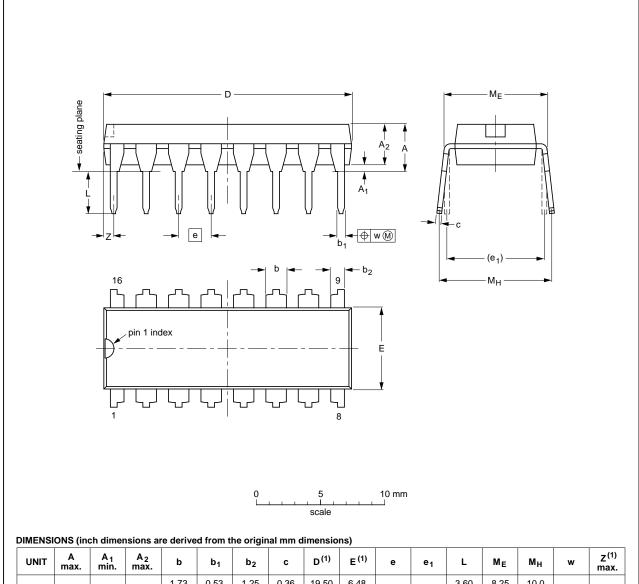
Table 10. Test data

Supply voltage	Input	Load			
V_{DD}	VI	t _r , t _f			
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF		

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

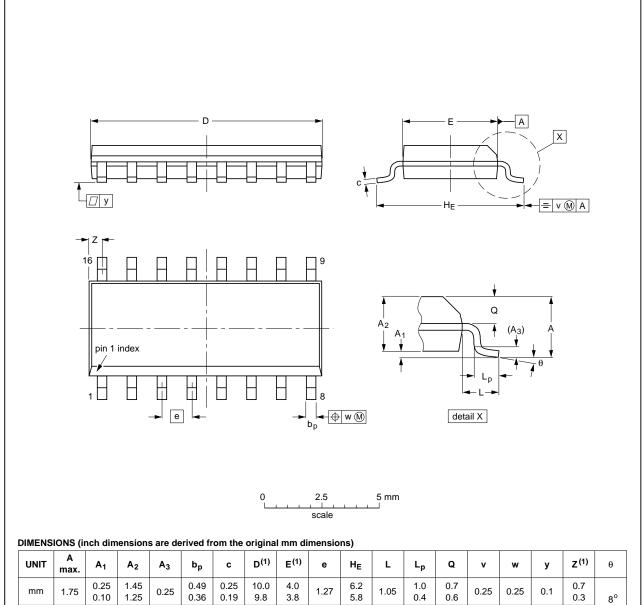
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC JEDEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT38-4						95-01-14 03-02-13	

Fig 9. Package outline SOT38-4 (DIP16)

HEF4020B

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	ø	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT109-1	076E07	MS-012				99-12-27 03-02-19	

Fig 10. Package outline SOT109-1 (SO16)

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13. Revision history

Table 11. Revision history

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Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4020B v.8	20111118	Product data sheet	-	HEF4020B v.7
Modifications:	 Legal pages 	s updated.		
	 Changes in 	"General description" and "	Features and benefits".	
	 Section "Ap 	plications" removed.		
HEF4020B v.7	20111010	Product data sheet	-	HEF4020B v.6
HEF4020B v.6	20091127	Product data sheet	-	HEF4020B v.5
HEF4020B v.5	20090707	Product data sheet	-	HEF4020B v.4
HEF4020B v.4	20081204	Product data sheet	-	HEF4020B_CNV v.3
HEF4020B_CNV v.3	19950101	Product specification	-	HEF4020B_CNV v.2
HEF4020B_CNV v.2	19950101	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition					
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.					
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.					
Product [short] data sheet	Production	This document contains the product specification.					

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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