ANALOG DEVICES

AD9363 Register Map Reference Manual
UG-1057

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

AD9363 Register Map

GENERAL DESCRIPTION

This reference manual contains a description of all of the user-programmable bits in the AD9363. When applicable, the map lists units, (such as dBFS) that the bits correspond to, the range of acceptable values, and the resolution of the value (such as 1 dB/LSB).

In many cases, multiple bits or bytes work together to serve a particular function (for example, those used to configure automatic gain control and those used to configure the digital interface). This section describes each bit but more information is available in the AD9363 Reference Manual.

While the register map is provided as a convenience for those who want to understand the low level operation of the device, it is not recommended to attempt to create your own software. Analog Devices, Inc., provides complete drivers for the AD9363 for both bare metal/No-OS and operating systems (Linux®). The AD9361, AD9364 and AD9363 share the same API. The AD9361, AD9363, and AD9364 drivers can be found at the following locations:

- Linux wiki page
- No-OS wiki page

Support for these drivers can be found at:

- Linux engineer zone page
- No-OS engineer zone page

Throughout this reference manual, a blank cell in the Default column of a register summary table indicates that there is no specific default setting available for the relevant register.

Complete specifications for the AD9363 can be found in the AD9363 data sheet, which is available from Analog Devices and should be consulted in conjunction with this user guide when using the evaluation board.

TABLE OF CONTENTS

REVISION HISTORY

11/2016—Revision 0: Initial Version

GENERAL SETUP AND DIGITAL DATA PORT CONFIGURATION REGISTERS

CHIP LEVEL SETUP REGISTERS (ADDRESS 0x000 THROUGH ADDRESS 0x007)

There are many thousands of filter and divider setting permutations, most of which are not valid operating modes. Analog Devices strongly recommends that customers use the software to program the AD9363 filters and clock dividers.

Table 1. Chip Level Setup Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x000	SPI configuration	Must be 0	3-wire SPI	LSB first	Open		LSB first	3-wire SPI	Must be 0	0x00	R/W
0x001	Tx monitor control	Open	Tx2 monitor enable	Tx1 monitor enable	Open	Set to 4'b0000				0x00	R/W
0x002	Tx enable and filter control	Tx channel enable[1:0]		THB3 enable and interpolation[1:0]		THB2 enable	THB1 enable	Tx FIR enable and interpolation[1:0]		0x5F	R/W
0x003	Rx enable and filter control	Rx channel enable[1:0]		RHB3 enable and decimation[1:0]		RHB2 enable	RHB1 enable	Rx FIR enable and decimation[1:0]		0x5F	R/W
0x004	Input select	Must be 0	Tx output	Rx input[5:0]						0x00	R/W
0x005	RF PLL dividers	Tx VCO divider[3:0]				Rx VCO divider[3:0]				0x00	R/W
0x006	Rx clock and data delay	DATA_CLK_x delay[3:0]				Rx data delay[3:0]				0x00	R/W
0x007	Tx clock and data delay	FB_CLK_x delay[3:0]				Tx Data delay[3:0]				0x00	R/W

SPI Register 0x000—SPI Configuration

This register is symmetrical (for example, Bit D6 is the same as Bit D1). The AD9363 powers up with a default serial peripheral interface (SPI) operation of MSB first. This register allows the baseband processor (BBP) to write any bits in Register 0x000 without having to reverse the bit order in the SPI command. Symmetrical bits are OR'ed together; therefore, setting one bit sets both bits.

Bit D7 and Bit D0—Must be 0

Bit D6 and Bit D1—3-Wire SPI

When clear, the SPI_DI pin is an input pin. When set, SPI_DI is bidirectional and SPI_DO is high impedance.

Bit D5 and Bit D2—LSB First

When clear, the SPI uses an MSB first format. When set, the SPI uses an LSB first format.

SPI Register 0x001—Tx Monitor Control

Bit D6—Tx2 Monitor Enable

This bit forces the Tx2 monitor path on, which shuts down the normal receive path. The receive path does not power up, even when the enable state machine moves to the Rx state. When this bit is set, the signal at the Tx Monitor 2 pin is sent as I and Q data to the Rx data port. To use transmit power monitoring, see the SPI Register 0x057—Analog Power-Down Override section and the SPI Register 0x06E—TPM Mode Enable section.

Bit D5—Tx1 Monitor Enable

This bit functions the same as Bit D6, but for the Tx_MON1 pin.

SPI Register 0x002—Tx Enable and Filter Control

Bits[D7:D6]—Tx Channel Enable[1:0]

The AD9361_EN_DIS_TX function sets these bits. These bits determine which of the two transmitters is enabled, with Bit D6 corresponding to Tx1 and Bit D7 corresponding to Tx2. Setting a bit enables a transmitter signal path. Clearing both bits disables both transmitters.

Bits[D5:D4]—THB3 Enable and Interpolation[1:0]

Note that there are several functions that calculate the digital filter settings. The AD9361_CALCULATE_RF_CLOCK_CHAIN function calculates all Rx and Tx rates.

These bits set interpolation of the digital filter that feeds the digital-to-analog converter (DAC) per Table 2.

Table 2. THB3 Interpolation Factor

Bits[D5:D4]	Interpolation Factor
00	Interpolate by 1, no filtering
01	Interpolate by 2 (half-band filter)
10	Interpolate by 3 and filter
11	Invalid

Bit D3—THB2 Enable

Setting this bit enables the interpolate by 2 THB2 half-band filter. Clearing this bit bypasses the filter. See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section.

Bit D2—THB1 Enable

Setting this bit enables the interpolate by 2 THB1 half-band filter. Clearing this bit bypasses the filter. See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section.

Bits[D1:D0]—Tx FIR Enable and Interpolation

These two bits control the programmable Tx finite impulse response (FIR) filter per Table 3. See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section.

Table 3. Tx FIR Interpolation and Filter Settings

Bits[D1:D0]	Interpolation Factor
00	Interpolate by 1 and bypass filter
01	Interpolate by 1 and enable filter
10	Interpolate by 2 and enable filter
11	Interpolate by 4 and enable filter

SPI Register 0x003—Rx Enable and Filter Control

Bits[D7:D6]—Rx Channel Enable[1:0]

The AD9361_EN_DIS_RX function sets these bits. These bits determine which of the two receivers is enabled, with Bit D6 corresponding to Receiver 1 and Bit D7 corresponding to Receiver 2. Setting a bit enables a receiver signal path. Clearing both bits disables both receivers.

Bits[D5:D4]—RHB3 Enable and Decimation

See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section (in the SPI Register 0x002—Tx Enable and Filter Control section). These bits set the decimation of the first filtering stage after the analog-to-digital converter (ADC) per Table 4.

Table 4. RHB3 Decimation Factor

Bits[D5:D4]	Decimation Factor
00	Decimate by 1, no filtering
01	Decimate by 2 (half-band filter)
10	Decimate by 3 and filter
11	Invalid

Bit D3—RHB2 Enable

See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section (in the SPI Register 0x002—Tx Enable and Filter Control section). Setting this bit enables the decimate by 2 RHB2 half-band filter. Clearing this bit bypasses the filter.

Bit D2—RHB1 Enable

See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section (in the SPI Register 0x002—Tx Enable and Filter Control section). Setting this bit enables the decimate-by 2 RHB1 half-band filter. Clearing this bit bypasses the filter.

Bits[D1:D0]—Rx FIR Enable and Decimation[1:0]

See the Bits[D5:D4]—THB3 Enable and Interpolation[1:0] section (in the SPI Register 0x002—Tx Enable and Filter Control section). These two bits control the programmable Rx FIR filter per Table 5.

Table 5. Rx FIR Decimation and Filter Settings

[D1:D0]	Decimation Factor and Filter Function
00	Decimate by 1 and bypass filter
01	Decimate by 1 and enable filter
10	Decimate by 2 and enable filter
11	Decimate by 4 and enable filter

SPI Register 0x004—Input Select

Bit D7—Must be 0

Bit D6—Tx Output

The ad9361_init configures this bit. Each transmitter signal path has two radio frequency (RF) output ports (A and B). Clearing this bit selects Tx1A and Tx2A, and setting the bit selects Tx1B and Tx2B.

Bits[D5:D0]—Rx Input[5:0]

The ad9361_init configures these bits. Each receiver signal path has three internal low noise amplifiers (LNAs). In addition, the receivers can operate in balanced or unbalanced mode. The AD9363 configures both receiver signal paths the same way, with each of the six bits activating a particular input. Valid cases are shown in Table 6. No other options are valid.

Table 6. Enabled Rx Inputs

Bits[D5:D0]	Enabled Rx Inputs
000001	Rx1A_N and Rx2A_N enabled; unbalanced
000010	Rx1A_P and Rx2A_P enabled; unbalanced
000100	Rx1B_N and Rx2B_N enabled; unbalanced
001000	Rx1B_P and Rx2B_P enabled; unbalanced
010000	Rx1C_N and Rx2C_N enabled; unbalanced
100000	Rx1C_P and Rx2C_P enabled; unbalanced
000011	(Rx1A_N and Rx1A_P) and (Rx2A_N and Rx2A_P) enabled; balanced
001100	(Rx1B_N and Rx1B_P) and (Rx2B_N and Rx2B_P) enabled; balanced
110000	(Rx1C_N and Rx1C_P) and (Rx2C_N and Rx2C_P) enabled; balanced

SPI Register 0x005—RF PLL Dividers

Bits[D7:D4]—Tx VCO Divider[2:0]

The AD9361_SET_TX_LO_FREQ function configures these bits. The internal voltage controlled oscillator (VCO) operating range is 6 GHz to 12 GHz. A divider after the VCO allows a wide range of possible Tx local oscillator (LO) frequencies. The register value maps per Equation 1.

$$Divider\ Value = 2(Tx\ VCO\ Divider\ bits + 1) \quad (1)$$

The BBP must program this register correctly for the Tx LO frequency to be correct. Table 7 shows register vs. desired Tx LO.

Table 7. Tx VCO Divider

Tx LO Frequency Range	Divide by	Tx VCO Divider[2:0] Setting
3000 MHz to 3800 MHz	2	1
1500 MHz to 3000 MHz	4	2
750 MHz to 1500 MHz	8	3
375 MHz to 750 MHz	16	4
325 MHz to 375 MHz	32	5

Bits[D3:D0]—Rx VCO Divider

The AD9361_SET_RX_LO_FREQ function configures these bits. These bits function the same as Bits[D7:D4] in this register, but program the Rx VCO divider.

SPI Register 0x006—Rx Clock and Data Delay

These bits affect the DATA_CLK and the Rx data delays. The typical delay is approximately 0.3 ns/LSB. The Rx frame is delayed by the same amount as the data port bits. The minimum delay setting is 0x0 and the maximum delay is 0xF. Set this register so that the data from the AD9363 meets BBP setup/hold specifications.

SPI Register 0x007—Tx Clock and Data Delay

This register function the same as Register 0x006 but affects the FB_CLK, TX_FRAME, and Tx data bits. Tx frame sync is delayed by the same amount as the data port bits. Set this register so that the data from the BBP meets the AD9363 setup/hold specifications.

CLOCK CONTROL REGISTERS (ADDRESS 0x009 THROUGH ADDRESS 0x00A)

Table 8. Clock Control Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x009	Clock enable	Open		Must be 0	Set to 1	Must be 0	Digital power-up	Set to 1	BB PLL enable	0x10	R/W
0x00A	BB PLL	CLK_OUT select[2:0]			CLK_OUT enable	DAC clock divide by 2	BB PLL divider[2:0]			0x03	RW

SPI Register 0x009—Clock Enable

The AD9361_INIT function sets up many registers, including Register 0x009.

Bit D5—Must Be 0

Bit D4—Set to 1

Bit D3—Must Be 0

Bit D2—Digital Power-Up

When clear, the AD9363 shuts down the digital logic clocks. The BBP can still write to the directly addressable SPI registers. When set, all digital clocks are operational. The AD9363 powers up with this bit clear and it is set during initialization.

Bit D1—Set to 1

Bit D0—BB PLL Enable

Clearing this bit disables the baseband (BB) phase-locked loop (PLL), and setting this bit enables the BB PLL. The AD9363 powers up with this bit clear and it is set during initialization.

SPI Register 0x00A—BB PLL

Bits[D7:D5]—CLK_OUT Select[2:0]

The CLK_OUTPUT_MODE_SELECT function controls these bits. These bits set the CLK_OUT frequency per Table 9. Set Bit D4 to enable this function.

Table 9. CLK_OUT Frequency

CLK_OUT Select[2:0]	CLK_OUT Frequency
000	ADC CLK buffered
001	ADC_CLK/2
010	ADC_CLK/3
011	ADC_CLK/4
100	ADC_CLK/8
101	ADC_CLK/16
110	ADC_CLK/32
111	ADC_CLK/64

Bit D4—CLK_OUT Enable

The AD9361_CLK_OUTPUT_MODE_SELECT function controls this bit. Setting this bit routes a clock with a rate specified in Table 9 to the CLK_OUT ball. When clear, the AD9363 drives out logic zero.

Bit D3—DAC Clock Divide by 2

The AD9361_CALCULATE_RF_CLOCK_CHAIN function configures this bit. When clear, the DAC clock rate equals the ADC clock rate. When set, the DAC clock equals ½ of the ADC rate.

Bits[D2:D0]—BBPLL Divider[2:0]

The AD9361_BBPLL_SET_RATE function controls these bits. The ADC clock rate equals the BB PLL divided by the factor in this register, shown in Equation 2.

$$ADC\ Clock\ Rate = \frac{BB\ PLL\ Clock\ Rate}{2^{BB\ \ PLL\ \ Divider[2:0]\ (\text{decimal})}} \quad (2)$$

The BB PLL divider[2:0] bits are valid from 1 through 6.

TEMPERATURE SENSOR REGISTERS (ADDRESS 0x00C THROUGH ADDRESS 0x00F)

Table 10. Temperature Sensors Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x00B	Temperature sense offset	Temperature sense offset[7:0]								0x00	R/W
0x00C	Temperature Sense 1	Open							Start temperature reading		R/W
0x00D	Temperature Sense 2	Measurement time interval[6:0]							Temperature sense periodic enable	0x03	R/W
0x00E	Temperature	Temperature[7:0]									R
0x00F	Temperature sensor configuration	Open					Temperature sensor decimation[2:0]			0x04	R/W

The AD9361_AUXADC_SETUP function handles temperature sensor setup, as well as auxiliary ADC setup. The temperature sensor is internal to the AD9363. To determine system temperature, use external temperature sensors.

SPI Register 0x00B—Temperature Sense Offset

See the SPI Register 0x00E—Temperature section.

SPI Register 0x00C—Temperature Sense 1

Bit D0—Start Temperature Reading

Set this bit to manually start a temperature reading; this action only applies if Register 0x00D, Bit D0 is clear. Bit D0 is not self-clearing. To calculate the temperature again, this bit must be cleared and then set again.

SPI Register 0x00D—Temperature Sense 2

Bits[D7:D1]—Measurement Time Interval[6:0]

These bits only apply if Bit D0 is set, in which case the AD9363 takes temperature readings periodically at the rate per Equation 3.

$$Period\ (\text{sec}) = \frac{Measurement\ Time\ Interval[6:0] \times 2^{29}}{BB\ PLL\ Clock\ Frequency\ (\text{Hz})} \quad (3)$$

Bit D0—Temperature Sense Periodic Enable

See Register 0x00D, Bits[D7:D1]in the Bits[D7:D1]—Measurement Time Interval[6:0] section and Register 0x00C, Bit D0 in the Bit D0—Start Temperature Reading section.

SPI Register 0x00E—Temperature

The temperature word is proportional to internal die temperature with a slope of 1.16 × temperature. The value in Register 0x00E is related to temperature and then added to the value in Register 0x00B. When reading the temperature, disable the auxiliary ADC by setting Register 0x01D, Bit D0 to ensure a valid temperature reading.

SPI Register 0x00F—Temperature Sensor Configuration

Bits[D2:D0]—Temperature Sensor Decimation[2:0]

Decimation of the auxiliary ADC is used to derive the temperature per Equation 4. The AD9363 uses a sigma-delta (Σ-Δ) auxiliary ADC to perform the temperature measurement. The auxiliary ADC clock rate is always the BB PLL rate divided by 64 when using the temperature sensor.

$$Temperature\ Sensor\ Decimation = 256 \times 2^{Temperature\ Sensor\ Decimation[2:0]} \quad (4)$$

PARALLEL PORT CONFIGURATION REGISTERS (ADDRESS 0x010 THROUGH ADDRESS 0x012)

Table 11. Parallel Port Configuration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x010	Parallel Port Configuration 1	Parallel port Tx swap IQ	Parallel port Rx swap IQ	Tx channel swap	Rx channel swap	Rx frame pulse mode	2R2T timing	Invert data bus	Invert DATA_CLK_x	0xC0	R/W
0x011	Parallel Port Configuration 2	FDD alternate word order	Must be 0		Invert Tx1	Invert Tx2	Invert Rx frame	Delay Rx data[1:0]		0x00	R/W
0x012	Parallel Port Configuration 3	FDD Rx rate = 2 × Tx rate	Swap ports	Single data rate	LVDS mode	Half duplex mode	Single port mode	Full port	Full duplex swap bit	0x04	R/W

SPI Register 0x010—Parallel Port Configuration 1

Bit D7—Parallel Port Tx Swap IQ

Clearing this bit swaps I and Q (performs spectral inversion).

Bit D6—Parallel Port Rx Swap IQ

This bit functions the same as Bit D7, but for the Rx path.

Bit D5—Tx Channel Swap

Setting this bit swaps the positions of the Tx1 and Tx2 samples.

Bit D4—Rx Channel Swap

This bit functions the same as Bit D5, but for the Rx path.

Bit D3—Rx Frame Pulse Mode

The AD9363 outputs an Rx frame sync signal to indicate the beginning of an Rx frame. When this bit is clear, the Rx frame goes high coincident with the first valid received sample. The Rx frame stays high as long as the receivers are enabled. When this bit is set, the Rx frame signal toggles with a duty cycle of 50%.

Bit D2—2R2T Timing

When set, the data port uses 2R2T timing, regardless of the number of enabled transmitters and receivers. When clear, the timing reflects the number of enabled signal paths.

Bit D1—Invert Data Bus

This bit inverts the data port(s) from Px_D11 to Px_D0, and back to Px_D0 to Px_D11.

Bit D0—Invert DATA_CLK_x

Setting this bit inverts DATA_CLK_x.

SPI Register 0x011—Parallel Port Configuration 2

Bit D7—FDD Alternate Word Order

This bit is valid only in full duplex, dual port, full port mode. When this bit is set, each port splits into two 6-bit halves. Rx1 uses 6 bits of a port and Rx2 uses the other 6 bits of the port (receivers are not interleaved). Tx1 and Tx2 are organized similarly.

Bits[D6:D5]—Must be 0

Bit D4—Invert Tx1

Setting this bit digitally multiplies the Tx1 signal by −1.

Bit D3—Invert Tx2

Setting this bit digitally multiplies the Tx2 signal by −1.

Bit D2—Invert Rx Frame

Setting this bit inverts the Rx frame.

Bits[D1:D0]—Delay Rx Data[1:0]

These bits set the delay of the Rx data relative to Rx frame, measured in ½ DATA_CLK_x cycles for double data rate (DDR) mode and full DATA_CLK_x cycles for single data rate (SDR) mode.

SPI Register 0x012—Parallel Port Configuration 3

Bit D7—FDD Rx Rate = 2 × Tx Rate

When clear, the Rx sample rate is equal to the Tx sample rate. When set, the Rx rate is twice the Tx rate. This bit can only be set when Bit D3 of Register 0x012 is clear (full duplex mode).

Bit D6—Swap Ports

Setting this bit swaps Port 0 and Port 1. This bit must be clear for LVDS mode.

Bit D5—Single Data Rate

When clear, both edges of DATA_CLK_x are used. When set, only one edge of DATA_CLK_x is used.

Bit D4—LVDS Mode

When clear, the data port uses single-ended CMOS mode. Set this bit to use LVDS mode. Full duplex mode (Register 0x012, Bit D3 is clear), DDR mode (Register 0x012, Bit D5 is clear), and dual port mode (Register 0x012, Bit D2 is clear) are required.

Bit D3—Half Duplex Mode

Clearing the bit allows simultaneous bidirectional data. Setting the bit allows data to flow in only one direction at a time. Normally, this bit equals the inverse of Register 0x013, Bit D0.

Bit D2—Single Port Mode

When clear, Port 0 and Port 1 are both used. When set, only one data port is used.

Bit D1—Full Port

This bit is used only in full duplex mode (Bit D3 is clear) and dual port mode (Bit D2 is clear). Setting this bit forces the receivers to be on one port and the transmitters to be on the on the other port. Clearing the bit mixes receivers and transmitters on each port.

Bit D0—Full Duplex Swap Bit

This bit toggles between the bits used for receive data and those used for transmit data with one exception. If the frequency division duplex (FDD) alternate word order bit (Register 0x011, Bit D7) is set, then the effect is to swap the most significant 6 bits with the least significant 6 bits. It is not always valid to set this bit.

ENABLE STATE MACHINE (ENSM) REGISTERS (ADDRESS 0x013 THROUGH ADDRESS 0x017)

Table 12. ENSM Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x013	ENSM mode	Open							FDD mode	0x01	R/W
0x014	ENSM Configuration 1	Enable Rx data port	Force Rx on	Force Tx on	ENSM pin control	Level mode	Force alert state	Auto gain lock	To alert	0x13	R/W
0x015	ENSM Configuration 2	FDD external control enable	Power down Rx synthesizer	Power down Tx synthesizer	TXNRX SPI control	Synthesizer pin control mode	Dual synthesizer mode	Rx synthesizer ready mask	Tx synthesizer ready mask	0x08	R/W
0x016	Calibration control	Rx baseband tune	Tx baseband tune	Must be 0	Tx quadrature calibration	Rx gain step calibration	Open	DC calibration RF start	DC calibration baseband start	0x00	R/W
0x017	State	Calibration sequence state[3:0]				ENSM state[3:0]					R

The AD9361_SET_EN_STATE_MACHINE_MODE function configures Register 0x013 through Register 0x015.

SPI Register 0x013—ENSM Mode

Bit D0 controls the ENSM. Clear this bit for time division duplex (TDD) mode; set this bit for FDD mode.

SPI Register 0x014—ENSM Configuration 1

Bit D7—Enable Rx Data Port for Cal

In TDD mode, during the Tx state, setting this bit enables the Rx data port. If Tx monitor(s) are also enabled, the Tx monitor I/Q data is present on the Rx input/output (I/O) port.

Bit D6—Force Rx On

Setting this bit puts the ENSM into the Rx state when operating in TDD mode; it is ignored in FDD mode. Clearing this bit moves the ENSM back to the alert state via the Rx flush state. During this state, the ENSM ignores SPI commands that affect it.

Bit D5—Force Tx On

Setting this bit puts the ENSM into the transmit state when operating in TDD mode. In FDD mode, setting this bit puts the ENSM into the FDD state. Clearing this bit moves the ENSM back to the alert state vis the flush state(s) and, during this state, the ENSM ignores SPI commands that affect it.

Bit D4—ENSM Pin Control

When this bit is set, the ENSM responds to the enable and TXNRX signals and changes states accordingly. When this bit is clear, SPI writes to the bits in Register 0x014 to change the state.

Bit D3—Level Mode

When this bit is clear, enable pulses move the ENSM among its states. When this bit is set, the level of the ENABLE pin and (in TDD mode) the level of the TXNRX signal determines the state.

Bit D2—Force Alert State

If the ENSM is in the wait state, setting this bit forces the ENSM to the alert state. From any other state, setting this bit moves the ENSM to the alert state if the to alert bit (Bit D0) is set; otherwise, it moves the ENSM to the wait state.

Bit D1—Auto Gain Lock

This bit only applies if the gain unlock control bit (Register 0x0FB, Bit D6) is set and only when automatic gain control (AGC) is used in fast attack mode. Setting this bit allows the gain to stay locked, even if certain overload conditions occur.

Bit D0—To Alert

If this bit is clear, the ENSM always moves from the Rx, Tx, or FDD states to the wait state. If this bit is set, the ENSM moves to the alert state.

SPI Register 0x015—ENSM Configuration 2

Bit D7—FDD External Control Enable

This bit only applies when the ENSM FDD mode bit (Register 0x013, Bit D0) is set. Setting this bit allows independent control of the receivers and transmitters using the ENABLE and TXNRX signals, and is commonly referred to as FDD independent control mode.

Bit D6—Power Down Rx Synthesizer

This bit is a test bit and is normally clear. Set this bit to power down the Rx RF synthesizer.

Bit D5—Power Down Tx Synthesizer

This bit is a test bit and is normally clear. Set this bit to power down the Tx RF synthesizer.

Bit D4—TXNRX SPI Control

This bit is only used in single synthesizer mode (Bit D2 is clear) and synthesizer enable pin control mode (Bit D3 is clear). See the Bit D3—Synthesizer Pin Control Mode section.

Bit D3—Synthesizer Pin Control Mode

This bit is used in single synthesizer mode (Bit D2 is clear). When set, the TXNRX pin controls which RF synthesizer is enabled. When clear, Bit D4 controls which synthesizer is enabled.

Bit D2—Dual Synthesizer Mode

If this bit is clear, only one RF synthesizer is on at any given time. When this bit is set, both synthesizers are always on.

Bit D1—Rx Synthesizer Ready Mask

This bit is normally clear. When this bit is clear, the ENSM does not move to the Rx state unless the Rx RF VCO is successfully calibrated. When set, the ENSM disregards the VCO calibration status.

Bit D0—Tx Synthesizer Ready Mask

This bit functions the same as Bit D1, but for the Tx VCO.

SPI Register 0x016—Calibration Control

Bit D7—Rx Baseband Tune

The AD9361_RX_RF_BANDWIDTH function configures and runs the Rx baseband filter calibration. Setting this bit starts the receiver analog baseband filter calibration and self clears when the calibration completes.

Bit D6—Tx Baseband Tune

The AD9361_TX_RF_BANDWIDTH function configures and runs the Tx baseband filter calibration. This bit functions the same as Bit D7, but for the transmit filter.

Bit D5—Must be 0

Bit D4—Tx Quadrature Calibration

The AD9361_TX_QUAD_CALIB FUNCTION configures and runs the Tx quadrature calibration. Setting this bit starts the Tx quadrature calibration. This bit self clears when the calibration completes.

Bit D3—Rx Gain Step Calibration

Setting this bit starts a low noise amplifier (LNA) and mixer gain step calibration, and self clears when the calibration completes. An external RF signal must be present at the Rx inputs.

Bit D1—DC Calibration RF Start

The AD9361_RF_DC_OFFSET_CALIB function configures and runs the RF dc calibration. Setting this bit performs an RF dc offset calibration of the Rx signal paths, and the bit self clears when the calibration completes.

Bit D0—DC Calibration Baseband Start

The AD9361_BB_DC_OFFSET_CALIB function configures and runs the baseband dc calibration. Setting this bit performs a baseband dc offset calibration of the Rx signal paths and self clears when the calibration completes.

SPI Register 0x017—State (Read Only)

Bits[D7:D4] Calibration Sequence State[3:0]

Table 13 shows the states of the calibration state machine.

Table 13.Calibration State

Calibration State	Register 0x017, Bits[7:4]
Calibrations Done	1
Baseband DC Offset Calibration	2
RF DC Offset Calibration	3
Tx1 Quadrature Calibration	4
Tx2 Quadrature Calibration	5
Rx Gain Step Calibration	9
Baseband Calibration Flush	A
RF Calibration Flush	B
Tx Quadrature Calibration Flush	C
Tx Power Detector Calibration Flush	E
Rx Gain Step Calibration Flush	F

Bits[D3:D0]—ENSM State[3:0]

Table 14 shows the states of the ENSM.

Table 14. ENSM State

ENSM State	Reg. 0x017, Bits[3:0]	Notes
Sleep	0	AD9363 clocks/baseband PLL disabled
Wait	0	Clocks enabled
Alert	5	Synthesizers enabled
Tx	6	Tx signal chain enabled
Tx Flush	7	Tx digital block flush time
Rx	8	Rx signal chain enabled
Rx Flush	9	Rx digital block flush time
FDD	A	Tx and Rx signal chains enabled
FDD Flush	B	Flush all digital signal path blocks

AUXILIARY DAC REGISTERS (ADDRESS 0x018 THROUGH ADDRESS 0x01B)

Table 15. Auxiliary DAC Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x018	Auxiliary DAC 1 word	Auxiliary DAC 1 word[9:2]								0x00	R/W
0x019	Auxiliary DAC 2 word	Auxiliary DAC 2 word[9:2]								0x00	R/W
0x01A	Auxiliary DAC 1 configuration	Open		Must be 0	Auxiliary DAC 1 step factor	Auxiliary DAC 1 V_{REF}[1:0]		Auxiliary DAC 1 word[1:0]		0x00	R/W
0x01B	Auxiliary DAC 2 configuration	Open		Must be 0	Auxiliary DAC 2 step factor	Auxiliary DAC 2 V_{REF}[1:0]		Auxiliary DAC 2 word[1:0]		0x00	R/W

The AD9361_AUXDAC_SETUP function configures the auxiliary DACs. Register 0x023, Register 0x026, and Register 0x030 to Register 0x033 determine the auxiliary DACs enable/disable state. For ease of use, review the SPI Register 0x023—Auxiliary DAC Enable Control section, the SPI Register 0x026—External LNA Control section, and the SPI Register 0x030 Through SPI Register 0x033—Auxiliary DACx Rx/Tx Delay[7:0] section.

SPI Register 0x018, SPI Register 0x019, SPI Register 0x01A, Bits[D1:D0], and SPI Register 0x01B, Bits[D1:D0]—Auxiliary DAC 1 Word and Auxiliary DAC 2 Word

The auxiliary DAC output voltage is defined by Equation 5.

SPI Register 0x01A—Auxiliary DAC 1 Configuration

Bit D5—Must be 0

Bit D4—Auxiliary DAC 1 Step Factor

If this bit is clear, the step factor in Equation 5 = 2. If the bit is set, the step factor = 1.

Bits[D3:D2]—Auxiliary DAC 1 V_{REF}[1:0]

These bits encode the V_{REF} factor in Equation 5. Table 16 shows the encoding.

Table 16. Auxiliary DAC V_{REF}

Auxiliary DAC 1 V_{REF}[1:0]	V_{REF} (V)
00	1.0
01	1.5
10	2.0
11	2.5

SPI Register 0x01B—Auxiliary DAC 2 Configuration

These bits function the same as Register 0x01A, but apply to Auxiliary DAC 2.

$$Auxiliary\ DAC\ V_{OUT}\ (\mathrm{V}) = 0.97 \times V_{REF} + (0.000738 + 9 \times 10^{-6} \times (V_{REF} \times 1.6 - 2)) \times Auxiliary\ DAC\ Word[9:0] \times Step\ Factor - 0.3572 \times Step\ Factor + 0.05 \quad (5)$$

where:
Auxiliary DAC V_{OUT}, at a maximum, is limited to 3 V for VDD_GPO = 3.3 V.
V_{REF} is set by Register 0x01A, Bits[D3:D2] (Auxiliary DAC 1) and Register 0x01B, Bits[D3:D2] (Auxiliary DAC 2).
Step Factor is set by Register 0x01A, Bit D4 (Auxiliary DAC 1) and Register 0x01B, Bit D4 (Auxiliary DAC 2).
The auxiliary DAC words are located in Register 0x018 through Register 0x01B.

AUXILIARY ADC REGISTERS (ADDRESS 0x01C THROUGH ADDRESS 0x01F)

Table 17. Auxiliary ADC Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x01C	Auxiliary ADC clock divider	Open		Auxiliary ADC clock divider[5:0]						0x10	R/W
0x01D	Auxiliary ADC configuration	Open				Auxiliary ADC decimation[2:0]			Auxiliary ADC power-down	0x01	R/W
0x01E	Auxiliary ADC word MSB	Auxiliary ADC word MSB[11:4]									R
0x01F	Auxiliary ADC word LSB	Open				Auxiliary ADC word LSB[3:0]					R

The AD9361_AUXADC_SETUP function configures the auxiliary ADC.

SPI Register 01C—Auxiliary ADC Clock Divider

Bits[D5:D0]—Auxiliary ADC Clock Divider[5:0]

The auxiliary ADC clock results from dividing down the baseband PLL (BB PLL), described in Equation 6. A divider value of 0 is invalid.

$$Auxiliary\ ADC\ Clock\ Frequency = \frac{BB\ PLL\ Frequency}{Auxiliary\ ADC\ Clock\ Divider[5:0]} \quad (6)$$

SPI Register 0x01D—Auxiliary ADC Configuration

Bits[D3:D1]—Auxiliary ADC Decimation[2:0]

These bits set the auxiliary ADC decimation per Equation 7.

$$Auxiliary\ ADC\ Decimation = 256 \times 2^{Auxiliary\ ADC\ Decimation[2:0]} \quad (7)$$

Bit D0—Auxiliary ADC Power-Down

Setting this bit powers down the auxiliary ADC.

SPI Register 0x01E and SPI Register 0x01F—Auxiliary ADC Word MSB and Auxiliary ADC Word LSB

These registers hold the 12-bit auxiliary ADC word. When reading the auxiliary ADC word, disable the temperature sensor or prevent it from updating.

GENERAL-PURPOSE OUTPUTS (GPOs), AUXILIARY DAC, AGC DELAY, AND SYNTHESIZER DELAY CONTROL REGISTERS (ADDRESS 0x020 THROUGH ADDRESS 0x033)

Table 18. GPOs, Auxiliary DAC, AGC Delay, and Synthesizer Delay Control Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x020	Auto GPO_x	GPO_x enable auto Rx[3:0]				GPO_x enable auto Tx[3:0]				0x33	R/W
0x021	AGC gain lock delay	Gain lock delay[7:0]								0x0A	R/W
0x022	AGC attack delay	Open	Invert bypassed LNA polarity	AGC attack delay[5:0]						0x0A	R/W
0x023	Auxiliary DAC enable control	Auxiliary DAC manual bar[1:0]		Auxiliary DAC auto Tx bar[1:0]		Auxiliary DAC auto Rx bar[1:0]		Auxiliary DAC initial bar[1:0]		0x3f	R/W
0x024	Rx load synthesizer delay	Must be 0x02								0x02	R/W
0x025	Tx load synthesizer delay	Must be 0x02								0x02	R/W
0x026	External LNA control	Auxiliary DAC manual select	External LNA 2 control	External LNA 1 control	GPO manual select	Open[3:0]				0x00	R/W
0x027	GPO force and initialization	GPO manual control[3:0]				GPO initialization state[3:0]				0x03	R/W
0x028	GPO_0 Rx delay	GPO_0 Rx delay[7:0]								0x00	R/W
0x029	GPO_1 Rx delay	GPO_1 Rx delay[7:0]								0x00	R/W
0x02A	GPO_2 Rx delay	GPO_2 Rx delay[7:0]								0x00	R/W
0x02B	GPO_3 Rx delay	GPO_3 Rx delay[7:0]								0x00	R/W
0x02C	GPO_0 Tx Delay	GPO_0 Tx delay[7:0]								0x00	R/W
0x02D	GPO_1 Tx Delay	GPO_1 Tx delay[7:0]								0x00	R/W
0x02E	GPO_2 Tx Delay	GPO_2 Tx delay[7:0]								0x00	R/W
0x02F	GPO_3 Tx Delay	GPO_3 Tx delay[7:0]								0x00	R/W
0x030	Auxiliary DAC 1 Rx delay	Auxiliary DAC 1 Rx delay[7:0]								0x00	R/W
0x031	Auxiliary DAC 1 Tx delay	Auxiliary DAC 1 Tx delay[7:0]								0x00	R/W
0x032	Auxiliary DAC 2 Rx delay	Auxiliary DAC 2 Rx delay[7:0]								0x00	R/W
0x033	Auxiliary DAC 2 Tx delay	Auxiliary DAC 2 Tx delay[7:0]								0x00	R/W

The AD9361_GPO_SETUP function configures the GPOs. See the Auxiliary DAC Registers (Address 0x018 Through Address 0x01B) section and the Auxiliary ADC Registers (Address 0x01C Through Address 0x01F) section to configure the auxiliary converters. When the AD9363 powers up into the sleep state, the default register values define the GPO logic levels. Thus, the GPOs auto toggle; GPO_0 and GPO_1 are high and GPO_2 and GPO_3 are low.

SPI Register 0x020—Auto GPO_x

Bits[D7:D4]—GPO_x Enable Auto Rx[3:0]

This nibble controls which GPO_x pins change state when the ENSM enters the Rx state. Bit D7 controls GPO_3, Bit D6 controls GPO_2, Bit D5 controls GPO_1, and Bit D4 controls GPO_0. These bits are ignored if Register 0x026, Bit D4 is set.

Bits[D3:D0]—GPO_x Enable Auto Tx[3:0]

These bits function the same as Bits[D7:D4], but apply when the ENSM enters the Tx state. These bits are ignored if Register 0x026, Bit D4 is set.

SPI Register 0x021—AGC Gain Lock Delay

This register only applies if Register 0x014, Bit D1 and Register 0xFB, Bit D6 are set, allowing the gain to stay locked even if certain overload conditions occur.

SPI Register 0x022—AGC Attack Delay

Bit D6—Invert Bypassed LNA Polarity

If the gain changes due to varying signal conditions every few milliseconds (or even more often) such that the LNA is alternating between bypassed (Index 0) and not bypassed (Index 1), the rapid phase switching plus compensation from this bit can cause a higher than expected dc offset. Only set this bit if the demodulating algorithm is sensitive to the phase changes that are already present in the LNA alone and if the gain is not expected to switch often enough to aggravate the dc offset algorithm. If neither of these phase changing options are acceptable, a custom gain table must be built to eliminate either LNA Index 0 or LNA Index 1 through Index 3. The analog.com Engineer Zone support pages contain documents with example custom gain tables and describe how to build such a table.

Bits[D5:D0]—AGC Attack Delay

These bits apply to fast AGC mode. The AGC attack delay prevents the AGC from starting its algorithm until the receive path settles. The delay counter starts when the ENSM enters the Rx state. The units are microseconds, resolution = 1 µs/LSB, range = 0 through 31 microseconds. For the value in microseconds to be accurate, Register 0x03A must be set correctly.

SPI Register 0x023—Auxiliary DAC Enable Control

Bits[D7:D6]—Auxiliary DAC Manual Bar[1:0]

Clearing Bit D7 manually enables Auxiliary DAC 2. Clearing Bit D6 manually enables Auxiliary DAC 1. These bits are ignored if Register 0x026, Bit D] is clear.

Bits[D5:D4]—Auxiliary DAC Auto Tx Bar[1:0]

Clearing Bit D5 causes Auxiliary DAC 2 to change state when the ENSM enters the Tx state. Bit D4 controls Auxiliary DAC 1 in the same manner. These bits are ignored if Register 0x026, Bit D7 is set.

Bits[D3:D2]—Auxiliary DAC Auto Rx Bar[1:0]

Clearing Bit D3 causes Auxiliary DAC 2 to change state when the ENSM enters the Rx state. Bit D2 controls Auxiliary DAC 1 in the same manner. These bits are ignored if Register 0x026, Bit D7 is set.

Bits[D1:D0]—Auxiliary DAC Initial Bar[1:0]

Clearing Bit D1 sets the state of Auxiliary DAC 2 to on when the ENSM is in the alert state. Bit D0 controls Auxiliary DAC 1 in the same manner. These bits are ignored if Register 0x026, Bit D7 is set.

SPI Register 0x024—Rx Load Synthesizer Delay

The bits in this register must be set to 0x02.

SPI Register 0x025—Tx Load Synthesizer Delay

The bits in this register must be set to 0x02.

SPI Register 0x026—External LNA Control

Bit D7—Auxiliary DAC Manual Select

When this bit is clear, the auxiliary DAC states slaves to the ENSM. When this bit is set, SPI writes to Register 0x023, Bits[D7:D6] manually control the state of the auxiliary DACs.

Bit D6—External LNA 2 Control

When set, the external LNA control bit in the Rx2 gain table sets the GPO_1 state.

Bit D5—External LNA 1 Control

This bit functions the same as Bit D6, but applies to the Rx1 gain table and to GPO_0.

Bit D4—GPO Manual Select

When this bit is clear, the GPOs slave to the ENSM. When this bit is set, Register 0x027, Bits[D7:D4] set the value of the GPOs.

SPI Register 0x027—GPO Force and Initialization

Bits[D7:D4]—GPO Manual Control[3:0]

When these bits are clear, the GPOs are logic low. When these bits are set, the GPOs are logic high. Bit D7 controls GPO_3, Bit D6 controls GPO_2, Bit D5 controls GPO_1, and Bit D4 controls GPO_0. These bits only apply when Register 0x026, Bit D4 is set.

Bits[D3:D0]—GPO Initialization State[3:0]

When these bits are clear, the GPOs are logic low in the sleep, wait, and alert states. When these bits are set, the GPOs are logic high. Bit D3 controls GPO_3, Bit D2 controls GPO_2, Bit D1 controls GPO_1, and Bit D0 controls GPO_0. These bits are only applicable when the GPO states are slaved to the ENSM, and if Register 0x026, Bit D] is clear.

SPI Register 0x028 Through SPI Register 0x02B—GPO_x Rx Delay[7:0]

These registers are only applicable if the GPOs are slaved to the ENSM (Register 0x026, Bit D4 is clear). These registers set the delay from ENSM changing to Rx to the time that the GPOs change logic level: 1 µs/LSB with a range from 0 µs to 255 µs. The delay from the ENSM change of Rx to alert is always fixed, allowing the Rx flush state before changing the GPO states. Register 0x03A must be set correctly for the delay resolution to be 1 µs/LSB.

SPI Register 0x02C Through SPI Register 0x02F—GPO_x Tx Delay[7:0]

These registers function the same as Register 0x028 to Register 0x02B, but for the transition from the alert state to the Rx state.

SPI Register 0x030 Through SPI Register 0x033—Auxiliary DACx Rx/Tx Delay[7:0]

These delays affect the state of the auxiliary DACs similar to how Register 0x028 through Register 0x02B affect the GPOs. These registers are only applicable if Register 0x026, Bit D7 is clear.

CONTROL OUTPUT REGISTERS (ADDRESS 0x035 THROUGH ADDRESS 0x036)

Table 19. Control Output Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x035	Control output pointer	Control output pointer[7:0]								0x00	R/W
0x036	Control output enable	Enable Control Output 7	Enable Control Output 6	Enable Control Output 5	Enable Control Output 4	Enable Control Output 3	Enable Control Output 2	Enable Control Output 1	Enable Control Output 0	0xFF	R/W

Table 20. Control Output Bit and Control Output Ball Mapping

Control Output Bit Position	CTRL_OUTx Pin Name	AD9363 Pin Designation
7	CTRL_OUT7	G4
6	CTRL_OUT6	F4
5	CTRL_OUT5	F5
4	CTRL_OUT4	F6
3	CTRL_OUT3	E6
2	CTRL_OUT2	E5
1	CTRL_OUT1	E4
0	CTRL_OUT0	D4

The AD9361_CTRL_OUTS_SETUP function configures the control outputs.

SPI Register 0x035—Control Output Pointer

This register sets the pointer to a table of control output signals. See the AD9363 Reference Manual for mapping of control output signals to pointer value and control output ball.

SPI Register 0x036—Control Output Enable

The bits in this register enable and disable the control output outputs. See Table 20 for the control output bit and control output ball mapping.

PRODUCT ID REGISTER (ADDRESS 0x037)

Table 21. Product ID Register Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x037	Product ID	Open				Always 1	Revision[2:0]				R

REFERENCE CLOCK CYCLES REGISTER (ADDRESS 0x03A)

Table 22. Reference Clock Cycles Register Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x03A	Reference clock cycles	Open	Reference clock cycles per µs[6:0]							0x00	R/W

SPI Register 0x037—Product ID

Bits[D2:D0] represent the revision of the device.

SPI Register 0x03A—Reference Clock Cycles

The AD9361_SET_REF_CLK_CYCLES function configures this register. Many delay settings assume a resolution of 1 LSB/µs. For this assumption to be correct, Register 0x03A must be programmed with the number of reference clock cycles per µs minus 1. The reference clock is an external reference.

DIGITAL I/O CONTROL REGISTERS (ADDRESS 0x03B THROUGH ADDRESS 0x03E)

Table 23. Digital I/O Control Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x03B	Digital I/O control	CLK_OUT drive	DATA_CLK_x drive	DATA_CLK_x slew[1:0]		Must be 0	Data port drive	Data port slew[1:0]		0x00	R/W
0x03C	LVDS bias control	CLK_OUT slew[1:0]		Rx on-chip term-ination	Bypass bias resistor	LVDS Tx LO VCM	LVDS bias[2:0]			0x03	R/W
0x03D	LVDS Invert Control 1	LVDS positive/negative invert[7:0]								0x00	R/W
0x03E	LVDS Invert Control 2	LVDS positive/negative invert[15:8]								0x00	R/W

Table 24. LVDS Signal Inversion Mapping

Register and Bits	Affected Signals	Chip Default Bit Value	Configuration for Chip Default	Recommended Configuration
SPI Register 0x03D				
Bit D7	P0_D3 and P0_D2	0	Inverted	1
Bit D6	P0_D1 and P0_D0	0	Inverted	1
Bit D5	P1_D11 and P1_D10	0	Inverted	1
Bit D4	P1_D9 and P1_D8	0	Inverted	1
Bit D3	P1_D7 and P1_D6	0	Inverted	1
Bit D2	P1_D5 and P1_D4	0	Inverted	1
Bit D1	P1_D3 and P1_D2	0	Inverted	1
Bit D0	P1_D2 to P1_D0	0	Inverted	1
SPI Register 0x03E				
Bit D7	FB_CLK_x	0	Not inverted	0
Bit D6	TX_FRAME_x	0	Not inverted	0
Bit D5	DATA_CLK_x	0	Not inverted	0
Bit D4	RX_FRAME_x	0	Not inverted	0
Bit D3	P0_D11 and P0_D10	0	Inverted	1
Bit D2	P0_D9 and P0_D8	0	Inverted	1
Bit D1	P0_D7 and P0_D6	0	Inverted	1
Bit D0	P0_D5 and P0_D4	0	Inverted	1

SPI Register 0x03B—Digital I/O Control

Bit D7—CLK_OUT Drive

This bit sets the CLK_OUT drive strength. Setting this bit increases the drive strength by approximately 20%.

Bit D6—DATA_CLK_x Drive

This bit sets the DATA_CLK drive strength. Setting this bit increases the drive strength by approximately 20%.

Bits[D5:D4]—DATA_CLK_x Slew[1:0]

These bits set the slew control for DATA_CLK_x. Set these bits to 1'b00 for the fastest rise and fall times; set these bits to 1'b11 for the slowest rise and fall times.

Bit D3—Must be 0

Bit D2—Data Port Drive

This bit sets the data port output driver strength. Setting this bit increases the drive strength by approximately 20%.

Bits[D1:D0]—Data Port Slew[1:0]

These bits set the slew control for the data ports. Set these bits to 1'b00 for the fastest rise and fall times; set these bits to 'b11 for the slowest rise and fall times.

SPI Register 0x03C—LVDS Bias Control

Bits[D7:D6]—CLK_OUT Slew[1:0]

These bits set the slew control for CLK_OUT. Set these bits to 1'b00 for the fastest rise and fall times; set these bits to 1'b11 for the slowest rise and fall times.

Bit D5—Rx On-Chip Termination

Use LVDS Rx100 on-chip termination for all datapath bits, TX_FRAME_x, and FB_CLK_x. Do not set this bit in CMOS mode.

Bit D4—Bypass Bias Resistor

This bit bypasses the bias resistor in the LVDS Rx comparator.

Bit D3—LVDS Tx LO VCM

This bit lowers the output common-mode voltage by 60 mV.

Bits[D2:D0]—LVDS Bias[2:0]

These bits control the LVDS driver amplitude. $|V_{OD}|$ = 75 mV to 450 mV; 75 mV/LSB.

SPI Register 0x03D and SPI Register 0x03E—LVDS Invert Control

The phase of any LVDS pair can be inverted from its default configuration by setting bits in these two registers (see Table 24). The default configuration for the data bits is inverted. Set Register 0x03D = 0xFF and Register 0x03E = 0x0F to prevent data inversion. Clock and frame signals are not inverted in the default case.

BASEBAND (BB) PLL CONTROL REGISTERS (ADDRESS 0x03F THROUGH ADDRESS 0x04E)

Table 25. BB PLL Control Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x03F	BB PLL Control 1	Must be 0				BB PLL SDM Enable B	Start BB VCO calibration	BB PLL SDM bypass	BB PLL reset bar	0x01	R/W
0x040	Must be 0	Must be 0								0x00	R/W
0x041	Fractional BB Frequency Word 1	Set to 0			Fractional BB frequency word[20:16]					0x00	R/W
0x042	Fractional BB Frequency Word 2	Fractional BB frequency word[15:8]								0x00	R/W
0x043	Fractional BB Frequency Word 3	Fractional BB frequency word[7:0]								0x00	R/W
0x044	Integer BB frequency word	Integer BB frequency word[7:0]								0x10	R/W
0x045	Reference clock scaler	Must be 0						Reference clock scaler[1:0]		0x00	R/W
0x046	Charge pump current	Must be 0		Charge pump current[5:0]						0x09	R/W
0x047	Must be 0	Must be 0								0x00	R/W
0x048	Loop Filter 1	C1 word[2:0]			R1 word[4:0]					0xC5	R/W
0x049	Loop Filter 2	R2 word[0]	C2 word[4:0]					C1 word[4:3]		0xB8	R/W
0x04A	Loop Filter 3	Bypass C3	Bypass R2	C3 word[3:0]				R2 word[2:1]		0x2E	R/W
0x04B	VCO control	Frequency calibration enable	Set to 2'b11		Must be 0	Force VCO band enable	Forced VCO band word[2:0]			0xC0	R/W
0x04C	Must be 0x86	Set to 0x86								0x00	R/W
0x04D	BB PLL Control 2	Must be 0					See description			0x00	R/W
0x04E	BB PLL Control 3	Must be 0			Set to 1	Must be 0				0x00	R/W

The BBPLL registers are completely configured by the AD9361_BBPLL_SET_RATE function. The AD9363 Reference Manual has more information about individual functions of the BB PLL.

SPI Register 0x03F—BB PLL Control 1

Bits[D7:D4]—Must be 0

Bit D3—BB PLL SDM Enable B

This is a test mode bit and is normally clear. Clearing this bit turns on the clock to the BB PLL Σ-Δ modulator (SDM). Set this bit to disable the SDM. Use this bit in conjunction with the BB PLL SDM bypass bit (Bit D1).

Bit D2—Start BB VCO Calibration

Set this bit after writing the BB PLL words to calibrate the VCO. Bit D7 of Register 0x04B must be set to enable the calibration. Clear the start BB VCO calibration bit after setting it (it is not self clearing). The set and clear instructions can be consecutive without waiting for the calibration to complete.

Bit D1—BB PLL SDM Bypass

This is a test mode bit and is normally clear. Setting this bit disconnects the SDM from the BB PLL, making it an integer PLL. Use this bit with the BB PLL SDM Enable B bit (Bit D3).

Bit D0—BB PLL Reset Bar

When this bit is clear, the BB PLL is disabled. Setting this bit enables the BB PLL. Set this bit after writing the BB PLL words.

$$BB\ PLL\ Integer\ Word = \text{floor}\left(\frac{BB\ PLL\ Frequency\ (\text{MHz})}{Reference\ Clock\ Frequency}\right) \quad (8)$$

$$BB\ PLL\ Fractional\ Word = \text{floor}\left(\left(\frac{BB\ PLL\ Frequency\ (\text{MHz})}{Reference\ Clock\ Frequency}\right) - \text{floor}\left(\frac{BB\ PLL\ Frequency\ (\text{MHz})}{Reference\ Clock\ Frequency}\right)\right) \times 2{,}088{,}960 \quad (9)$$

$$f_{OUT} = f_{REF} \times \left[N_{INTEGER} + \frac{N_{FRACTIONAL}}{2{,}088{,}960}\right] \quad (10)$$

where:
$N_{INTEGER}$ is the BB PLL integer word (decimal).
$N_{FRACTIONAL}$ is the BB PLL fractional word (decimal).

SPI Register 0x040—Must be 0

SPI Register 0x041, Bits[D7:D5]—Set to 0

SPI Register 0x041, Bits[D4:D0] Through SPI Register 0x044—Fractional and Integer BB Frequency Words

See Equation 8, Equation 9, and Equation 10.

SPI Register 0x045—Reference Clock Scaler

Bits[D7:D2]—Must be 0

Bits[D1:D0]—Reference Clock Scaler[1:0]

The reference clock frequency is scaled before it enters the BB PLL (00 = x1, 01 = x½, 10 = x¼, and 11 = x2).

SPI Register 0x046—Charge Pump Current

Bits[D7:D6]—Must be 0

Bits[D5:D0]—Charge Pump Current[5:0]

These bits control the charge pump bleed current setting. The resolution is 25 µA, offset is 25 µA, and the range is 25 µA to 1575 µA.

SPI Register 0x047—Must be 0.

Bit D7—Must be 0

Bits[D6:D0]—Must be 0

SPI Register 0x048 through SPI Register 0x04A—Loop Filter

These registers are set by the AD9361_BBPLL_SET_RATE function. The AD9363 Reference Manual has more information about the loop filter.

SPI Register 0x04B—VCO Control

Bit D7—Frequency Calibration Enable

Set this bit to enable VCO calibration. See the Bit D2—Start BB VCO Calibration section in the SPI Register 0x03F—BB PLL Control 1 section.

Bits[D6:D5]—Set to 2'b11

Bit D4—Must be 0

Bit D3—Force VCO Band Enable

See Bits[D2:D0].

Bits[D2:D0]—Forced VCO Band Word[2:0]

When a BB PLL VCO calibration completes, the VCO is in one of five bands, coded in this register as 0 through 4. Setting Bit D3 forces the band word to the value written in Bits[D2:D0].

SPI Register 0x04C—Set to 0x86

SPI Register 0x04D—BB PLL Control 2

Bits[D6:D3]—Must be 0

Bits[D2:D0]—See Description

These are internal BB PLL bits. After setting Register 0x04C to Register 0x086, set Register 0x04D to 0x01 and then to 0x05.

SPI Register 0x04E—BB PLL Control 3

Bits[D7:D5]—Must be 0

Bit D4—Set to 1

Bits[D3:D0]—Must be 0

POWER-DOWN OVERRIDE REGISTERS (ADDRESS 0x050 THROUGH ADDRESS 0x058)

Table 26. Power-Down Override Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x050	Rx synthesizer power-down override	Open			Rx LO power-down	Rx synthesizer VCO ALC power-down	Rx synthesizer PTAT power-down	Rx synthesizer VCO power-down	Rx synthesizer VCO LDO power-down	0x00	R/W
0x051	Tx synthesizer power-down override	Open			Tx LO power-down	Tx synthesizer VCO ALC power-down	Tx synthesizer PTAT power-down	Tx synthesizer VCO power-down	Tx synthesizer VCO LDO power-down	0x00	R/W
0x052	Control 0	Must be 0						Must be 2'b11		0x03	R/W
0x053	Must be 0	Must be 0								0x00	R/W
0x054	Rx1 ADC power-down override	Rx1 ADC power-down[7:0]								0x00	R/W
0x055	Rx2 ADC power-down override	Rx2 ADC power-down[7:0]								0x00	R/W
0x056	Tx Analog Power-Down Override 1	Tx secondary filter power-down[1:0]		Tx BB filter power-down[1:0]		Tx DAC power-down[1:0]		Tx DAC bias power-down[1:0]		0x00	R/W
0x057	Analog power-down override	Open		Rx external VCO buffer power-down	Tx external VCO buffer power-down	Tx monitor power-down[1:0]		Tx upconverter power-down[1:0]		0x3C	R/W
0x058	Miscel-laneous power-down override	Open	Rx LNA power-down	Open		Rx calibration power-down[1:0]		Must be 1	Master bias power-down	0x30	R/W

SPI Register 0x050—Rx Synthesizer Power-Down Override

Bit D4—Rx LO Power-Down

This state machine enables and disables the Rx synthesizer. Therefore, if Bit D4 is set, the Rx LO dividers power up and power down when the Rx synthesizer powers up and powers down. The Rx LO dividers are always powered down for external VCO operation.

Bit D3—Rx Synthesizer VCO ALC Power-Down

Setting this bit powers down the Rx synthesizer VCO automatic level control (ALC).

Bit D2—Rx Synthesizer PTAT Power-Down

Proportional to absolute temperature (PTAT) is a temperature compensated current used for the Rx synthesizer. This bit is OR'ed with the inverse of Register 0x242, Bits[D4:D3]. To turn off PTAT, set Register 0x050, Bit D2 and clear Register 0x242, Bits[D4:D3]. The synthesizer can still operate, but is not temperature compensated.

Bit D1—Rx Synthesizer VCO Power-Down

Setting this bit powers down the Rx synthesizer VCO.

Bit D0—Rx Synthesizer VCO LDO Power-Down

Setting this bit powers down the Rx synthesizer VCO LDO.

SPI Register 0x051—Tx Synthesizer Power-Down Override

This register is the same as Register 0x050, but controls the transmitter LO circuits.

SPI Register 0x052—Control 0

Bits[D7:D2]—Must be 0

Bits[D1:D0]—Must be 2'b11

SPI Register 0x053—Must be 0

SPI Register 0x054 and SPI Register 0x055—Rx1 and Rx2 ADC Power-Down Override

These registers control the receive ADCs. Only 0x00 (ADC on) and 0xFF (ADC off) are valid settings.

SPI Register 0x056—Tx Analog Power-Down Override 1

Bits[D7:D6]—Tx Secondary Filter Power-Down[1:0]

Setting these bits powers down the Tx secondary filter. Bit D6 applies to Tx1 and Bit D7 applies to Tx2.

Bits[D5:D4]—Tx BB Filter Power-Down[1:0]

Setting these bits powers down the Tx baseband (BB) low-pass filters. Bit D4 applies to Tx1 and Bit D5 applies to Tx2.

Bits[D3:D2]—Tx DAC Power-Down[1:0]

Setting these bits powers down the Tx DACs. Bit D2 applies to Tx1 and Bit D3 applies to Tx2.

Bits[D1:D0]—Tx DAC Bias Power-Down[1:0]

Setting these bits powers down the Tx DAC bias supplies. Bit D0 applies to Tx1 and Bit D1 applies to Tx2.

SPI Register 0x057—Analog Power-Down Override

Bit D5—Rx External VCO Buffer Power-Down

Clear this bit to use an external VCO.

Bit D4—Tx External VCO Buffer Power-Down

This bit functions the same as Bit D5, but applies to the Tx VCO.

Bits[D3:D2]—Tx Monitor Power-Down[1:0]

Setting these bits powers down the Tx monitor LO circuitry. Bit D2 applies to Tx Monitor 1 and Bit D3 applies to Tx Monitor 2. These bits are set by default. When the Tx monitor function is used (see Register 0x001 and Register 0x06E), clear these bits enable the LO circuitry.

Bits[D1:D0]—Tx Upconverter Power-Down[1:0]

Setting these bits powers down the Tx upconverters. Bit D0 applies to Tx1 and Bit D1 applies to Tx2.

SPI Register 0x058—Miscellaneous Power-Down Override

Bit 7—Open

This bit is not used.

Bit D6—Rx LNA Power-Down

Setting this bit powers down the Rx LNAs.

Bits[D3:D2]—Rx Calibration Power Down[1:0]

Setting these bits powers down the Rx calibration blocks. Bit D3 applies to Rx1 and Bit D4 applies to Rx2.

Bit D1—Set to 1

Set this bit to 1.

Bit D0—Master Bias Power-Down

Setting this bit powers down all analog biases. Only the leakage current flows.

OVERFLOW REGISTERS (ADDRESS 0x05E THROUGH ADDRESS 0x05F)

Table 27. Overflow Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x05E	Channel 1 overflow	BB PLL lock	Channel 1 INT3	Channel 1 HB3	Channel 1 HB2	Channel 1 QEC	Channel 1 HB1	Channel 1 TFIR	Channel 1 RFIR		R
0x05F	Channel 2 overflow	Open	Channel 2 INT3	Channel 2 HB3	Channel 2 HB2	Channel 2 QEC	Channel 2 HB1	Channel 2 TFIR	Channel 2 RFIR		R

None of the overflow bits self clear. During initialization, some of these overflow bits may show overflow conditions. To read the current status of the bits, perform two consecutive SPI reads.

SPI Register 0x05E—Channel 1 Overflow

Bit D7—BB PLL Lock

If this bit is set, the BB PLL is locked.

Bit D6—Channel 1 INT3

If this bit is set, a digital overflow occurs in the Tx1 interpolate by 3 filter (INT3).

Bit D5—Channel 1 HB3

If this bit is set, a digital overflow occurs in the Tx1 Half-Band 3 filter (HB3).

Bit D4—Channel 1 HB2

If this bit is set, a digital overflow occurs in the Tx1 Half-Band 2 (HB2) filter.

Bit D3—Channel 1 QEC

If this bit is set, a digital overflow occurs in the Tx1 quadrature error correction (QEC) filter.

Bit D2—Channel 1 HB1

If this bit is set, a digital overflow occurs in the Tx1 Half-Band 1 filter (HB1).

Bit D1—Channel 1 TFIR

If this bit is set, a digital overflow occurs in the Tx1 FIR filter (TFIR).

Bit D0—Channel 1 RFIR

If this bit is set, a digital overflow occurs in the Rx1 FIR filter (RFIR).

SPI Register 0x05F—Channel 2 Overflow

This register is the same as Register 0x05E, but applies to Channel 2.

TRANSMITTER (Tx) CONFIGURATION REGISTERS

Tx PROGRAMMABLE FIR FILTER REGISTERS (ADDRESS 0x060 THROUGH ADDRESS 0x065)

Table 28. Tx Programmable FIR Filter Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x060	Tx filter coefficient address	Tx filter coefficient address[7:0]									R/W
0x061	Tx Filter Coefficient Write Data 1	Tx filter coefficient write data[7:0]									R/W
0x062	Tx Filter Coefficient Write Data 2	Tx filter coefficient write data[15:8]									R/W
0x063	Tx Filter Coefficient Read Data 1	Tx filter coefficient read data[7:0]									R
0x064	Tx Filter Coefficient Read Data 2	Tx filter coefficient read data[15:8]									R
0x065	Tx filter configuration	Number of taps[2:0]			Select Tx channel[1:0]		Write Tx	Start Tx clock	Filter gain	0x00	R/W

The AD9361_SET_TX_FIR_CONFIG function sets up the Tx FIR coefficients. See the AD9363 Reference Manual for more information.

SPI Register 0x060—Tx Filter Coefficient Address

The digital filter coefficients are indirectly addressable. The word in this register is the address of the coefficient.

SPI Register 0x061 and SPI Register 0x062—Tx Filter Coefficient Write Data 1 and Tx Filter Coefficient Write Data 2

Write the coefficient value to these registers. Write these registers (along with Register 0x060) before setting Register 0x065, Bit D2. Coefficients are 16-bit words in twos complement format. The least significant bit is bit 0.

SPI Register 0x063 and SPI Register0x064—Tx Filter Coefficient Read Data 1 and Tx Filter Coefficient Read Data 2

To read coefficients, write the address in Register 0x060 and then read Register 0x063 and Register 0x064. Coefficients are 16-bit words in twos complement format. The least significant bit is bit 0.

SPI Register 0x065—Tx Filter Configuration

Bits[D7:D5]—Number of Taps[2:0]

The number of taps (see Equation 11) must be correct.

$$Number\ of\ Taps = 16 \times (Number\ of\ Taps + 1) \quad (11)$$

Bits[D4:D3]—Select Tx Channel[1:0]

When writing coefficients, Bit D3 causes a write to Tx1, Bit D4 causes a write to Tx2, and both bits set writes to both Tx filters. When reading coefficients, setting both bits is invalid.

Bit D2—Write Tx

Set this self clearing bit to write a coefficient. Each write operation must set this bit. After the table is programmed, write to Register 0x065 with the write Tx bit cleared and Bit D0 high. Then, write to Register 0x065 again with Bit D0 clear, thus ensuring that the write bit resets internally before the clock stops. Wait four Tx sample periods after setting Bit D2 high while the data writes into the table.

Bit D1—Start Tx Clock

Set this bit to start the programming clock when writing coefficients.

Bit D0—Filter Gain

Setting this bit attenuates the digital samples by 6 dB.

Tx MONITOR REGISTERS (ADDRESS 0x067 THROUGH ADDRESS 0x071)

Table 29. Tx Monitor Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x067	Tx monitor low gain	Open		Tx monitor track	Tx monitor low gain[4:0]					0x13	R/W
0x068	Tx monitor high gain	Open			Tx monitor high gain[4:0]					0x18	R/W
0x069	Tx monitor delay counter	Tx monitor delay counter[7:0]								0x00	R/W
0x06A	Tx level threshold	Tx level threshold[5:0]						Tx monitor delay counter[9:8]		0x00	R/W
0x06B	Tx RSSI 1	Tx RSSI 1[8:1]									R
0x06C	Tx RSSI 2	Tx RSSI 2[8:1]									R
0x06D	Tx RSSI LSB	Open						Tx RSSI 2[1]	Tx RSSI 1[0]		R
0x06E	TPM mode enable	Tx Monitor 2 enable	One shot mode	Tx Monitor 1 enable	Open	Tx monitor duration[3:0]				0xA9	R/W
0x06F	Temperature gain coefficient	Temperature gain coefficient for Tx monitor[7:0]								0x00	R/W
0x070	Tx Monitor 1 configuration	Must be 6'b110000						Tx Monitor 1 TIA gain[1:0]		0xc1	R/W
0x071	Tx Monitor 2 configuration	Must be 6'b110000						Tx Monitor 2 TIA gain[1:0]		0xc1	R/W

SPI Register 0x067—Tx Monitor Low Gain

Bit D5—Tx Monitor Track

Setting this bit enables dc offset tracking for the Tx monitor.

Bits[D4:D0]—Tx Monitor Low Gain[4:0]

This value sets the Rx LPF gain index when the Tx attenuation value in Register 0x073 and Register 0x074 is less than or equal to the threshold value in Register 0x078.

SPI Register 0x068—Tx Monitor High Gain

This value sets the Rx LPF gain index when the Tx attenuation value in Register 0x073 and Register 0x074 is greater than the threshold value in Register 0x078.

SPI Register 0x069 and SPI Register 0x06A, Bits[D1:D0]—Tx Monitor Delay Counter

After the ENSM enters the Tx state and if the level threshold in Register 0x06A, Bits[D7:D2] = 0, the Tx monitor delay counter starts. If Register 0x06A, Bits[D7:D2] is nonzero, the AD9363 compares 6 MSBs of the I and Q samples with Register 0x06A, Bits[D7:D2]. If Register 0x06A, Bits[D7:D2] are exceeded, the Tx monitor delay counter starts. After it expires, the AD9363 measures the Tx received signal strength indicator (RSSI). The resolution is 64 × ADC clocks/LSB.

SPI Register 0x06A—Tx Level Threshold

Bits[D7:D2]—Tx Level Threshold[5:0]

See Register 0x069.

SPI Register 0x06B Through SPI Register 0x06D—Tx RSSI x

These registers set the Tx RSSI words. The resolution is 0.25 dB/LSB, and the unit is negative dB.

SPI Register 0x06E—TPM Mode Enable

Bit D7—Tx Monitor 2 Enable

This bit enables the TX_MON2 function. When this bit is set, the signal at the TX_MON2 pin is passed to the Tx power monitoring (TPM) block when the ENSM moves to the Tx state. When the ENSM moves to the Rx state, the Rx path operates normally. When this bit is clear, the Tx Monitor 2 function is disabled. See Register 0x001 and Register 0x057.

Bit D6—One Shot Mode

If this bit is set, the AD9363 performs one Tx RSSI measurement when the ENSM enters the Tx state. If the bit is clear, the AD9363 continuously measures Tx RSSI until the ENSM exits the Tx state.

Bit D5—Tx Monitor 1 Enable

This bit is the same as Bit D7, but for the TX_MON1 pin.

Bits[D3:D0]—Tx Monitor Duration[3:0]

This register specifies the duration of the Tx RSSI measurement per Equation 12.

$$Duration\ (\text{Tx Sample Cycles}) = 16 \times 2^{Tx\ Monitor\ Duration[3:0]} \quad (12)$$

SPI Register 0x06F—Temperature Gain Coefficient for Tx Monitor[7:0]

If very high accuracy is required, during system characterization, the ratio of gain difference per °Cis determined and then coded in twos complement notation. The resolution is 0.0078 dB/°C/LSB.

SPI Register 0x070 and SPI Register 0x071—Tx Monitor 1 Configuration and Tx Monitor 2 Configuration

Bits[D7:D2]—Must be 6'b110000

Bits[D1:D0]—Tx Monitor x TIA Gain[1:0]

These bits control the Tx monitor front-end gain, per Table 30.

Table 30. Tx Monitor Gain

Tx Monitor Gain[1:0]	Tx Monitor Gain
00	Open
01	0 dB
10	6 dB
11	9.5 dB

Tx POWER CONTROL AND ATTENUATION REGISTERS (ADDRESS 0x073 THROUGH ADDRESS 0x07C)

Table 31. Tx Power Control and Attenuation Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x073	Tx1 Attenuation 0	Tx1 attenuation[7:0]								0x00	R/W
0x074	Tx1 Attenuation 1	Open							Tx1 attenuation[8]	0x00	R/W
0x075	Tx2 Attenuation 0	Tx2 attenuation[7:0]								0x00	R/W
0x076	Tx2 Attenuation 1	Open							Tx2 attenuation[8]	0x00	R/W
0x077	Tx Attenuation offset	Open	Mask cleat attenuation update	Tx attenuation offset[5:0]						0x40	R/W
0x078	Tx Attenuation threshold	Tx attenuation threshold[7:0]								0x3c	R/W
0x079	Select Tx1/Tx2	Open	Select Tx1 and Tx2	Must be 0	Open					0x00	R/W
0x07A	Open	Open								0x00	R/W
0x07B	Open	Open								0x00	R/W
0x07C	Immediate update	Open	Immediately update TPC attenuation	Must be 0	Open					0x00	R/W

The AD9361_SET_TX_ATTENUATION function configures attenuation.

SPI Register 0x073 and SPI Register 0x074—Tx1 Attenuation[8:0]

This 9-bit word sets the Tx path attenuation. Zero = 0 attenuation. The resolution is 0.25 dB/LSB, and the range is 0 to 359 (decimal).

SPI Register 0x075 and SPI Register 0x076—Tx2 Attenuation[8:0]

The Tx2 attenuation functions the same as Register 0x073 and Register 0x074, but for Tx2.

SPI Register 0x077—Tx Attenuation Offset

Bit D6—Mask Clear Attenuation Update

When this bit is clear, the immediately update Tx transmit power control (TPC) attenuation bit in Register 0x07C, Bit D6 self clears. When this bit is set, the, the immediately update TPC attenuation bit does not self clear.

Bits[D5:D0]—Tx Attenuation Offset[5:0]

This unsigned value adds to the words in Register 0x073 through Register 0x076, resulting in new attenuation words. The resolution is 0.25 dB/LSB.

SPI Register 0x078—Tx Attenuation Threshold

Refer to Register 0x067, Bits[4:0] and Register 0x068. The resolution is 0.25 dB/LSB.

SPI Register 0x079—Select Tx1/Tx2

Bit D6—Select Tx1 and Tx2

Use the Tx1 attenuation value for both Tx1 and Tx2.

Bit D5—Must be 0

SPI Register 0x07C—Immediate Update

Bit D6—Immediately Update TPC Attenuation

See Register 0x077, Bit D6.

Bit D5—Must be 0

Tx QUADRATURE CALIBRATION PHASE, GAIN, AND OFFSET CORRECTION REGISTERS (ADDRESS 0x08E THROUGH ADDRESS 0x09F)

Table 32. Tx Quadrature Calibration Phase, Gain, and Offset Correction Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x08E	Tx1 Output 1 phase correction	Tx1 Output 1 phase correction[7:0]									R/W
0x08F	Tx1 Output 1 gain correction	Tx1 Output 1 gain correction[7:0]									R/W
0x090	Tx2 Output 1 phase correction	Tx2 Output 1 phase correction[7:0]									R/W
0x091	Tx2 Output 1 gain correction	Tx2 Output 1 gain correction[7:0]									R/W
0x092	Tx1 Output 1 Offset I	Tx1 Output 1 Offset I[7:0]									R/W
0x093	Tx1 Output 1 Offset Q	Tx1 Output 1 Offset Q[7:0]									R/W
0x094	Tx2 Output 1 Offset I	Tx2 Output 1 Offset I[7:0]									R/W
0x095	Tx2 Output 1 Offset Q	Tx2 Output 1 Offset Q[7:0]									R/W
0x096	Tx1 Output 2 phase correction	Tx1 Output 2 phase correction[7:0]									R/W
0x097	Tx1 Output 2 gain correction	Tx1 Output 2 gain correction[7:0]									R/W
0x098	Tx2 Output 2 phase correction	Tx2 Output 2 phase correction[7:0]									R/W
0x099	Tx2 Output 2 gain correction	Tx2 Output 2 gain correction[7:0]									R/W
0x09A	Tx1 Output 2 Offset I	Tx1 Output 2 Offset I[7:0]									R/W
0x09B	Tx1 Output 2 Offset Q	Tx1 Output 2 Offset Q[7:0]									R/W
0x09C	Tx2 Output 2 Offset I	Tx2 Output 2 Offset I[7:0]									R/W
0x09D	Tx2 Output 2 Offset Q	Tx2 Output 2 Offset Q[7:0]									R/W
0x09E	Open	Open									
0x09F	Force bits	Force Output 2 Tx2 offset	Force Output 2 Tx1 offset	Force Output 2 Tx2 phase and gain	Force Output 2 Tx1 phase and gain	Force Output 1 Tx2 offset	Force Output 1 Tx1 offset	Force Output 1 Tx2 phase and gain	Force Output 1 Tx1 phase and gain	0x00	R/W

SPI Register 0x08E—Tx1 Output 1 Phase Correction

If Register 0x09F, Bit D0 is clear, after a Tx quadrature calibration completes, this register holds the phase correction word for Tx1A. If Register 0x09F, Bit D0 is set, the value written to this register is used as the phase correction word.

SPI Register 0x08F—Tx1 Output 1 Gain Correction

If Register 0x09F, Bit D0 is clear, after a Tx quadrature calibration completes, this register holds the gain correction word for Tx1A. If Register 0x09F, Bit D0 is set, the value written to this register is used as the gain correction word.

SPI Register 0x090—Tx2 Output 1 Phase Correction

This register functions the same as Register 0x08E, but applies to Tx2 and the force bit is Bit D1 in Register 0x09F.

SPI Register 0x091—Tx2 Output 1 Gain Correction

This register functions the same as Register 0x08F, but applies to Tx2 and the force bit is Bit D1 in Register 0x09F.

SPI Register 0x092—Tx1 Output 1 Offset I

If Register 0x09F, Bit D2 is clear after a Tx quadrature calibration completes, this register holds the LO leakage correction word for the I signal path of Tx1A. If Register 0x09F, Bit D2 is set, the value written to this register is used as the LO leakage correction word.

SPI Register 0x093—Tx1 Output 1 Offset Q

This register functions the same as Register 0x092, but applies to the Q signal path.

SPI Register 0x094—Tx2 Output 1 Offset

This register functions the same as Register 0x092, but applies to Tx2 and the force bit is Bit D3 in Register 0x09F.

SPI Register 0x095—Tx2 Output 1 Offset Q

This register functions the same as Register 0x092, but applies to the Q signal path of Tx2 and the force bit is Bit D3 in Register 0x09F.

SPI Register 0x096—Tx1 Output 2 Phase Correction

This register functions the same as Register 0x08E, but applies to Tx1B and the force bit is Bit D4 in Register 0x09F.

SPI Register 0x097—Tx1 Output 2 Gain Correction

This register functions the same as Register 0x08F, but applies to Tx1B and the force bit is Bit D4 in Register 0x09F.

SPI Register 0x098—Tx2 Output 2 Phase Correction

This register functions the same as Register 0x08E, but applies to Tx2B of Tx2 and the force bit is Bit D5 in Register 0x09F.

SPI Register 0x099—Tx2 Output 2 Gain Correction

This register functions the same as Register 0x08F, but applies to Tx2B of Tx2 and the force bit is Bit D5 in Register 0x09F.

SPI Register 0x9A—Tx1 Output 2 Offset I

This register functions the same as Register 0x092, but applies to Tx1B and the force bit is Bit D6 in Register 0x09F.

SPI Register 0x09B—Tx1 Output 2 Offset Q

This register functions the same as Register 0x092, but applies to the Tx1B Q signal path and the force bit is Bit D6 in Register 0x09F.

SPI Register 0x09C—Tx2 Output 2 Offset I

This register functions the same as Register 0x092, but applies to Tx2B of Tx2 and the force bit is Bit D7 in Register 0x09F.

SPI Register 0x09D—Tx2 Output 2 Offset Q

This register functions the same as Register 0x092, but applies to the Q signal path of Tx2B of Tx2 and the force bit is Bit D7 in Register 0x09F.

SPI Register 0x09F—Force Bits

These bits force the values in Register 0x08E through Register 0x09D to be the Tx quadrature calibration correction words.

Tx QUADRATURE CALIBRATION CONFIGURATION REGISTERS (ADDRESS 0x0A0 THROUGH ADDRESS 0x0AE)

Table 33. Tx Quadrature Calibration Configuration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x0A0	Quadrature calibration NCO frequency and phase offset	Open	Rx NCO frequency[1:0]		Rx NCO phase offset[4:0]					0x0C	R/W
0x0A1	Quadrature calibration control	Free run enable	Set to 1	DC offset enable	Gain enable	Phase enable	Must be 0	Set to 2'b11		0x78	R/W
0x0A2	Set to 0x7F	Set to 0x7F								0x1F	R/W
0x0A3	Tx NCO frequency	Tx NCO frequency[1:0]		Must be 0						0x00	R/W
0x0A4	Set to 0xF0	Set to 0xF0								0x10	R/W
0x0A5	Magnitude of f_{TEST} threshold	Magnitude of f_{TEST} threshold[7:0]								0x06	R/W
0x0A6	Magnitude of f_{TEST} Threshold 2	Magnitude of f_{TEST} Threshold 2[7:0]								0x06	R/W
0x0A7	Quadrature calibration status, Tx1	Tx1 convergence count[5:0]						Tx1 LO conver-gence	Tx1 SSB conver-gence		R
0x0A8	Quadrature calibration status, Tx2	Tx2 convergence count[5:0]						Tx2 LO conver-gence	Tx2 SSB conver-gence		R
0x0A9	Set to 0xFF	Set to 0xFF								0x20	R/W
0x0AA	Tx quadrature full/LMT gain	Open	Rx full table/LMT table gain[6:0]							0x0A	R/W
0x0AB	Must be 0	Must be 0								0x00	R/W
0x0AC	Must be 0	Must be 0								0x00	R/W
0x0AD	Must be 0	Must be 0								0x00	R/W
0x0AE	Tx quadrature LPF gain	Open			Rx LPF gain[4:0]					0x18	R/W

The AD9361_TX_QUAD_CALIB function configures these registers, but the numerically controlled oscillator (NCO) phase offset value in Register 0x0A0 must be determined empirically for many combinations of sampling rates and digital filter configurations. Analog Devices Engineer Zone describes in detail how to configure the registers for a successful Tx quadrature calibration.

SPI Register 0x0A0—Quadrature Calibration NCO Frequency and Phase Offset

Bits[D6:D5]—Rx NCO Frequency[1:0]

This value sets the test frequency, per Equation 13, for the Rx path that processes the Tx test tone. Set the Rx NCO frequency equal to the Tx NCO frequency (see Register 0x0A3, Bits[D7:D6]).

$$Rx\ NCO\ Test\ Frequency = \frac{CLKRF \times (Rx\ NCO\ Frequency[1:0] + 1)}{32} \quad (13)$$

where *CLKRF* is the clock at the input to the Rx FIR filter.

Bits[D4:D0]—Rx NCO Phase Offset[4:0]

These bits compensate for the delay of the test signal through the signal path. These bits must be correct and are affected by the digital filter settings.

SPI Register 0x0A1—Quadrature Calibration Control

Bit D7—Free Run Enable

This bit is normally clear. When this bit is clear, the Tx quadrature calibration runs until the errors are below the thresholds in Register 0x0A5 and Register 0x0A6, up to a maximum time set by the quadrature calibration count (Register 0x0A9). This mode forces the algorithm to finish. If the bit is set, the algorithm does not finish until (or if) it meets the thresholds.

Bit D6—Set to 1

Bit D5—DC Offset Enable

This bit is normally set. When this bit is set, a Tx quadrature calibration performs a dc offset correction. Clearing the bit disables this correction.

Bit D4—Gain Enable

This bit is normally set. When this bit is set, a Tx quadrature calibration performs a gain offset correction. Clearing this bit disables this correction.

Bit D3—Phase Enable

This bit is normally set. When this bit is set, a Tx quadrature calibration performs a phase offset correction. Clearing this bit disables this correction.

Bit D2—Must be 0

Bits[D1:D0]—Set to 2'b11

SPI Register 0x0A2—Set to 0x7F

SPI Register 0x0A3—Tx NCO Frequency

Bits[D7:D6]—Tx NCO Frequency[1:0]

These bits set the test waveform frequency per Equation 14.

$$Tx\ NCO\ Test\ Frequency = \frac{CLKTF \times (Tx\ NCO\ Frequency[1:0] + 1)}{32} \quad (14)$$

where *CLKTF* is the clock at the output of the Tx FIR filter.

Bits[D5:D0]—Must be 0

SPI Register 0x0A4—Set to 0xF0

SPI Register 0x0A5 and SPI Register 0x0A6—Magnitude of f_{TEST} Threshold and Magnitude of f_{TEST} Threshold 2

These registers are thresholds for LO leakage and quadrature correction. These registers are normally set to 0x01 for best performance.

SPI Register 0x0A7 and SPI Register 0x0A8—Quadrature Calibration Status, Tx1 and Quadrature Calibration Status, Tx2

Bits[D7:D2]—Convergence Count[5:0]

These bits indicate the duration of the Tx quadrature calibration. Higher values on these bits indicate a longer calibration duration.

Bit D1—LO Convergence

If this bit equals one, the LO leakage algorithm converged.

Bit D0—SSB Convergence

If this bit equals one, the quadrature calibration algorithm converged

SPI Register 0x0A9—Set to 0xFF

Set this register to 0xFF. This register sets the maximum time that the Tx quadrature calibration algorithm can run.

SPI Register 0x0AA—Tx Quadrature Full/LMT Gain

The AD9363 uses Rx circuitry for the Tx quadrature calibration. Register 0x0AA sets the Rx gain for the calibration. When using the full gain table mode, Register 0x0AA specifies the gain index. When using the split table mode, Register 0x0AA specifies the LMT index and Register 0x0AE specifies the LPF index.

SPI Register 0x0AB—Must be 0

SPI Register 0x0AC—Must be 0

SPI Register 0x0AD—Must be 0

SPI Register 0x0AE—Tx Quadrature LPF Gain

This register only applies if the split gain table is used. See Register 0x0AA.

Tx BASEBAND FILTER (BBF) REGISTERS (ADDRESS 0x0C2 THROUGH ADDRESS 0x0CC)

Table 34. Tx BBF Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x0C2	Tx BBF R1	Override enable	Open		R1[4:0]					0x1F	R/W
0x0C3	Tx BBF R2	Open			R2[4:0]					0x1F	R/W
0x0C4	Tx BBF R3	Open			R3[4:0]					0x1F	R/W
0x0C5	Tx BBF R4	Open			R4[4:0]					0x1F	R/W
0x0C6	Tx BBF RP	Open			RP[4:0]					0x1F	R/W
0x0C7	Tx BBF C1	Open		C1[5:0]						0x2A	R/W
0x0C8	Tx BBF C2	Open		C2[5:0]						0x2A	R/W
0x0C9	Tx BBF CP	Open		CP[5:0]						0x2A	R/W
0x0CA	Tuner power-down	Must be 0x2				Set to 0	Tuner PD	Set to 2'b10		0x20	R/W
0x0CB	Tx BBF R2B	Must be 0	Open	R2B override	R2B[4:0]					0x00	R/W

The AD9361_SET_TX_RF_BANDWIDTH function configures these registers based on the RF bandwidth.

SPI Register 0x0C2—Tx BBF R1

Bit D7—Override Enable

Setting this bit forces the baseband filter to use the values written in Register 0x0C2 through Register 0x0CB.

Bits[D4:D0]—R1[4:0]

Tx baseband filter R1 word.

SPI Register 0x0C3 Through SPI Register 0x0C5—Tx BBF R2 Through Tx BBF R4

Tx baseband filter R2 through R4 words.

SPI Register 0x0C6—Tx BBF RP

Tx baseband filter real pole (RP) word.

SPI Register 0x0C7 and SPI Register 0x0C8—Tx BBF C1 and Tx BBF C2

Tx baseband filter C1 and C2 words.

SPI Register 0x0C9—Tx BBF CP

Tx baseband filter real pole word.

SPI Register 0x0CA—Tuner PD

Bits[D7:D3]—Set to 0x2

Bit D3—Set to 0

Bit D2—Tuner Power-Down

Clear this bit to run a Tx baseband filter calibration. Set the bit after the calibration completes.

Bits[D1:D0]—Set to 2'b10

SPI Register 0x0CB—Tx BBF R2B

Bit D7—Must be 0

Bit D5—R2B Override

This is a force bit but it only allows the R2B value to be forced. Use this bit only if performing a manual calibration.

Bits[D4:D0]—R2B[4:0]

Tx baseband filter R2B control word.

Tx SECONDARY FILTER REGISTERS (ADDRESS 0x0D0 THROUGH ADDRESS 0x0D3)

Table 35. Tx Secondary Filter Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x0D0	Configuration 0	Must be 0x5				C_C[1:0]		Amplifier bias[1:0]		0x55H	R/W
0x0D1	Resistor	Open				Resistor[3:0]				0x0FH	R/W
0x0D2	Capacitor	Open		Capacitor[5:0]						0x1FH	R/W
0x0D3	Must be 0x60	Must be 0x60								0x60H	R/W

The AD9361_SET_TX_RF_BANDWIDTH function configures these registers based on the RF bandwidth. These registers provide filtering for Tx noise that is far out from the channel. Typically, set the filter corner to 5× the baseband bandwidth.

SPI Register 0x0D0—Configuration 0

Bits[D7:D4]—Must be 0x5

Bits[D3:D2]—C_C[1:0]

Compensation network for the amplifiers, set per Table 36.

Table 36. Secondary Filter C_C and Amplifier Bias

RF Bandwidth (RF BW)	C_C[1:0]	Amplifier Bias[1:0]
≤9 MHz	10	01
9 MHz < RF BW ≤ 20 MHz	01	10

Bits[D1:D0]—Amplifier Bias[1:0]

These bits set amplifier bias current. Set per Table 36. Higher current equals lower noise and wider bandwidth.

SPI Register 0x0D1—Resistor[3:0]

Secondary filter resistor, which, along with the capacitor[5:0] bits, sets the 3 dB corner (see Register 0x0D2). The settings are per Table 37.

Table 37. Post Secondary Filter Stage Resistance

Resistor[3:0]	Post Filter Stage Resistance (Ω)
0001	800
0011	400
0100	200
1100	100

SPI Register 0x0D2—Capacitor[5:0]

Secondary filter capacitor, which, along with the resistor, sets the 3 dB corner (see Register 0x0D1). Set the capacitor such that resistor is as low as possible.

SPI Register 0x0D3—Must be 0x60

Tx BBF TUNER CONFIGURATION REGISTERS (ADDRESS 0x0D6 THROUGH ADDRESS 0x0D7)

Table 38. Tx BBF Tuner Configuration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x0D6	Tx BBF tune divider	Tx BBF tune divider[7:0]								0x12	R/W
0x0D7	Tx BBF tune mode	Open	Must be 2'b00		Must be 1	Must be 3'b111			Tx BBF tune divider[8]	0x1E	R/W

The AD9361_SET_TX_RF_BANDWIDTH function configures these registers based on the RF bandwidth.

SPI Register 0x0D6 and SPI Register 0x0D7, Bit D0

The Tx BBF uses a clock during calibration, derived by dividing down the BB PLL per Equation 15.

$$Tx\ BBF\ Tune\ Divider = \text{ceil}\left(\frac{BB\ PLL\ Frequency \times \ln(2)}{BBW \times 3.2 \times \pi}\right) \quad (15)$$

SPI Register 0x0D7—Tx BBF Tune Mode

Bits[D6:D5]—Must be 2'b00

Bit D4—Must be 1

Bits[D3:D1]—Must be 3'b111

RECEIVER CONFIGURATION REGISTERS

Rx PROGRAMMABLE FIR FILTER REGISTERS (ADDRESS 0x0F0 THROUGH ADDRESS 0x0F6)

Table 39. Rx Programmable FIR Filter Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x0F0	Rx filter coefficient address	Rx filter address[7:0]									R/W
0x0F1	Rx Filter Coefficient Data 1	Rx filter coefficient write data[7:0]									R/W
0x0F2	Rx Filter Coefficient Data 2	Rx filter coefficient write data[15:8]									R/W
0x0F3	Rx Filter Coefficient Read Data 1	Rx filter coefficient readback data[7:0]									R
0x0F4	Rx Filter Coefficient Read Data 2	Rx filter coefficient readback data[15:8]									R
0x0F5	Rx filter configuration	Number of taps			Select Rx channel[1:0]		Write Rx	Start Rx clock	Open	0x00	R/W
0x0F6	Rx filter gain	Open						Filter gain[1:0]		0x00	R/W

The AD9361_SET_RX_FIR_CONFIG function loads the FIR filter coefficients and sets up the other FIR parameters.

SPI Register 0x0F0—Rx Filter Coefficient Address

The digital filter coefficients are indirectly addressable. Register 0x0F0 holds the address of the coefficient address.

SPI Register 0x0F1 and SPI Register 0x0F2—Rx Filter Coefficient Data 1 and Rx Filter Coefficient Data 2

Write the coefficient values to these registers. Write these registers (along with Register 0x0F0) before setting Register 0x0F5, Bit D5. Coefficients are in twos complement format, 16-bits wide.

SPI Register 0x0F3 and Register 0x0F4—Rx Filter Coefficient Read Data 1 and Rx Filter Coefficient Read Data 2

When reading coefficients, write the address in Register 0x0F0, write Register 0x0F5 to start the programming clock, then read Register 0x0F3 and Register 0x0F4. Coefficients are in twos complement format, 16-bits wide.

SPI Register 0x0F5—Rx Filter Configuration

Bits[D7:D5]—Number of Taps[2:0]

The number of taps of the Rx filter must be correct, per Table 40. The number of taps can be read by first writing to Register 0x0F5 to turn on the clock, select the correct receiver, and to read Register 0x0F5.

Table 40. Rx Filter Taps

Number of Taps	Number of Taps[2:0]
16	000
32	001
48	010
64	011
80	100
96	101
112	110
128	111

Bits[D4:D3]—Select Rx Channel[1:0]

When writing coefficients, Bit D3 causes a write to Rx1, Bit D4 causes a write to Rx2, and both bits set writes to both Rx filters. When reading, setting both bits is an invalid case.

Bit D2—Write Rx

Set this self clearing bit to write a coefficient. Each write operation must set this bit. After the table is programmed, write to Register 0x0F6 with the write Tx bit cleared and Bit D1 high. Then, write to Register 0x0F6 again with Bit D1 clear, thus ensuring that the write bit resets internally before the clock stops. Wait 4 Tx sample periods after setting Bit D2 high while the data writes into the table.

Bit D1—Start Rx Clock

Set this bit to start the programming clock.

SPI Register 0xF6—Rx Filter Gain

These bits affect how much digital gain adds to the digital samples after the RFIR filter, per Table 41.

Table 41. Rx Filter Gain

Rx Filter Gain[1:0]	Gain (dB)
3	−12
2	−6
1	0 (default)
0	+6

GAIN CONTROL GENERAL SETUP REGISTERS (ADDRESS 0x0FA THROUGH ADDRESS 0x10E)

Table 42. Gain Control General Setup Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x0FA	AGC Configuration 1	Set to 3'b111			Slow attack hybrid mode	Rx2 gain control setup[1:0]		Rx1 gain control setup[1:0]		0xE0	R/W
0x0FB	AGC Configuration 2	Must be 0	Gain unlock control	Open		Use full gain table	Enable digital gain	Manual gain control, Rx2	Manual gain control, Rx1	0x08	R/W
0x0FC	AGC Configuration 3	Manual (CTRL_INx) increment gain step size[2:0]			Increment/ decrement LMT gain	Use AGC for LMT/LPF gain	ADC overrange sample size[2:0]			0x03	R/W
0x0FD	Maximum LMT/full gain	Open	Maximum full table/LMT table index[6:0]							0x4C	R/W
0x0FE	Peak wait time	Manual (CTRL_INx) decrement gain step size[2:0]			Peak overload wait time[4:0]					0x44	R/W
0x0FF	Open	Open									R/W
0x100	Digital gain	Digital gain step size[2:0]			Maximum digital gain[4:0]					0x6F	R/W
0x101	AGC lock level	Enable digital saturation overage	AGC lock level (fast)/AGC inner high threshold (slow)[6:0]							0x0A	R/W
0x102	Open	Open									R/W
0x103	Gain Step Configuration 1	Must be 0			Decrement step size for large LMT overload/Full Table Case 3[2:0]			Open		0x08	R/W
0x104	ADC small overload threshold	ADC small overload threshold[7:0]								0x2F	R/W
0x105	ADC large overload threshold	ADC large overload threshold[7:0]								0x3A	R/W
0x106	Gain Step Configuration 2	Open	Fast attack only; decrement step size for small LPF gain change/ Full Table Case 2[2:0]			Decrement step size for large LPF gain change/ Full Table Case 1[3:0]				0x25	R/W
0x107	Small LMT overload threshold	Force peak detector reset, Rx2	For peak detector reset, Rx1	Small LMT overload threshold[5:0]						0x3F	R/W
0x108	Large LMT overload threshold	Open		Large LMT overload threshold[5:0]						0x1F	R/W
0x109	Rx1 manual LMT/full gain	Power measured in State 5[3]	Rx1 manual full table/LMT table gain index[6:0]							0x4C	R/W
0x10A	Rx1 manual LPF gain	Power measured in State 5[2:0]			Rx1 manual LPF gain[4:0]					0x58	R/W
0x10B	Rx1 manual digital/ forced gain	Open		Force Rx1 digital gain	Rx1 manual/forced digital gain[4:0]					0x00	R/W
0x10C	Rx2 manual LMT/full gain	Open	Rx2 manual full table/LMT table gain index[6:0]							0x4C	R/W
0x10D	Rx2 manual LPF gain	Open			Rx2 manual LPF gain[4:0]					0x18	R/W
0x10E	Rx2 manual digital/ forced gain	Open		Force Rx2 digital gain	Rx2 manual/forced digital gain[4:0]					0x00	R/W

These registers are configured by the AD9361_SET_RX_GAIN_CONTROL_MODE function. For some applications, register values may need to be modified. See the AD9363 Reference Manual for more information.

SPI Register 0x0FA—AGC Configuration 1

Bits[D7:D5]—Set to 3'b111

Bit D4—Slow Attack Hybrid AGC Mode

Set this bit to use hybrid AGC mode. Otherwise, clear this bit.

Bits[D3:D2]—Rx2 Gain Control Setup[1:0]

The gain control operation maps to these setup bits per Table 43.

Table 43. Gain Control Setup

Gain Control Setup[1:0]	Gain Control Mode
0	Manual gain
1	Fast attack AGC
2	Slow attack AGC
3	Hybrid AGC; also set in Register 0x0FA, Bit D4

Bits[D1:D0]—Rx1 Gain Control Setup[1:0]

These bits function the same as Bits[D3:D2], but apply to Rx1.

SPI Register 0x0FB—AGC Configuration 2

Bit D7—Must be 0

Bit D6—Gain Unlock Control

This bit applies to fast AGC mode and allows the gain to stay locked, even under certain overload conditions.

Bit D3—Use Full Gain Table

Set this bit to use the full gain table. Clear to use the split gain table.

Bit D2—Enable Digital Gain

This bit is used in split table mode to enable the digital gain pointer.

Bit D1—Manual Gain Control, Rx2

This bit applies to manual gain control (MGC). If this bit is clear, SPI writes change the gain. When this bit is set, the control input pins control the gain. If this bit transitions high, the gain resets to the maximum value.

Bit D0—Manual Gain Control, Rx1

This bit functions the same as Bit D1, but applies to Rx1.

SPI Register 0x0FC—AGC Configuration 3

Bits[D7:D5]—Manual (CTRL_INx) Increment Gain Step Size[2:0]

These bits apply to MGC and if the CTRL_INx signals control the gain (Register 0x0FB, Bits[D1:D0] are set). The gain index increases by this register + 1 when certain CTRL_INx signals transition high.

Bit D4—Increment/Decrement LMT Gain

This bit applies to MGC, if the CTLR_INx signals control the gain (Register 0x0FB, Bits[D1:D0] are set), if the split gain table is used, and if Register 0x0FB, Bit D3 is clear. If this bit is set, the gain of the LNA, mixer, and transimpedance amplifier (TIA) changes. If this bit is clear, the LPF gain changes.

Bit D3—Use AGC for LMT/LPF Gain

This bit applies to MGC, if the CTRL_INx signals control the gain, (Register 0x0FB, Bits[D1:D0] are set), and to the split gain table (Register 0x0FB, Bit D3 is clear). If this bit is clear, Bit D4 determines where the gain changes. If this bit is set, the AGC determines where the gain changes.

Bits[D2:D0]—ADC Overrange Sample Size[2:0]

These bits + 1 equals the number of ADC output samples used to determine an ADC overload.

SPI Register 0x0FD—Maximum LMT/Full Gain

This register must be set to the maximum gain index of the gain table.

SPI Register 0x0FE—Peak Wait Time

Bits[D7:D5]—Manual (CTRL_INx) Decrement Gain Step Size[2:0]

These bits apply to MGC and if the CTRL_INx signals control the gain (Register 0x0FB, Bits[D1:D0] are set). The gain index decreases by these bits +1 when certain CTRL_INx signals transition high.

Bits[D4:D0]—Peak Overload Wait Time[4:0]

These bits set the wait time in CLKRF cycles that the peak detectors are held in reset after a gain change, which affects all gain control modes.

SPI Register 0x100—Digital Gain

Bits[D7:D5]—Digital Gain Step Size[2:0]

These bits apply to AGC modes, if digital gain is enabled (Register 0x0FB, Bit D2 is set), and the split table (Register 0x0FB, Bit D3 is clear). If digital saturation occurs, digital gain reduces by this register +1.

Bits[D4:D0]—Maximum Digital Gain[4:0]

These bits apply if digital gain is enabled (Register 0x0FB, Bit D2 is set), equals the maximum allowable digital gain, and applies to all gain control modes. The maximum value is 31 dB. The resolution is 1 dB/LSB.

SPI Register 0x101—AGC Lock Level

Bit D7—Enable Digital Saturation Overage

This bit applies to fast AGC mode and the full gain table. When this bit is clear, digital saturation does not cause a gain decrease. When this bit is set, digital saturation causes a gain decrease.

Bits[D6:D0]—AGC Lock Level (Fast)/AGC Inner High Threshold (Slow)[6:0]

These bits apply to AGC. This register specifies the fast AGC lock level or specifies the slow AGC inner high threshold. The resolution is −1 dBFS/LSB.

SPI Register 0x103—Gain Step Configuration 1

Bits[D7:D5]—Must be 0

Bits[D4:D2]—Step Size for Large LMT Overload/Full Table Case 3[2:0]

These bits apply to AGC and determine how much the gain changes for large LMT in split table mode, or the small ADC overload for the full table.

SPI Register 0x104—ADC Small Overload Threshold

This register sets the small ADC overload and is one of two registers that the AGC compares against ADC output samples. Ensure that this register is smaller than Register 0x105.

SPI Register 0x105—ADC Large Overload Threshold

This register functions the same as Register 0x104, but must be the larger of the two values.

SPI Register 0x106—Gain Step Configuration 2

Bits[D6:D4]—Fast Attack Only; Decrement Step Size for: Small LPF Gain Change/Full Table Case 2[2:0]

These bits apply to AGC and determine how much the gain changes for large LPF in split table mode, the large LMT, or large ADC overloads in full table mode.

Bits[D3:D0]—Decrement Step Size for Large LPF Gain Change/Full Table Case 1

These bits apply to AGC and determine how much the gain changes for large LPF in split table mode, the large LMT, and large ADC overloads in full table mode.

SPI Register 0x107—Small LMT Overload Threshold

Bit D7—Force Peak Detector Reset, Rx2

Setting this bit forces the Rx2 ADC and LMT peak detectors to ignore peak overloads.

Bit D6—Force Peak Detector Reset, Rx1

This bit functions the same as Bit D7, but applies to Rx1.

Bits[D5:D0]—Small LMT Overload Threshold[5:0]

These bits, mapped per Equation 16, set the small LMT overload threshold and comprise one of two values that the AGC compares against the signal at the input to the LPF. Ensure that this register is smaller than Register 0x108. The valid range is from 0x07 to 0x31.

$$\textit{LMT Overload Threshold}\ (\text{mV peak}) = 16\ \text{mV} \times (\textit{LMT Overload Threshold[5:0]} + 1) \quad (16)$$

SPI Register 0x108—Large LMT Overload Threshold

This register functions the same as Register 0x107 (and uses the same equation), but must be larger than Register 0x107, Bits[D5:D0].

SPI Register 0x109—Rx1 Manual LMT/Full Gain

Bit D7—Power Measured in State 5[3]

This bit is the same as the decimate power measurement duration bits (Register 0x15C, Bits[D3:D0]), but applies only to State 5 (gain lock) for fast AGC mode.

Bits[D6:D0]—Rx1 Manual Full Table/LMT Table Gain Index[6:0]

For MGC, write this register to set the full table or LMT index. For AGC, this register holds the current full or LMT index.

SPI Register 0x10A—Rx1 Manual LPF Gain

Bits[D7:D5]—Power Measured in State 5[2:0]

See Register 0x109, Bit D7.

Bits[D4:D0]—Rx1 Manual LPF Gain[4:0]

These bits apply to split table mode. For MGC, write this register to set the LPF gain table index value. For AGC, this register holds the current LPF index.

SPI Register 0x10B—Rx1 Manual Digital Gain

Bits[D4:D0]—Rx1 Manual/Forced Digital Gain

These bits apply to the split table. In MGC, write this register to set the digital gain. In AGC mode, these bits hold the digital gain.

SPI Register 0x10C Through SPI Register 0x10E—Manual Gain Registers

These registers are the same as Registers 0x109 through Registers 0x10B, but apply to Rx2.

FAST ATTACK AGC SETUP REGISTERS (ADDRESS 0x110 THROUGH ADDRESS 0x11B)

Table 44. Fast Attack AGC Setup Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x110	Configuration 1	Enable gain increment after gain lock	Go to optimized gain if energy is lost or EN_AGC is high	Go to set gain if EN_AGC is high	Go to set gain if in exit Rx state	Do not unlock gain if energy is lost	Go to optimized gain if in exit Rx state	Do not unlock gain If large ADC or LMT overage	Enable increment gain	0x02	R/W
0x111	Configuration 2 and settling delay	Use last lock level for set gain	Enable LMT gain increment for lock level	Go to maximum gain or optimal gain if EN_AGC is high	Settling delay[4:0]					0xCA	R/W
0x112	Energy lost threshold	Post lock level step size for LPF table/full table[1:0]		Energy lost threshold[5:0]						0x4A	R/W
0x113	Stronger signal threshold	Post lock level step for LMT table[1:0]		Stronger signal threshold[5:0]						0x4A	R/W
0x114	Low power threshold	Do not unlock gain if ADC overage	Low power threshold[6:0]							0x80	R/W
0x115	Strong signal freeze	Do not unlock gain if stronger signal	Open							0x64	R/W
0x116	Final overrange and optimal gain	Final overrange count[2:0]			Open	Optimize gain offset[3:0]				0x65	R/W
0x117	Energy detect count	Increment gain step (LPF/LMT)[2:0]			Energy detect count[4:0]					0x08	R/W
0x118	AGC lock level upper limit	Open		AGCLL maximum increase[5:0]						0x3F	R/W
0x119	Gain lock exit count	Open		Gain lock exit count[5:0]						0x08	R/W
0x11A	Initial LMT gain limit	Open	Initial LMT gain limit[6:0]							0x1C	R/W
0x11B	Increment time	Increment time[7:0]								0x0A	R/W

These registers are configured by the AD9361_SET_RX_GAIN_CONTROL_MODE function. For some applications, register values may need to be modified. Many bits in this section change operation depending on other bit settings. See the AD9363 Reference Manual for more information.

SPI Register 0x110—Configuration 1

Bit D7—Enable Gain Increment after Gain Lock

This bit applies to fast AGC mode and if the enable gain increment bit (Register 0x110, Bit D0) is set. Set Register 0x110, Bit D7 to allow gain increases after the gain is locked, but before State 5. The signal power must be lower than the low power threshold in Register 0x114 for longer than the increment time duration register (Address 0x11B); if this is the case, the gain increases by the increment gain step set by Register 0x117, Bits[D7:D5].

Bit D6—Go to Optimal Gain if is Energy Lost or EN_AGC is High

If this bit is set and fast AGC is in State 5, the gain index goes to the optimize gain value if an energy lost state occurs or, if Register 0x0FB, Bit D6 is high, when the EN_AGC signal goes high.

Bit D5—Go to Set Gain if EN_AGC is High

If this bit is set and fast AGC is in State 5, the gain index goes to the set gain value if EN_AGC goes high. Register 0x0FB, Bit D6 must be set.

Bit D4—Go to Set Gain if in Exit Rx State

If this bit is set and fast AGC is in State 5, the gain index goes to the set gain value when the ENSM exits the Rx state.

Bit D3—Do Not Unlock Gain if Energy is Lost

If this bit is set and fast AGC is in State 5, the gain does not change, even if the average signal power decreases more than the energy lost threshold register (Address 0x112).

Bit D2—Go to Optimized Gain if in Exit Rx State

If this bit is set and the fast AGC is in State 5, the gain goes to the optimize gain value if the ENSM exits the Rx state.

Bit D1—Do Not Unlock Gain if Large ADC or LMT Overage

If this bit is set and fast AGC is in State 5, the gain does not change, even if large ADC or large LMT overloads occur.

Bit D0—Enable Increment Gain

Setting this bit allows the fast AGC to increase the gain while optimizing the gain index. Clearing this bit prevents the gain from increasing in any condition.

SPI Register 0x111—Configuration 2 and Settling Delay

Bit D7—Use Last Lock Level for Set Gain

This bit only applies if fast AGC mode uses set gain. Set this bit to use the last gain index of the previous frame for set gain. Clear this bit to use the first gain index of the previous frame.

Bit D6—Enable LMT Gain Increment for Lock Level

This bit applies to fast AGC mode and the split gain table. Set this bit to allow the AGC to use LMT gain if the gain index must increase when moving to the AGC lock level in Register 0x101. The maximum LMT gain allowed is set by the LMT gain step (Register 0x103, Bits[D4:D2]). The difference (if any) is compensated for by the LPF gain.

Bit D5—Go to Maximum Gain or Optimal Gain if EN_AGC is High

If this bit is set and the EN_AGC signal goes high, the fast AGC mode goes to either the maximum gain index or the optimize gain value, depending on Register 0x110, Bit D6.

Bits[D4:D0]—Settling Delay[4:0]

These bits apply to all gain control modes. These bits set the delay between a gain change and a power measurement. The delay equals this register × 2 in CLKRF cycles.

SPI Register 0x112—Energy Lost Threshold

Bits[D7:D6]—Post Lock Level Step Size for LPF Table/Full Table[1:0]

These bits set the reduction to the gain index if a large LMT or large ADC overload occurs after the lock level but before fast AGC mode, State 5. If the number of overloads exceeds the final overrange count (Register 0x116, Bits[D7:D5]), the AGC algorithm restarts. Depending on various conditions, if a split table is used, the gain may reduce in in the LPF or the LMT (see Register 0x113, Bits[D7:D6]).

Bits[D5:D0]—Energy Lost Threshold[5:0]

These bits apply if fast AGC mode is in State 5. If the signal power decreases by this threshold and the signal power remains at this level or lower for a duration that is twice the gain lock exit count (Register 0x119), the gain may unlock, depending on other AGC configuration bits. The resolution is 1 dB/LSB.

SPI Register 0x113—Stronger Signal Threshold

Bits[D7:D6]—Post Lock Level Step for LMT Table[1:0]

See Register 0x112, Bits[D7:D6].

Bits[D5:D0]—Stronger Signal Threshold[5:0]

These bits apply if fast AGC mode is in State 5. If the signal power increases by this threshold and the signal power remains at this level or higher for a duration that is twice the gain lock exit count (Register 0x119), the gain may unlock, depending on other AGC configuration bits. The resolution is 1 dB/LSB.

SPI Register 0x114—Low Power Threshold

Bit D7—Do Not Unlock Gain if ADC Overage

If this bit is set and fast AGC mode is in State 5, the gain does not change, even if large ADC overloads occur.

Bits[D6:D0]—Low Power Threshold[6:0]

This threshold is used by fast AGC mode to determine if the gain must be increased if Register 0x110, Bit D0 is set. This threshold can also be used to trigger a CTRL_OUTx signal transition in MGC mode. The units are −dBFS; the resolution is 0.5 dB/LSB.

SPI Register 0x115—Do Not Unlock Gain if Stronger Signal

If this bit is set and fast AGC mode is in State 5, the gain does not change, even if the signal power increases by more than the stronger signal threshold in Register 0x113, Bits[D5:D0].

SPI Register 0x116—Final Overrange and Optimal Gain

Bits[D7:D5]—Final Overrange Count[2:0]

See Register 0x112, Bits[D7:D6].

Bits[D3:D0]—Optimize Gain Offset[3:0]

These bits are the offset added to the last gain lock level of the previous frame. The result is the optimize gain index.

SPI Register 0x117—Energy Detect Count

Bits[D7:D5]—Increment Gain Step LPF/LMT[2:0]

Fast AGC mode increases the gain index by this amount if the signal power decreases below the low power threshold, as described in Register 0x114, Bits[D6:D0], and only if the enable increment gain bit (Register 0x110, Bit D0) is set.

Bits[D4:D0]—Energy Detect Count[4:0]

Fast AGC mode delays moving from State 1 to State 2 until no peak overloads are detected for the value of this counter; this is measured in CLKRF cycles. The resolution is 1 CLKRF cycle/LSB.

SPI Register 0x118—AGC Lock Level Maximum Increase

This register sets the maximum gain index increase that the fast AGC can use for the lock level adjustment.

SPI Register 0x119—Gain Lock Exit Count

See Register 0x112, Bits[D5:D0].

SPI Register 0x11A—Initial LMT Gain Limit

This register applies to AGC modes. The LMT table splits at this value.

SPI Register 0x11B—Increment Time[7:0]

This register sets the time that the signal power must remain below the low power threshold in Register 0x114, Bits[D6:D0] before fast AGC mode changes gain. This register can also be used by MGC (see Register 0x114, Bits[D6:D0]). The resolution is 1 CLKRF cycle/LSB.

SLOW ATTACK AND HYBRID AGC REGISTERS (ADDRESS 0x120 THROUGH ADDRESS 0x12A)

Table 45. Slow Attack and Hybrid AGC Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x120	AGC inner low threshold	Prevent gain increment	AGC inner low threshold[6:0]								R/W
0x121	LMT overload counters	Large LMT overload exceeded counter[3:0]				Small LMT overload exceeded counter[3:0]					R/W
0x122	ADC overload counters	Large ADC overload exceeded counter[3:0]				Small ADC overload exceeded counter[3:0]					R/W
0x123	Gain Step 1	Immediate gain change if large LMT overload	AGC inner high threshold exceeded step size[2:0]			Immediate gain change if large ADC overload	AGC inner low threshold exceeded step size[2:0]				R/W
0x124	Gain Update Counter 1	Gain update counter[7:0]									
0x125	Gain Update Counter 2	Gain update counter[15:8]									
0x126	Open	Open									
0x127	Open	Open									
0x128	Digital saturation counter	Open		Double gain counter	Enable synchro-nization for gain counter	Digital saturation exceeded counter[3:0]					R/W
0x129	Outer power thresholds	AGC outer high threshold[3:0]				AGC outer low threshold[3:0]					R/W
0x12A	Gain Step 2	AGC outer high threshold exceeded step size[3:0]				AGC outer low threshold exceeded step size[3:0]					R/W

These registers are configured by the AD9361_SET_RX_GAIN_CONTROL_MODE function. For some applications, register values may need to be modified. See the AD9363 Reference Manual for more information.

SPI Register 0x120—AGC Inner Lower Threshold

Bit D7—Prevent Gain Increment

Setting this bit prevents a gain increase if a small LMT or small ADC overload occurs.

Bits[D6:D0]—AGC Inner Low Threshold[6:0]

These bits set the slow AGC inner low window threshold in negative dBFS and with a resolution of 1 dB/LSB.

SPI Register 0x121—LMT End Overload Counters

Bits[D7:D4]—Large LMT Overload Exceeded Counter[3:0]

This counter specifies the number of large LMT overloads that must occur before the gain decreases by the LMT gain step in Register 0x103, Bits[D4:D2].

Bits[D3:D0]—Small LMT Overload Exceeded Counter[3:0]

These bits apply if the prevent gain increment bit (Register 0x120, Bit D7 is set. This counter specifies the number of small LMT overloads that must occur to prevent a gain increase.

SPI Register 0x122—ADC Overload Counters

Bits[D7:D4]—Large ADC Overload Exceeded Counter[3:0]

This counter specifies the number of large ADC overloads that must occur before the gain decreases by the large ADC overload gain step in Register 0x106, Bits[D3:D0].

Bits[D3:D0]—Small ADC Overload Exceeded Counter[3:0]

These bits apply if the prevent gain increment bit in Register 0x120, Bit D7 is set. This counter specifies the number of small ADC overloads that must occur to prevent a gain increase.

SPI Register 0x123—Gain Step 1

Bit D7—Immediate Gain Change if Large LMT Overload

Set this bit to allow large LMT overloads to reduce the gain immediately.

Bits[D6:D4]—AGC Inner High Threshold Exceeded Step[2:0]

These bits set the gain decrease amount when the inner high threshold is exceeded.

Bit D3—Immediate Gain Change if Large ADC Overload

This bit performs the same operation described in Register 0x123, Bit D7, but applies to the large ADC overload.

Bits[D2:D0]—AGC Inner Low Threshold Exceeded Step[2:0]

These bits are the same as Register 0x123, Bits[D6:D4], but apply to the inner low threshold.

SPI Register 0x124 and SPI Register 0x125—Gain Update Counter

These registers apply to slow AGC mode. Gain changes cannot occur until this counter expires, unless the immediate update bits are set in Register 0x123, Bit D7 or Register 0x123, Bit D3. The counter clocks at the CLKRF rate and starts counting 3 CLKRF cycles after the ENSM enters the Rx state and is clocked at the CLKRF rate. The depth of the counter is equal to double the value in these registers or, if Bit D5 in Register 0x128 is set, it is equal to 4× the value in these registers. If the enable synchronization for gain counter bit (Register 0x128, Bit D4) is set, CTRL_IN2 transitioning high resets the counter.

SPI Register 0x128—Digital Saturation Counter

Bit D5—Double Gain Counter

See Register 0x124 and Register 0x125.

Bit D4—Enable Synchronization for Gain Counter

See Register 0x124 and Register 0x125.

Bits[D3:D0]—Digital Saturation Exceeded Counter

These bits apply if the prevent gain increment bit (Register 0x120, Bit D7) is set. This counter specifies the number of digital saturation events that must occur to prevent a gain increase.

SPI Register 0x129—Outer Power Thresholds

Bits[D7:D4]—AGC Outer High Threshold[3:0]

The outer high threshold equals the inner high threshold (Register 0x101) plus this value. The resolution is 1 dB/LSB.

Bits[D3:D0]—AGC Outer Low Threshold[3:0]

The outer low threshold equals the inner low threshold (Register 0x120, Bits[D6:D0]) plus this value. The resolution is 1 dB/LSB.

SPI Register 0x12A—Gain Step 2

Bits[D7:D4]—AGC Outer High Threshold Exceeded Step[3:0]

Slow AGC mode changes the gain by this amount when the outer high threshold is exceeded.

Bits[D3:D0]—AGC Outer Low Threshold Exceeded Step[3:0]

The slow AGC changes gain by this amount when the outer low threshold is exceeded.

EXTERNAL LNA GAIN WORD REGISTERS (ADDRESS 0x12C THROUGH ADDRESS 0x12D)

SPI Register 0x12C and SPI Register 0x12D—Ext LNA High Gain and Ext LNA Low Gain

These registers can have nonzero values only if an external LNA is used (which has two gain modes that it can switch between) and the external LNA is controlled by the GPOs triggered by bits in the gain table. Program Register 0x12C with the high gain (nonbypass) value and program Register 0x12D with the low gain (bypass) value. The device considers both values to represent positive gain in the front end prior to the AD9363. Both registers range from 0 dB to 31.5 dB in 0.5 dB steps/LSB.

Table 46. External LNA Gain Word Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x12C	External LNA high gain	Open		External LNA high gain[5:0]							R/W
0x12D	External LNA low gain	Open		External LNA low gain[5:0]						0x00	R/W

AGC GAIN TABLE REGISTERS (ADDRESS 0x130 THROUGH ADDRESS 0x137)

Table 47. AGC Gain Table Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x130	Gain table address	Open	Gain table address[6:0]								R/W
0x131	Gain Table Write Data 1	External LNA control	LNA gain[1:0]		Must be 0	Mixer gain[3:0]					R/W
0x132	Gain Table Write Data 2	Open		TIA gain	LPF gain[4:0]						R/W
0x133	Gain Table Write Data 3	Open		RF dc Calibration	Digital gain[4:0]						R/W
0x134	Gain Table Read Data 1	External LNA control	LNA gain[1:0]		Must be 0	Mixer gain[3:0]					R
0x135	Gain Table Read Data 2	Open		TIA gain	LPF gain[4:0]						R
0x136	Gain Table Read Data 3	Open		RF dc calibration	Digital gain[4:0]						R
0x137	Gain table configuration	Open			Receiver select[1:0]		Write gain table	Start gain table clock	Open	0x08	R/W

The AD9361_LOAD_GT function loads Analog Devices standard gain tables based on the configuration and carrier frequency. Gain tables are written and read back in to/out of the AD9363 using these registers. The gain tables are stored in locations that are indirectly addressable.

SPI Register 0x130—Gain Table Address

This is the gain table index address. The maximum range is 0 to 90 (decimal) in full table mode and 0 to 40 (decimal) in split table mode.

SPI Register 0x131—Gain Table Write Data 1

Bit D7—External LNA Control

This bit, routed to a GPO_x pin, controls the bypass pin on a bypassable external LNA. The external LNA then becomes part of the gain control loop. See Register 0x026, Bits[D6:D5].

Bits[D6:D5]—LNA Gain[1:0]

These bits are the internal LNA gain index. There are four possible values ranging from 0 through 3; 3 represents the maximum gain, and 0 is the minimum gain.

Bit D4—Must be 0

Bits[D3:D0]—Mixer Gain[3:0]

These bits are the mixer gain index. There are 16 values ranging from 0x0 through 0xF; 0xF represents the maximum gain, and 0 is the minimum gain.

SPI Register 0x132—Gain Table Write Data 2

Bit D5—TIA Gain

This bit is the TIA gain. If this bit is 0, the TIA gain equals −6 dB; if the bit is set, the gain equals 0 dB.

Bits[D4:D0]—LPF Gain[4:0]

These bits are the LPF index. The range is 0 dB to 24 dB. The resolution is 1 LSB/1 dB (full gain table only).

SPI Register 0x133—Gain Table Write Data 3

Bit D5—RF DC Calibration

Setting this bit causes the initial RF dc calibration to occur at the gain index specified in Register 0x130 (full gain table only).

Bits[D4:D0]—Digital Gain[4:0]

The digital gain maps as 1 dB gain/LSB.

SPI Register 0x134 Through SPI Register 0x136—Gain Table Read Data 1 Through Gain Table Read Data 3

Use these registers to read gain tables from the AD9363.

SPI Register 0x137—Gain Table Configuration

Bits[D4:D3]—Receiver Select[1:0]

Bit D3 accesses Rx1 and Bit D4 accesses Rx2. When reading the gain table, setting both bits is invalid.

Bit D2—Write Gain Table

Set this self clearing bit to write the values in Register 0x130 through Register 0x133 to the gain table. After writing all table entries, write Register 0x137 with the write gain table bit cleared and the start gain table clock bit high. Then, write Register 0x137 again with the clock start bit cleared; this ensures that the write bit clears after the last write operation.

Bit D1—Start Gain Table Clock

Set this bit only when writing to the gain table. The gain table requires four Rx sample periods after the write gain table bit goes high for the value to write into the table.

MIXER SUBTABLE REGISTERS (ADDRESS 0x138 THROUGH ADDRESS 0x13F)

Table 48. Mixer Subtable Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x138	Mixer subtable address	Must be 0				Mixer subtable address[7:0]					R/W
0x139	Mixer subtable gain word write	Open	Mixer subtable gain word write[6:0]								R/W
0x13A	Mixer subtable bias word write	Open			Mixer subtable bias word write[4:0]						R/W
0x13B	Mixer subtable control word write	Open		Mixer subtable control word write[5:0]							R/W
0x13C	Mixer subtable gain word read	Open	Mixer subtable gain word read[6:0]								R
0x13D	Mixer subtable bias word read	Open			Mixer subtable bias word read[4:0]						R
0x13E	Mixer subtable control word read	Open		Mixer subtable control word read[5:0]							R
0x13F	Mixer subtable configuration	Open					Write mixer subtable	Start mixer subtable clock	Open	0x00	R/W

These registers are programmed by the mixer subtable function, AD9361_LOAD_GT. Do not program these registers in a way that is different from what is described in the API.

SPI Register 0x138—Mixer Subtable Word Address

Bits[D7:D4]—Must be 0

Bits[D3:D0]—Mixer Subtable Address[7:0]

These bits are the subtable address with a valid range of 0 to 0xF.

SPI Register 0x139—Mixer Subtable Gain Word Write

Program the mixer gain in dB × 4 into this register so that the RSSI algorithm compensates for mixer gain correctly.

SPI Register 0x13A—Mixer Subtable Bias Word Write

This register sets the mixer bias word for the mixer subtable.

SPI Register 0x13B—Mixer Subtable Control Word Write

This register sets the mixer subtable control word.

SPI Register 0x13C Through Register 0x13E—Mixer Subtable Word Reads

Read the mixer subtable using these registers after setting the address in Register 0x138.

SPI Register 0x13F—Mixer Subtable Configuration

Bit D2—Write Mixer Subtable

Set this bit when writing to the subtable. Set this bit each time new words in Register 0x139 through Register 0x13B are written to Address 0x138.

Bit D1—Start Mixer Subtable Clock

This bit is used when writing to the mixer subtable. Allow at least 4 Rx sample periods between consecutive writes.

CALIBRATION GAIN TABLE REGISTERS (ADDRESS 0x140 THROUGH ADDRESS 0x144)

Table 49. Calibration Gain Table Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x140	Word address	Calibration table address[7:0]									R/W
0x141	Gain difference word/error write	Open		Calibration table gain difference/error word[5:0]							W
0x142	Gain error read	Open			Calibration table gain error[4:0]						R
0x143	Configuration	Open	Calibration table select[1:0]		Read select	Write mixer error table	Write LNA error table	Write LNA gain diff	Start calibration table clock	0x00	R/W
0x144	LNA gain difference readback	Open		LNA calibration table gain difference word[5:0]							R

See the AD9363 Reference Manual for more information about calibrating the Rx RSSI function.

SPI Register 0x140—Word Address

Program the index of the gain stage in this register.

SPI Register 0x141—Gain Diff Word/Error Write

If the write LNA gain difference bit (Register 0x143, Bit D1) is set, then Register 0x141 is the difference between the LNA maximum gain and the gain at the index in Register 0x140. The resolution is 0.5 dB. If the write mixer error table bit (Register 0x143, Bit D3) or the write LNA error table bit (Register 0x143, Bit D2) are set, then the error words can be programmed into this register for the index specified in Register 0x140. The error word resolution is 0.25 dB/LSB.

SPI Register 0x142—Gain Error Read

This is the gain error determined by the calibration at the index in Register 0x140. The resolution is 0.25 dB/LSB.

SPI Register 0x143—Configuration

Bits[D6:D5]—Calibration Table Select[1:0]

When these bits are set, Bit D5 accesses Rx1 and Bit D6 accesses Rx2. When reading these bits, only one bit may be set.

Bit D4—Read Select

Clear this bit to read mixer errors and set this bit to read LNA errors.

Bit D3—Write Mixer Error Table

Set this self clearing bit to write a mixer error word. Bit D2 and Bit D1 must be clear. After writing all of the values, clear the write mixer error table bit and set the start calibration table clock bit. Then, write to Register 0x143 again with the clock start bit cleared; this ensures that the write signal resets before the clock stops.

Bit D2—Write LNA Error Table

Set this self clearing bit to write an LNA error word. Bit D3 and Bit D1 must be clear. After writing all of the values, clear the write mixer error table bit and set start calibration table clock bit. Then, write to Register 0x143 again with the clock start bit cleared; this ensures that the write signal resets before the clock stops.

Bit D1—Write LNA Gain Difference

Set this self clearing bit to write a gain difference word. Bit D3 and Bit D2 must be clear. After writing all of the values, clear the write mixer error table bit and set start calibration table clock bit. Then, write to Register 0x143 again with the clock start bit cleared; this ensures that the write signal resets before the clock stops.

Bit D0—Start Calibration Table Clock

Set this bit to access the calibration gain table registers.

SPI Register 0x144—LNA Gain Difference Readback

Read back LNA gain difference words from this register after writing the address of the table to Register 0x140.

GENERAL CALIBRATION REGISTERS (ADDRESS 0x145 THROUGH ADDRESS 0x149)

Table 50. General Calibration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x145	Maximum mixer calibration gain index	Open			Maximum mixer calibration gain index[4:0]					0x0B	R/W
0x146	Temperature gain coefficient	Temperature gain coefficient[7:0]								0x00	R/W
0x147	Settle time	Enable digital gain correction	Force temperature sensor for calibration	Settle time[5:0]						0x10	R/W
0x148	Measurement duration	Open				Gain calibration measurement duration[3:0]				0x04	R/W
0x149	Calibration temperature sensor word	Calibration temperature sensor word[7:0]								0x00	R/W

SPI Register 0x145—Max Mixer Calibration Gain Index

This register is used only when calibrating Rx RSSI using the gain step calibration, initialized by Register 0x016, Bit D3. Set the value of this register to 0xF.

SPI Register 0x146—Temperature Gain Coefficient

This value is used with RSSI temperature compensation. This value represents the LNA and mixer dependence on temperature in dB/°C, which is then stored in this register. The value is coded in twos complement notation and the resolution is 0.0078 dB with an approximate maximum of ±1 dB/°C. This register is used with the calibration temperature sensor word bit in Register 0x149.

SPI Register 0x147—Settle Time

Bit D7—Enable Digital Gain Correction

Set this bit to enable gain step error correction after a gain step calibration runs. See Register 0x140.

Bit D6—Force Temperature Sensor for Calibration

This bit must be clear when running the gain step calibration described in Register 0x140 through Register 0x143. This bit must be set to enable temperature compensation during operation.

Bits[D5:D0]—Settle Time[5:0]

These bits specify the time duration, in CLKRF cycles, before the power measurement for the gain calibration algorithm at a specific gain starts. This delay allows the analog circuitry to settle. The default value of 0x10 is sufficient for most scenarios.

SPI Register 0x148—Measurement Duration

This register specifies the duration of the power measurement used for gain calibration. The duration is per Equation 17.

$$Duration\ (\text{CLKRF cycles}) = 2^{Gain\ Calibration\ Measurement\ Duration[3:0]} \quad (17)$$

SPI Register 0x149—Calibration Temperature Sensor Word

When gain step calibration occurs, the AD9363 stores the temperature at which the calibration occurred in this register.

RSSI MEASUREMENT CONFIGURATION REGISTERS (ADDRESS 0x150 THROUGH ADDRESS 0x15D)

Table 51. RSSI Measurement Configuration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x150	Duration 0, Duration 1	Measurement Duration 1[3:0]				Measurement Duration 0[3:0]				0x08	R/W
0x151	Duration 2, Duration 3	Measurement Duration 3[3:0]				Measurement Duration 2[3:0]					R/W
0x152	Weight 0	Weighted Multiplier 0[7:0]								0x00	R/W
0x153	Weight 1	Weighted multiplier 1[7:0]								0x00	R/W
0x154	Weight 2	Weighted Multiplier 2[7:0]								0x00	R/W
0x155	Weight 3	Weighted Multiplier 3[7:0]								0x00	R/W
0x156	RSSI delay	RSSI delay[7:0]								0x00	R/W
0x157	RSSI wait time	RSSI wait[7:0]								0x00	R/W
0x158	RSSI configuration	RFIR for RSSI measurement[1:0]		Start RSSI measurement	RSSI mode select[2:0]			Must be 0	Default RSSI measurement mode	0x01	R/W
0x159	Open	Open									R/W
0x15A	Open	Open								0x00	R/W
0x15B	Open	Open								0x00	R/W
0x15C	Decimate power duration	Open	Use HB1 output for decimate power measurement	Set to 1	Open	Decimate power measurement duration[3:0]				0x15	R/W
0x15D	LNA gain	Maximum LNA gain[6:0]							Open	0xB1	R/W

The AD9361_RSSI_SETUP function configures the RSSI based on various parameters.

SPI Register 0x150 and SPI Register 0x151—Duration 0 Through Duration 3

If the default RSSI measurement mode bit (Register 0x158, Bit D0) is set, then Equation 18 sets the RSSI measurement duration.

$$Duration\ (\text{Rx samples}) = 2^{Measurement\ Duration[3:0]} \quad (18)$$

If Register 0x158, Bit D0 is clear, the duration equals Equation 19.

$$Duration\ (\text{Rx samples}) = \sum_{i=D}^{3} 2^{Measurement\ Duration\ i[3:0]} \quad (19)$$

The maximum value for any nibble is 0xE (not 0xF).

SPI Register 0x152 Through SPI Register 0x155—Weight 0 Through Weight 3

If Register 0x158, Bit D0 is clear, calculate the weights per Equation 20 and load the value to Register 0x152 through Register 0x155. The total of all the weights must equal 0xFF.

$$Weight\ n = 255 \times \left(\frac{2^{Measurment\ Duration\ n}}{RSSI\ Measurment\ Duration} \right) \quad (20)$$

SPI Register 0x156 and SPI Register 0x157—RSSI Delay and RSSI Wait

When the RSSI algorithm starts or restarts (see Register 0x158, Bits[D4:D2]), the AD9363 waits for the delay counter to expire before calculating the RSSI. The counter is clocked at the Rx sample rate, divided by 8. For subsequent calculations, the algorithm waits for the wait counter to expire before recalculating. The counter is clocked at the Rx sample rate divided by 4.

SPI Register 0x158—RSSI Configuration

Bits[D7:D6]—RFIR for RSSI Measurement[1:0]

If the datapath Rx FIR is bypassed (see Register 0x003, Bits[D1:D0]), the RSSI calculation can still use the RFIR per Table 5.

Bit D5—Start RSSI Measurement

Setting this bit restarts the RSSI algorithm if Bits[D4:D2] = 3'b100.

Bits[D4:D2]—RSSI Mode Select[2:0]

The RSSI algorithm starts or restarts when an or events in Table 52 occur. If the EN_AGC pin is used, the RSSI delay in Register 0x156 must be 0.

Table 52. RSSI Mode

Bits[D4:D2]	RSSI Algorithm Starts or Restarts When
000	AGC in fast attack mode locks the gain
001	EN_AGC pin is pulled high
010	AD9363 enters Rx mode
011	Gain change occurs
100	SPI write to Register 0x158, Bit D5
101	Gain change occurs or EN_AGC pin is high

Bit D1—Must be 0

Bit D0—Default RSSI Measurement Mode

See Register 0x150 and Register 0x151.

SPI Register 0x15C—Decimate Power Duration

Bit D6—Use HB1 Output for Decimate Power Measurement

Set this bit to use the HB1 output for power measurements. Clear this bit to use the Rx FIR output.

Bit D5—Set to 1

Bits[D3:D0]—Decimate Power Measurement Duration[3:0]

The power measurement duration used by the gain control algorithm (not the RSSI), per Equation 21.

$$Duration\ (\text{Rx cycles}) = 16 \times 2^{Decimate\ Power\ Measurement\ Duration[3:0]} \quad (21)$$

SPI Register 0x15D—LNA Gain

Bits[D7:D1]—Maximum LNA Gain[6:0]

These bits are used by the RSSI and must equal the maximum LNA gain in decibels multiplied by 4, and converted to hexadecimal. The resolution is 0.25 dB.

POWER WORD REGISTERS (ADDRESS 0x161 THROUGH ADDRESS 0x163)

SPI Register 0x161 and SPI Register 0x163—Channel 1 and Channel 2 Rx Filter Power

This read only register holds the Rx1 and Rx2 power measured at the output of the RFIR filter or the HB1 filter in negative dBFS with steps of 0.25 dB/LSB. HB1 is used if the use HB1 output for decimate power measurement bit (Register 0x15C, Bit D6) is set.

Table 53. Power Word Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x161	Channel 1 Rx filter power	Channel 1 Rx filter power[7:0]									R
0x162	Open	Open									R
0x163	Channel 2 Rx filter power	Channel 2 Rx filter power[7:0]									R

Rx QUADRATURE CALIBRATION REGISTERS (ADDRESS 0x169 THROUGH ADDRESS 0x16B)

Table 54. Rx Quadrature Calibration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x169	Calibration Configuration 1	Enable phase correction	Enable gain correction	Must be 0		Free run mode	Enable correction word decimation	Enable tracking mode, Channel 2	Enable tracking mode, Channel 1	0xC0	R/W
0x16A	Must be 0x75	Must be 0x75								0x08	R/W
0x16B	Must be 0x95	Must be 0x95								0x08	

SPI Register 0x169—Calibration Configuration 1

Bit D7—Enable Phase Correction

This is a test bit that is normally set. Set this bit to enable phase correction.

Bit D6—Enable Gain Correction

This is a test bit that is normally set. Set this bit to enable gain correction.

Bits[D5:D4]—Must be 0

Bit D3—Free Run Mode

Set this bit when enabling tracking.

Bit D2—Enable Correction Word Decimation

Set this bit to decimate the correction word before applying it to the data.

Bit D1—Enable Tracking Mode, Channel 2

Set this bit to enable Rx quadrature tracking for Rx2.

Bit D0—Enable Tracking Mode, Channel 1

Set this bit to enable Rx quadrature tracking for Rx1

SPI Register 0x16A—Must be 0x75

SPI Register 0x16B—Must be 0x95

Rx PHASE AND GAIN CORRECTION REGISTERS (ADDRESS 0x170 THROUGH ADDRESS 0x182)

Table 55. Rx Phase and Gain Correction Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x170	Rx1A phase correction	Rx1A phase correction[7:0]									R/W
0x171	Rx1A gain correction	Rx1A gain correction[7:0]									R/W
0x172	Rx2A phase correction	Rx2A phase correction[7:0]									R/W
0x173	Rx2A gain correction	Rx2A gain correction[7:0]									R/W
0x174	Rx1A Q offset	Rx1A Q dc offset[7:0]									R/W
0x175	Rx1A offset	Rx1A I dc offset[5:0]						Rx1A Q dc offset[9:8]			R/W
0x176	Input A offsets	Rx2A Q dc offset[3:0]				Rx1A I dc offset[9:6]					R/W
0x177	Rx2A offset	Rx2A I dc offset[1:0]		RxA Q dc offset[9:4]							R/W
0x178	Rx2A I offset	Rx2A I dc offset[9:2]									R/W
0x179	Rx1B/Rx1C phase correction	Rx1B/Rx1C phase correction[7:0]									R/W
0x17A	Rx1B/Rx1C gain correction	Rx1B/Rx1C gain correction[7:0]									R/W
0x17B	Rx2B/Rx2C phase correction	Rx2B/Rx2C phase correction[7:0]									R/W
0x17C	Rx2B/Rx2C gain correction	Rx2B/Rx2C gain correction[7:0]									R/W
0x17D	Rx1B/Rx1C Q offset	Rx1B/Rx1C Q dc offset[7:0]									R/W
0x17E	Rx1B/Rx1C I offset	Rx1B/Rx1C I dc offset[5:0]						Rx1B/Rx1C Q dc offset[9:8]			R/W
0x17F	Input B/Input C offsets	Rx2B/Rx2C Q dc offset[3:0]				Rx2B/Rx2C I dc offset[9:6]					R/W
0x180	Rx2B/Rx2C offset	Rx2B/Rx2C I dc offset[1:0]		Rx2B/Rx2C Q dc offset[9:4]							R/W
0x181	Rx2B/Rx2C I offset	Rx2B/ Rx2C I dc offset[9:2]									R/W
0x182	Force bits	Rx2B/ Rx2C force offset	Rx1B/Rx1C force offset	Rx2B/ Rx2C force phase/ gain	Rx1B/ Rx1C force phase/ gain	Rx2A force offset	Rx1A force offset	Rx2A force phase/ gain	Rx1A force phase/gain	0x00	R/W

SPI Register 0x170—Rx1A Phase Correction

If Register 0x182, Bit D0 is clear, after an Rx quadrature calibration completes, this register holds the phase correction word for the Rx1A input in twos complement format. If Register 0x182, Bit D0 is set, the value written to this register is the forced phase correction word.

SPI Register 0x171—Rx1A Gain Correction

If Register 0x182, Bit D0 is clear, after an Rx quadrature calibration completes, this register holds the gain correction word for the Rx1A signal path in twos compliment format. If Register 0x182, Bit D0 is set, the value written to this register is the forced phase correction word.

SPI Register 0x172—Rx2A Phase Correction

This register functions the same as Register 0x170, but applies to Rx2. The force bit is Register 0x182, Bit D1.

SPI Register 0x173—Rx2A Gain Correction

This register functions the same as Register 0x171, but applies to Rx2. The force bit is Register 0x182, Bit D1.

SPI Register 0x174 and SPI Register 0x175, Bits[D1:D0]—Rx1A Q DC Offset

If Register 0x182, Bit D2 is clear, after an Rx quadrature calibration completes, these registers hold the Rx1A Q signal path dc offset correction word at the current gain index in twos complement format. If Register 0x182, Bit D2 is set, the value written to this register is the forced dc offset correction word.

SPI Register 0x175, Bits[D7:D2] and SPI Register 0x176, Bits[D3:D0]—Rx1A Offsets

These bits function the same as Register 0x174 and Register 0x175, Bits[D1:D0], but refer to the Rx1A I signal path. The force bit is Register 0x182, Bit D2.

SPI Register 0x176, Bits[D7:D4] and SPI Register 0x177, Bits[D5:D0]—Rx2A Q Offset

These bits function the same as Register 0x174 and Register 0x175. Bits[D1:D0], but refer to the Rx2A Q signal path. The force bit is Register 0x182, Bit D3.

SPI Register 0x177, Bits[D7:D6] and SPI Register 0x178, Bits[D7:D0]—Rx2A I Offset

These bits function the same as Register 0x174 and Register 0x175, Bits[D1:D0], but apply to the Rx2 I signal path. The force bit is Register 0x182, Bit D3.

SPI Register 0x179 Through SPI Register 0x181—Receiver B and Receiver C Inputs

These bits function the same as Register 0x170 through Register 0x178, but apply to the Receiver B and Receiver C LNA inputs. The force bits are Register 0x182, Bits[D7:D4].

SPI Register 0x182—Force Bits

These bits force the AD9363 to use the values in Register 0x170 through Register 0x181 as the Rx quadrature calibration correction words.

Rx DC OFFSET CONTROL REGISTERS (ADDRESS 0x185 THROUGH ADDRESS 0x194)

Table 56. Rx DC Offset Control Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x185	Wait count	Wait count[7:0]								0x10	R/W
0x186	RF dc offset count	RF dc offset count[7:0]								0xB4	R/W
0x187	RF DC Offset Configuration 1	Open		DAC full scale[1:0]		Must be 0x4				0x1C	R/W
0x188	RF dc offset attenuation	RF dc offset table update count[2:0]			RF dc offset attenuation[4:0]					0x05	R/W
0x189	Must be 0x30	Must be 0x30								0x30	R/W
0x18A	Open	Open								0xFF	R/W
0x18B	DC Offset Configuration 2	Must be 1	Enable fast settle mode	Enable baseband dc offset tracking	Reset accum-ulator on gain change	Enable RF offset tracking	DC offset update[2:0]			0x8D	R/W
0x18C	RF calibration gain index	Open	RF minimum calibration gain index[6:0]							0x00	R/W
0x18D	SOI Threshold	Open	RF SOI threshold[6:0]							0x64	R/W
0x18E	Open	Open								0x00	R/W
0x18F	Open	Open									R/W
0x190	Baseband dc offset shift	Must be 0	Baseband tracking decimate[1:0]		Baseband dc M shift[4:0]					0x0D	R/W
0x191	Baseband dc offset fast settle shift	Readback channel select	Update tracking word	Force Rx null	Baseband dc tracking fast settle M shift[4:0]					0x06	R/W
0x192	Baseband fast settle duration	Baseband dc tracking fast settle duration[7:0]								0x03	R/W
0x193	Baseband dc offset count	Must be 0x3F								0x3F	R/W
0x194	Baseband dc offset attenuation	Open				Baseband dc offset attenuation[3:0]				0x01	R/W

The AD9361_BB_DC_OFFSET_CALIB and the AD9361_RF_DC_OFFSET_CALIB functions configure the baseband dc and RF dc registers and run the calibrations.

SPI Register 0x185—Wait Count

This register sets the Rx path settling time delay after gain changes are made. All calibrations wait for this counter before starting calculations. CLKRF clocks the counter.

SPI Register 0x186—RF DC Offset Count

This register affects both RF dc offset initialization and tracking and it sets the number of integrated samples and the loop gain. The number of samples equals 256 × RF dc offset count[7:0] in CLKRF cycles. Increasing this value increases loop gain.

SPI Register 0x187—RF DC Offset Configuration 1

Bits[D5:D4]—DAC Full Scale[1:0]

These bits set the range of current injected by the correction DAC per Table 57. Increasing this value increases loop gain.

Table 57.DC Offset Correction Step Size

DAC Full Scale[1:0]	DC Offset Correction Step Size
00	Default range of offset correction DAC
01	2× range and step size of offset correction DAC
10	4× range and step size of offset correction DAC
11	8× range and step size of offset correction DAC

Bits[D3:D0]—Must be 0x4

SPI Register 0x188—RF DC Offset Attenuation

Bits[D7:D5]—RF DC Offset Table Update Count[2:0]

These bits determine the number of internal correction word table entries to update when a correction word is updated in the RF correction table. This occurs for the initial RF calibration and during tracking. The correction word at the current gain index, m, updates along with following gain indices: m + 1, m + 2 … m + n.

Bits[D4:D0]—RF DC Offset Attenuation[4:0]

These bits control the attenuator for the initialization and tracking RF dc offset calibrations. The integrated data shifts by this twos complement value and ranges from −16 to +15.

SPI Register 0x18B—DC Offset Configuration 2

Bit D7—Must be 1

Bit D6—Enable Fast Settle Mode

These bits apply to baseband dc offset tracking (Bit D5 is set). The algorithm uses the baseband dc tracking fast settle shift M attenuation value in Register 0x191 for the baseband fast settle duration time in Register 0x192, followed by the baseband dc M shift attenuation value in Register 0x190. The value in Register 0x190 is used until the gain changes, at which time this sequence repeats. If the fast settle attenuation value is lower than the other attenuation value, then the baseband dc tracking algorithm converges faster. Convergence that is too fast can affect subcarriers near dc.

Bit D5—Enable Baseband DC Offset Tracking

Set this bit to enable baseband dc offset tracking. Correction words apply at a rate set by the decimation setting (Register 0x190, Bits[D6:D5]).

Bit D4—Reset Accumulator on Gain Change

This bit applies if using baseband dc offset tracking (Bit D5 is set). When set, the dc offset accumulator clears when gain changes occur.

Bit D3—Enable RF Offset Tracking

Setting this bit enables RF dc offset tracking.

Bits[D2:D0]—DC Offset Update[2:0]

These bits specify when correction words apply during RF dc tracking, per Table 58. See Register 0x18D for the signal of interest (SOI) threshold.

Table 58. DC Offset Update Conditions

Bit D2	Bit D1	Bit D0
Gain change; apply a new tracking word when a gain change occurs	SOI threshold; apply a new tracking word when the received signal is less than the SOI threshold	Exit Rx mode; apply a new tracking word after the ENSM exits the Rx state

SPI Register 0x18C—RF Calibration Gain Index

This register sets the starting gain index for RF dc offset calibration. This 7-bit word represents the LNA gain (2 bits), the mixer gain (4 bits), and the TIA gain (1 bit).

SPI Register 0x18D—RF SOI Threshold

This register sets the SOI threshold in negative dBFS with 1 dB/LSB resolution. See Register 0x18B, Bit D1.

SPI Register 0x190—BB DC Offset Shift

Bit D7—Must be 0

Bits[D6:D5]—Baseband Tracking Decimation[1:0]

These bits apply in baseband dc offset tracking mode (Register 0x18B, Bit D5 is set). These bits set the correction word update rate per Table 59.

Table 59. Decimation in Baseband DC Offset Tracking Mode

Register 0x190, Bits[D6:D5]	Decimation	Update Rate
00	No decimation	CLKRF
01	Decimate by 2	CLKRF/2
10	Decimate by 4	CLKRF/4

Bits[D4:D0]—Baseband DC Shift M[4:0]

These bits apply to baseband dc tracking mode (Register 0x18B, Bit D5 is set). These bits determine the loop gain attenuation. The integrated data shifts by baseband dc M shift + 1. M ranges from 1 to 32.

SPI Register 0x191—BB DC Offset Fast Settle Shift

Bit D7—Read Back Channel Select

Set this bit to read back Rx1 baseband dc tracking correction words in Register 0x1A2 through Register 0x1A5. Clear this bit to read Rx2 words. See Bit D6.

Bit D6—Update Tracking Words

Toggle this bit to copy the current baseband dc tracking words to Register 0x1A2 through Register 0x1A5. Correction word updates occur quickly; therefore, these words are not copied to the SPI registers unless this bit transitions high, preventing the words from changing during the SPI read. The bit is not self clearing.

Bit D5—Force Rx Null

This is a test bit. Setting this bit grounds the input to the LPF.

Bits[D4:D0]—Baseband DC Tracking Fast Settle Shift M[4:0]

These bits apply in baseband dc fast settle tracking mode (Register 0x18B, Bits[D5:D6] are set). The range is 1 through 32.

SPI Register 0x192—BB Tracking Fast Settle Duration

This register applies to baseband dc fast settle tracking mode (Register 0x18B, Bits[D6:D5] are set). These bits set the fast settle M shift duration. See Register 0x18B, Bit D6. The total time is this register value × 8 and is measured in CLKRF cycles.

SPI Register 0x193—Must be 0x3F

SPI Register 0x194—Baseband DC Offset Attenuation

Bits[D3:D0]—Baseband DC Offset Attenuation[3:0]

These bits set the baseband dc offset loop gain attenuation during the initial calibration. The range is +7 to −8.

Rx BASEBAND DC OFFSET REGISTERS (ADDRESS 0x19A THROUGH ADDRESS 0x1A5)

SPI Register 0x19A through SPI Register 0x19D—Rx1 Baseband DC I/Q Words

These registers are the Rx1 baseband dc offset I/Q correction words. During calibration, correction words are calculated for different LPF gains. The words read back in these registers are the correction words corresponding to the current LPF gain index.

SPI Register 0x19E through SPI Register 0x1A1—Rx2 Baseband DC I/Q Words

These registers function the same as Register 0x19A through Register 0x19D, but apply to Rx2.

SPI Registers 0x1A2 through SPI Register 0x1A5—Rx1/Rx2 Baseband Tracking Correction I/Q Words

These registers are the baseband dc offset tracking I/Q correction words. When the read back channel select bit (Register 0x191, Bit 7) is set, the words correspond to Rx1; otherwise, they correspond to Rx2. Register 0x191, Bit 6 must transition high to load the latest tracking words into these registers.

Table 60. Rx Baseband DC Offset Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x19A	Rx1 Baseband DC Word I MSB	Open	Rx1 Baseband DC Offset Correction Word I[14:8]								R
0x19B	Rx1 Baseband DC Word I LSB	Rx1 Baseband DC Offset Correction Word I[7:0]									R
0x19C	Rx1 Baseband DC Word Q MSB	Open	Rx1 Baseband DC Offset Correction Word Q[14:8]								R
0x19D	Rx1 baseband DC Word Q LSB	Rx1 Baseband DC Offset Correction Word Q[7:0]									R
0x19E	Rx2 Baseband DC Word I MSB	Open	Rx2 Baseband DC Offset Correction Word I[14:8]								R
0x19F	Rx2 Baseband DC Word I LSB	Rx2 Baseband DC Offset Correction Word I[7:0]									R
0x1A0	Rx2 Baseband DC Word Q MSB	Open	Rx2 Baseband DC Offset Correction Word Q[14:8]								R
0x1A1	Rx2 Baseband DC Word Q LSB	Rx2 Baseband DC Offset Correction Word Q[7:0]									R
0x1A2	Baseband Track Correction Word I MSB	Open	Rx1/Rx2 Baseband DC Offset Tracking Correction Word I[14:8]								R
0x1A3	Baseband Track Correction Word I LSB	Rx1/Rx2 Baseband DC Offset Tracking Correction Word I[7:0]									R
0x1A4	Baseband Track Correction Word Q MSB	Open	Rx1/Rx2 Baseband DC Offset Tracking Correction Word Q[14:8]								R
0x1A5	Baseband Track Correction Word Q LSB	Rx1/Rx2 Baseband DC Offset Tracking Correction Word Q[7:0]									R

RSSI READBACK REGISTERS (ADDRESS 0x1A7 THROUGH ADDRESS 0x1AC)

Table 61. RSSI Readback Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x1A7	Rx1 RSSI symbol	Rx1 RSSI symbol[8:1]									R
0x1A8	Rx1 RSSI preamble	Rx1 RSSI preamble[8:1]									R
0x1A9	Rx2 RSSI symbol	Rx2 RSSI symbol[8:1]									R
0x1AA	Rx2 RSSI preamble	Rx2 RSSI preamble[8:1]									R
0x1AB	Symbol LSB	Open						Rx2 RSSI symbol[0]	Rx1 RSSI symbol[0]		R
0x1AC	Preamble LSB	Open						Rx2 RSSI preamble[0]	Rx1 RSSI preamble[0]		R

The AD9361_GET_RX_RSSI function reads the RSSI words.

SPI Register 0x1A7 and Register 0x1AB, Bit D0—Rx1 RSSI Symbol

This register updates after every measurement interval. The typical valid range is 0 to 457 (decimal) (for 9 bits). The resolution is 0.25 dB/LSB for 9 bits and 0.5 dB/LSB for 8 bits. The RSSI compensates for Rx gain.

SPI Register 0x1A8 and Register 0x1AC, Bit D0—Rx1 RSSI Preamble

This register updates once after the event set in Register 0x158, Bits[D4:D2], with the exception that it does not update after gain changes. The typical valid range is 0 to 457 (decimal) (for 9 bits). The resolution is 0.25 dB/LSB for 9 bits and 0.5 dB for 8 bits. The RSSI compensates for Rx gain.

SPI Register 0x1A9 and SPI Register 0x1AB, Bit D1—Rx2 RSSI Symbol

These registers function the same as Register 0x1A7 and Register 0x1AB, Bit D0, but apply to Rx2.

SPI Register 0x1AA and SPI Register 0x1AC, Bit D1—Rx2 RSSI Preamble

These registers function the same as Register 0x1A8 and Register 0x1AC, Bit D0, but apply to Rx2.

Rx TIA REGISTERS (ADDRESS 0x1DB THROUGH ADDRESS 0x1DF)

Table 62. Rx TIA Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x1DB	Rx TIA configuration	TIA select C_C[2:0]			Open	TIA 2 Override C	TIA 2 Override R	TIA 1 Override C	TIA 1 Override R	0x60	R/W
0x1DC	TIA 1 C LSB	TIA 1 RF[1:0]			TIA 1 C LSB[5:0]					0x03	R/W
0x1DD	TIA 1 C MSB	Open	TIA 1 C MSB[6:0]							0x0B	R/W
0x1DE	TIA 2 C LSB	TIA 2 RF[1:0]			TIA 2 C LSB[5:0]					0x03	R/W
0x1DF	TIA 2 C MSB	Open	TIA 2 C MSB[6:0]							0x0B	R/W

The AD9361_SET_RX_RF_BANDWIDTH function configures these registers.

SPI Register 0x1DB—Rx TIA Configuration

Bits[D7:D5]—TIA Select C_C[2:0]

These bits must be set per Table 63.

Table 63. TIA Select C_C

Baseband (Real) Bandwidth (BBBW)	TIA Select C_C[2:0]
BBBW ≤ 3 MHz	7
3 MHz < BBBW < 10 MHz	3
BBBW ≥ 10 MHz	1

Bit D3—TIA 2 Override C

This is a test bit. Override the digital control of the Rx2 TIA feedback capacitors with TIA 2 C LSB and TIA 2 C MSB.

Bit D2—TIA 2 Override R

This is a test bit. Override digital control of the Rx2 TIA feedback resistor with TIA 2 RF[1:0].

Bit D1—TIA 1 Override C

This is a test bit. This bit functions the same as Bit D3, but applies to Rx1.

Bit D0—TIA 1 Override R

This is a test bit. This bit functions the same as Bit D2, but applies to Rx1.

SPI Register 0x1DC—TIA C LSB

Bits[D7:D6]—TIA 1 RF[1:0]

These bits set the value of the feedback resistor in the Rx1 TIA per Table 64. TIA 1 Override R is set (Register 0x1DB, Bit D0).

Table 64. TIA Forced Feedback Resistor Value

TIA RF[1:0]	R_{TIA} (kΩ)	Gain (dB)
01	3.50	0
11	1.75	−6

Bits[D5:D0]—TIA C LSB[5:0] and Register 0x1DD

Sets value of the feedback capacitor.

SPI Register 0x1DE and SPI Register 0x1DF

These registers function the same as Register 0x1DC and Register 0x1DD, but apply to Rx2. The override bit for the Rx2 feedback resistor is Register 0x1DB, Bit D2.

Rx BASEBAND FILTER (BBF) REGISTERS (ADDRESS 0x1E0 THROUGH ADDRESS 0x1F5)

Table 65. Rx BBF Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x1E0	Rx1 BBF R1A	Force Rx1 resistors	Open	Rx1 BBF R1A[5:0]						0x03	R/W
0x1E1	Rx2 BBF R1A	Force Rx2 resistors	Open	Rx2 BBF R1A[5:0]						0x03	R/W
0x1E2	Rx1 tune control	Open					Must be 0	Must be 1	Rx1 phase detector tune	0x00	R/W
0x1E3	Rx2 tune control	Open					Must be 0	Must be 1	Rx2 phase detector tune	0x00	R/W
0x1E4	Rx1 BBF R5	Rx1 BBF R5[7:0]								0x01	R/W
0x1E5	Rx2 BBF R5	Rx2 BBF R5[7:0]								0x01	R/W
0x1E6	Rx BBF R2346	Tune override	Open				Rx BBF R2346[2:0]			0x01	R/W
0x1E7	Rx BBF C1 MSB	Open		Rx BBF C1 MSB[5:0]						0x00	R/W
0x1E8	Rx BBF C1 LSB	Open	Rx BBF C1 LSB[6:0]							0x60	R/W
0x1E9	Rx BBF C2 MSB	Open		Rx BBF C2 MSB[5:0]						0x00	R/W
0x1EA	Rx BBF C2 LSB	Open	Rx BBF C2 LSB[6:0]							0x60	R/W
0x1EB	Rx BBF C3 MSB	Open		Rx BBF C3 MSB[5:0]						0x00	R/W
0x1EC	Rx BBF C3 LSB	Open	Rx BBF C3 LSB[6:0]							0x60	R/W
0x1ED	Rx BBF CC1 control	Open	Rx BBF CC1 control[6:0]							0x07	R/W
0x1EE	Must be 0x60	Must be 0x60								0x60	R/W
0x1EF	Rx BBF C_C2 control	Open	Rx BBF C_C2 control[6:0]							0x07	R/W
0x1F0	Rx BBF Power R_Z Byte 1	Rx BBF Power 3 control[1:0]		Rx BBF R_Z3 control[1:0]		Rx BBF Power 2 control[1:0]		Rx BBF R_Z2 control[1:0]		0xCC	R/W
0x1F1	Rx BBF C_C3 control	Open	Rx BBF C_C3 control[6:0]							0x07	R/W
0x1F2	Rx BBF R5 tune	Rx BBF R5 tune[7:0]								0x00	R/W
0x1F3	Rx BBF tune	Must be 0	Must be 2'b01		Rx BBF R5 tune	Open				0x20	R/W
0x1F4	Rx1 BBF manual gain	Open		Rx1 BBF force gain	Rx1 BBF biquad gain[1:0]		Rx1 BBF pole gain[2:0]			0x00	R/W
0x1F5	Rx2 BBF manual gain	Open		Rx2 BBF force gain	Rx2 BBF biquad gain[1:0]		Rx2 BBF pole gain[2:0]			0x00	R/W

The AD9361_SET_RX_RF_BANDWIDTH function configures these registers for the correct filter corner based on the RF bandwidth.

SPI Register 0x1E0—Rx1 BBF R1A

Bit D7—Force Rx1 Resistors

This is a test bit and is normally cleared. Setting this bit forces the use of the resistor register values.

Bits[D5:D0]—Rx1 BBF R1A[5:0]

This register, in combination with R4 (Register 0x1E6), sets the biquad signal gain (R4/R1A = A_V).

SPI Register 0x1E1—Rx2 BBF R1A

This register is the same as Register 0x1E0, but applies to Rx2.

SPI Register 0x1E2—Rx1 Tune Control

Bit D2—Must be 0

Bit D1—Must be 1

Bit D0—Rx1 Phase Detector Tune

Clear this bit before starting a baseband filter calibration. Set the bit after the calibration completes.

SPI Register 0x1E3—Rx2 Tune Control

This register is the same as Register 0x1E2, but applies to Rx2.

SPI Register 0x1E4—Rx1 BBF R5

This register, along with R6 (Register 0x1E6), controls the pole signal gain (R6/F5 = A_V). If this register is nonzero, Register 0x1F2 must be zero.

SPI Register 0x1E5—Rx2 BBF R5

This register is the same as Register 0x1E4, but applies to Rx2.

SPI Register 0x1E6—Rx BBF R2346

Bit D7—Tune Override

This bit is normally clear. Setting this bit overrides the calibration values, forcing the filter to use the R2346 value and all capacitor words.

Bits[D2:D0]—Rx BBF R2346

These bits control the value of the R2, R3, R4, and R6 resistors.

SPI Register 0x1E7 and SPI Register 0x1E9—Rx BBF C1 and Rx BBF C2 MSB

These bits affect the C1 and C2 BBF capacitors. Typically, both registers, along with Register 0x1EB, use the same word.

SPI Register 0x1E8 and SPI Register 0x1EA—Rx BBF C1 and Rx BBF C2 LSB

These bits affect the C1 and C2 BBF capacitors. Typically, both registers, along with Register 0x1EC, use the same word.

SPI Register 0x1EB—Rx BBF C3 MSB

These bits affect the C3 BBF capacitor. This register is typically equal to Register 0x1E7 and Register 0x1E9.

SPI Register 0x1EC—Rx BBF C3 LSB

These bits affect the C3 BBF capacitor. This register is typically equal to Register 0x1E8 and Register 0x1EA.

SPI Register 0x1ED—Rx BBF CC1 Control

These bits control the Miller compensation capacitor for Op Amp 1.

SPI Register 0x1EE—Must be 0x60

SPI Register 0x1EF—Rx BBF C_C2 Control

This register is the same as Register 0x1ED, but applies to Op Amp 2.

SPI Register 0x1F0—Rx BBF Power R_Z Byte1

Bits[D7:D6]—Rx BBF Power 3 Control[1:0]

These bits are the Op Amp 3 power control.

Bits[D5:D4]—Rx BBF R_Z3 Control[1:0]

These bits control the Op Amp 3 zero compensation resistor.

Bits[D3:D2]—Rx BBF Power 2 Control[1:0]

These bits are the Op Amp 2 power control.

Bits[D1:D0]—Rx BBF R_Z2 Control[1:0]

These bits control the Op Amp 2 zero compensation resistor.

SPI Register 0x1F1—Rx BBF C_C3 Control

Same as Register 0x1ED, but applies to Op Amp 3.

SPI Register 0x1F2—Rx BBF R5 Tune

This register, along with the value of R6 (Register 0x1E6), sets the pole signal gain during calibration. If this is nonzero, Register 0x1E4 and Register 0x1E5 must be all zeros.

SPI Register 0x1F3—Rx BBF Tune

Bit D7—Must be 0

Bits[D6:D5]—Must be 2'b01

Bit D4—Rx BBF R5 Tune

Setting this bit forces the value in Register 0x1F2 to be used for tuning.

SPI Register 0x1F4 and SPI Register 0x1F5—Rx1/Rx2 BBF Man Gain

Bit D5—Rx BBF Force Gain

This bit forces the values in the lower bits to be used for the biquad and pole gain.

Bits[D4:D3]—Rx BBF Biquad Gain[1:0]

These bits are only applicable if Bit D5 is set. These bits force the biquad gain.

Bits[D2:D0]—Rx BBF Pole Gain[1:0]

These bits are only applicable if Bit D5 is set. These bits force the pole gain.

Rx BBF TUNER CONFIGURATION REGISTERS (ADDRESS 0x1F8 THROUGH ADDRESS 0x1FC)

Table 66. Rx BBF Tuner Configuration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x1F8	Rx BBF tune divide	Rx BBF tune divide[7:0]								0x14	R/W
0x1F9	Rx BBF tune configuration	Open	Must be 2'b00		Rx tune evaluation time	Must be 3'b111			Rx BBF tune divide[8]	0x1E	R/W
0x1FA	Must be 0x01	Must be 0x01								0x01	R/W
0x1FB	Rx BBBW MHz	Open			Rx tune BBBW MHz[4:0]					0x05	R/W
0x1FC	Rx BBBW kHz	Open	Rx tune BBBW kHz[6:0]							0x00	R/W

The AD9361_SET_RX_RF_BANDWIDTH function configures these registers for the correct filter corner based on the RF bandwidth.

SPI Register 0x1F8 and SPI Register 0x1F9, Bit D0—Rx BBF Tune Divide

The tuning algorithm generates a tune clock derived from the BB PLL frequency. This register sets a divider that outputs the tune clock, set per Equation 22. See the AD9363 Reference Manual for more information about the tune clock used for the calibration algorithm.

$$Rx\ BBF\ Tune\ Divide[8:0] = \text{ceil}\left(\frac{BB\ PLL\ Frequency \times \ln(2)}{BBBW \times 1.4 \times 2 \times \pi}\right) \quad (22)$$

The range of the divider is 1 to 511.

SPI Register 0x1F9—Rx BBF Tune Configuration

Bits[D6:D5]—Must be 2'b00

Bit D4—Rx Tune Evaluation Time

This bit sets the delay in tune clock cycles (set by the divider described previously) before the tune comparator outputs can be sampled; 0 = 16 cycles and 1 = 32 cycles.

Bits[D3:D1]—Must be 3'b111

SPI Register 0x1FA—Must be 0x01

SPI Register 0x1FB—Rx BBBW MHz

Program this register with the floor of the baseband bandwidth in MHz to set the R_Z and C_C of the filter. For example, if the channel (RF) bandwidth = 10 MHz, Rx BBBW MHz = floor(10/2) = 5 MHz. the range is from 0 MHz to 31 MHz. the resolution is 1 MHz/LSB.

SPI Register 0x1FC—Rx BBBW kHz

The BBP must program this register per Equation 23.

$$Rx\ Tune\ BBBW\ (\text{kHz}),\ Bits[6:0] = \text{round}\left(\frac{(BBBW - \text{floor}(BBBW)) \times 1000}{7.8125}\right) \quad (23)$$

Rx ANALOG REGISTERS

Rx SYNTHESIZER REGISTERS (ADDRESS 0x230 THROUGH ADDRESS 0x251)

Table 67. Rx Synthesizer Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x230	Disable VCO calibration	Must be 0x5				Must be 3'b010			Disable VCO calibration	0x54	R/W
0x231	Integer Byte 0	Synthesizer integer word[7:0]								0x00	R/W
0x232	Integer Byte 1	SDM bypass	SDM power-down	Open			Synthesizer integer word[10:8]			0x00	R/W
0x233	Fractional Byte 0	Synthesizer fractional word[7:0]								0x00	R/W
0x234	Fractional Byte 1	Synthesizer fractional word[15:8]								0x00	R/W
0x235	Fractional Byte 2	Open	Synthesizer fractional word[22:16]							0x00	R/W
0x236	Force ALC	Force ALC enable	Force ALC word[6:0]							0x00	R/W
0x237	Force VCO Tune 0	Force VCO tune[7:0]								0x00	R/W
0x238	Force VCO Tune 1	Must be 0						Force VCO tune enable	Force VCO tune[8]	0x00	R/W
0x239	ALC/varactor	Initial ALC value[3:0]				VCO varactor[3:0]				0x82	R/W
0x23A	VCO output	Open	$\overline{\text{POR}}$ VCO	Open		VCO output level[3:0]				0x0A	R/W
0x23B	Charge pump current	Set to 1	V_{TUNE} output	Charge pump current[5:0]						0x00	R/W
0x23C	Charge pump offset	Synthesizer recalib-ration	Open	Charge pump offset[5:0]						0x00	R/W
0x23D	Charge pump configuration	Must be 0	Dither mode	Open	Charge pump offset off	Force charge pump calibration	Charge pump calibration enable	Must be 2'b00		0x80	R/W
0x23E	Loop Filter 1	Loop Filter C2[3:0]				Loop Filter C1[3:0]				0x00	R/W
0x23F	Loop Filter 2	Loop Filter R1[3:0]				Loop Filter C3[3:0]				0x00	R/W
0x240	Loop Filter 3	Loop Filter Bypass R3	Loop Filter Bypass R1	Loop Filter Bypass C2	Loop Filter Bypass C1	Loop Filter R3[3:0]				0x00	R/W
0x241	Dither/charge pump calibration	Number SDM dither bits[3:0]				Forced charge pump calibration word[3:0]				0x00	R/W
0x242	VCO Bias 1	Open	Must be 0		VCO bias temperature coefficient[1:0]		VCO bias reference[2:0]			0x04	R/W
0x243	Must be 0x0D	Must be 0x0D								0x0D	R/W
0x244	Calibration status	Charge pump calibration valid	Open	Charge pump calibration done	VCO calibration busy	Charge pump calibration word[3:0]					R
0x245	Must be 0x00	Must be 0x00								0x00	R/W
0x246	Set to 0x02	Set to 0x02								0x00	R/W
0x247	Charge pump overage/VCO lock	Charge pump overage high	Charge pump overage low	Open				Rx PLL lock	Open		R
0x248	Set to 0x0B	Set to 0x0B								0x07	R/W
0x249	VCO calibration	Set to 1	Must be 3'b000			VCO calibration count[1:0]		Must be 2'b10		0x02	R/W
0x24A	Lock detect configuration	Open				Lock detect count[1:0]		Lock detect mode[1:0]		0x02	R/W
0x24B	Must be 0x17	Must be 0x17								0x17	R/W
0x24C	Must be 0x00	Must be 0								0x00	R/W
0x24D	Must be 0x00	Must be 0								0x00	R/W
0x24E	Open	Open								0x00	R/W

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x24F	Open	Open								0x00	R/W
0x250	Set to 0x70	Set to 0x70								0x63	R/W
0x251	VCO Varactor Control 1	Open				VCO varactor reference[3:0]				0x08	R/W

The AD9361_TXRX_SYNTH_CP_CALIB function sets up all registers in this section. See the AD9363 Reference Manual for more details.

SPI Register 0x230—Disable VCO Calibration

Bits[D7:D4]—Must be 0x5

Bits[D3:D1]—Must be 3'b010

Bit D0—Disable VCO Calibration

Set this bit to prevent a VCO calibration when the integer frequency word changes or when the ENSM changes from the Tx state to the alert state when the ENSM is in TDD mode. BitD0 in Register 0x270 prevents a VCO calibration when the ENSM moves from the Rx state to the alert state.

SPI Register 0x231, SPI Register 0x232, Bits[D2:D0], and SPI Register 0x233 Through SPI Register 0x235—VCO Frequency Words

These words set the VCO frequency, which ranges from 6 GHz to 12 GHz. The dividers in Register 0x005 divide this frequency down to the final LO frequency required by the application between 325 MHz to 3.8 GHz.

Equation 24 and Equation 25 derive the integer and fractional words. All frequencies must use the same units (for example, MHz).

$$N_{Integer} = \text{floor}\left(\frac{f_{RF\ PLL}}{f_{REF}}\right) \quad (24)$$

$$N_{Fractional} = \text{round}\left(8{,}388{,}593 \times \left(\frac{f_{RF\ PLL}}{f_{REF}} - N_{Integer}\right)\right) \quad (25)$$

where:
$N_{Integer}$ is the 11-bit integer word programmed in Register 0x231 and Register 0x232.
f_{REF} is the reference clock frequency (external). This rate is after the reference divider in Register 0x2AB, Bit D0 and Register 0x2AC, Bit D7.
$N_{Fractional}$ is the 23-bit fractional word programmed in Register 0x233 through Register 0x235.

SPI Register 0x232

Bit D7—SDM Bypass

Test bit, normally cleared. Setting this bit bypasses the SDM of the Rx RFPLL.

Bit D6—SDM Power-Down

This is a test bit and is normally cleared. Setting this bit disables the Rx RF PLL SDM.

SPI Register 0x236—Force ALC

Bit D7—Force ALC Enable

Setting this bit forces the automatic level control to use the force word in Bits[D6:D0] instead of the word generated during calibration. This bit is set when using the fast lock feature of the VCO. See Register 0x25A through Register 0x25F.

Bits[D6:D0]—Force ALC Word[6:0]

After a VCO calibration, these bits hold the resulting VCO amplitude word.

SPI Register 0x237—Force VCO Tune 0

After a VCO calibration, this register holds the lower 8 bits of the VCO capacitor word. This register can also be used in a test mode to force the capacitor word if the force VCO tune enable bit (Register 0x238, Bit D1) is set. The AD9363 sets this register automatically when using the fast lock feature.

SPI Register 0x238—Force VCO Tune 1

Bits[D7:D2]—Must be 0

Bit D1—Force VCO Tune Enable

Setting this bit forces the VCO to use the force word in Register 0x237 and Register 0x238, Bit D0 instead of the word it generates during calibration. This bit is set when using the fast lock feature of the VCO. See Register 0x25A through Register 0x25F.

Bit D0—Force VCO Tune[8]

This bit is the most significant bit of the VCO capacitor tune word. See Register 0x237.

SPI Register 0x239—ALC/Varactor

Bits[D7:D4]—Initial ALC Value[3:0]

These bits set the initial ALC value (VCO bias DAC setting) when running a VCO calibration.

Bits[D3:D0]—VCO Varactor[3:0]

These bits set the varactor size that sets the VCO gain (K_V). A higher register value equals a higher K_V. The total varactor value (Register 0x239, Bits[D3:D0] + Register 0x251, Bits[D3:D0]) must be 15 (decimal) or less. See Register 0x251 for other restrictions on the setting of these bits.

SPI Register 0x23A—VCO Output

Bit D6—Power-On Reset ($\overline{\text{POR}}$)

Clearing this bit resets the VCO calibration logic. Clear this bit before running the VCO calibration.

Bits[D3:D0]—VCO Output Level[3:0]

These bits set the VCO output voltage level that sets the VCO phase noise performance and power consumption. The range is 0.5 V to 1.5 V, and the step size is 67 mV.

SPI Register 0x23B—Charge Pump Current

Bit D7—Set to 1

Bit D6—V_{TUNE} Output

This is a test mode bit and is normally clear. If set, the AD9363 outputs V_{TUNE} on the external Rx LO pin. This pin is normally an input but if this bit is set, it is an output.

Bits[D5:D0]—Charge Pump Current[5:0]

These bits set the charge pump current. Range: 0.1 mA to 6.4 mA, resolution = 100 µA/LSB.

SPI Register 0x23C—Charge Pump Offset

Bit D7—Synthesizer Recalibration

Setting this self clearing bit forces the charge pump to recalibrate either the next time the synthesizer powers up, or when the charge pump calibration enable bit (Register 0x23D, Bit D2) is cleared and then set. Clear this bit for normal operation.

Bits[D5:D0]—Charge Pump Offset[5:0]

These bits only apply if the charge pump offset off bit (Register 0x23D, Bit D4) is cleared. These bits set the charge pump bleed current. The step size is 12.5 µA/LSB with a range of 0 µA to 787.5 µA.

SPI Register 0x23D—Charge Pump Configuration

Bit D7—Must be 0

Bit D6—Dither Mode

This bit determines the pseudorandom binary sequency (PRBS) length. When this bit is clear, the PRBS is 17 bits long. When this bit is set, the PRBS is 23 bits long.

Bit D4—Charge Pump Offset Off

Setting this bit disables the charge pump bleed current. Clear to use the value in the charge pump offset bits (Register 0x23C, Bits[D5:D0]) as the offset current.

Bit D3—Force Charge Pump Calibration

Setting this bit overrides the calibration result with the value in Register 0x241, Bits[D3:D0]. In this case, the charge pump calibration word in Register 0x244, Bits[D3:D0] reflects the value in Register 0x241, Bits[D3:D0]. Clear this bit for normal operation.

Bit D2—Charge Pump Calibration Enable

Set this bit to start the charge pump calibration. When this bit is clear, the charge pump does not calibrate.

SPI Register 0x23E—Loop Filter 1

Bits[D7:D4]—Loop Filter C2[3:0]

These bits set the second pole loop filter capacitor.

Bits[D3:D0]—Loop Filter C1[3:0]

These bits set the capacitor for the loop filter.

SPI Register 0x23F—Loop Filter 2

Bits[D7:D4]—Loop Filter R1[3:0]

These bits set the resistor value for the loop filter zero. There are 16 resistors in parallel. The range is 8.68 kΩ to 543 Ω (all resistors in parallel with the bits set to zero). Setting the Loop Filter Bypass R1 bit (Register 0x240, Bit D6) shorts R1.

Bits[D3:D0]—Loop Filter C3[3:0]

These bits set the third pole loop filter capacitor. The range is 2.86 pF to 47.4 pF; the resolution is 2.86 pF at 27°C.

SPI Register 0x240—Loop Filter 3

Bit D7—Loop Filter Bypass R3

Setting this bit bypasses R3 of the loop filter. See Bits[D3:D0].

Bit D6—Loop Filter Bypass R1

Setting this bit bypasses R1 of the loop filter. See Register 0x23F, Bits[D7:D4].

Bit D5—Loop Filter Bypass C2

See Register 0x23E, Bits[D7:D4]. Setting this bit shorts out an additional LSB of C2.

Bit D4—Loop Filter Bypass C1

See Register 0x23E, Bits[D3:D0]. Setting this bit shorts out an additional LSB of C1.

Bits[D3:D0]—Loop Filter R3[3:0]

These bits set the third pole loop filter resistor. There are 16 resistors in parallel. The range is 2.79 kΩ to 174 Ω (all resistors in parallel with all bits set to zero). Setting the Loop Filter Bypass R3 bit (Register 0x240, Bit D7) bit shorts R3.

SPI Register 0x241—Dither/Charge Pump Calibration

Bits[D7:D4]—Number of Dither Bits[3:0]

These bits set the number of dither bits added to the 23-bit fractional synthesizer word. The range is 0 to 15.

Bits[D3:D0]—Forced Charge Pump Calibration Word[3:0]

Writing this nibble overwrites the charge pump calibration word if the force charge pump calibration bit in Register 0x23D, Bit D3 is set.

SPI Register 0x242—VCO Bias 1

Bits[D6:D5]—Must be 0

Bits[D4:D3]—VCO Bias Temperature Coefficient[1:0]

These bits control the VCO bias DAC temperature coefficient.

Bits[D2:D0]—VCO Bias Reference[2:0]

These bits control the VCO bias reference DAC. The range is 50 μA to 400 μA; the resolution is 50 μA.

SPI Register 0x243—Must be 0x0D

SPI Register 0x244—Calibration Status

Bit D7—Charge Pump Calibration Valid

This bit is set after a successful charge pump calibration, remains set, and another charge pump calibration does not begin, even if the Rx RF PLL powers down. This bit clears if the charge pump calibration enable bit in Register 0x23D, Bit D2 goes low or if the force charge pump calibration bit in Register 0x23D, Bit D3 goes high.

Bit D5—Charge Pump Calibration Done

This bit set indicates that a charge pump calibration is successful. This bit clears when the Rx PLL powers down, such as occurs in TDD mode.

Bit D4—VCO Calibration Busy

This bit set indicates that a VCO calibration is running.

Bits[D3:D0]—Charge Pump Calibration Word[3:0]

These bits are the charge pump calibration result. If the force charge pump calibration bit (Register 0x23D, Bit D3) is set, then these bits are forced by the forced charge pump calibration word in Register 0x241, Bits[D3:D0].

SPI Register 0x245—Must be 0x00

SPI Register 0x246—Must be 0x02

SPI Register 0x247—Charge Pump Overage/VCO Lock

Bit D7—Charge Pump Overage High

This bit applies if Register 0x24B, Bit D6 is clear. If this bit is set, the charge pump output is above the value in Register 0x24B.

Bit D6—Charge Pump Overage Low

This bit applies if Register 0x24B, Bit D6 is clear. If set, the charge pump output is below the value in Register 0x24B.

Bit D1—Rx PLL Lock

This bit applies if Register 0x24A, Bits[D1:D0] = 2'b01 or 2'b10. If set, the synthesizer locked in the number of clock cycles set by the lock detect count bits (Register 0x24A, Bits[D3:D2]).

SPI Register 0x248—Must be 0x0B

SPI Register 0x249—VCO Calibration

Bit D7—Set to 1

Bits[D6:D4]—Must be 3'b000

Bits[D3:D2]—VCO Calibration Count[1:0]

These bits set the VCO frequency calibration counter length (00 = 128, 01 = 256, 10 = 512, and 11 = 1024).

Bits[D1:D0]—Must be 2'b10

SPI Register 0x24A—Lock Detect Configuration

Bits[D3:D2]—Lock Detect Count[1:0]

If the RF PLL locks within the specified time, the Rx PLL lock bit (Register 0x247, Bit D1) goes high. The time is measured in reference clock cycles per Table 68.

Table 68.Lock Detect Count

Lock Detect Count[1:0]	Reference Clock Cycles
00	256
01	512
10	1024
11	2048

Bits[D1:D0]—Lock Detect Mode[1:0]

These bits set the lock detect mode of operation per Table 69.

Table 69. RF PLL Lock Detect Mode

Lock Detect Mode[1:0]	RF PLL Lock Detect Mode
00	Disable lock detect
01	Run lock detect once, when RF PLL is enabled
10	Run lock detect continuously
11	Do not use

SPI Register 0x24B—Must be 0x17

SPI Register 0x24C—Must be 0

SPI Register 0x24D—Must be 0

SPI Register 0x250—Must be 0x70

SPI Register 0x251—VCO Varactor Control 1

These bits set the number of varactors connected to the VCO varactor reference voltage. There are four ports. See Table 70 for example valid settings. It is never valid to set the same bit in both words (Register 0x239, Bits[D3:D0] and Register 0x251, Bits[D3:D0]).

Table 70.VCO Varactor Connections

Register 0x239, Bits[D3:D0]	Register 0x251, Bits[D3:D0]
0000	0000
0001	0000
0010	0001

Rx FAST LOCK REGISTERS (ADDRESS 0x25A THROUGH ADDRESS 0x25F)

Table 71. Rx Fast Lock Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x25A	Rx fast lock setup	Rx fast lock profile[2:0]			Open	Rx fast lock load synthesizer	Rx fast lock profile initialize	Rx fast lock profile pin select	Rx fast lock mode enable	0x00	R/W
0x25B	Rx fast lock setup initial delay	Rx fast lock initial delay[7:0]								0x00	R/W
0x25C	Rx fast lock program address	Rx fast lock program address[7:0]									R/W
0x25D	Rx fast lock program data	Rx fast lock program data[7:0]									R/W
0x25E	Rx fast lock program read	Rx fast lock program read data[7:0]									R
0x25F	Rx fast lock program control	Open						Rx fast lock program write	Rx fast lock program clock enable	0x00	R/W

The Linux and No-OS drivers contain functions for setting up and using the fast lock function. See the AD9363 Reference Manual for more information and function names.

SPI Register 0x25A—Rx Fast Lock Setup

Bits[D7:D5]—Rx Fast Lock Profile[2:0]

These bits are ignored if Bit D1 is set. These bits select the profile number (0 to 7) when creating or using a profile.

Bit D3—Rx Fast Lock Load Synthesizer

Setting this bit forces a VCO calibration. After calibration completes, the AD9363 saves the resulting calibration words and then this bit self clears. This is only valid when Bit D0 and Bit D2 are set. If the VCO tune and VCO ALC words entries are written manually into the profile along with the other parameters, then it is not necessary to set this bit and run a VCO calibration.

Bit D2—Rx Fast Lock Profile Initialize

Set this bit when creating a profile. This bit set allows the calibrated VCO values to be saved to a specific profile. To create more than one profile, this bit must be set low and then high again. This bit is only valid when Bit D0 is set. Clear this bit to use saved profiles (after all fast lock programming completes).

Bit D1—Rx Fast Lock Profile Pin Select

With this bit set, the CTRL_IN0 through CTRL_IN2 pins select the Rx fast lock profile. With this bit clear, Bits[D7:D5] select the fast lock profile. This bit is only valid when Bit D0 is set.

Bit D0—Rx Fast Lock Mode Enable

Set this bit when creating or using profiles.

SPI Register 0x25B—Rx Fast Lock Setup Initial Delay

These bits set the time that the charge pump current, R1, R3, and C3 of the loop filter remain at their initial values before changing to final values during fast lock. The delay is 250 ns/LSB, and the range is 0 ns to 63.75 µs. All profiles share this delay setting.

SPI Register 0x25C—Rx Fast Lock Program Address

These bits set the profile calibration word. To write all setup words for a particular profile into the table, hold the upper nibble constant and write the lower nibble 13 or 15 times (0x0 to 0xD or 0xF), changing the data written to Register 0x25D, Bits[D3:D0] for each write operation.

SPI Register 0x25D—Rx Fast Lock Program Data

This word is the data written to the internal address specified in Register 0x25C when creating a profile.

SPI Register 0x25E—Rx Fast Lock Program Read Data

Read Register 0x25E to see the programmed word at Address 0x25C.

SPI Register 0x25F—Rx Fast Lock Program Control

Bit D1—Rx Fast Lock Program Write

Set this self clearing bit any time a write operation to the fast lock table is performed. Also, set Bit D0.

Bit D0—Rx Fast Lock Program Clock Enable

Set this bit to 1 to read data from or write data to a profile.

Rx LO GENERATION REGISTER (ADDRESS 0x261)

Table 72. Rx LO Generation Register

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x261	Rx LO generation power mode	Open		Power mode[1:0]		Open				0x00	R/W

SPI Register 0x261—Rx LO Generation Power Mode

The AD9361_TXRX_SYNTH_CP_CALIB function configures this register. Write 0x00 to Register 0x261 when using the internal VCO and write 0x30 to Register 0x261 when using an external LO.

Tx SYNTHESIZER REGISTERS (ADDRESS 0x270 THROUGH ADDRESS 0x291)

Table 73. Tx Synthesizer Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x270	Disable VCO calibration	Must be 0x05				Must be 3'b010			Disable VCO calibration	0x54	R/W
0x271	Integer Byte 0	Synthesizer integer word[7:0]								0x00	R/W
0x272	Integer Byte 1	SDM bypass	SDM power-down	Open			Synthesizer integer word[10:8]			0x00	R/W
0x273	Fractional Byte 0	Synthesizer fractional word[7:0]								0x00	R/W
0x274	Fractional Byte 1	Synthesizer fractional word[15:8]								0x00	R/W
0x275	Fractional Byte 2	Open	Synthesizer fractional word[22:16]							0x00	R/W
0x276	Force ALC	Force ALC enable	Force ALC word[6:0]							0x00	R/W
0x277	Force VCO Tune 0	Force VCO tune[7:0]								0x00	R/W
0x278	Force VCO Tune 1	Must be 0						Force VCO tune enable	Force VCO tune[8]	0x00	R/W
0x279	ALC/varactor	Initial ALC value[3:0]				VCO varactor[3:0]				0x82	R/W
0x27A	VCO output	Open	$\overline{\text{POR}}$ VCO logic	Open		VCO output level[3:0]				0x0A	R/W
0x27B	Charge pump current	Set to 1	V_{TUNE} output	Charge pump current[5:0]						0x00	R/W
0x27C	Charge pump offset	Synth re-calibration	Open	Charge pump offset[5:0]						0x00	R/W
0x27D	Charge pump configuration	Must be 0	Dither mode	Open	Charge pump offset Off	Force charge pump calibration	Charge pump calibration enable	Must be 2'b00		0x80	R/W
0x27E	Loop Filter 1	Loop Filter C2[3:0]				Loop Filter C1[3:0]				0x00	R/W
0x27F	Loop Filter 2	Loop Filter R1[3:0]				Loop Filter C3[3:0]				0x00	R/W
0x280	Loop Filter 3	Loop Filter Bypass R3	Loop Filter Bypass R1	Loop Filter Bypass C2	Loop Filter Bypass C1	Loop Filter R3[3:0]				0x00	R/W
0x281	Dither/charge pump calibration	Number SDM dither bits[3:0]				Forced charge pump calibration word[3:0]				0x00	R/W
0x282	VCO Bias 1	Open	Must be 0		VCO bias temperature coefficient[1:0]		VCO bias reference[2:0]			0x04	R/W
0x283	Must be 0x0D	Must be 0x0D								0x0D	R/W
0x284	Calibration status	Charge pump calibration valid	Open	Charge pump calibration done	VCO calibration busy	Charge pump calibration word[3:0]					R
0x285	Must be 0x00	Must be 0x00								0x00	R/W
0x286	Set to 0x02	Set to 0x02								0x00	R/W
0x287	Charge pump overrange/VCO lock	Charge pump overrange high	Charge pump overrange low	Open				Tx PLL lock	Open		R

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x288	Set to 0x0B	Set to 0x0B								0x07	R/W
0x289	VCO calibration	Set to 1	Must be 3'b000			VCO calibration count[1:0]		Must be 2'b10		0x02	R/W
0x28A	Lock detect configuration	Open				Lock detect count[1:0]		Lock detect mode[1:0]		0x02	R/W
0x28B	Must be 0x17	Must be 0x17								0x40	R/W
0x28C	Must be 0x00	Must be 0x00								0x00	R/W
0x28D	Must be 0x00	Must be 0x00								0x80	R/W
0x28E	Open	Open								0x00	R/W
0x28F	Open	Open								0x00	R/W
0x290	Set to 0x70	Set to 0x70								0x63	R/W
0x291	VCO Varactor Control 1	Open				VCO varactor reference[3:0]				0x08	R/W

The AD9361_TXRX_SYNTH_CP_CALIB function sets up all registers in this section. See the AD9363 Reference Manual for more details. The Tx registers are identical to the Rx registers in Address 0x230 through Address 0x251. See those registers for definitions. The description in Register 0x231 refers to the reference divider if an external clock is used. For Tx frequency words in Address 0x271 through Address 0x275, the reference divider is in Register 0x2AC, Bits[D3:D2].

Tx SYNTHESIZER FAST LOCK REGISTERS (ADDRESS 0x29A THROUGH ADDRESS 0x29F)

Table 74. Tx Synthesizer Fast Lock Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x29A	Tx fast lock setup	Tx fast lock profile[2:0]			Open	Tx fast lock load synthesizer	Tx fast lock profile initialize	Tx fast lock profile pin select	Tx fast lock mode enable	0x00	R/W
0x29B	Tx fast lock setup initial delay	Tx fast lock initial delay[7:0]								0x00	R/W
0x29C	Tx fast lock program address	Tx fast lock program address[7:0]									R/W
0x29D	Tx fast lock program data	Tx fast lock program data[7:0]									R/W
0x29E	Tx fast lock program read	Tx fast lock program read data[7:0]									R
0x29F	Tx fast lock program control	Open						Tx fast lock program write	Tx fast lock program clock enable	0x00	R/W

These registers are identical to the Rx fast lock registers (Address 0x25A through Address 0x25F) but apply to the Tx profiles. See the Rx Fast Lock Registers (Address 0x25A Through Address 0x25F) section. The Linux and No-OS drivers contain functions for setting up and using the fast lock function. See the AD9363 Reference Manual for more information and function names.

Tx LO GENERATION REGISTER (ADDRESS 0x2A1)

Table 75. Tx LO Generation Register

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x2A1	Tx LO generation power mode	Power mode[3:0]				Open				0x00	R/W

The AD9361_TXRX_SYNTH_CP_CALIB function configures this register. Write 0x261 to Register 0x000 when using the internal VCO and write 0x261 to Register 0x0F0 when using an external LO.

MASTER BIAS AND BAND GAP CONFIGURATION REGISTERS (ADDRESS 0x2A6 AND ADDRESS 0x2A8)

Table 76. Master Bias and Band Gap Configuration Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x2A6	Set to 0x0E	Set to 0x0E								0x04	R/W
0x2A8	Set to 0x0E	Set to 0x0E								0x00	R/W

The AD9361_INIT function configures these registers correctly. These registers set up the master bias and band gap reference in the AD9363. Configure these registers before enabling the clocks in Register 0x009.

REFERENCE DIVIDER REGISTERS (ADDRESS 0x2AB AND ADDRESS 0x2AC)

Table 77. Reference Divider Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x2AB	Reference Divider Configuration 1	Open					Set to 2'b11		Rx reference divider[1]	0x04	R/W
0x2AC	Ref Divider Configuration 2	Rx reference divider[0]	Set to 3'b111			Tx reference divider[1:0]		Set to 2'b11		0x00	R/W

The AD9361_INIT function configures these registers.

SPI Register 0x2AB—Reference Divider Configuration 1

Bits[D2:D1]—Set to 2'b11

Bit D0—Rx Reference Divider[1]

This is the most significant bit of the Rx path divider control bits, mapped per Table 78. The LSB is in Register 0x2AC, Bit D7.

Table 78. Rx Ref Divider Ratio

Rx Reference Divider[1]	Divider Ratio
00	1
01	½
10	¼
11	2

SPI Register 0x2AC—Ref Divider Configuration 2

Bit D7—Rx Reference Divider[0]

See Register 0x2AB, Bit D0.

Bits[D6:D4]—Set to 3'b111

Bits[D3:D2]—Tx Reference Divider[1:0]

These bits control the Tx path divider, per Table 78.

Bits[D2:D1]—Set to 2'b11

Rx GAIN READBACK REGISTERS (ADDRESS 0x2B0 THROUGH ADDRESS 0x2B9)

Table 79. Rx Gain Readback Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x2B0	Gain Rx1	Open	Full Table Gain Index Rx1/LMT Gain Rx1[6:0]								R
0x2B1	LPF Gain Rx1	Open			LPF Gain Rx1[4:0]						R
0x2B2	Digital Gain Rx1	Open			Digital Gain Rx1[4:0]						R
0x2B3	Fast attack state	Open	Fast Attack State Rx2[2:0]			Open	Fast Attack State Rx1[2:0]				R
0x2B4	Slow loop state	Open	Slow Loop State Rx2[2:0]			Open	Slow Loop State Rx1[2:0]				R
0x2B5	Gain Rx2	Open	Full Table Gain Index Rx2/LMT Gain Rx1[6:0]								R
0x2B6	LPF Gain Rx2	Open			LPF Gain Rx2[4:0]						R
0x2B7	Digital Gain Rx2	Open			Digital Gain Rx2[4:0]						R
0x2B8	Overage Signals Rx1	Open	Gain lock	Low power	Large LMT overload	Small LMT overload	Large ADC overload	Small ADC overload	Digital saturation		R
0x2B9	Overage Signals Rx2	Open	Gain lock	Low power	Large LMT overload	Small LMT overload	Large ADC overload	Small ADC overload	Digital saturation		R

SPI Register 0x2B0—Gain Rx1

Register 0x2B0 holds the Rx1 gain index when the AD9363 is in the Rx or FDD states and is valid in all gain control modes. In full table mode, Register 0x2B0 holds the full table index. For split table mode, Register 0x2B0 holds the LMT index.

SPI Register 0x2B1—LPF Gain Rx1

LPF gain for split gain table mode.

SPI Register 0x2B2—Digital Gain Rx1

Digital gain for split gain table mode.

SPI Register 0x2B3—Fast Attack State

Bits[D6:D4]—Fast Attack State Rx2[2:0]

The state of the Rx2 fast AGC state machine per Table 80.

Table 80. Fast Attack AGC States

Fast Attack State Rx2[2:0]	State Name	Description
0	Reset peak detectors	The state machine initializes to this state at the start of Rx on. The AD9363 holds all power and peak detectors in reset.
1	Peak detect	In State 1, the AD9363 detects peak overloads and reduces gain until the overloads cease.
2	Power measure-ment	The state machine waits for settling delay, measures power, and then adjusts gain to match the signal level to the AGC lock level.
3	Final settling	If large peak overloads occur, the AD9363 decreases gain and moves to final over range state, else it moves to State 5.
4	Final overrange	The state machine resets the peak detectors and for the peak wait duration. On expiration of this counter, the state machine transitions to State 3.
5	Gain lock	The state machine remains in this state until unlocked.

Bits[D2:D0]—Fast Attack State Rx1[2:0]

Same as Bits[D6:D4] but apply to Rx1.

SPI Register 0x2B4—Slow Loop State

Bits[D6:D4]—Slow Loop State Rx2[1:0]

The state of the Rx2 slow AGC per Table 81.

[D2:D1]—Slow Loop State Rx1[1:0]

Same as Bits[D6:D4] but apply to Rx1.

Table 81. Slow Attack AGC States

Slow Attack State Rx2[1:0]	State Name	Description
0	Reset	The state machine initializes to this state at the start of Rx on. The gain update counter and related functionality resets to 0.
1	Slow measurement	Power measurement of the signal occur. A counter increments until it reaches the gain update count, at which time the state machine moves to the gain change state.
2	Gain change	Based on the results of the previous slow measurement state, the gain changes accordingly.
3	Clear peak detectors	The peak detector thresholds clear and the state machine stays in this state until the settling delay expires. This allows the Rx signal to settle before the AD9363 makes the next power measurement.

SPI Register 0x2B5 Through SPI Register 0x2B7

These registers are the same as Address 0x2B0 through Address 0x2B2 but apply to Rx2.

SPI Register 0x2B8—Overage Signals Rx1

Bit D6—Gain Lock

This bit, when set, indicates that the Rx1 fast AGC has locked the gain.

Bit D5—Low Power

This bit, when high, indicates that the Rx1 average signal power has dropped below the low power threshold.

Bit D4—Large LMT Overload

This bit, when set, indicates that a large LMT overload occurred in Rx1.

Bit D3—Small LMT Overload

This bit, when set, indicates that a small LMT overload occurred in Rx1.

Bit D2—Large ADC Overload

This bit, when set, indicates that a large ADC overload occurred in Rx1.

Bit D1—Small ADC Overload

This bit, when set, indicates that a small ADC overload occurred in Rx1.

Bit D0—Digital Saturation

This bit, when set, indicates that the signal saturated between HB1 RFIR in Rx1.

SPI Register 0x2B9—Overage Signals Rx2 (Test Register)

This register functions the same as Register 0x2B8, but applies to Rx2.

CONTROL REGISTER (ADDRESS 0x3DF)

Table 82.

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x3DF	Control	Open							Set to 1	0x00	R/W

The AD9361_INIT function sets up this register.

DIGITAL TEST REGISTERS (ADDRESS 0x3F4 THROUGH ADDRESS 0x3F6)

Table 83. Digital Test Registers Summary Map

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0x3F4	BIST configuration	Tone frequency[1:0]		Tone level[1:0]		BIST control point[1:0]		Tone/ PRBS	BIST enable	0x00	R/W
0x3F5	BIST Config-uration 2	Data port SP, HD loop test OE	Rx mask	Channel	Must be 4'b0000				Data port loop test enable	0x00	R/W
0x3F6	BIST and data port test configuration	Must be 2'b00		BIST Mask Channel 2 Q data	BIST Mask Channel 2 I data	BIST Mask Channel 1 Q data	BIST Mask Channel 1 I data	Must be 2'b00		0x00	R/W

See Engineer Zone for a FAQ describing the built in self test (BIST) functions in more detail.

SPI Register 0x3F4—BIST Configuration (Test Register)

Bits[D7:D6]—Tone Frequency[1:0]

Sets the BIST frequency according to Equation 26.

$$BIST\ Tone\ Frequency = \frac{CLK \times (Tone\ Frequency[1:0] + 1)}{32} \quad (26)$$

where:
BIST Tone Frequency units are the same as for *CLK*.
CLK is the clock rate shown in Table 85.

Bits[D5:D4]—Tone Level[1:0]

Sets the gain of the tone signal per Table 84. FS represents a full scale digital output.

Table 84. BIST Tone Level

Tone Level[1:0]	Amplitude
00	±full scale (FS)
01	±FS/2
10	±FS/4
11	±FS/8

Bits[D3:D2]—BIST Control Point[1:0]

These bits control where the BIST signal is injected per Table 85.

Table 85.BIST Control Point

BIST Control Point[1:0]	Injection Point	Clock used for BIST Tone Frequency	Comments
00	Input of Tx (output of data port)	Tx sample rate	Tx only
01	Not used	Not used	Not used
10	Input of data port	Rx sample rate	Rx only
11	Not used	Not used	Not used

Bit D1—Tone/PRBS

When this bit is clear, the BIST outputs a PRBS signal. When set, the BIST outputs a tone.

Bit D0—BIST Enable

Set this bit to enable the BIST generator.

SPI Register 0x3F5—BIST Configuration 2

Bit D7—Data Port SP, HD Loop Test OE

See Bit D0. Setting Bit D7 enables the Rx I/O port, even in half duplex mode when looping Tx data back to the Rx I/O port.

Bit D6—Rx Mask

Set this bit to mask the analog signals from propagating to the digital blocks.

Bit D5—Channel

When this bit is clear, observe Channel 1. When the bit is set, observe Channel 2.

Bits[D4:D1]—Must be 4'b0000

Bit D0—Data Port Loop Test Enable

When set, this bit loops Tx I/O data back onto the Rx I/O port. If in half duplex mode, also set Bit D7.

SPI Register 0x3F6—BIST and Data Port Test Configuration (Test Register)

Bits[D7:D6]—Must be 2'b00

Bits[D5:D2]—BIST Mask Bits

Setting one of these 4 bits zeroes out the data in question. For example, setting Bit D5 zeroes out the Channel 2 Q data.

Bits[D1:D0]—Must be 2'b00

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG15146-0-11/16(0)

www.analog.com