

AD9363 Reference Manual

GENERAL INFORMATION

Complete specifications for the [AD9363](#) device can be found in the [AD9363](#) data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board

Additional information about the [AD9363](#) registers can be found in the [AD9363 Register Map Reference Manual](#), available by registering at the [Integrated Wideband RF Transceiver Design Resources](#) web page and clicking the **Download the AD9363 Design File Package** icon. The register map is provided as a convenient and informational resource for those who want to understand the low level operation of the device; however, it is not recommended to attempt to create your own software.

Analog Devices provides complete drivers for the [AD9363](#) for both bare metal/No-OS and Linux® operating systems. The [AD9361](#), [AD9363](#), and [AD9364](#) share the same application programming interface (API). The AD9361 drivers can be found at the following online locations:

- [Linux](#) wiki page
- [No-OS](#) wiki page

Support for these drivers can be found at the following online locations:

- [Linux Engineer Zone®](#) page
- [No-OS Engineer Zone](#) page

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REVISION HISTORY

11/2016—Revision 0: Initial Version

TERMINOLOGY

Automatic Gain Control (AGC)

AGC is where an algorithm in the [AD9363](#) controls the receive path gain.

Automatic Level Control (ALC)

The voltage controlled oscillator (VCO) ALC helps maintain an optimal amplitude on the VCO resonator, providing optimum phase noise performance.

Baseband

Baseband received signals are signals that are already down-converted from radio frequency (RF). Baseband transmit signals are signals that are not yet upconverted to radio frequency.

Baseband Processor (BBP)

The BBP is also referred to as the digital baseband.

Baseband DC Calibration

Baseband dc calibration is an on-chip calibration that reduces the dc power in the received data by adding digital correction words to the data between the Half-Band 1 filter and the receive finite impulse response (FIR) filter. See the Initialization and Calibration section for more information.

Direct Current (DC)

DC literally means direct current; however, in this reference manual, dc refers to undesired received power in the center of the complex received baseband spectrum.

Enable State Machine (ENSM)

The ENSM is an on-chip state machine that moves the [AD9363](#) through its states and also controls other functions related to the [AD9363](#). See the Enable State Machine (ENSM) Guide section for more information.

Frequency Division Duplex (FDD)

FDD is the condition in which transmit and receive signals can be present simultaneously, but use different frequencies.

GSM/EDGE

GSM is the global system for mobile communication, and EDGE means the enhanced data rates for GSM evolution.

LMT

The LMT comprises three components: the low noise amplifier (LNA), mixer, and transimpedance amplifiers (TIA). Thus, the acronym for these three components together is LMT. LMT refers to both the LMT gain table and an analog peak detector that monitors the signal level at the input of the analog low-pass filter. See the Gain Control section for more information.

Local Oscillator (LO)

The LO refers to the desired radio frequency carrier frequency for the receiver and the transmitter.

Low-Pass Filter (LPF)

The LPF refers to the third-order analog low-pass filter preceding the receive analog-to-digital converter (ADC) and following the transmit digital-to-analog converter (DAC).

Lookup Table

Several calibrations and functions depend on either reading or storing lookup tables for future use.

Manual Gain Control

Manual gain control is where the baseband processor controls some or all of the gain control parameters in the [AD9363](#).

Phase-Locked Loop (PLL)

The [AD9363](#) uses PLLs to generate the various clock rates within the chip, as well as the transmit and receive LO frequencies.

Radio Frequency (RF)

In this user guide, the acronym, RF, is used for radio frequency.

RF DC Calibration

RF dc calibration is an on-chip calibration that reduces dc power in the received data by applying a compensating voltage between the LNA and the mixer. See the Initialization and Calibration section for more information.

Time Division Duplex (TDD)

TDD is where transmit and receive signals can be present on the same frequency, but at different times.

Voltage Controlled Oscillator (VCO)

A VCO is a circuit in which the output frequency of the oscillator is controlled by an input voltage level. These VCOs are part of the PLLs on the [AD9363](#). The [AD9363](#) must calibrate the VCOs before the frequency produced by the VCOs is accurate and stable.

REGISTER AND BIT SYNTAX

When describing a value of just a few bits, the following format is used:

x'byyy.

where:

x is the number of bits described.

b indicates binary.

yyy represents three digital bits with values of 0 or 1.

For example, if two bits equal 2'b01, then the LSB = 1 and the next higher bit = 0.

INITIALIZATION AND CALIBRATION

INITIALIZATION AND CALIBRATION OVERVIEW

The AD9363 powers up into a sleep state for minimal power consumption. Before the AD9363 is operational, the device clocks must be enabled and initial calibration must be completed. Table 2 describes the operation of the various initialization calibrations.

INITIALIZATION AND CALIBRATION DETAILS

Initialization calibrations are calibrations that must be run each time the AD9363 device is powered up or when a hard reset is performed using the RESET pin. Several of the calibrations only need to run once during initialization and do not rerun during operation. Other calibrations are dependent on the carrier frequency, temperature, or other parameters and must run initially and when certain events occur (such as changing the carrier frequency to more than 100 MHz). As long as power is applied to the AD9363 device, the calibration results are stored, including while in the sleep state.

The six calibrations in the calibration control are part of a calibration sequence state machine. After a calibration completes, the bit that was set to initialize the calibration self clears.

If more than one calibration is enabled in a single register write, the calibrations progress in a set order controlled by a state

machine in the AD9363. Table 1 lists the sequence of calibrations.

When the calibration sequence state holds a value of 0x1, the calibrations are complete. Some calibrations depend on the results of previously run calibrations. The receive (Rx) baseband filter and the transmit (Tx) baseband filter calibration are not part of the calibration sequence state machine and must run only when all other calibrations are not running.

Table 1. Automatic Calibration Sequence and Calibration Status

Calibration Sequence State[3:0]	Active Calibration
0x0	Calibration wait state
0x1	Calibrations complete
0x2	Baseband dc offset
0x3	RF Rx dc offset
0x4	Tx1 quadrature
0x5	Tx2 quadrature
0x6	Rx1 quadrature
0x7	Rx2 quadrature
0x8	Tx monitor (dc offset)
0x9	Rx LNA gain step
0xA to 0xF	Flush states

Table 2. Initialization Calibrations

Calibration	Run Frequency	Calibration Done Bit
Baseband Phase-Locked Loop VCO RF Synthesizer Charge Pump	Occurs once; any time the baseband PLL frequency changes. Occurs once.	Register 0x05E, Bit 7 = 1 when locked Rx: Register 0x244, Bit 7 = 1 when done Tx: Register 0x284, Bit 7 = 1 when done
RF Synthesizer VCO	Occurs automatically when an integer frequency word is written. In TDD, this calibration occurs when the TXNRX pin changes logic level.	Rx: Register 0x247, Bit 1 = 1 when locked Tx: Register 0x287, Bit 1 = 1 when locked
Baseband Rx Analog Filter Tune	Occurs once; updates when the bandwidth changes.	Register 0x016, Bit 7, self clears when done
Baseband Tx Analog Filter Tune	Occurs once; updates when the bandwidth changes.	Register 0x016, Bit 6, self clears when done
Baseband Tx Secondary Filter Tune	Occurs once; manual equations, updates when the bandwidth changes.	Not applicable
Rx TIAs	Occurs once; manual equations, updates when the bandwidth changes.	Not applicable
Rx ADC Setup	Occurs once; manual equations or lookup table, updates when the ADC sampling rate changes.	Not applicable
Baseband DC Offset	Occurs once.	Register 0x016, Bit 0, self clears when done
RF DC Offset	Occurs whenever the LO frequency changes by more than 100 MHz.	Register 0x016, Bit 1, self clears when done
Rx Quadrature	Occurs whenever the LO frequency changes by more than 100 MHz.	Tracking runs continuously
Tx Quadrature	Occurs whenever the LO frequency changes by more than 100 MHz.	Register 0x016, Bit 4, self clears when done

BASEBAND PHASE-LOCKED LOOP VCO CALIBRATION

The baseband phase-locked loop VCO calibration must be run during initialization of the AD9363 device. This calibration is run as part of the AD9361_BBPLL_SET_RATE function. The maximum calibration time is calculated using Equation 1.

$$BB\ PLL_{MAX_VCO_CAL_TIME} = \left(\frac{Divide\ Setting}{REF_CLK \times Scale} \right) \times 3456 \quad (1)$$

where *BB PLL* is the baseband phase-locked loop.

RF SYNTHESIZER CHARGE PUMP CALIBRATION

The charge pump calibration must be run once during initialization of the AD9363 device. This calibration matches the up and down currents for the charge pumps of the radio frequency PLLs, and it is run during the AD9361_TXRX_SYNTH_CP_CALIB function. This calibration must be run the first time the AD9363 device enters the alert state. The calibration completes after a maximum of 36,864 (SCALED_REF_CLK_IN) cycles.

RF SYNTHESIZER VOLTAGE CONTROLLED OSCILLATOR (VCO) CALIBRATION

The AD9363 contains two synthesizers. When using TDD mode, the Rx synthesizer is enabled only when TXNRX is low. The Tx synthesizer is enabled only when TXNRX is high.

During initial calibrations, it is recommended to set the AD9363 to FDD mode to enable both synthesizers while in the alert state and to simplify the calibrations.

The VCO calibration is run during the following two functions, AD9361_SET_RX_LO_FREQ and AD9361_SET_TX_LO_FREQ, using the following steps.

1. Set up any synthesizer setup registers.
2. Write the fractional frequency words.
3. Write the integer frequency word.

The calibration time can be traded off with calibration accuracy. For example, in FDD applications use the longest calibration for better accuracy because, once in the FDD state, it may be a long time before a synthesizer VCO calibration occurs again.

In TDD, the calibration time must be set to meet the TDD turn-around time, yet must also achieve the most accurate calibration possible. In TDD, the Rx VCO calibration occurs each time the receiver synthesizer powers up, that is, when TXRX switches from a high to a low logic level. Similarly, the Tx VCO calibration occurs each time the transmitter synthesizer powers up, that is, when TXNRX switches from a low to a high logic level. See Equation 2 for the calculation of the calibration time.

$$RF\ PLL_{MAX_VCO_CAL_TIME} (\mu s) = 2\ \mu s + Wait_2 + \left(\frac{12 + N_{COUNT}}{REF_CLK \times Scale} + Wait_{ALC} \right) \times 9 \quad (2)$$

where:

$$Wait_2 = \frac{8}{REF_CLK} + \frac{18}{REF_CLK \times Scale}$$

$$N_{COUNT} = 2^{(7 + VCO\ Calibration\ Count)}$$

$$Wait_{ALC} = \frac{40}{REF_CLK \times Scale}$$

The VCO calibrations can be masked (disabled) for certain cases, such as the fast lock synthesizer mode or when an FDD application is required. By using the FDD synthesizer lookup table instead of the TDD synthesizer lookup table, a temperature stable lock can be acquired for cases where there is not enough time to run the VCO calibration in TDD.

Detect calibration completion by reading the Rx PLL lock bit and the Tx PLL lock bit. The lock bits read Logic 1 when the PLLs are locked. The bits are also available on the control output pins.

Table 3. Example Calculated VCO Calibration Times for FDD Default Settings

VCO Calibration Count	REF_CLK	Scale	Wait ₂ (μs)	Wait _{ALC} (μs)	N _{COUNT}	Calibration Time (μs)
3	19.20	2	0.885	1.042	1024	255.073
3	30.72	2	0.553	0.651	1024	160.171
3	40.00	2	0.425	0.500	1024	123.475

Table 4. Example Calculated VCO Calibration Times for TDD Default Settings

VCO Calibration Count	REF_CLK	Scale	Wait ₂ (μs)	Wait _{ALC} (μs)	N _{COUNT}	Calibration Time (μs)
1	19.20	2	0.885	1.042	256	75.073
1	30.72	2	0.553	0.651	256	47.671
1	40.00	2	0.425	0.500	256	37.075

BASEBAND Rx ANALOG FILTER CALIBRATION

The baseband receiver (Rx) analog filter calibration tunes the cutoff frequency of the third-order Butterworth receiver anti-aliasing filter. The Rx filter is located just before the ADC in the Rx signal path and is normally calibrated to 1.4× the baseband channel bandwidth. This calibration is important for Rx interferer rejection. Note that the baseband channel bandwidth is half the complex bandwidth and coerced between 28 MHz and 0.20 MHz for the equations used in this filter tuning. To calibrate this filter, the baseband PLL is divided down using a divide by 1 to 511 divider dedicated to the Rx tuner block as shown in the following equation:

$$Divider = \text{ceiling} \left(\frac{Baseband\ PLL\ (MHz) \times \ln(2)}{BBBW_{Desired\ (MHz)} \times 2.8 \times \pi} \right) \quad (3)$$

where $BBBW$ is the baseband bandwidth.

Table 5. Typical Rx Baseband Filter Calibration Times

Standard	Desired Baseband Bandwidth (MHz)	Baseband PLL Frequency (MHz)	Rx Baseband Frequency Divider (Decimal)	Actual Baseband Bandwidth (MHz)	Maximum Calibration Time (μs)
LTE 5 MHz	2.5	983.04	31	2.499	19.236
LTE 10 MHz	5	983.04	16	4.841	9.928
LTE 15 MHz	7.5	737.28	8	7.262	6.619
LTE 20 MHz	10	983.04	8	9.683	4.964

The Rx baseband analog filter calibration runs during the AD9361_SET_RX_RF bandwidth function. Monitor calibration completion on a control output pin or by reading the calibration control register until the Rx baseband filter calibration bit self clears.

Because the filter calculation uses a ceiling function to generate the divider, there is some quantization of the corner frequency. If the quantization is too large, it may be necessary to adjust the desired baseband bandwidth (BBBW) to compensate.

$$BBBW_{ACTUAL\ (MHz)} = \left(\frac{Baseband\ PLL\ (MHz) \times \ln(2)}{2.8 \times \pi \times Divider} \right) \quad (4)$$

$$Calibration\ Time\ (\mu s) = 610 \times \frac{\ln(2)}{BBBW_{ACTUAL\ (MHz)} \times 2.8 \times \pi} \quad (5)$$

BASEBAND Tx ANALOG FILTER CALIBRATION

The baseband transmitter (Tx) analog filter calibration tunes the cutoff frequency of the third-order Butterworth transmitter anti-imaging filter. The Tx filter is located just after the DAC in the Tx signal path and is normally calibrated to 1.6× the baseband channel bandwidth. Note that the baseband channel bandwidth is half the complex bandwidth and coerced between 20 MHz and 0.625 MHz for the equations used in this filter tuning. To generate this Tx tune clock, the baseband PLL is divided down using a divide by 1 to 511 divider dedicated to the Tx tuner block as shown in the following equation:

$$Divider = \text{Ceiling} \left(\frac{BasebandPLL_{MHz} \times \ln(2)}{BBBW_{DESIRED, MHz} \times 3.2 \times \pi} \right) \quad (6)$$

where $BBBW$ is the baseband bandwidth.

The Tx baseband analog filter calibration runs as part of the AD9361_SET_TX_RF_BANDWIDTH function. Monitor calibration completion on a control output pin or by reading the

calibration control register until the Tx baseband filter calibration bit self clears.

Similar to the baseband Rx analog filter, there is quantization of the corner frequency for the Tx analog filter. If the quantization becomes too large, it may be necessary to adjust the desired baseband bandwidth (BBBW) to compensate.

$$BBBW_{ACTUAL(MHz)} = \left(\frac{BasebandPLL_{MHz} \times \ln(2)}{2.8 \times \pi \times Divider} \right) \quad (7)$$

$$Calibration\ Time\ (\mu s) = 610 \times \frac{\ln(2)}{BBBW_{ACTUAL(MHz)} \times 2.8 \times \pi} \quad (8)$$

BASEBAND Tx SECONDARY FILTER

The baseband transmitter (Tx) secondary filter is a tunable single-pole filter after the baseband Tx analog filter. The Tx secondary filter corner is ideally set to 5× the baseband bandwidth to help filter out of band Tx noise emissions. This filter is programmed when the AD9361_SET_TX_RF_BANDWIDTH function is called.

Table 6. Typical Tx Baseband Filter Calibration Times

Standard	Desired Baseband Bandwidth (MHz)	Baseband PLL Frequency (MHz)	Rx Baseband Frequency Divider (Decimal)	Actual Baseband Bandwidth (MHz)	Maximum Calibration Time (μs)
LTE 5 MHz	2.5	983.04	28	35.1086	10.1115
LTE 10 MHz	5	983.04	14	70.2171	5.0558
LTE 15 MHz	7.5	737.28	7	105.326	3.3705
LTE 20 MHz	10	983.04	7	140.434	2.5278

Rx TRANSIMPEDANCE AMPLIFIER CALIBRATION EQUATIONS

The receiver (Rx) transimpedance amplifier (TIA) is located between the mixer and Rx baseband analog filter. The TIA has two gain settings (0 dB gain and –6 dB gain), and applies a single-pole filter with a corner at 2.5× the baseband bandwidth. The corner frequency of the Rx TIA is programmed when the AD9361_SET_RX_RF_BAND-WIDTH function is called. When the gain index in the AD9363 Rx gain table changes the Rx TIA gain setting, the AD9363 automatically scales the amplifier to maintain the same corner frequency.

Rx ADC SETUP

The receive ADC is a third-order, continuous time, delta-sigma (Δ - Σ) modulator that is highly programmable. Although the values in many, but not all, of the ADC registers change with sampling clock frequency, the correct initial settings are critical for proper operation. The ADC is programmed with the AD9361_SET_RX_RF_BANDWIDTH function.

BASEBAND DC OFFSET CALIBRATION

It is recommended to run the baseband dc offset calibration once during the device initialization in the alert state. Because the baseband signal path does not change with different wireless standards or clock frequencies, it does not need to be run again. The baseband dc offset correction values are stored for all of the Rx analog baseband filter gain steps. The correction words are applied as the Rx gain changes based on the current Rx gain table index. This calibration is run during the AD9361_BB_DC_OFFSET_CALIB function call.

The one shot baseband dc offset calibration completes in a finite time, depending on the device settings. The calibration time is 404,000 CLKRF cycles.

BASEBAND DC OFFSET TRACKING

Use baseband dc offset tracking in conjunction with the RF dc offset tracking option. A high-pass filter loop is used to track dc changes caused by the RF dc offset and the Rx quadrature correction block. The speed and accuracy of the baseband dc tracking loop are configurable. Also, an option exists for the baseband dc offset tracking to attack and settle quickly after a gain change, and then, after a certain time, switch to slower dc offset tracking updates.

When using the tracking mode, first run an initial one shot baseband dc offset calibration to minimize any static dc offsets in the signal chain. Next, enable tracking together with the desired tracking loop settings. Enable baseband dc offset tracking in the AD9361_TRACKING_CONTROL function call.

RF DC OFFSET CALIBRATION

Run the RF dc offset calibration once during initialization or, potentially, when moving to a new carrier frequency that is more than 100 MHz away from the previous carrier frequency. Run this calibration in the alert state while the Rx synthesizer is enabled. The calibration is run during the AD9361_RF_DC_OFFSET_CALIB function. The internal calibration results lookup table stores separate results for the RF RxA input.

If using the RF RxB or RF RxC inputs together with the RF RxA input, run the calibration twice, once with each input band selected. After calibrating each band, switching from the RF RxA input to the RF RxB or RF RxC input does not require another calibration. However, because the RF RxB and RF RxC inputs use the same calibration results, switching from Input B to Input C may require running the RF dc offset calibration.

When using the full Rx gain table, the RF dc offset calibration only calibrates at gain indexes designated to calibrate in the Rx gain table. This is because several consecutive gain steps may leave the front-end gain at the same setting, changing baseband gain settings only. The RF dc offset correction is only designed to remove dc offset due to the radio frequency portions of the signal chain. By only running the calibration at gain indexes that actually change the front-end gain, the calibration time is reduced. If the lookup table does not hold a dc correction value for the current Rx gain index, it uses the dc offset correction for the next higher gain index that was calibrated. In the case of a split Rx gain table, the calibration runs at each LMT gain index.

Enable the RF dc offset tracking using the AD9361_TRACKING_CONTROL function. The tracking triggers a radio frequency dc offset update based on three events, as follows: Rx gain change, no energy detected, or when the enable state machine exits the Rx state. The dc offset update bit field setting allows enabling or disabling any combination of these events. Disabling the RF dc offset tracking uses the initially calibrated RF dc offset and never updates the correction words.

To calculate the calibration time and accuracy, use Equation 9 and Equation 10. The calibration begins at minimum gain (index = 0) and moves toward maximum gain. The RF dc offset correction for each enable Rx gain index is stored in a lookup table and applied when using the Rx gain index. If the full Rx gain table is used, the RF dc offset is calibrated only at gain indexes specified to calibrate in the Rx gain table. If the Rx gain table is split, the number of enable gain indexes in Equation 10 equals 41 gain steps.

$$\text{Length of Each Average} = (((\text{RF DC Offset Count} \times 256) + 255) + 32) \quad (9)$$

$$\text{Total Calibration Time (CLKRF Clock Cycles)} = 21 \times \text{Length of Each Average} \times (\text{Number of Enabled Gain Indexes} + 1) \quad (10)$$

Rx QUADRATURE TRACKING CALIBRATION

The Rx quadrature tracking uses the receive data to continuously minimize the phase and gain error in the receive path. The tracking algorithm is configured and enabled in the AD9361_TRACKING_CONTROL function. As soon as the AD9363 enable state machine enters the receive or frequency division duplex state, the tracking begins minimizing the quadrature error.

Tx QUADRATURE CALIBRATION

The Tx quadrature calibration uses a calibration signal internally to minimize the transmitter dc offset, gain, and phase errors to improve the performance of the transmit chain. The AD9361_TX_QUAD_CALIB function configures and runs this calibration during initialization in the alert state. Monitor the completion of the calibration by reading the calibration control register until the appropriate bit self clears.

When changing the carrier frequency, a much faster refresh calibration can be initiated to update the transmit offset, gain, and phase error corrections. It is also recommended to refresh the calibration results if the device temperature changes dramatically. The auxiliary ADC can be used to measure the device temperature using the internal temperature sensor, and to know when to refresh the Tx quadrature calibration.

The Tx quadrature calibration is a convergence algorithm, but it has a maximum calibration time. Use Equation 11 to calculate the number of CLKRF clock cycles used for maximum

calibration time. CLKRF is the clock rate at the output of the transmit FIR filter (after transmit FIR interpolation).

$$\begin{aligned} Tx_{Quad} \text{ Calculation Time (CLKRF clock cycles)} &= \\ \text{Number of Tx Channels} \times 94,464 &\quad (11) \end{aligned}$$

The Tx quadrature calibration stores a separate set of calibration results for the Tx_A and Tx_B output paths. When using both the Tx_A and the Tx_B outputs, run the calibration twice, once with each output path selected.

To set up the Tx quadrature calibration, first confirm that the numerically controlled oscillator (NCO) frequency is within the Rx baseband filter bandwidth. Depending on the digital filter configuration, it may be necessary to sweep the NCO phase offset to find the optimal setting. More information on the setup of this phase sweep can be found in the *AD9361 Transmit Quadrature Calibration (Tx Quad Cal)* FAQ on the [AD9631 Engineer Zone website](#).

If using a custom Rx gain table, verify that the Tx quadrature calibration gain index in Register TX QUAD FULL/LMT GAIN points to an index with the TIA index = 1 and the low-pass filter index = 0.

When using a split gain table, verify that the Tx quadrature calibration gain index in the Tx quad full/LMT gain register points to a gain index with the TIA index = 1. For a split gain table, set the low-pass filter index in the Tx quad LPF gain register to a value of 0x00.

REFERENCE CLOCK REQUIREMENTS

The [AD9363](#) uses fractional-N PLLs to generate the transmitter and receiver LO frequencies, as well as the oscillator (the baseband PLL) used for the data converters, digital filters, and input/output port. These PLLs all require a reference clock input, which can be provided by an external oscillator.

Applications, such as wireless base stations, require the reference clock to lock to a system master clock. In these situations, use an external oscillator, such as a VCTCXO, in conjunction with a synchronizing PLL, such as the [AD9548](#).

REFERENCE CLOCK SETUP AND OPERATION

The external reference clock must be ac-coupled to XTALN (Pin M12). The clock frequency must be between 5 MHz and 320 MHz, and can be scaled by $1\times$, $\frac{1}{2}\times$, $\frac{1}{4}\times$, and $2\times$ using the baseband PLL and the Rx and Tx reference dividers.

The valid frequency range for the radio frequency PLL phase detectors is 10 MHz to 80 MHz, and the scaled frequency of the reference clock must be within this range. For optimum phase noise, operate the scaled clock as close to 80 MHz as possible. The selection between the digital controlled crystal oscillator (DCXO) and the external reference clock is made using the `AD9361_INIT` function.

It is recommended that the level for the clock be 1.3 V p-p maximum (lower swings can be used but limit the performance). This signal can be a clipped sine wave or a CMOS signal. The best performance is achieved with the highest slew rate possible.

XTALN (Pin M12) has an input resistance of $\sim 10\text{ k}\Omega$ in parallel with 10 pF.

PHASE NOISE SPECIFICATION

The [AD9363](#) Rx and Tx radio frequency PLLs use external clock as their reference clock. For this reason, it is extremely critical that the clock source have a very low phase noise. The recommended phase noise specification is shown in Figure 1.

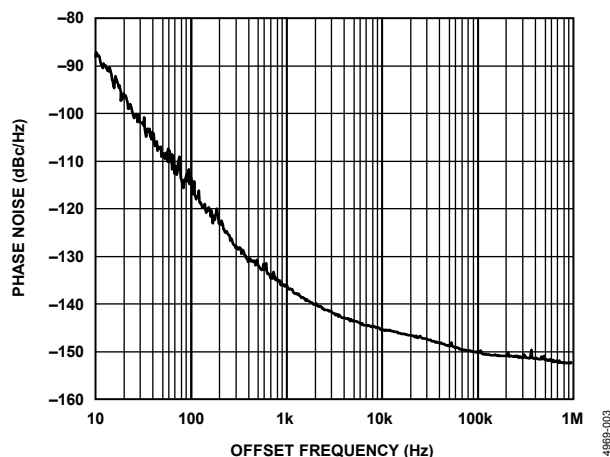


Figure 1. Phase Noise vs. Offset Frequency

RADIO FREQUENCY AND BASEBAND PLL SYNTHESIZER

PLL SYNTHESIZERS OVERVIEW

The AD9363 transceiver contains two identical radio frequency PLL synthesizers to generate the required LO signals; these synthesizers are independently programmed. One synthesizer is programmed for the Rx channel, and the other synthesizer is programmed for the Tx channel. The transceiver also contains a baseband PLL synthesizer to generate the required sampling and internal operational clocks. The PLL synthesizers are all of fractional-N architecture with completely integrated VCOs and loop filters; they require no external components to cover the entire frequency range of the device. This configuration allows the use of any convenient reference frequency for operation on any channel with any sample rate.

For FDD operation, the frequency of Tx and Rx can be the same or different, and both radio frequency PLL synthesizers operate simultaneously. For TDD operation, the radio frequency PLL synthesizers alternately turn on as appropriate for Rx and Tx frames.

RF PLL INTRODUCTION

The fundamental frequency of the radio frequency PLLs ranges from 325 MHz to 3.8 GHz. LO frequencies ranging from 6 GHz to 12 GHz are created by dividing the PLL frequency. The Rx

PLL is configured and calibrated using the AD9361_SET_RX_LO_FREQ function, and the Tx PLL is configured using the AD9361_SET_TX_LO_FREQ function. Each synthesizer must be configured and calibrated separately.

AD9363 PLL ARCHITECTURE

The following sections provide block diagrams of the AD9363 PLL; these diagrams show the reference block, the main PLL block, and the LO generator output block. The VCO always operates between 6 GHz and 12 GHz.

Reference Block

The reference frequency must be an external clock source provided to the input to the device. The reference is then split and applied to three independent conditioning blocks, also known as REF dividers. The conditioning blocks provide four options such that the PLL reference frequency, f_{REF} (the loop reference applied to the PLL phase detector), is either buffered, doubled, halved, or divided by four. Independent blocks make it possible to have a different f_{REF} for the RF and baseband PLLs. The reference scalars are set using the AD9361_INIT function. For best RF PLL performance, Analog Devices recommends selecting a reference clock that scales as close to 80 MHz as possible.

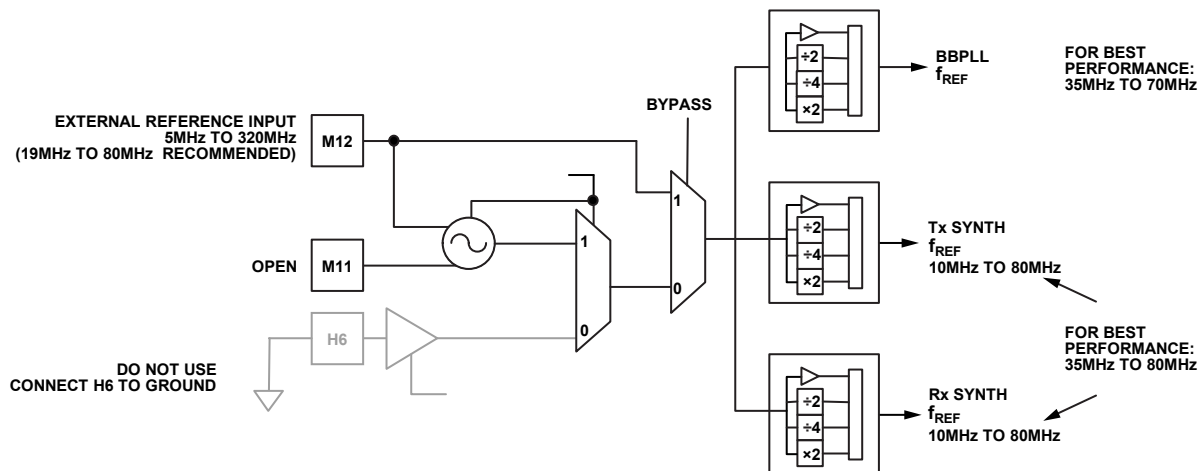


Figure 2. PLL Reference Block

14959-004

The independent Rx and Tx PLLs use fractional-N techniques to achieve channel synthesis. The entire PLL is integrated on chip, including the VCO and the loop filter. The PLL always operates over the range of 6 GHz to 12 GHz. The charge pump current is programmable, as are all of the loop filter components, allowing optimization of performance parameters for almost any application.

Configuration for a given frequency consists of a combination of calculating the required divider values and referring to an Analog Devices supplied lookup table to configure the VCO for stable performance over temperature. The main PLL output is divided by the VCO divider block to create the frequency bands that allow the device to operate continuously from 325 MHz to 3.8 GHz. Figure 4 shows how the bands are created. The synthesizer configuration registers, loop filter, integer and fractional words, and VCO divider are calculated in the AD9361_RX_LO_FREQ and AD9361_TX_LO_FREQ function calls.



Figure 3. PLL Synthesizer Block Diagram (Rx and Tx Synthesizers are Identical)



Figure 4. VCO Divider

CHARGE PUMP CURRENT

The charge pump current is 6-bit programmable and varies from 0.1 mA to 6.4 mA with 0.1 mA steps. The charge pump current must be calibrated during initialization, after which time it can use the lookup tables supplied by Analog Devices during operation.

RF PLL LOOP FILTER

The RF PLL loop filter is fully integrated on chip and is a standard, passive, Type II third-order filter with five 4-bit programmable components (see Figure 5). The loop filter values are included in the lookup tables provided by Analog Devices; do not modify the values in these lookup tables.

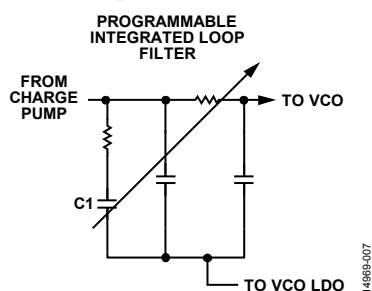


Figure 5. Loop Filter

VCO CONFIGURATION

VCO configuration consists of writing a few static registers from a lookup table provided by Analog Devices and then enabling an automatic calibration procedure to configure the VCO tune voltage (V_{TUNE}) and ALC. The VCO is triggered in one of three ways:

- Moving from a wait state to an alert state.
- Moving from a synthesizer power-down state to an alert state (TDD operation)/
- Writing the LSBs of the Rx or Tx frequency integer word.

Perform all lookup table writes for the VCO, loop filter, and other synthesizer settings into the chip before triggering the VCO calibration. Complete charge pump calibration before beginning a VCO calibration.

When in TDD mode using hardware (ENABLE/TXNRX) control and with the device state machine in the alert state, the synthesizers power up and power down with the state of the TXNRX control line. A typical example sequence for TDD operation is as follows:

1. Rx.
2. Alert.
3. Tx.
4. Alert.
5. Rx.

The baseband controller sets the level of the TXNRX line in alert mode to steer the device into the correct next state. Then, the state machine advances to the next state with the following enable edge. During alert, as the baseband controller changes the level of TXNRX from low to high, the Rx synthesizer turns off, the Tx synthesizer turns on, and a Tx VCO calibration triggers. Similarly, during a following cycle, as the baseband controller changes the state of TXNRX from high to low, the Tx synthesizer turns off, the Rx synthesizer turns on, and a Rx VCO calibration triggers.

Operationally, the baseband processor transitions the TXNRX line shortly after entering the alert mode so that the synthesizer has as much time as possible between frames to calibrate and lock. The typical TDD calibration plus lock times range from 45 μ s to 60 μ s. For faster lock times, see the TDD Mode Faster Lock Times section.

VCO Calibration

VCO calibration time is programmable. Typically, a fast calibration is appropriate for TDD systems and a slow calibration is appropriate for FDD systems. For TDD operation, the synthesizer is on for a short time only, so there is little danger for temperature drift to cause lock loss. For FDD operation, the synthesizer can potentially be locked indefinitely, so a longer, more accurate calibration is required to ensure that V_{TUNE} is sufficiently centered. See the RF Synthesizer Voltage Controlled Oscillator (VCO) Calibration section for calibration time examples.

The device includes a fast lock mode that makes it possible to achieve faster than normal frequency changes by storing all synthesizer programming information, including the VCO calibration result of this section, into either device registers of the baseband processor memory space to be recalled at a later time (see the Fast Lock Profiles section for details).

LOCK DETECTOR

A lock detector bit is provided to indicate that the corresponding synthesizer has achieved lock in the configured number of clocks. Configure the lock detector by setting the mode and count values in the lock detect configuration registers.

The lock detect count bits set the maximum time allowed for the RF PLL to lock. If the RF PLL locks within the specified time, the bits go high. The time is measured in reference clock cycles, per Table 7. It is recommended to use at least 1024 reference clock cycles.

Table 7. Lock Detect Count

Lock Detect Count (Decimal)	Number of Reference Clock Cycles
0	256
1	512
2	1024
3	2048

The lock detect mode bits set the lock detect mode of operation, per Table 8. It is recommended to use the run lock detect continuously mode.

Table 8. RF PLL Lock Detect Mode

Lock Detect Count (Decimal)	RF PLL Lock Detect Mode
0	Disable lock detect
1	Run lock detect one time only, when RF PLL is enabled
2	Run lock detect continuously
3	Do not use

SYNTHESIZER LOOKUP TABLE

Analog Devices provides synthesizer lookup tables to generate the static register writes required for the VCO and loop filter. There is a set of tables for FDD operation and another set of tables for TDD operation. Each set of tables covers the entire VCO frequency range as well as three different RF PLL loop reference frequencies.

The FDD tables enable the VCO temperature compensation for the user to employ longer, more accurate calibration times, allowing the device to remain in operation indefinitely. In the TDD tables, temperature compensation is not enabled, assuming that the VCO is to be calibrated between the Tx and Rx frames. If temperature compensation is required in a TDD operation, then the FDD tables can be used during the TDD synthesizer calibrations.

The lookup tables are separated into three tables by reference frequency: 40 MHz, 60 MHz, and 80 MHz. The correct table to reference is the one that most closely matches the loop f_{REF} value for the operating mode. Refer to Table 9 for lookup selection based on scaled reference frequency.

Table 9. Lookup Table Reference

RF PLL f_{REF} (MHz)	Correct Lookup Table to Reference
35 to 50	Use the 40 MHz lookup table
50 to 70	Use the 60 MHz lookup table
70 to 80	Use the 80 MHz lookup table

TDD Mode Faster Lock Times

In TDD mode, the Rx and Tx synthesizers are alternately turned on and off, following the state of the TXNRX control line. Typically, the synthesizer is set to trigger a VCO calibration each time it powers up so that it has a fresh calibration value. If the LO frequency in TDD mode does not change from frame to frame, it is not necessary to recalibrate the VCO each time. The synthesizers retain the VCO calibration result even after the synthesizer is powered down. When bursting between Tx, alert, Rx, and so forth on the same LO frequency, the synthesizer must only relock and can possibly be completed in 25 μ s or less, depending on the loop bandwidth.

Perform the following steps to set up the synthesizer in this mode:

1. Set up the VCO for an FDD calibration.
2. Perform the VCO calibration.
3. Set the disable VCO calibration bit.

Step 3 disables the triggering of all VCO calibrations, including writing of the new integer word. If a new calibration is required, clear this bit.

Note that, if the LO frequency is changed, the VCOs must be recalibrated to retain the information pertaining to the new frequency.

BASEBAND PLL

The baseband PLL is a fractional-N synthesizer that synthesizes the digital clocks for the AD9363 chip. The baseband PLL synthesizes an integer multiple of the receive ADC clock, the transmit DAC clock, all analog calibration clocks, as well as the clocks used in the digital section. The baseband PLL operates in the range of 715 MHz to 1.430 GHz, which allows practically any sample rate to be generated from any reference frequency. Table 10 lists common communication systems, their system sample rate, and the corresponding baseband PLL frequency.

Table 10. Clock Rates for the Rx and Tx Digital Datapaths and the Appropriate Baseband PLL Output Frequencies

System	Sample Rate (MSPS)	Baseband PLL (MHz)
GSM	0.542	832
LTE 1.4	1.92	983.04
LTE 3.0	3.84	983.04
LTE 5	7.68	983.04
LTE 10	15.36	983.04
LTE 15	23.04	737.28
LTE 20	30.72	983.04
WiMax 1.75	2	1024
WiMax 3.5	4	1024
WiMax 4.375	5	1280
WiMax7	8	1024
WiMax 8.75	10	1280
WiMAX 5	5.6	716.8
WiMAX 10	11.2	716.8
WiMAX 20	22.4	1075.2
802.11a	20	1280
802.11n	40	1280

The output of the baseband PLL drives a programmable divider chain, resulting in the desired sample rate and bus communication rate. The required baseband PLL frequency is typically back calculated by deciding how the channel filtering is to be accomplished and then selecting the appropriate output divider that allows the baseband PLL to operate within range. See the Filter Guide section for available filtering, decimation, and integration setup options.

Baseband PLL VCO

The baseband PLL VCO is a multiband ring oscillator with a VCO gain (K_V) rating of 550 MHz/V that requires a frequency calibration prior to operation. The calibration is configured and run with the AD9361_BBPLL_SET_RATE function.

Figure 7 shows a block diagram of the baseband PLL. The reference frequency for the loop is the output of the reference scaler block, which is identical to, but independent from, the reference scaler blocks for the RF PLLs.

The reference block is configured to buffer, multiply, or divide the device reference frequency before passing to the baseband PLL phase detector. For best performance, configure the baseband PLL reference scaler block such that the resulting baseband PLL f_{REF} is between 35 MHz and 70 MHz.

Baseband PLL Charge Pump

The baseband PLL charge pump has programmable output current from 25 μ A to 1575 μ A in 25 μ A steps. In addition, a programmable bleed current is available. This is an NMOS current source that is programmable from 0 μ A to 316 μ A.

Baseband PLL Loop Filter

The baseband PLL loop filter is fully integrated on chip and is a standard, passive, Type II third-order filter with five programmable components. The filter is programmed by the AD9361_BBPLL_SET_RATE function.

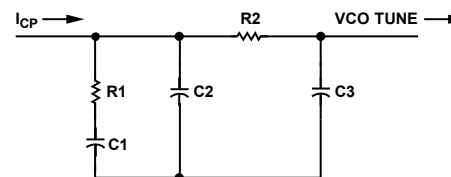


Figure 6. Baseband PLL Internal Loop Filter ($R2$ and $C3$ Can Be Bypassed)

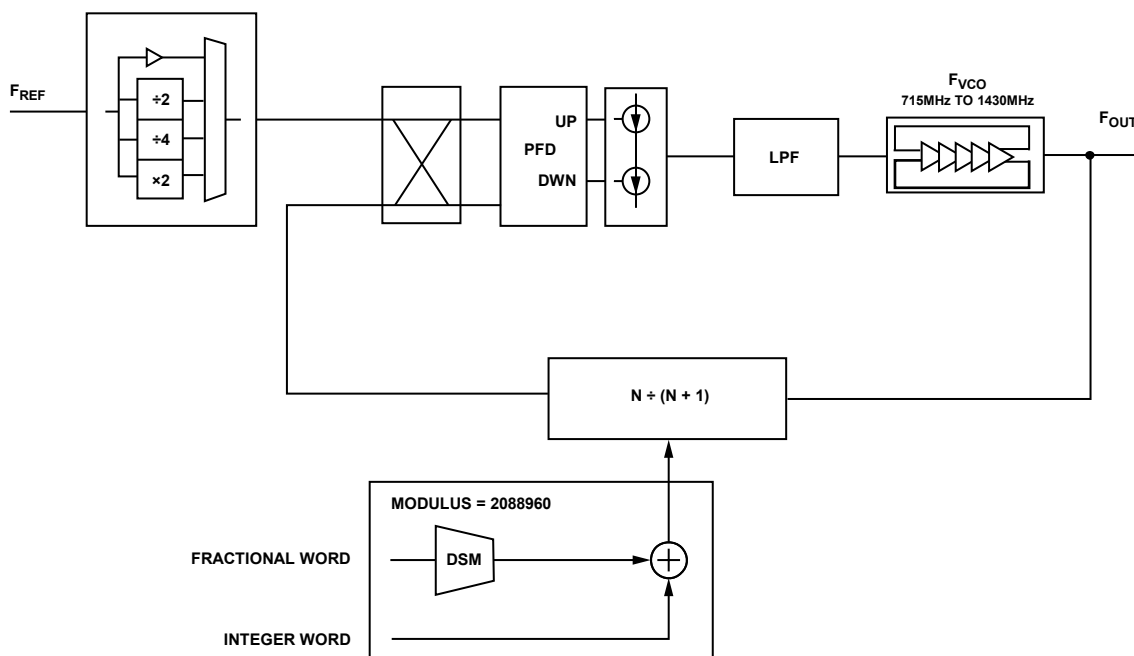


Figure 7. Baseband PLL Block Diagram

FAST LOCK PROFILES

FAST LOCK PROFILES OVERVIEW

The [AD9363](#) includes a fast lock mode that makes it possible to achieve faster than normal frequency changes by storing sets of synthesizer programming information (called profiles) either in device registers or in the baseband processor memory space to be recalled later. The fast lock mode eliminates most of the overhead of synthesizer programming by allowing up to eight full receive profiles and eight full transmit profiles of frequency configuration information, including VCO calibration results, to be stored in the device for faster frequency changes.

To use a particular profile, it must first be configured. Typically, this is accomplished at power-up; however, a new or updated profile can be defined at any convenient time. There are three processes to define a profile:

- The synthesizer is configured, calibrated, and allowed to lock at a particular frequency.
- The VCO calibration time is set to the longest, most accurate time period (FDD mode) because these values are stored for future use.
- The baseband processor transfers the resulting information from Step 1 and Step 2 from the synthesizer registers into the fast lock memory space according to profile number.

These steps are repeated for each desired profile; that is, Profile 0 to Profile 7 (Rx) and Profile 0 to Profile 7 (Tx).

If more than the eight on-chip profiles are required, the synthesizer is tuned and calibrated as if the information were to be stored in a profile, but instead, it is stored in the baseband processor memory space and written into the desired profile at a later, more convenient time. In this way, an unlimited number of profiles can be available, and a given profile can be changed or updated at any appropriate time during operation.

In addition, the user can define a higher initial charge pump current and R1 value of the loop filter to increase the bandwidth of the synthesizer for a programmable amount of time to further reduce lock time. These values are defined in the profile information, as well.

Recall a profile in one of two ways, as follows:

- Issue a single SPI command that contains the desired profile number and transfer bit, or
- Set the appropriate code on the control input pins.

The on-chip stored profile information is then transferred into the synthesizer registers, the synthesizer is configured immediately, and it is released to lock as quickly as the loop bandwidth allows.

Fast Lock Initial Wider Bandwidth Option

VCO calibration is eliminated in fast lock and, therefore, may provide fast enough synthesizer locking for a particular application. However, when a profile is selected, it is also possible to initially have different loop filter values and charge pump current

resulting in a wider loop bandwidth for a programmable time period, possibly resulting in an even faster lock mode. After the time period expires, the loop filter values adopt the steady state narrow values of the profile. If this feature is not required or desired, simply program the initial values the same as the narrow values.

Assuming the same phase margin for wide (initial) and narrow bandwidth is desired, for a bandwidth ratio,

$$N = \text{Initial Bandwidth} / \text{Narrow Bandwidth},$$

$$CP_CURRENT_INIT = CP_CURRENT_NARROW \times N^2$$

$$R1_INIT = R1_NARROW / N$$

In practice, CP_CURRENT_INIT achieves its maximum before it can actually be the square of the narrow value. Although this occurs, a lock time advantage remains possible. However, these absolute values that result in the fastest lock and settling times need optimization by the customer during product development. Note that charge pump currents and all loop filter components can be completely different between wide (initial) and narrow values, so exercise care when configuring to result in optimum and stable performance in both wide and narrow bandwidth modes. The amount of time that the wider bandwidth is active is programmed into the fast lock setup initial delay register in increments of 250 ns per bit.

CONFIGURING AND USING A FAST LOCK PROFILE

The fast lock registers (Address 0x25C through Address 0x25F for Rx, and Address 0x29F for Tx) allow access to the internal memory area. See Table 11 for Rx and Table 12 for Tx fast lock register contents. The following procedure describes how to define a particular profile to the currently programmed synthesizer frequency:

1. If using faster lock (wide bandwidth), determine fast lock delay and N. If not using wide bandwidth, delay is not important and $N = 1$.
2. Configure the profiles.
 - a. Calibrate the synthesizer to the desired frequency using FDD calibration settings.
 - b. Create the profile and store it in the [AD9363](#) using the AD9361_FASTLOCK_STORE function.
 - c. If the profile also must be stored in the baseband processor, use the AD9361_FASTLOCK_SAVE function.
3. Use the profile.
 - a. To use a profile stored inside the [AD9363](#), use the AD9361_FASTLOCK_RECALL function.
 - b. If the profile is stored in the baseband processor, first load it into the [AD9363](#) using the AD9361_FASTLOCK_LOAD function and then use the recall function to use that profile.

Table 11. Receive Fast Lock Internal Addressing

Program Address [7:4]	Assignment	Program Address [3:0]	Assignment (Written to Register 0x25D)	Location of Setup Words
0	Profile 0	0	Synthesizer integer word[7:0]	Register 0x231, Command Bits[D7:D0]
1	Profile 1	1	Synthesizer integer word[10:8]	Register 0x232, Command Bits[D2:D0]
2	Profile 2	2	Synthesizer fractional word[7:0]	Register 0x233, Command Bits[D7:D0]
3	Profile 3	3	Synthesizer fractional word[15:8]	Register 0x234, Command Bits[D7:D0]
4	Profile 4	4	Synthesizer fractional word[22:16]	Register 0x235, Command Bits[D6:D0]
5	Profile 5	5	VCO bias reference[2:0] shift left by 4 + VCO varactor[3:0]	Register 0x242, Command Bits[D2:D0] Register 0x239, Command Bits[D3:D0]
6	Profile 6	6	VCO bias TCF[1:0] shift left by 6 + Charge pump current (INIT)[5:0]	Register 0x242, Command Bits[D4:D3] Set per Initial N calculation
7	Profile 7	7	Charge pump current[5:0]	Register 0x23B, Bits[D5:D0]
8	Not used	8	Loop Filter R3[3:0] shift left by 4 + Loop Filter R3 (INIT)[3:0]	Register 0x240, Command Bits[D3:D0] Set desired initial value
9	Not used	9	Loop Filter C3[3:0] shift left by 4 + Loop Filter C3 (INIT)[3:0]	Register 0x23F, Command Bits[D3:D0] Set desired initial value
A	Not used	A	Loop Filter C1[3:0] shift left by 4 + Loop Filter C2[3:0] shift right by 4	Register 0x23E, Command Bits[D3:D0] Register 0x23E, Command Bits[D7:D4]
B	Not used	B	Loop Filter R1[3:0] + Loop Filter R1 (INIT)[3:0]	Register 0x23F, Command Bits[D7:D4] Set per Initial N calculation
C	Not used	C	VCO varactor reference TCF[2:0] + Rx VCO divider[3:0]	Register 0x250, Command Bits[D6:D4] Register 0x005, Command Bits[D3:D0]
D	Not used	D	VCO calibration offset[3:0] shift left by 1 + VCO varactor reference[3:0]	Register 0x238, Command Bits[D6:D3] Register 0x251, Command Bits[D3:D0]
E	Not used	E	Force VCO tune[7:0]	Register 0x237, Command Bits[D7:D0]
F	Not used	F	Force ALC word [6:0] shift left by 1 + Force VCO tune[8]	Register 0x236, Command Bits[D6:D0] Register 0x238, Command Bit D0

Table 12. Transmit Fast Lock Internal Addressing

Program Address [7:4]	Assignment	Program Address [3:0]	Assignment (Written to Register 0x25D)	Location of Setup Words
0	Profile 0	0	Synthesizer integer word [7:0]	Register 0x271, Command Bits[D7:D0]
1	Profile 1	1	Synthesizer integer word [10:8]	Register 0x272, Command Bits[D2:D0]
2	Profile 2	2	Synthesizer fractional word [7:0]	Register 0x273, Command Bits[D7:D0]
3	Profile 3	3	Synthesizer fractional word [15:8]	Register 0x274, Command Bits[D7:D0]
4	Profile 4	4	Synthesizer fractional word [22:16]	Register 0x275, Command Bits[D6:D0]
5	Profile 5	5	VCO bias reference [2:0] shift left by 4 + VCO varactor [3:0]	Register 0x282, Command Bits[D2:D0] Register 0x279, Command Bits[D3:D0]
6	Profile 6	6	VCO bias TCF [1:0] shift left by 3 + Charge pump current (INIT) [5:0]	Register 0x282, Command Bits[D4:D3] Set per Initial N calculation
7	Profile 7	7	Charge pump current [5:0]	Register 0x27B, Bits[D5:D0]
8	Not used	8	Loop Filter R3 [3:0] shift left by 4 + Loop Filter R3 (INIT) [3:0]	Register 0x280, Command Bits[D3:D0] Set per Initial N calculation
9	Not used	9	Loop Filter C3 [3:0] shift left by 4 + Loop Filter C3 (INIT) [3:0]	Register 0x27F, Command Bits[D3:D0] Set per Initial N calculation
A	Not used	A	Loop Filter C1 [3:0] shift left by 4 + Loop Filter C2 [3:0] shift right by 4	Register 0x27E, Command Bits[D3:D0] Register 0x27E, Command Bits[D7:D4]
B	Not used	B	Loop Filter R1 [3:0] + Loop Filter R1 (INIT) [3:0]	Register 0x27F, Command Bits[D7:D4] Set per Initial N calculation
C	Not used	C	VCO varactor reference TCF [2:0] + Rx VCO divider [3:0]	Register 0x290, Command Bits[D6:D4] Register 0x005, Command Bits[D7:D4]
D	Not used	D	VCO calibration offset [3:0] shift left by 1 + VCO varactor reference [3:0]	Register 0x278, Command Bits[D6:D3] Register 0x291, Command Bits[D3:D0]
E	Not used	E	Force VCO tune [7:0]	Register 0x277, Command Bits[D7:D0]
F	Not used	F	Force ALC word [6:0] shift left by 1 + Force VCO tune [8]	Register 0x276, Command Bits[D6:D0] Register 0x278, Command Bit D0

FAST LOCK PIN SELECT

The previous example demonstrated how to setup profiles and select a profile using SPI commands. It is also possible to use hardware control to select a particular profile. The control input pins in this mode select the desired profile. This mode is enabled by setting Bit D1, fast lock profile pin select, in the receive register, Register 0x25A and/or the transmit register,

Register 0x29A, together with enabling fast lock mode in the same registers.

When this mode is set, CTRL_IN0 through CTRL_IN2 select the profile (if both pin select bits are set, profiles are selected in parallel). In the system design, note that the CTRL_INx pins are configurable for other functions as well, so they are not available for other functions simultaneously with this function.

ENABLE STATE MACHINE (ENSM) GUIDE

ENSM OVERVIEW

The AD9363 transceiver includes an enable state machine that allows real-time control over the current state of the device. The enable state machine has two possible control methods: SPI control and pin control.

The enable state machine is controlled asynchronously by writing SPI registers to advance the current state to the next state. The ENABLE and TXNRX pins allow real-time control of the current state. The enable state machine also allows either TDD or FDD operation.

The AD9361_SET_EN_STATE_MACHINE_MODE function configures the enable state machine.

In Figure 8, the shaded areas represent the various states that do not require user control and fall through to the next state after a set time. The to alert signal is a setting in the ENSM Configuration 1 register.

To move to the wait state, clear the to alert bit while in the receive or transmit states. In that configuration, when moving out of the receive, transmit, or FDD states, the enable state machine transitions to the wait state. The sleep state is the wait state with the AD9363 clocks disabled. To enter the sleep state, transition to the wait state, then disable the AD9363 clocks in the baseband PLL register.

ENSM Definitions

Table 13 lists the various states available in the enable state machine.

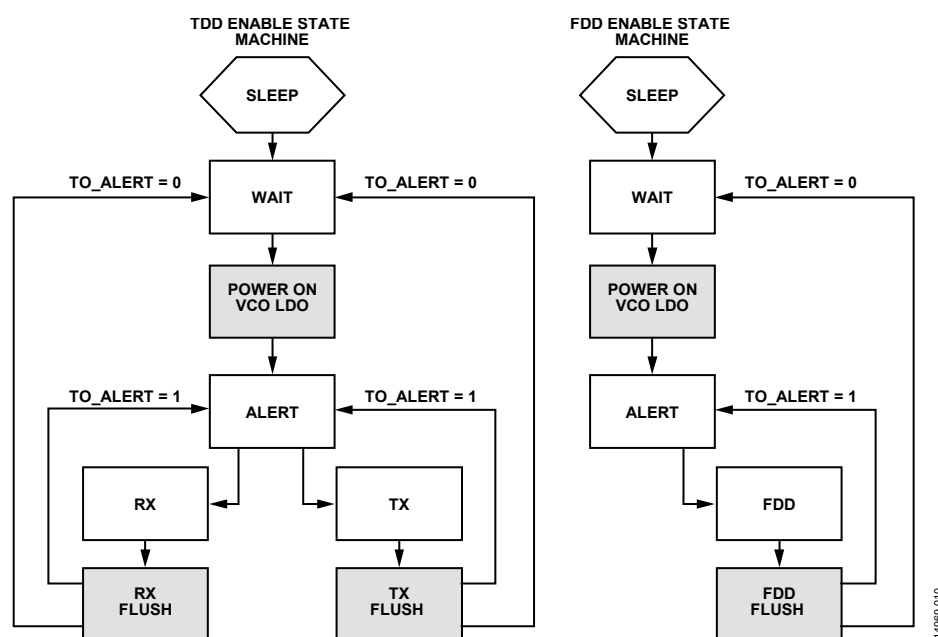


Figure 8. TDD and FDD Diagrams for the Enable State Machine

Table 13. Enable State Machine (ENSM) State Values

ENSM State Name	Value in ENSM State (Decimal)	Description
Sleep	0	Wait state, AD9363 clocks and baseband PLL are disabled.
Wait ¹	0	Synthesizers disabled (power saving mode).
Calibration	1, 2, 3	Calibration for a change in frequency.
Wait to Alert Delay	4	Fixed delay set by Register 0x024 and Register 0x025.
Alert	5	Synthesizers enabled.
Tx	6	Tx signal chain enabled.
Tx Flush	7	Time to allow the digital filters and signal path to flush.
Rx	8	Rx signal chain enabled.
Rx Flush	9	Time to allow the digital filters and signal path to flush.
FDD	10	Tx and Rx signal chains enabled.
FDD Flush	11	Time to allow the digital filters and signal path to flush.

¹ This state requires user interaction to move to the next state.

MODES OF OPERATION

The enable state machine can be controlled by SPI writes or via the ENABLE and TXNRX pins. SPI control is considered asynchronous to the data clock because the SPI clock can be derived from a different clock reference and continue to function properly. The SPI control enable state machine method is recommended when real-time control of the synthesizers is not necessary. SPI control can be used for real-time control as long as the baseband processor has the ability to perform timed SPI writes accurately.

Hardware (Pin) Control

The ENABLE/TXNRX pin control method is recommended when the baseband processor has extra control outputs that can be controlled in real time, allowing a simple 2-wire interface to control the state of the [AD9363](#) device. The ENABLE pin can be driven by either a pulse (edge detected internal to the [AD9363](#)) or a level to advance the current state of the enable state machine to the next state.

If a pulse is used on the ENABLE pin, it must have a minimum pulse width of one FB_CLK_x cycle. In level mode, the ENABLE and TXNRX pins are also edge detected in the [AD9363](#), and must meet the same minimum pulse width requirements of one FB_CLK_x cycle. For more information about using these pins, see the ENABLE/TXNRX Pin Control section.

SPI Control

SPI control is disabled by default and can be enabled in the Enable State Configuration 1 register. Once in the alert state, the [AD9363](#) enables its RF synthesizers for the transmitters and receivers. If, for some reason, the synthesizers do not calibrate correctly, the enable state machine is unable to transition to the receive or transmit states. This feature protects the [AD9363](#) from transmitting or receiving data when the synthesizers are not calibrated properly, protecting the wireless spectrum. When in the alert state and with the RF PLLs properly calibrated, the enable state machine is ready to move into the receive, transmit, or FDD state.

To move from alert to receive, set the force Rx on bit. To return to alert or wait, clear this bit. To move from alert to transmit or FDD mode, set the force transmit on bit. To return to alert or the wait state, clear this bit.

In FDD mode, the force Rx on bit is ignored. Whereas in TDD mode, the enable state machine must transition to the alert state between receive and transmit states. The enable state machine cannot move from receive directly to transmit, or from transmit directly to receive.

After sending the force alert state bit from the wait state, allow the enable state machine (ENSM) time to pass through ENSM State 4 before sending another command. The time for ENSM State 4 to complete depends on the time setting written into the receive and transmit load synthesizer delay registers. This delay is 2 μ s.

After sending the SPI write to exit the receive or transmit states, allow six ADC_CLK/64 clock cycles of flush time before sending another enable state machine SPI command. If a SPI command is received during an intermediate ENSM state, the command is ignored.

ENABLE/TXNRX Pin Control

ENABLE/TXNRX pin control mode is enabled by default. The ENABLE pin can operate with a pulse or a level to transition the ENSM state to the next state. In pulse mode, a pulse with a minimum width of one FB_CLK_x cycle is necessary to advance the current ENSM state. The baseband processor sends an ENABLE pulse to move into receive or transmit, and then another pulse when it is time to return to the alert or wait state.

In TDD, the state of the TXNRX pin controls whether the [AD9363](#) transitions from alert to receive or alert to transmit. If TXNRX is high, the device moves into the receive state. Set the TXNRX pin level during the alert state. The logic level of TXNRX must not change during the receive, transmit, or FDD states.

In level mode, the ENABLE pin level controls the ENSM state. The falling edge of the ENABLE pin moves the [AD9363](#) device into the alert state. TXNRX must be set or cleared while in the alert state. The rising edge of the ENABLE pin moves the [AD9363](#) into the receive state when TXNRX is low and into the transmit state when TXNRX is high. In FDD mode, the logic level of TXNRX is ignored.

The enable state machine exits the receive, transmit, or FDD states when the ENABLE pin is pulled back to a logic low. If the to alert bit is clear, the device moves from receive, transmit, or FDD to the wait state. To move from wait to alert in level mode, the baseband processor can drive a pulse on the ENABLE pin or perform a SPI write to the force alert state bit. If an ENABLE pulse is used, it must have a pulse width larger than one FB_CLK_x cycle wide. The rising edge of the ENABLE pulse advances the ENSM state from wait to alert. The falling edge of the ENABLE pulse is ignored in alert. See Figure 9 through Figure 12 for simplified diagrams. When moving from wait to alert, time must be allowed for State 4 to complete before sending another ENABLE pulse. The time required to wait depends on the Rx and Tx load synthesizer delay. Also, after the Rx, Tx, and FDD states, allow six ADC_CLK/64 clock cycles for each corresponding flush state to complete.

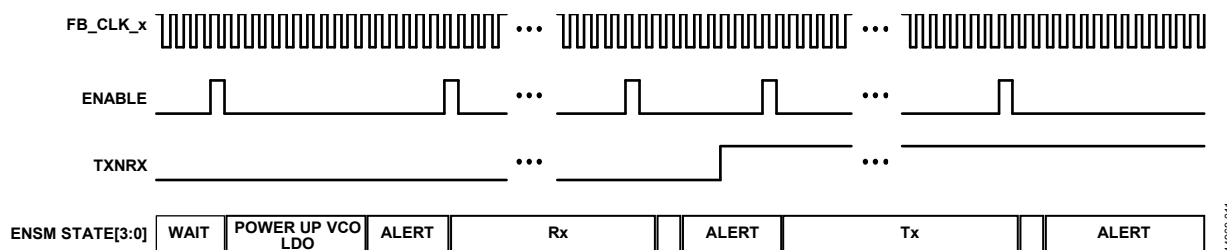


Figure 9. ENABLE Pulse Mode, TDD (Minimum Pulse Width = 1 FB_CLK_x Cycle)

14969-011

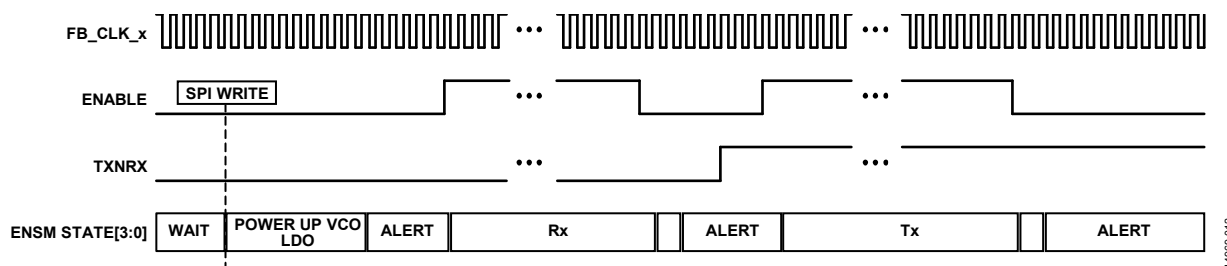


Figure 10. ENABLE Level Mode (TDD)

14969-012

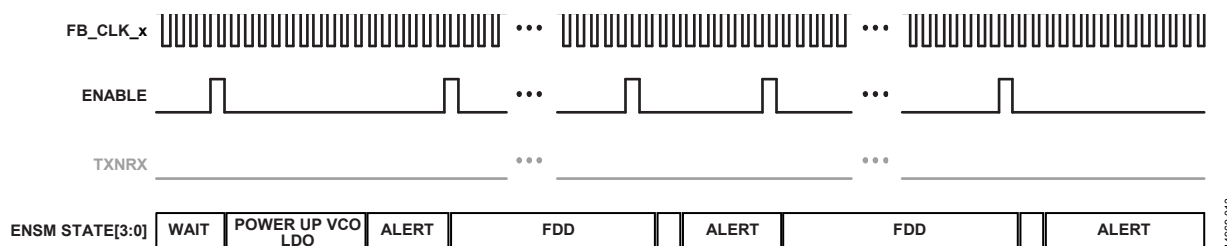


Figure 11. ENABLE Pulse Mode, FDD (Minimum Pulse Width = 1 FB_CLK_x Cycle)

14969-013

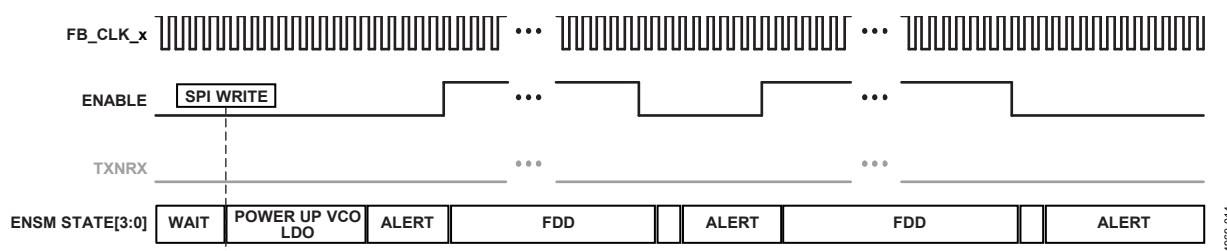


Figure 12. ENABLE Level Mode (FDD)

14969-014

FDD Independent Control

When the AD9363 is in FDD mode, the FDD independent control option allows the receive chain and transmit chain to be enabled independently. This mode is enabled by setting the FDD external control enable bit (Register 0x015, Bit D7). Note that SPI writes must be used to move the enable state machine into the FDD state.

The ENABLE and TXNRX pins are then internally remapped to force Rx on and force Tx on, respectively. Once in the FDD state, the control combinations that are listed in Table 14 are available.

Table 14. ENABLE/TXNRX Pin Alternative Functionality

Pin Level	Description
ENABLE Low, TXNRX Low	Rx and Tx signal chains disabled (operates like the alert state).
ENABLE High, TXNRX Low	Rx signal chain enabled, Tx signal chain disabled (operates like the Rx state).
ENABLE Low, TXNRX High	Rx signal chain disabled, Tx signal chain enabled (operates like Tx state).
ENABLE High, TXNRX High	Rx signal chain enabled, Tx signal chain enabled (operates like the FDD state).

Note that, because the enable state machine always remains in the FDD state, it never moves to the FDD flush state. Therefore, the baseband processor must allow enough time after enabling the receive chain for the digital filters to flush, and allow enough time after sending transmit data for the Tx to finish its transmission before disabling the corresponding signal chain. If TX_FRAME is held low, the data port in the [AD9363](#) forces zeros into the Tx datapath.

In pulse mode, the baseband processor sends pulses on the ENABLE pin to enable and disable the receive signal chain. Pulses sent on the TXNRX pin enable and disable the transmit signal chain.

When using a SPI write to move from alert into the FDD state, both the Rx and Tx signal chains start disabled until the first pulse is received. The pulse must have a minimum pulse width of one FB_CLK_x cycle. No maximum pulse width is defined; the pulse is edge detected and internally generates a one cycle wide pulse.

Enable State Machine and RF VCO Calibrations

The enable state machine controls an internal signal that tells the Rx and Tx synthesizers when to calibrate. In FDD mode, both the Rx and Tx synthesizers calibrate when moving from wait to alert and when the integer RF word is written; otherwise, the synthesizers remain powered on and locked.

Similar to FDD mode, in TDD mode, the enabled synthesizer (depending on the TXNRX logic level) calibrates when moving from wait to alert. When in the alert, receive, or transmit state, the enabled synthesizer (depending on the TXNRX logic level) calibrates when the integer frequency word is written in the SPI register map.

In TDD mode, the synthesizers do not remain locked. While in the receive state, the transmit synthesizer is disabled to save power. While in the transmit state, the receive synthesizer is disabled. However, in TDD mode, the enable state machine generates a signal to recalibrate the correct VCO when the state of TXNRX changes. This signal is issued from the enable state machine to the synthesizer after the delay in the Rx or Tx load synthesizer delay completes.

It is important to change the state of TXNRX as soon as the device moves into the alert state to allow time for the selected synthesizer to calibrate before moving into the receive or transmit states.

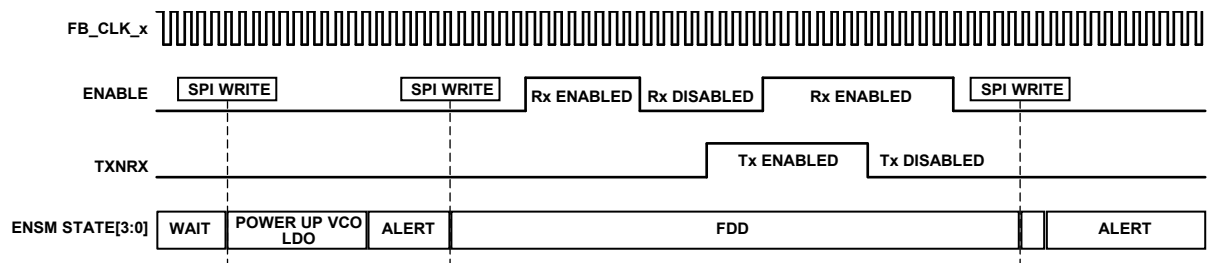


Figure 13. FDD Independent Control, Level Mode

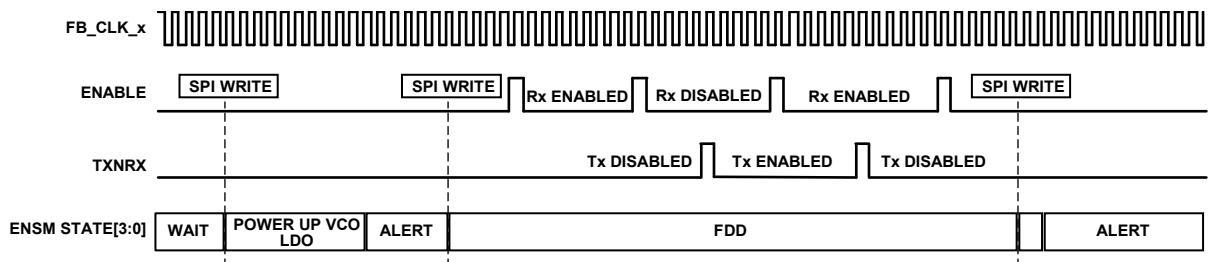


Figure 14. FDD Independent Control, Pulse Mode

SLEEP STATE

The AD9363 initially powers up in a very low power state, referred to as the sleep state. In this state, the AD9363 SPI registers are powered up; however, all internal clocks and other circuits are powered down. After power-up, the baseband processor programs the AD9363 using the SPI port and runs the internal calibrations necessary for optimal performance. After normal transmit/receive operation, if the AD9363 is not required for radio activity, the baseband processor can instruct the AD9363 to return to the sleep state to minimize power consumption.

The sleep state is technically the enable state machine (ENSM) wait state with the digital clocks turned off. When returning to the sleep state, all calibration results are stored because the AD9363 SPI registers remain powered up.

Sleep Procedure

The sleep procedure assumes that the device is currently in the alert state prior to beginning the sleep procedure. The sleep procedure is as follows:

1. Disable VCO calibrations to prevent VCO settings from being overwritten by possible automatic calibrations.
 - a. Perform an SPI write to Register 0x230 = 0x55 to set Bit 0 and disable the receive VCO calibration.
 - b. Perform an SPI write to Register 0x270 = 0x55 to set Bit 0 and disable the transmit VCO calibration.
2. Move the enable state machine from the alert to the wait state using the SPI port. Note that when using FDD operation, only the force Tx on bit controls the enable state machine. When using TDD operation, using the force Rx on bit limits the energy that is transmitted from the AD9363. In either case, power down the external power amplifier before moving the AD9363 into the FDD or Tx states.
 - a. Perform an SPI write to Register 0x014 = 0x00 to clear the alert bit (Bit 0).
 - b. Perform an SPI write to Register 0x014 = 0x20 to move the AD9363 to the FDD state by setting the force Tx on bit (Bit 5).
 - c. Wait. Wait for the FDD flush time (six ADC_CLK/64 clock cycles).
 - d. Perform an SPI write to Register 0x014 = 0x00 to move the AD9363 to the wait state by clearing Bit 5.
 - e. Perform an SPI write to Register 0x009 = 0x00 to turn off all clocks and place the AD9363 into the sleep state.

Wake-Up Procedure

To wake up the AD9363, take the following steps:

1. Enable the digital clocks and the baseband PLL.
2. Move the AD9363 into the alert state.
 - a. Perform an SPI write to Register 0x009 = 0x17 to turn on all clocks (assumes external clocks in this case).
 - b. Wait. Wait for the baseband PLL to lock in Register 0x05E, Bit 7 (locked = 1).
 - c. Perform an SPI write to Register 0x014 = 0x54, allow the Rx VCO calibration, and clear Register 0x230 (Bit 0).
 - d. Perform an SPI write to Register 0x270 = 0x54, allow the Tx calibration, and clear Register 0x270 (Bit 0).

Calibrations After Waking From Sleep

Although the previous calibration results are stored through the sleep state, some calibrations may need to be updated if time permits. For example, the AD9363 is normally set to track dc offset over time after it is in the receive state. The first time the AD9363 returns to the receive or FDD state, the dc offset may not be optimal. Running the RF dc offset calibration may improve the dc offset for the first time that the device reenters the receive state. Another advantage is that the calibration stores RF dc offset corrections for all front-end gain indexes. The tracking mode only allows the RF dc offset to update at the current gain index.

Time Division Duplex (TDD) Considerations

If using TDD operation, the receive VCO and/or transmit VCO (whichever is used first) must be calibrated before moving into the receive or transmit states by toggling TXNRX after enabling the VCO calibrations in Register 0x230 and Register 0x270. The TXNRX edge triggers the calibration to occur.

Frequency Division Duplex (FDD) Considerations

In FDD operation, a VCO calibration is not required.

FILTER GUIDE

FILTER GUIDE OVERVIEW

This section contains a description of the analog and digital filtering available in both the transmit and receive signal paths of the AD9363.

TRANSMIT SIGNAL PATH

The AD9363 transmit (Tx) signal path receives 12-bit twos complement data in I-Q format from the AD9363 digital interface, and each channel (I and Q) passes this data through four digital interpolating filters to a 12-bit DAC. Each of the four interpolating filters can be bypassed. The analog output of the DAC is passed through two low-pass filters prior to the RF mixer. The corner frequency for each low-pass filter is programmable using the AD9361_SET_TX_RF_BANDWIDTH function. Figure 15 shows a block diagram for the AD9363 Tx signal path. Note that both the I and Q paths are schematically identical to each other.

Overranging is detected in the Tx digital signal path at each state and limited to the maximum code value (preventing data wrapping). An overrange occurrence can be monitored in the overflow registers or at the control output pins.

Tx DIGITAL FILTER BLOCKS

The four blocks leading up to the DAC in Figure 15 comprise the digital filtering for the transmit path. These programmable filters provide the bandwidth limiting required prior to conversion from digital to analog. They also provide interpolation to translate from the input data rate to the rate needed for proper digital-to-analog conversion. In each filter, interpolation is performed first, followed by the filter transfer function.

Use the AD9361_CALCULATE_RF_CLOCK_CHAIN functions to configure the digital filters. The ADC sample clock, ADC_CLK, is the fastest signal path clock available in the digital processing section of the device; thus, it is used as the master clock reference for the digital filters in the Tx signal path. The sample clock of each fixed coefficient filter is always equal to the output data clock. The following sections describe the details of these blocks.

Tx FIR

The first digital filter in the transmit signal path is a programmable polyphase FIR filter (Tx FIR). The Tx FIR filter can also interpolate by a factor of 1, 2, or 4, or it can be bypassed

when it is not needed. This filter is controlled in the AD9361_SET_TX_FIR_CONFIG function. The filter taps are stored in 16-bit twos complement format, and the number of taps is configurable between a minimum of 16 taps and a maximum of 128 taps in groups of 16. The Tx FIR also has a programmable gain setting of 0 dB or -6 dB. Each coefficient is stored in two registers as a 16-bit number.

The Tx FIR uses the Tx DAC sample clock, DAC_CLK, as its sample clock. DAC_CLK is either set equal to ADC_CLK or is set to ADC_CLK/2. The Tx FIR calculates 16 taps per clock cycle. This limits the number of available taps to the ratio of DAC_CLK to the input data rate multiplied by 16. For example, with an input data rate of 25 MHz and DAC_CLK equal to 100 MHz, the ratio of the DAC_CLK to the input data rate is 100/25 or 4. In this scenario, the total number of taps available is 64.

Another limitation is the memory inside of the filter. The total number of operations that can be performed is limited to 64 per clock cycle. This means that the number of taps available is limited to 64 with an interpolation factor set to 1. If an interpolation rate greater than 1 is used, the memory space can be used to include more taps. Table 15 lists the allowable number of taps for each interpolation rate.

Table 15. Filter Taps Based on Interpolation Rate

Interpolation	Maximum Number of Taps
1	64
2	128
4	128

Tx HB1

Tx HB1 is a fixed coefficient, half-band interpolating filter. Tx HB1 can interpolate by a factor of 2, or it may be bypassed. Tx HB1 has the following coefficients: [-53, 0, +313, 0, -1155, 0, +4989, +8192, +4989, 0, -1155, 0, +313, 0, -53]. Note that the full-scale range for this filter is 8192 (2^{13}).

Tx HB2

Tx HB2 is a fixed coefficient, half-band interpolating filter. Tx HB2 can interpolate by a factor of 2, or it may be bypassed. Tx HB2 has the following coefficients: [-9, 0, +73, +73, 0, -9]. Note that the full-scale range for this filter is 128 (2^7).

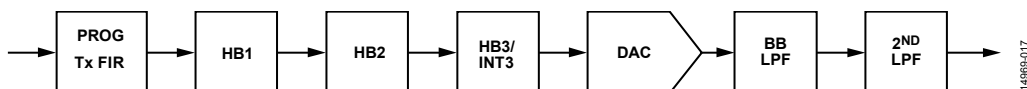


Figure 15. AD9363 Tx Signal Path

Tx HB3/INT3

Tx HB3/INT3 provides the choice between two different fixed coefficient interpolating filters. Tx HB3/INT3 can interpolate by a factor of 2 or 3, or it may be bypassed. Tx HB3 has the following coefficients: [+36, -19, 0, -156, -12, 0, +479, +223, 0, -1215, -993, 0, +3569, +6277, +8192, +6277, +3569, 0, -993, -1215, 0, +223, +479, 0, -12, -156, 0, -19, +36]. Note that the full-scale range for the Tx HB3 filter is 8192 (2^{13}). It is important to note that if the interpolation factor for this filter is set to 3, then the decimation factor for the Rx HB3/DEC3 filter must also be set to 3 to align the clocks properly.

Digital Tx Block Delay

The digital transmit (Tx) filter blocks are designed to minimize delay caused by mathematical operations so that the total delay is dominated by the inherent filter delays. The contribution of each block to the total data latency is approximated using the following relationship:

$$\Delta t_{DATA} = \frac{N}{2} \times \frac{1}{f_s} \quad (12)$$

where:

N is the filter order (number of taps).

f_s is the output sampling clock frequency (after any interpolation).

Tx ANALOG FILTER BLOCKS

Analog filtering after the DAC reduces spurious outputs by removing sampling artifacts and providing general low-pass filtering prior to upconversion. The corner frequency for these filters is programmed using the AD9361_SET_TX_RF_BANDWIDTH function call.

Tx Baseband Low-Pass Filter

The transmit (Tx) baseband low-pass filter is a third-order, Butterworth, low-pass filter with a programmable 3 dB corner frequency. The Tx baseband low-pass filter corner frequency is programmable over the range of 625 kHz to 16 MHz and is typically calibrated to 1.6× the baseband channel bandwidth.

Tx Secondary Low-Pass Filter

The transmit (Tx) secondary low-pass filter is a single-pole low-pass filter with a programmable 3 dB corner frequency. The Tx secondary low-pass filter corner frequency is programmable over the range of 2.7 MHz to 50 MHz and it is typically calibrated to 5× the baseband channel bandwidth.

Rx SIGNAL PATH

The AD9363 receive (Rx) signal path passes downconverted signals (I and Q) to the baseband receiver section. The baseband Rx signal path is composed of two programmable analog low-pass filters, a 12-bit ADC, and four stages of digital decimating filters. Each of the four decimating filters can be bypassed. Figure 16 shows a block diagram for the AD9363 Rx signal path. Note that both the I and Q paths are schematically identical to each other.

The digital Rx HB filters are sized to eliminate overranging. The Rx FIR filter can overrange based on the filter coefficients. The Rx FIR output is limited to the maximum code value when overranging occurs (preventing data wrapping). An overrange occurrence in the Rx FIR filter is indicated in the overflow register, or at the CTRL_OUTx pins.

Rx ANALOG FILTER BLOCKS

Analog filtering before the ADC reduces spurious signal levels by removing mixer products and providing general low-pass filtering prior to upconversion. The corner frequency for these filters is programmed using the AD9361_SET_RX_BANDWIDTH function call.

Rx TIA Low-Pass Filter

The receive (Rx) TIA low-pass filter is a single-pole low-pass filter with a programmable 3 dB corner frequency. The corner frequency is programmable over the range of 1 MHz to 25 MHz. The Rx TIA low-pass filter is typically calibrated to 2.5× the baseband channel bandwidth.

Rx Baseband Low-Pass Filter

The receive (Rx) baseband low-pass filter is a third-order Butterworth low-pass filter with a programmable 3 dB corner frequency. The corner frequency is programmable over the range of 200 kHz to 14 MHz, and it is typically calibrated to 1.4× the baseband channel bandwidth.

Rx DIGITAL FILTER BLOCKS

The four blocks following the ADC in Figure 16 comprise the digital filtering for the receive path. These programmable filters provide the bandwidth limiting and out of band noise and spurious signal reduction after digitization. They also provide decimation required to generate the correct data rates. In each filter, decimation is performed after the filtering occurs. ADC_CLK serves as the master clock reference for all digital filters in the receive signal path. The sample clock of each fixed coefficient filter is always equal to the input data clock. These digital filters are configured using the AD9361_CALCULATE_RF_CLOCK_CHAIN function.

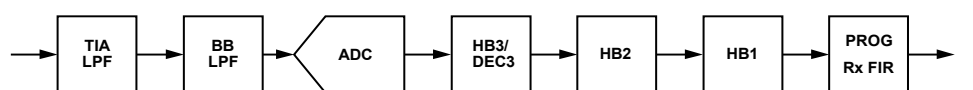


Figure 16. AD9363 Rx Signal Path

Rx HB3/DEC3

Rx HB3/DEC3 provides the choice between two different fixed coefficient decimating filters. Rx HB3/DEC3 can decimate by a factor of 2 or 3, or it may be bypassed. Rx HB3 has the following coefficients: [1, 4, 6, 4, 1], and Rx DEC3 has the following coefficients: [+55, +83, 0, -393, -580, 0, +1914, +4041, +5120, +4041, +1914, 0, -580, -393, 0, +83, +55]. Note that the full-scale range for the Rx HB3 filter is 16 (2^4), and the full-scale range for the Rx DEC3 filter is 16,384 (2^{14}). It is important to note that if the decimation factor this filter is set to 3, then the interpolation factor for the Tx HB3/INT3 filter must also be set to 3 to align the clocks properly.

Rx HB2

Rx HB2 is a fixed coefficient half-band decimating filter. Tx HB2 can decimate by a factor of 2 or it may be bypassed. Rx HB2 has the following coefficients: [-9, 0, +73, +128, +73, 0, -9]. Note that the full-scale range for this filter is 256 (2^8).

Rx HB1

Rx HB1 is a fixed coefficient half-band decimating filter. Rx HB1 can decimate by a factor of 2 or it may be bypassed. Rx HB1 has the following coefficients: [-8, 0, +42, 0, -147, 0, +619, +1013, +619, 0, -147, 0, +42, 0, -8]. Note that the full-scale range for this filter is 2048 (2^{11}).

Rx FIR Filter

The last digital filter in the receive signal path is a programmable polyphase FIR filter. The Rx FIR filter can also decimate by a factor of 1, 2, or 4, or it can be bypassed if it is not needed. The filter taps are configurable in groups of 16, between a minimum of 16 taps and a maximum of 128 taps. The taps are in 16-bit twos complement format. The Rx FIR also has a programmable gain of -12 dB, -6 dB, 0 dB, or +6 dB. The filter provides a fixed 6 dB gain to maximize dynamic range, so the programmable gain is typically set to -6 dB to produce a net gain of 0 dB. Each coefficient is stored in two registers as a 16-bit number.

The Rx FIR has two options for its sample clock, either ADC_CLK or ADC_CLK/2. The Rx FIR calculates 16 taps per clock cycle. This limits the number of available taps to the ratio of the sample to the output data rate of the filter multiplied by 16. For example, with an output data rate of 50 MHz and a sample clock at 200 MHz, the ratio of the sample clock to the output data rate is 200/50 or 4. In this scenario, the total number of taps available is 64.

Unlike the Tx FIR, the Rx FIR has enough internal memory to allow the maximum number of taps to be used for any decimation setting. This means that all 128 taps can be used if the previously described clock ratio is satisfied. This filter is setup using the AD9361_SET_RX_FIR_CONFIG function call.

DIGITAL Rx BLOCK DELAY

The digital Rx filter blocks are designed to minimize delay caused by mathematical operations so that the total delay is dominated by the inherent filter delays. Each contribution of the block to the total data latency is approximated using the following relationship:

$$\Delta t_{DATA} = \frac{N}{2} \times \frac{1}{f_s} \quad (13)$$

where:

N is the filter order (number of taps).

f_s is the input sampling clock frequency (before any decimation).

Example—LTE 10 MHz System

In this example, the receiver is set to operate in an LTE 10 MHz system using a 40 MHz reference clock. All 128 FIR filter taps are used and the data rate is set to 15.36 MSPS. To achieve this data rate with the given reference clock, each digital filter (Rx HB3, Rx HB2, Rx HB1, and the Rx FIR filter) have their decimation factors set to 2. The resulting sample clocks are as follows:

- Rx HB3 (4th-order filter) = 245.76 MHz
- Rx HB2 (6th-order filter) = 122.88 MHz
- Rx HB1 (14th-order filter) = 61.44 MHz
- Rx FIR (128th-order filter) = 30.72 MHz

The resulting data delay due to digital filter is

$$\begin{aligned} \Delta t &= 2 \times \left(\frac{1}{245.76 \text{ MHz}} + 3 \times \frac{1}{122.88 \text{ MHz}} + 7 \times \frac{1}{61.44 \text{ MHz}} + \right. \\ &\quad \left. 64 \times \frac{1}{30.72 \text{ MHz}} \right), \text{ or} \\ \Delta t &= 2.23 \mu\text{s} \end{aligned} \quad (14)$$

Note that the Rx FIR filter is the largest component of this value due to its large number of taps and lower sampling frequency. For rough estimate calculations, the half-band filters can be ignored, provided that the order of the Rx FIR filter is much larger than the orders of the half-band filters.

GAIN CONTROL

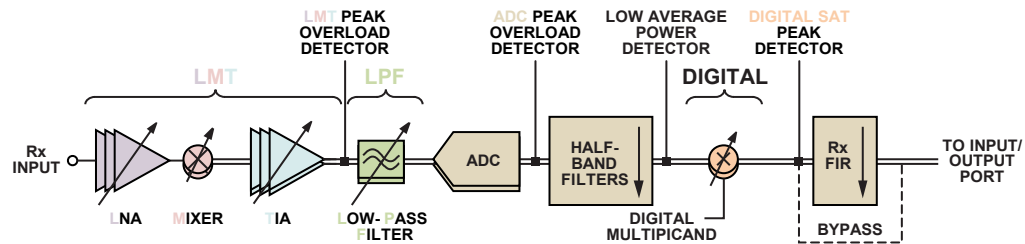


Figure 17. AD9363 Rx Signal Path

GAIN CONTROL OVERVIEW

The AD9363 transceiver has several gain control modes that enable its use in a variety of applications. Full AGC modes are available that address TDD and FDD scenarios. In addition, the AD9363 has manual gain control options that allow the baseband processor to control the gain of the receiver. The AD9361_SET_RX_GAIN_CONTROL_MODE function configures all of the gain control modes.

The AD9363 receive signal path can be separated into several blocks, as shown in Figure 17. The gain of almost all of the blocks is variable, as shown by the arrows through the shapes in Figure 17.

Each receiver has its own gain table that maps a gain control word to each of the variable gain blocks in shown in Figure 18. A pointer to the table determines the control word values sent to each block, as shown in Figure 18.

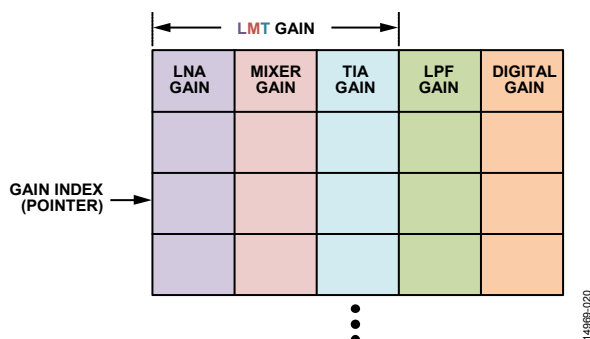


Figure 18. AD9363 Gain Table Mapping

Whether AGC or manual gain control is used, the pointer moves up and down the table, which changes the gain in one or more of the blocks shown in Figure 17.

The ADC maximum input (0 dBFS) is 0.625 V peak. However, to avoid compression, the maximum recommended peak input level to the ADC is 0.5 V peak, which is 1.9 dB lower than full scale.

GAIN CONTROL THRESHOLD DETECTORS

The AD9363 uses detectors to determine if the received signal is overloading a particular block or if the signal has dropped below the programmable thresholds. LMT and ADC overload detectors (also referred to as peak detectors) react to nearly instantaneous overload events. In contrast, a power measurement in the AD9363 occurs over 16 or more Rx samples. Figure 17 shows the location of these in the signal path.

LMT OVERLOAD DETECTOR

The LNA/mixer/transimpedance amplifier (LMT) overload detector is an analog peak detector that determines if the received signal is overloading the blocks before the analog low-pass filter. If an LMT overload occurs but the ADC does not overload, it may indicate that an out of band interfering signal is resulting in the overload condition.

There are two different LMT overload thresholds, one to indicate larger overloads and one to indicate smaller overloads. Both thresholds are programmable and are configured in the AD9361_SET_RX_GAIN_CONTROL_MODE function. Set the small threshold such that it is lower than or equal to the large threshold because the AGC is affected differently, depending on which threshold is exceeded. In manual gain control mode, the baseband processor can monitor the overload flags via the control output pins. Equation 15 describes both large and small thresholds.

$$\text{LMT Overload Threshold (mV peak)} = 16 \text{ mV} \times (\text{LMT Overload Threshold}[5:0] + 1) \quad (15)$$

ADC OVERLOAD DETECTOR

The ADC is a highly oversampled Σ - Δ modulator with an output ranging from +4 to -4. A particular ADC output sample does not necessarily represent the input signal at a particular time. Rather, a positive value indicates that the input signal is more positive since the last sample and a negative value indicates that the input signal is more negative since the last sample. Because the ADC is highly oversampled, the ADC clock is much faster than the receive sample rate. Decimating and low-pass filtering result in digital samples that represent the analog signal.

When the ADC is overloaded, the error between its samples and the input signal causes the ADC to output more samples with values of +4 or -4 as it struggles to track the input signal. Figure 19 shows how the ADC overload detector processes signals and how the thresholds are used.

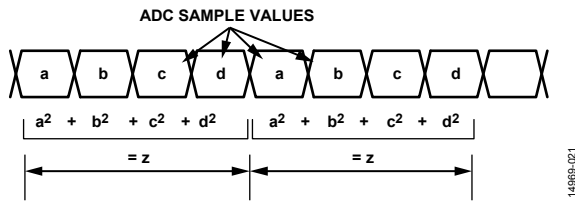


Figure 19. ADC Overrange Detection Algorithm

There are two programmable thresholds that are both configured in the AD9361_SET_RX_GAIN_CONTROL_MODE function. The thresholds are common to both receivers. The number of samples to use in the sum of squares calculation is also set in the AD9361_SET_RX_GAIN_CONTROL_MODE function. The resulting value, z , shown in Figure 19, is compared against the two thresholds, and if a particular threshold is exceeded, a flag is set. In manual gain control mode, the baseband processor can monitor the overload flag(s) via the control output pins.

LOW POWER THRESHOLD

The low power threshold is an absolute threshold measure in -dBFS with a resolution of 0.5 dBFS per LSB. The range is from 0 dBFS to -63.5 dBFS. The value is programmed with the AD9361_SET_RX_GAIN_CONTROL_MODE function. The AD9363 uses this threshold in the fast attack AGC mode, and it can also be used in manual gain control mode, both of which are describe in the Fast Attack AGC Mode section and the Manual Gain Control Mode Overview section.

In fast attack AGC mode, the low power flag does not assert immediately after the average signal power drops below the low power threshold. The flag asserts only after the signal power remains below the low power threshold for a time equal to the increment time. The increment time value is measure in CLKRF cycles (the clock used at the input of the Rx FIR filter).

In manual gain control mode, the increment time value is not used and the low power flag asserts as soon as the power drops below the low power threshold.

AVERAGE SIGNAL POWER

When measuring power, such as for low power threshold, the measurement is an average of a certain number of samples set by the decimated power measurement duration set in the AD9361_SET_RX_GAIN_CONTROL_MODE function. The duration is common to both receivers. At the end of each measurement period, the average signal power value updates. The actual duration in receive sample periods is expressed in Equation 16.

$$\text{Power Measurement Duration (Rx Sample Periods)} = 16 \times 2^{\text{Decimation Power Measurement Duration}[3:0]} \quad (16)$$

SETTLING TIMES

After a gain change, the AD9363 must reset overload detectors and power measurement circuits and wait for the receive path to settle before reenabling detectors and power measurement blocks.

PEAK OVERLOAD WAIT TIME

All gain control modes use peak overload wait time. After a gain change, the AD9363 waits for the time set by this register before reenabling its LMT and ADC overload detectors, allowing the signal in the analog path and the ADCs to settle. The default is fine for all applications, unless an external LNA with a bypass mode is part of the signal path. The peak overload wait time is set using the AD9361_SET_RX_GAIN_CONTROL_MODE function and is clocked at the CLKRF rate (the input to the Rx FIR filter clock rate).

SETTLING DELAY

All AGC modes use settling delay, which is the time that the AGC holds the power measurement blocks in reset after a gain change. Power measurement occurs at the output of the receive (Rx) HB1 filter, which is the input to the Rx FIR filter, so that all stages up to the Rx FIR must be settled before power measurement resumes after a gain change.

The delay is equal to the register value multiplied by two, and is clocked at the CLKRF rate. The default for settling delay is 20 CLKRF cycles and is based on a CLKRF rate of 30.72 MHz. For optimum fast attack AGC performance, the delay must scale with CLKRF (see Equation 16).

GAIN TABLE OVERVIEW

The AD9363 uses a pointer to a row in a gain table. That row contains the gain values of each independent gain block. In this way, a gain index value (pointer) maps to a set of gain values for each gain block. However, there are two different ways that the AD9363 can implement the gain table.

In full table mode, there is one table for the receiver. In split table mode, the AD9363 splits the LMT and low-pass filter tables apart and controls each independently with separate pointers. If digital gain is enabled, there is a third table that is independently controlled, also with its own pointer.

Each receiver has its own set of two (or three) tables. The gain table mode is set in the AD9361_LOAD_GT_FUNCTION. The table architecture affects all gain control modes and is a common setting for both receivers.

Full Table Mode

Full table mode is useful for most situations. A single gain table contains all of the variable gain blocks in the receive signal path. Figure 20 shows a portion of a full gain table. The figures also shows the gain of each block next to each gain index. If the gain index moves up or down, the gain indices of one or more blocks changes.

If the gain index pointer moves down one step (to a table index of 54), both the LNA gain and the low-pass filter gain change. These changes allow the AD9363 to handle widely varying signal levels yet optimize noise figure and linearity.

To read back the full table gain index in any gain control mode, use the AD9361_GET_RX_RF_GAIN function. The maximum LMT/full gain register limits the maximum index allowed.

Split Table Mode

In situations where high power out of band interfering signals are often present, it can be advantageous to split the gain table to optimize noise figure in the presence of these interferers. In this case, separate pointers control the LMT gain and the low-pass filter gain independently (and digital gain if it is enabled). This allows the gain to be changed in the area of the receive path that is overloading. Recall that for the full gain table, gain changes could affect any or all of the gain blocks in the receive path, regardless of where the overload occurs.

The architecture of the LMT table depends on which gain control mode is used; this aspect is covered in the next sections, including

the details of the various gain control modes. An LMT table must be written to the AD9363 using the AD9361_LOAD_GT function. A low-pass filter table, per se, does not exist. Instead, the low-pass filter index directly translates to low-pass filter gain in dB. The same is true of digital gain (when it is enabled). Low-pass filter gain ranges from 0 to 24 (decimal) whereas digital ranges, as mentioned previously, range from 0 to 31 (decimal).

The total gain in dB of the AD9363 is not necessarily equal to the LMT and low-pass filter indices added together. The actual gain of the LMT stages vary with LO frequency and, in addition, some of the LMT steps are larger than 1 dB. Thus, changing the LMT index by one may not change the gain by 1 dB. This concept is easier to understand when looking at the tables.

The maximum index when using the split table mode is 40 (decimal).

To read back the split table gain indices in any gain control mode, use the AD9361_GET_RX_RF_GAIN function.

Table 16. Reading Split Table Gain Indices

Register	Function
0x2B0, Bits[D6:D0]	Rx1 LMT gain index
0x2B1, Bits[D4:D0]	Rx1 low-pass filter gain index
0x2B2, Bits[D4:D0]	Rx1 digital gain index (when enabled)
0x2B5, Bits[D6:D0]	Rx2 LMT gain index
0x2B6, Bits[D4:D0]	Rx2 low-pass filter gain index
0x2B7, Bits[D4:D0]	Rx2 digital gain index (when enabled)

TABLE INDEX	LNA INDEX	LNA GAIN	MIXER INDEX	MIXER GAIN	TIA INDEX	TIA GAIN	LPF INDEX	LPF GAIN	DIGITAL INDEX	DIGITAL GAIN	TOTAL GAIN (dB)
54	2	17	4	15	1	0	17	17	0	0	49
55	3	21	4	15	1	0	14	14	0	0	50
56	3	21	4	15	1	0	15	15	0	0	51

Figure 20. Portion of the Analog Devices 2300 MHz Full Gain Table Example

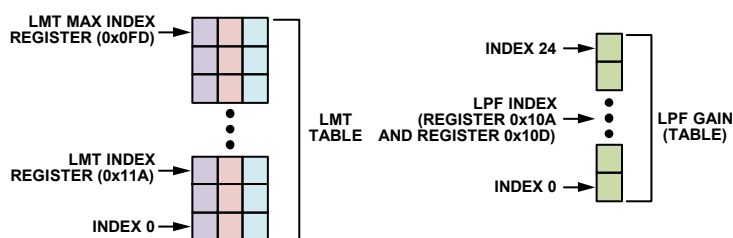


Figure 21. Split Table in Manual Gain Mode, SPI Writes Control Gain Indices

DIGITAL GAIN

All modes (manual gain control and AGC) and both gain table modes allow the addition of digital gain. The maximum allowable index for a full gain table is 90 (decimal). The maximum digital index is 31 (decimal). A standard full gain table with only analog gain has a maximum index of 76 (decimal). For the gain tables provided by Analog Devices, this leaves 24 (decimal) indices for digital gain. Alter-native gain tables that reach their maximum analog gain at an index lower than 76 (decimal) can accommodate more digital gain steps (up to 31).

It is important to note that digital gain does not increase the signal-to-noise ratio (SNR) because it merely multiplies the digital word by a factor. In this way, both noise and signal are increased and the SNR remains the same. For many applications, digital gain is not required. Further, modifying the gain table and sacrificing analog gain to add more digital gain decreases system performance.

In some cases, however, it is desired that the signal power received by the baseband processor be equal to some nominal value. For very low signal levels in which the maximum analog gain is still not high enough to achieve this goal, use variable digital gain.

MANUAL GAIN CONTROL MODE OVERVIEW

In manual gain control mode, the baseband processor controls the gain index pointer(s). This mode is setup with the AD9361_SET_RX_GAIN_CONTROL_MODE function. In its simplest form, in manual gain control mode, the baseband processor evaluates the digital signal level at the input/output (I/O) port and then adjusts the gain appropriately. In this scenario, the baseband processor needs no other information beyond the digital signal level that it receives. For the full (single) gain table, this is all that is needed—an overload requires that the gain be decreased.

However, the AD9363 has programmable thresholds that indicate the condition of the signal in each receiver. Routing these signals to the control output pins and then connecting them to the baseband processor inputs allows the baseband processor to determine the status of the received signals in more detail. For a split gain table, this information allows the baseband processor to adjust the gain in the area that is overloading because it indicates where the overload is occurring (LMT, low-pass filter, or digital).

The baseband processor can control manual gain in one of two ways. The default method uses SPI writes of the gain indices. Alternatively, the baseband processor can pulse the control input pins to move the gain indices. CTRL_IN0 causes the gain index to increase for Rx1 and CTRL_IN1 causes the gain index to decrease for TX1. Similarly, CTRL_IN2 causes the gain to increase for Rx2 and CTRL_IN3 causes the gain to decrease for Rx2. This mode can be configured using the AD9361_SET_RX_GAIN_CONTROL_MODE function. The pulse is asynchronous; therefore, setup and hold are not relevant but the time,

high and low, must be at least two CLKRF cycles for the AD9363 to detect the event. CLKRF is the clock used at the input of the receive FIR filters.

In full table mode, a single index for the receive controls the gain. If SPI writes control the gain, then writing the registers sets the gain index directly. If the control input pins control the gain, then pulsing the various pins moves the gain index pointer(s) up and down the full table.

In split table mode, if the baseband processor uses SPI writes to control the gain, then separate register writes are needed to set the LMT and low-pass filter gain indexes. Digital gain (when enabled) requires a third register write. If the baseband processor uses the control inputs to change the gain in split table mode, then there are two options. There are only four control inputs but there are eight different analog gain adjustments to make (low-pass filter, LMT, Rx1, Rx2, increment, and decrement for each). One option is to use a SPI bit to determine where the gain index changes (LMT or low-pass filter). Clearing Bit D3 in Register 0x0FC (use AGC for LMT/LPF gain bit) enables this option. Bit D4 in Register 0x0FC (increment/decrement LMT gain bit) selects the gain change location. For this option, the gain table architecture still looks like that in Figure 20. When digital gain is enabled, the baseband processor must change this gain via SPI writes; the CTRL_INx pins do not change digital gain in split table mode.

Alternatively, if the AGC for LMT/LPF gain bit is set, the AD9363 peak detectors determine where the gain changes. In this option, the architecture of the split table changes, as shown in Figure 21.

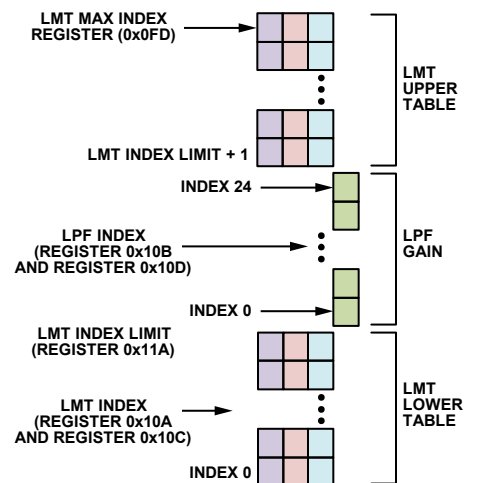


Figure 22. Split Table in Manual Gain Mode, Control Inputs and Peak Detectors Control Gain Indices

Note that the LMT table is split into two sections: an upper LMT table and a lower LMT table. The dividing line is the initial LMT gain limit.

Additionally, where overloads occur (and where the gain indices are currently pointing) affects where the gain changes, as noted in Table 17. As the table demonstrates, the algorithm decreases LMT gain first and then, when the LMT index reaches the LMT index limit, the type of overload determines where the gain decreases. Increment and decrement registers

(Register 0x0FC and Register 0x0FE) set the amount of gain change.

If more than one overload condition occurs simultaneously, the LMT overloads are first priority, ADC overloads are second, and digital saturation is third.

Table 17. Manual Gain Split Table Gain Change Location vs. Index Position and Overload Location

Overload Type	Gain Index Position(s)	Change Gain In
Large LMT	LMT index > 0	LMT table
	LMT index = 0	LPF table
Large or Small ADC	LMT index is in upper LMT table (index > initial LMT gain limit)	LMT table
	LMT index is in lower LMT table (index ≤ initial LMT gain limit)	LPF table
Digital Saturation	Not applicable	Digital table

SLOW ATTACK AGC MODE

Slow attack AGC mode is intended to slowly change signals, such as those found in FDD applications (for example, WCDMA and FDD LTE). The slow attack AGC uses a second-order control loop with hysteresis that changes the gain to keep the average signal power within a programmable window. The power is measured between HB1 and the Rx FIR filter. This is the same location as the low power detector in Figure 17. In addition, the baseband processor can set bits to enable faster reactions for signals that exceed the LMT and ADC thresholds. Enable slow attack AGC mode using the AD9361_SET_RX_GAIN_CONTROL_MODE function.

Figure 23 shows the concept of the control loop; inner high threshold values and inner low threshold values are stored in negative dBFS. The outer high threshold and outer low threshold are stored as dB deltas to the inner thresholds. The A, B, C, and D step sizes are programmable. These step sizes determine how much the gain index pointer changes after the average signal power exceeds a threshold.

Note that the AD9363 does not have default thresholds or step sizes. The baseband processor must write all of these values using the AD9361_SET_RX_GAIN_CONTROL_MODE function.

SLOW ATTACK AGC GAIN UPDATE TIME

When the average signal power exceeds a threshold, the gain does not necessarily change immediately. In FDD systems, there are typically brief periods (such as those around slot boundaries) that accommodate gain changes or other system parameter updates.

To accommodate this aspect of FDD protocols, the AD9363 gain updates only after the gain update counter expires. The counter is clocked at the CLKRF rate (the input rate of the RFIR). The depth of the counter can be set equal to the value in the gain update counter register.

The counter clock begins running three clock cycles after the AD9363 enters the receive state. Because the baseband processor is responsible for moving the AD9363 among its states, it can determine when the gain update counter expires. In this way, the gain update counter can be set such that it always expires at slot (or other) boundaries. Additionally the baseband processor can reset the gain update counter by setting the enable sync for gain counter bit and taking CTRL_IN2 high.

The slow AGC mode is typically configured to have multiple power measurement cycles within each gain update period. The last power measurement performed before a gain update boundary determines whether (and by how much) the gain changes.

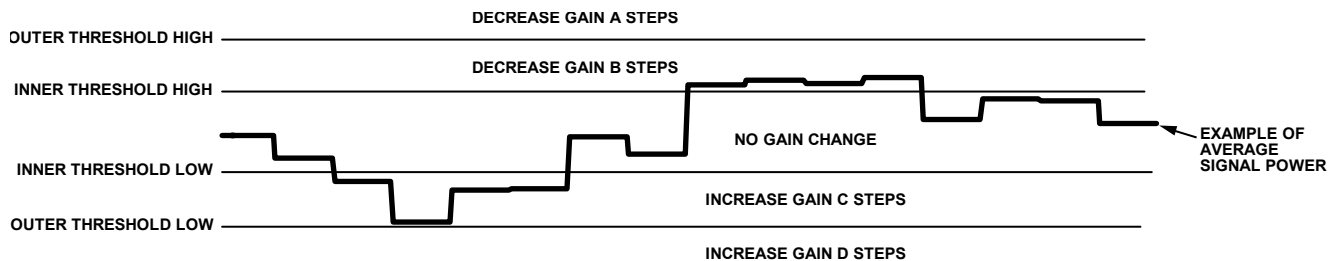


Figure 23. Slow Attack AGC Control Loop Limits and Step Sizes

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OVERLOADS IN SLOW ATTACK AGC MODE

In addition to the control loop discussed previously, the slow attack AGC can react more quickly to peak overload events such as the large LMT and large ADC overloads.

In slow attack mode, the [AD9363](#) counts the number of times a particular overload event occurs. Only if the event(s) occur more than a programmable number of times does the gain change. Even for these peak overloads, the gain only changes when the gain update counter expires. The counters are stored as the LMT and ADC overload counters. The [AD9363](#) does not have default values for these counters so the baseband processor must write all of these values using the `AD9361_SET_RX_GAIN_CONTROL_MODE` function.

During the a gain change event, the highest priority is given to the large LMT detector, followed by the large ADC detector, and followed lastly by the power detectors used by the second-order window control loop.

It is also possible to set up the [AD9363](#) such that large LMT overloads and/or large ADC overloads result in an immediate gain change, ignoring the gain update counter. This mode is set with Bit D7 (immediate gain change if large LMT overload) and Bit D3 (immediate gain change if large ADC overload), both in SPI Register 0x123.

If the average signal power falls below one or both of the control loop low thresholds (which normally results in a gain increase)

but one or both of the small peak overload detectors (LMT or ADC) has tripped, setting Bit D7 (prevent gain increase) in Register 0x120 prevents the gain from increasing. Like LMT and ADC overloads, the [AD9363](#) uses a counter to determine how many times digital saturation has occurred. This counter is the digital saturation exceeded counter (Bits[D3:D0] of Register 0x128), and if it is exceeded, the gain index is reduced.

SLOW ATTACK AGC AND GAIN TABLES

In full table mode, a single table controls the gain of all Rx signal path stages. Table 18 shows the effect of peak overloads (after their associated counters are exceeded). Recall that a particular overload condition results in the gain index moving a programmable number of steps but the gain may change in any number of different gain blocks.

In split table mode, the gain table is split as described previously and as shown in Figure 21.

In a split table, there are two independent index pointers for analog gain and one additional pointer for digital gain (if enabled). Table 19 describes the effect of various peak overload conditions, identical to the split table shown in the Gain Table Overview section. If the gain changes in the LPF table, the LPF step size used is decrement step size for large LPF gain changes, as defined in the [AD9363 Register Map Reference Manual](#).

Similarly, if the gain is changed in the LMT table, the step size used is decimated step size for large LMT overload

Table 18. Slow Attack AGC Full Gain Table Overload Steps

Peak Overload	Reduce Gain by Number of Indices (Step Size)	Step Size Location
Large LMT	Decrement step size for large LMT Overload	Step size for: large LMT overload/Full Table Case 3
Large ADC	Decrement step size for large LPF gain change	Decrement step size for: large LPF gain change/Full Table Case 1
Digital Saturation	Digital gain step size + 1	Digital gain step size

Table 19. Slow Attack/Hybrid AGC Split Gain Table Overload Steps

Overload Type	Gain Index Position(s)	Change Gain Table
Large LMT	LMT index > 0	LMT table
Large LMT	LMT index = 0	LPF table
Large or Small ADC	LMT index is in upper LMT table (index > initial LMT gain limit)	LMT table
Large or Small ADC	LMT index is in lower LMT table (index ≤ initial LMT gain limit)	LPF table
Digital Saturation	Not applicable	Digital table

HYBRID AGC MODE

Hybrid AGC mode is the same as slow AGC mode, with the exception that the gain update counter is not used. Instead, gain updates occur when the baseband processor pulls the CTRL_IN2 signal high. The hybrid term arises because the baseband processor takes some control of the algorithm away from the AD9363, so that gain control is no longer completely automatic. Hybrid mode is enabled with the AD9361_SET_RX_GAIN_CONTROL_MODE function.

FAST ATTACK AGC MODE

Fast attack AGC mode is intended for waveforms that burst on and off, such as those found in TDD applications or GSM/EDGE FDD applications. The AGC responds quickly to overloads at the start of a burst so that the AGC can settle to an optimum gain index by the time the data portion of the signal arrives. The AGC also has an optional slow decay that allows the gain to increase if the signal power decreases while the AGC is locking to an optimum gain. Fast attack mode is configured with the AD9361_SET_RX_GAIN_CONTROL_MODE function.

When the AD9363 enters the Rx state, the fast attack AGC state machine leaves State 0 and enters State 1, as shown in Figure 24. The goal of the state machine is to adjust the gain index to realize the optimum receive gain in a short period. The AGC progresses through several states on its way to gain lock, in which state the gain does not change (unlock) unless large signal level changes occur or if the burst ends. When the gain unlocks, the AGC state machine returns to its reset state and restarts. Figure 24 shows a high level diagram of the AGC states.

STATE 0—RESET

The AGC remains in State 0 when the AD9363 is not in the Rx state. The AGC performs no actions while in this state.

STATE 1—PEAK OVERLOAD DETECT

When the AD9363 enters the Rx state, the AGC first waits for a time in microseconds set by the AGC attack delay register. This delay allows the receive path to settle before the AGC begins determining the optimum gain index.

After this delay, the AGC enters State 1, where it detects peak overloads (LMT and ADC) and adjusts the gain. The digital saturation detector is also enabled, but in State 1 the signal may not have enough time to reach the detector. Each time the gain changes, the AD9363 holds the peak detectors in a reset state until the peak overload wait time counter expires. If no peak overloads are detected for the energy detect count, then the AGC can proceed to State 2. The energy detect count is clocked at the CLKRF rate (the clock used at the input to the Rx FIR filter).

The overloads affect the gain index in different ways for different gain table types, as shown in the Table 20 and Table 21. In full gain table mode, the AD9363 uses different step sizes (changes in gain index) for differing extremes of overload. Table 20 shows where the step sizes are stored for the fast attack AGC in full table mode.

The Case 1 step size is typically larger than Case 2, which itself is typically larger than Case 3.

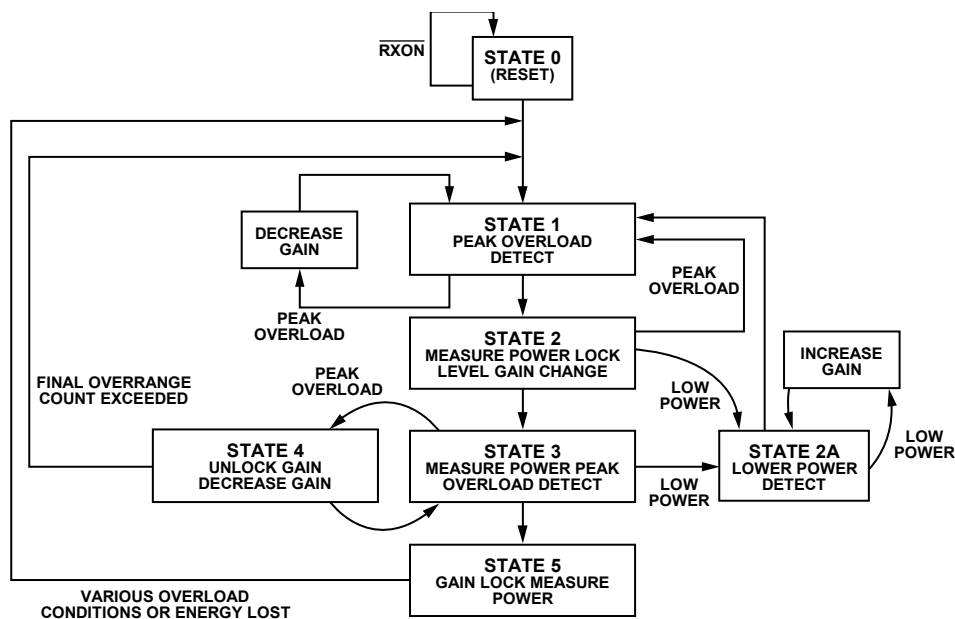


Figure 24. Fast Attack AGC High Level Stage Diagram

Table 21 shows the effects of various overloads when using a split table. Figure 25 shows the split table architecture. Note that the gain first decreases from the LMT table regardless of where the overload occurs. When the gain index reaches the LMT index limit, the gain decreases where the overload occurs.

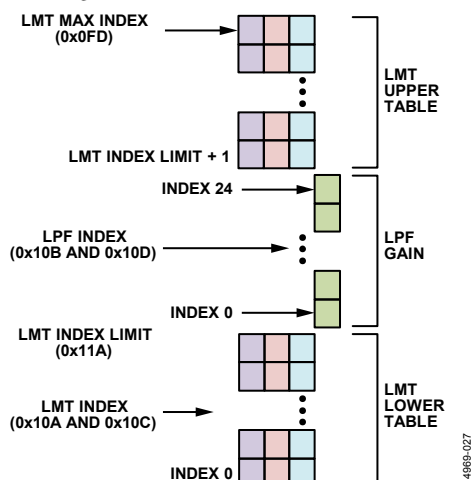


Figure 25. Fast AGC Split Gain Table Architecture

STATE 2—MEASURE POWER AND LOCK LEVEL GAIN CHANGE

Upon entering State 2, the AGC waits for a time equal to settling delay minus energy detect count. The subtraction is performed because the AGC has already waited for the energy detect counter to expire to exit State 1. Thus, the delay before measuring power does not need to repeat the count through this delay. After the delay is calculated, the AGC measures average signal power at the output of the HB1 filter (see the Average Signal Power section).

The AGC keeps the LMT, ADC, and digital saturation overload detectors enabled while it is in State 2. If overloads occur, the AGC returns to State 1 to reduce the gain.

If the enable increase gain bit (Register 0x110, Bit D0) is set, then the AGC is allowed to increase gain if the average signal power stays below the low power threshold for a time greater than the increment time. The gain step size used is as follows: increment gain step + 1. The gain continues to increase until the signal does not remain below the low power threshold longer than the increment time. Figure 24 shows this as State 2A. The AGC exits State 2A by returning to State 1 to recheck for peak overloads.

If the AGC enters State 2 and does not detect a low power condition, or the enable increase gain bit (Bit D0) is cleared, then the measured signal power is compared against the AGC lock level (fast). The AGC then adjusts the gain to match the average signal power to the AGC lock level setting. The lock level is stored in $-dBFS$ in a resolution of 1 dB/LSB. If the gain must increase to achieve the lock level setting, there is a maximum amount that it can increase, set by the AGC lock level maximum increase bits (SPI Register 0x118, Bits[5:0]).

In the full gain table mode, the AGC simply changes the gain index such that the signal power matches the lock level (unless limited by the AGC lock level maximum increase bits (Bits[5:0])). In split table mode, if the enable LMT gain increase for lock level bit (Register 0x111, Bit D6) is set high, the actions are per Table 22. If Bit D6 is not set high, then only LPF gain can be used for gain increases. In addition, regardless of the bit setting, if a small LMT overload occurs during the lock level calculation, LMT gain cannot increase to meet the lock level.

Table 20. Fast Attack AGC Peak Overload Step Sizes for Full Gain Table .

Peak Overloads	Reduce Gain by this many Indices (Step Size)	Step Size Set By
Large ADC, Large LMT, or Digital Saturation	Decrement step size for Full Table Case 1 Fast attack only; decrement step size for Full Table Case 2	Register 0x106, Bits[D3:D0] Register 0x106, Bits[D6:D4]
Small ADC	Decrement step size for Full Table Case 3	Register 0x103, Bits[D4:D2]

Table 21. Fast Attack AGC Peak Overload Step Sizes for Split Gain Table

Overload Type	Gain Index Position	Change Gain In
Large LMT	Not applicable	LMT table
Large or Small ADC	LMT index is in upper LMT table (index > initial LMT gain limit) LMT index is in lower LMT table (index ≤ initial LMT gain limit)	LMT table LPF table
Digital Saturation	Not applicable	Digital table

Table 22. Fast Attack AGC Lock Level Gain Index Change for Split Gain Table

If the Gain Must	Do This First	And If	Then Do This
Decrease	Reduce LPF gain index	LPF gain index = 0	Reduce LMT gain index
Increase	Increase LMT gain up to LMT step size	Total gain change > LMT step size	Increase LPF gain index

STATE 3—MEASURE POWER AND PEAK OVERLOAD DETECT

When the AGC enters State 3, it locks the gain. This state can affect other portions of the [AD9363](#) such as dc offset tracking updates and RSSI measurement start times.

The AGC continues to measure power and it keeps its large LMT, large ADC, and digital saturation overload detectors enabled.

If the enable gain increase after gain lock bit (Register 0x110, Bit D7) is set and the enable increase gain bit (Register 0x110, Bit D0) is set, then the AGC checks for a low power condition. This method is the same as that used in State 2 (including the transition to State 1 if the gain must increase). If Bit D7 is clear, the AGC does not perform the low power test in State 3. If the AGC exits State 3 due to a low power condition, the gain unlocks.

When the thresholds have been set correctly, the overload detectors do not assert even after the lock level adjustment, unless the signal of interest (SOI) level increases or an out of band blocker is suddenly present. To guard against these possibilities, the AGC monitors its overload detectors. If overloads occur after the lock level adjustment, the AGC uses different step sizes to change the gain.

In full gain table mode, regardless of the type of overload, the step size (number of indices reduced) is always the post lock level step size for full table value. In split gain table mode, the step size is the post lock level step size for the LPF table for ADC overloads, and the post lock level step for the LMT table for LMT overloads.

These step sizes are usually smaller than those used in State 1 and State 2. State 1 and State 2 overload step sizes are designed to respond to large overloads quickly. Any potential overload occurring in State 3 is normally smaller and requires less adjustment.

STATE 4—UNLOCK GAIN

If LMT or ADC overloads occur, the AGC decreases gain in State 4. The gain unlocks while the AGC is in State 4. The AGC then returns to State 3.

The AGC counts the number of overload conditions that occur after the lock level adjustment. If this number exceeds the final overrange count, then the AGC returns to State 1 and resets its peak detectors.

STATE 5—GAIN LOCK AND MEASURE POWER

When the AGC reaches State 5, the AGC locks the gain (if it was unlocked). The AGC also measures the average signal power when the gain locks and stores this value as a reference power level. This value is used for comparisons against other thresholds, which can unlock the gain. State 5 is the final state in the AGC algorithm and is intended to maintain the same gain as in State 4, unless a large change in signal amplitude occurs (such as the end of the burst or subframe, or a large interfering signal suddenly arrives or departs). In State 2 and State 3, the measurement length is set by Bits[D3:D0] in Register 0x15C (decimate power measurement duration, refer to the [AD9363 Register Map Reference Manual](#)). In State 5, the measurement length is set by Bit D7 in Register 0x109 (power measurement in State 5 bit). The mapping of bits to duration is the same for both sets of registers (Register 0x15C and Register 0x109) and is defined in Equation 17.

$$\text{Decimate Power Measurement Duration (Rx Sample Periods)} = 16 \times 2^{\text{Decimate Power Measurement Duration}[2:0]} \quad (17)$$

The reason for the difference is that in earlier states, the object is to lock the gain as quickly as possible. Thus, a shorter measurement time may be used for earlier states, but a longer time may be used after the gain locks.

When the gain unlocks, the AGC can reset the gain to maximum gain or to one of several other gain positions as shown in Table 23. When the gain unlocks, the AGC returns to State 1 (or State 0 if the [AD9363](#) exits the Rx state). When the AGC returns to State 1, it sets the digital gain to 0 dB (unless the digital gain is forced to a fixed value). In the fast attack AGC setup register (Register 0x110, Configuration 1), Bit D2 and Bit D5 can be set to optimize the gain and set gain and both bits can reduce the time required for gain lock because they both use the previous burst gain index information.

Set gain can use either the beginning or ending gain lock index of the previous burst. The setting of the use last lock level for set gain bit (Bit D7, Register 0x111) determines which gain index is used. The front of the burst is typically used if a preamble or boosted portion of the signal occurs at the beginning of the burst. The AGC locks on that boosted portion. If the entire burst uses the same nominal power level, then the AGC uses the end of the burst gain index.

If the thresholds are set correctly, then the most likely scenario is for the AGC to unlock the gain at the end of the burst (energy lost threshold) or if the [AD9363](#) exits the Rx state. Unlocking the gain for an ADC overload is similar to a stronger signal test but is a peak detector rather than a power detector. Unlocking the gain for a large LMT overload checks for large interfering signals and is a peak detector. All of these tests are recommended for a typical fast AGC configuration. Even in this simple case, there are options for what happens to the gain index when the gain unlocks (see Table 24).

Table 23. Gain Unlock Index Options

Gain Index When Reset	Set By	Definition
Maximum Gain	Maximum full table or maximum LMT table index (Register 0x0FD) and maximum LPF of 0x18.	Maximum analog gain.
Optimize Gain	AGC gain lock index at end of last burst plus optimize gain offset (Register 0x116, Bits[D3:D0]).	An optimized value that reduces the amount of steps the AGC typically takes to lock the gain for each burst.
Set Gain	AGC gain lock index at the start of the last burst or AGC gain lock index at the end of the last burst.	Similar to optimize gain but allows use of front of burst gain or end of burst gain setting.
No Gain Change	Not applicable.	No change to the gain index.

Table 24. Gain Unlock Condition vs. Gain Index

Condition that Unlocks Gain	Gain Index Type ¹	Set Bits	Clear Bits
Exit Rx State	Maximum gain	None	Register 0x110, Bit D4; Register 0x110, Bit D2
	Optimize gain	Register 0x110, Bit D2	Register 0x110, Bit D4
	Set Gain	Register 0x110, Bit D4	Register 0x110, Bit D2
Energy Lost Threshold Exceeded	Maximum gain	None	Register 0x110, Bit D6, and Register 0x110, Bit D3 only when Register 0x0FB, Bit D6 is set
	Optimize gain	Register 0x110, Bit D6	Register 0x110, Bit D3 only when Register 0x0FB, Bit D6 is set
Stronger Signal Threshold Exceeded	No change	None	Register 0x115, Bit D7 only when Register 0x0FB, Bit D6 is set
Large ADC Overload	No change	None	Register 0x114, Bit D7 and Register 0x110, Bit D1 when Register 0x0FB, Bit D6 is set
Large LMT Overload	No change	None	Register 0x110, Bit D1 when Register 0x0FB, Bit D6 is set

¹ A gain index of no change indicates that the gain index does not immediately change but the AGC algorithm does start over so the gain index very likely changes after the AGC moves through its states and relocks. For other gain types, such as set gain, the AGC first changes the gain index to the proper position and then restarts the algorithm.

Table 25. Preventing Gain Unlock Conditions in State 5

EN_AGC Pin Status	Do Not Unlock Gain When:	Set Bits
Not used	Energy lost threshold exceeded	Register 0x0FB, Bit D6; Register 0x014, Bit D1; Register 0x110, Bit D3
	Stronger signal threshold exceeded	Register 0x0FB, Bit D6; Register 0x014, Bit D1; Register 0x115, Bit D7
	Large ADC or large LMT overload	Register 0x0FB, Bit D6; Register 0x014, Bit D1; Register 0x110, Bit D1
Used	Energy lost threshold exceeded	Register 0x0FB, Bit D6; Register 0x110, Bit D3
	Stronger signal threshold exceeded	Register 0x0FB, Bit D6; Register 0x115, Bit D7
	Large ADC or large LMT overload	Register 0x0FB, Bit D6; Register 0x110, Bit D1

Table 26. Gain Unlock Condition vs. Gain Index

Condition that Unlocks Gain	Gain Index Type	Set Bits	Clear Bits
EN_AGC Pulled High	Maximum gain	Register 0x0FB, Bit D6 and Register 0x111, Bit D5	Register 0x110, Bits[D6:D5]
	Optimize gain	Register 0x0FB, Bit D6; Register 0x110, Bit D6; and Register 0x111, Bit D5	Register 0x110, Bit D5
	Set gain	Register 0x0FB, Bit D6 and Register 0x110, Bit D5	Register 0x111, Bit D5
	No change	Register 0x0FB, Bit D6	Register 0x110, Bit D5 and Register 0x111, Bit D5

When comparing the signal power with the energy lost threshold, there is also a time factor. Each time the signal power value updates, the AGC computes the difference between the power measured at the beginning of gain lock and the current signal power. This difference is compared against the energy lost threshold. If the difference exceeds the threshold for a time equal to twice the gain lock exit count, the gain unlocks as shown in Table 24. The gain lock exit count is clocked at the CLKRF rate. The same comparison is made for the stronger signal threshold, listed in Table 25.

The large ADC threshold is stored in Register 0x105 and the large LMT threshold is stored in Register 0x108. For the peak detectors, there are no time requirements. A single overload unlocks the gain.

Generally, the AGC is the best arbiter of when the gain unlocks. However, in some situations, it may be advantageous for the baseband processor to initiate an unlock condition. When the baseband processor pulls the EN_AGC pin high, the gain unlocks and the AGC algorithm restarts. The baseband processor cannot force the gain to lock at a certain time, but it can control when the gain unlocks. Table 26 shows how to use this feature.

If the thresholds are set correctly, the typical setup that unlocks the gain when the [AD9363](#) exits Rx mode, or if the burst/subframe ends, is sufficient for most applications. However, it is also possible to prevent the gain from unlocking in some instances (see Table 25). The settings are dependent on whether the baseband processor uses the EN_AGC pin to unlock the gain. If this is the case, then the EN_AGC pin must be low except when the gain is to be unlocked. If the EN_AGC pin is not used, then the auto gain lock delay bit (Bit D1 in Register 0x014) must be set high. The delay value must be updated in the AGC gain lock delay register (Bits[D7:D0] in Register 0x021).

CUSTOM GAIN TABLES

CUSTOM GAIN TABLES OVERVIEW

Analog Devices supplies gain tables to use with the [AD9363](#), but some applications require modifying these tables to optimize the RF performance (for example, using an external LNA or creating 3 dB gain steps). This section shows how to modify the gain tables that the [AD9363](#) uses for all gain control modes. Once created, load the custom gain table into the [AD9363](#) using the `AD9361_LOAD_GT` function.

The various gain block indices map to approximate gain per the following tables (all values are for 2300 MHz). Note that these are nominal values and some variation with carrier frequency, temperature, and process is expected for the LNA and mixer tables. For accurate gain vs. gain index values, RF characterization must be performed with the specific customer configuration.

Table 27. Internal LNA Index vs. Internal LNA Gain

Internal LNA Index	Internal LNA Gain (dB)
0	3
1	14
2	17
3	21

Table 28. Mixer Gain vs. Index

Mixer Index (decimal)	Mixer Index Gain (dB)
0	0
1	3
2	9
3 to 15	= index + 11

Table 29. TIA Gain vs. Index

TIA Index	Internal LNA Gain (dB)
0	−6
1	0

Table 30. LPF Index vs. LPF Gain

LPF Index (decimal)	LPF Gain (dB)
0 to 24	= index

Table 31. Digital Index vs. Digital Gain

Digital Index (decimal)	Digital Gain (dB)
0 to 31	= index

Table 32 is a small portion of a full gain table. This is the same format as the Analog Devices supplied full gain table along with APIs, but some of the columns are color coded to aid in the clarity of the column purposes. It is important to note that the baseband processor only uses the values in the table index column as well as the Register 0x131, Register 0x132, and Register 0x133 columns when programming a gain table into the [AD9363](#); these columns have register addresses as column headers. The Register 0x131, Register 0x132, Register 0x133 columns are concatenations of various gain stage indices. For example, Register 0x131 is a digital word that includes the gain indices for the external LNA, the internal LNA, and the mixer. All other columns are to make the gain table more readable.

Starting at the far left of Table 32, the table index is the index or pointer to the table. When the [AD9363](#) is in the FDD or receive states, this index controls the receive path gain.

The next column to the right is the external LNA index. See the External LNA section for details on how the [AD9363](#) can control an external LNA. Briefly, a bit in the gain table can be output to a general-purpose output (GPO) to control the gain of an external LNA.

The next column to the right is the external LNA gain. This column has no purpose except to indicate total receive path gain when using an external LNA.

Moving one column to the right leads to the internal LNA index. This is the internal LNA index, which controls LNA gain. internal LNA gain in dB is next to the internal LNA index column, which is used only to add to the gains of other stages and which results in the estimated total receive path gain.

Again, moving one column to the right results in the mixer index and next to that column is the mixer gain, both of which are analogous to the internal LNA index and internal LNA gain described previously.

The Reg. 0x131 column is the digital word that is a concatenation of all of the previous indices.

The TIA index and TIA gain are related, as described previously, to other gain stages. The LPF index is always equal to the LPF gain in dB, so the index column only is shown. The Reg. 0x132 column is a concatenation of the TIA and LPF indices.

The RF dc calibration bit (Register 0x133, Bit D5) is described in the RF DC Calibration Bit section. Digital gain, like the LPF gain, is equal to the digital index so the index column only is shown. Column Reg. 0x133 is a concatenation of the dc calibration bit and the digital index.

Finally, the Total Gain column shows the estimated total Rx path gain of the [AD9363](#) for each gain index.

RF DC CALIBRATION BIT

As referenced in the RF DC Offset Calibration section, the RF dc calibration bit (Register 0x133, Bit D5) is set for unique combinations of LMT gains. Setting this bit forces the RF dc calibration algorithm to reduce RF dc offset at those gain indices that involve unique LMT gain settings. In a split gain table, each index has this bit set because each index is likely a unique LMT gain configuration. In a full table, each index does not have a unique LMT gain setting. There may be several gain indices

using the same LMT configuration while the LPF gain changes for each index. In this case, set the RF dc calibration bit in the lowest index of the unique LMT gain. In Table 32, note that the RF dc calibration bit (see the DC Cal. column) is set for Index 0 but not set for Index 1 through Index 7. In all of these indices, only LPF gain is changing so the RF dc calibration bit is only set for one index. The RF dc offset correction words used for Index 0 are also used for the higher indices.

Table 32. Portion of the Analog Devices 800 MHz Full Gain Table

Table Index	External LNA		Internal LNA		Mixer		Reg. 0x131	TIA		LPF Index	Reg. 0x132	DC Cal.	Digital Index	Reg. 0x133	Total Gain
	Index	Gain	Index	Gain	Index	Gain		Index	Gain						
0	0	0	0	5	0	0	0	0	-6	0	0	1	0	20	-1
1	0	0	0	5	0	0	0	0	-6	0	0	0	0	0	-1
2	0	0	0	5	0	0	0	0	-6	0	0	0	0	0	-1
3	0	0	0	5	0	0	0	0	-6	1	1	0	0	0	0
4	0	0	0	5	0	0	0	0	-6	2	2	0	0	0	+1
5	0	0	0	5	0	0	0	0	-6	3	3	0	0	0	+2
6	0	0	0	5	0	0	0	0	-6	4	4	0	0	0	+3
7	0	0	0	5	0	0	0	0	-6	5	5	0	0	0	+4
8	0	0	0	5	1	3	1	0	-6	3	3	1	0	20	+5
9	0	0	0	5	1	3	1	0	-6	4	4	0	0	0	+6
10	0	0	0	5	1	3	1	0	-6	5	5	0	0	0	+7
11	0	0	0	5	1	3	1	0	-6	6	6	0	0	0	+8
12	0	0	0	5	1	3	1	0	-6	7	7	0	0	0	+9
13	0	0	0	5	1	3	1	0	-6	8	8	0	0	0	+10

MAXIMUM FULL TABLE/LMT TABLE INDEX

All Analog Devices suggested gain tables have a maximum full table index of 76 (decimal). The split table maximum index is 40 (decimal). The maximum full table/LMT table index register sets the highest gain table index that is calibrated as described in the RF DC Calibration Bit section. The chip default is 0x76 (decimal). Therefore, if a suggested full table is used, no change is required. If the baseband processor programs a gain table with a different maximum index or a split table is used, this value must be changed to the proper maximum index value.

EXTERNAL LNA

An external LNA may be added to the receive path to improve the system noise figure. All gain control modes work seamlessly with external LNAs, whether they are fixed gain devices or devices that can be bypassed with the use of a control signal. Note that the maximum single-ended level allowed at an AD9363 RF pin is 2.5 dBm peak. It is recommended that the system engineer perform an analysis of the maximum possible signal at the external LNA input added to the external LNA gain to determine if the external LNA gain is acceptable. If the signal level at the AD9363 RF input is greater than the maximum allowable level, then an external LNA with lower gain or an attenuator must be used.

Fixed gain LNAs are external amplifiers (or attenuators) that always provide a nominal amount of gain. This gain is not controllable and the LNA cannot be bypassed. In this case, there are no programming changes necessary for the AD9363.

Variable gain external LNAs use a control signal to select between two different gains. Usually one is the high gain setting and the other is the low gain or bypass setting, which is typically a loss. The external LNA uses high gain in most conditions unless the input to the internal LNA is too high (2.5 dBm peak). For those conditions, the external LNA uses low gain (bypass mode).

If manual gain mode is used, then there are two methods of controlling the external LNA gain. In the first method, the

baseband processor controls the gain using a GPO pin connected to the external LNA. Because the baseband controls the gain in the AD9363, it can control the gain of the external LNA. In the second method, the gain table, in conjunction with an AD9363 GPO, controls the external LNA. A bit in the gain table drives GPO_0 for Rx1 and GPO_1 for Rx2. Setting this bit to zero results in a low GPO output level whereas setting it to one results in a high GPO output level. To route the external LNA bits set in the gain table to GPO_x pins, set the external LNA1 control and external LNA2 control bits.

For AGC modes, the AD9363 must control the external LNA gain because the changes occur quickly and the baseband process does not have knowledge of the gain index until it is selected by the AGC.

Every time the gain changes, the gain control algorithm waits for a duration equal to the peak wait time while the analog signal path settles. Increase this value to allow the settling time of the external LNA, otherwise, the peak detectors enable before the analog stages settle.

To use the AD9363 to measure RSSI, program the external LNA high gain (Register 0x12C) and external LNA low gain (Register 0x12D) registers with the external LNA gain values. The device considers both values to represent positive gain in the front end prior to the AD9363. Both registers use 0.5 dB/LSB resolution and range from 0 dB to 31.5 dB.

If the low gain value is negative, offset the external LNA high gain register by an amount equal to the negative gain value and set the external LNA low gain register value to 0. For example, when the high gain value = 15 dB and the low gain value = -5 dB, program the external LNA high gain (Register 0x12C, Bits[5:0]) = 20 dB and the external LNA low gain (Register 0x12D, Bits[5:0]) = 0 dB. This prevents a step in the RSSI value when the external LNA goes from an on to an off condition.

RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)

RSSI OVERVIEW

Given the wide variety of applications for which the AD9363 is suited, the RSSI may be set up in one of several configurations, allowing the user to optimize the RSSI to produce extremely accurate results with a minimum of baseband processor interaction. RSSI accuracy is inherently accurate but can be improved through various means, including gain step calibration.

The AD9363 measures RSSI by measuring the power level in dB and compensating for the receive path gain. The various options available support both TDD and FDD applications. Note that the RSSI value is not in absolute units. Equating the RSSI readback value to an absolute power level (for example, in dBm) requires a factory calibration. To calibrate the RSSI word to an absolute reference, inject a signal into the antenna port of the completed system and read the RSSI word. From this test, generate a correction factor that equates the RSSI word to the injected signal level at the antenna port. This calibration is separate from the gain step calibration.

MODE SELECT AND MEASUREMENT DURATION

The RSSI mode select bits determine what event starts or restarts the RSSI algorithm and clears the accumulator, per Table 33.

If the default RSSI measurement mode bit (Register 0x158, Bit D0) is set, then the duration is a simple power of two value shown in Equation 18.

If the default RSSI measurement mode bit is clear, then non power of two durations are possible, per Equation 19. The four duration values are stored in Register 0x150 and Register 0x151. The duration is always in Rx sample rate cycles.

RSSI Weight

If the default RSSI measurement mode bit is clear, then the RSSI measurement duration consists of up to four values summed together. Because each value can be different, each value must be correctly weighted by its duration in Rx samples. Use Equation 20 to calculate the weight. If the default RSSI

measure-ment mode bit is set, the AD9363 automatically populates Multiplier 0 with 0xFF and the other multipliers with 0x00. When calculated correctly, the total of all four weights added together = 255 (decimal).

RSSI Delay and RSSI Wait

When the RSSI algorithm starts or restarts, the AD9363 first waits for the Rx signal path to settle. This is the RSSI delay and it is clocked at the Rx sample rate divided by 8. From this point, the RSSI algorithm alternates between measuring RSSI and waiting to measure RSSI. The purpose of the RSSI wait value is to align the RSSI measurement start with boundaries (such as slot boundaries) and is most useful in FDD applications. Figure 26 shows the use of RSSI wait, RSSI delay, and the measurement duration.

$$\text{RSSI Total Measurement Duration} = 2^{\text{Measurement Duration}[3:0]} \quad (18)$$

$$\text{RSSI Total Measurement Duration} = \sum_{i=0}^3 0 \cdot 2^{\text{Measurement Duration}[3:0]} \quad (19)$$

Weighted Multiplier $n =$

$$255 \times \left(\frac{2^{\text{Measurement Duration}[3:0]}}{\text{RSSI Total Measurement Duration}} \right) \quad (20)$$

Table 33. RSSI Mode Select

RSSI Mode Select	RSSI Algorithm (Re)Starts When:	Useful For:
000	AGC fast track mode locks the gain	TDD
001	EN_AGC pin is pulled high	TDD, measuring a symbol late in the burst
010	AD9363 enters Rx mode	TDD
011	Gain change occurs	FDD
100	SPI write to Register 0x158, Bit D5	FDD
101	Gain change occurs or EN_AGC pin pulled high	FDD

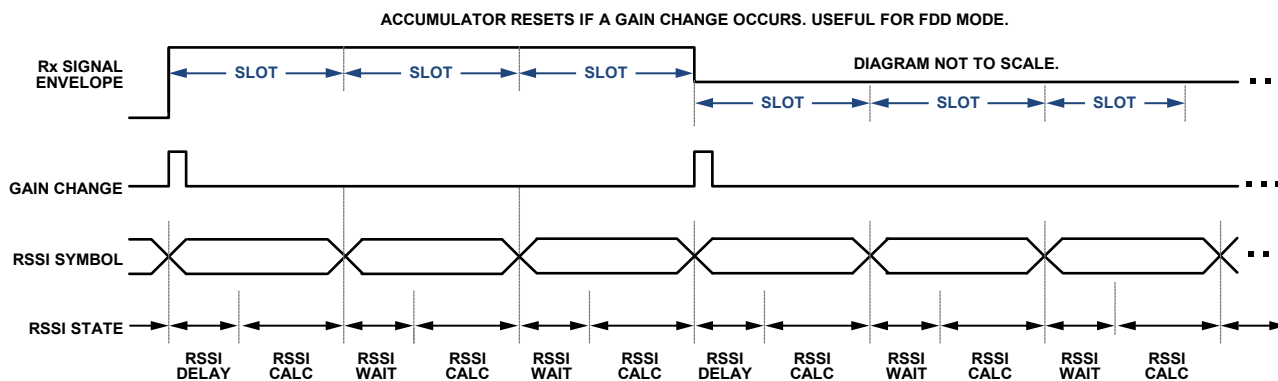


Figure 26. RSSI in an FDD Application

RSSI PREAMBLE AND RSSI SYMBOL

The first RSSI calculation performed after the RSSI delay counter expires is stored in both the RSSI symbol and RSSI preamble registers. The RSSI preamble value remains fixed and does not continue to update unless the algorithm restarts. The RSSI symbol value updates at the end of each calculation as shown in Figure 26. An exception is that the RSSI preamble words do not update after a gain change (RSSI mode select settings 3'b011 and 3'b101).

The RSSI symbol value is stored in 0.5 dB/LSB resolution. An additional LSB is also available, and if this bit is used, the resulting 9-bit word has a resolution of 0.25 dB/LSB. In either case, the range is 0 dB to –128 dB (note the negative sign). As the input signal power at the receiver increases, the RSSI value becomes less negative.

The RSSI preamble can also be treated as an 8-bit or 9-bit word. The range and format is the same as the RSSI symbol.

RSSI RFIR

If the Rx signal path RFIR is used, RSSI uses the data from this FIR for its calculation. If the Rx signal path RFIR is bypassed, it is still possible to use the RFIR for the RSSI data. The RFIR for RSSI measurement bits set the RSSI RFIR operation per the following table.

Table 34. RSSI RFIR

RFIR for RSSI Measurement (Decimal)	RSSI RFIR Decimation Factor and Filter Function
0	Decimate by 1 and bypass filter
1	Decimate by 1 and enable filter
2	Decimate by 2 and enable filter
3	Decimate by 4 and enable filter

RSSI GAIN STEP CALIBRATION

After the AD9363 digitizes and filters the signal, the RSSI algorithm subtracts the gain of the receive path. The resulting value is in dB and referenced to the input of the AD9363. If the actual gain of the AD9363 is different from the gain used by the RSSI algorithm, then as the receive path gain changes, the RSSI word may differ from an expected value. RSSI error typically is within 2 dB of the expected value, which is satisfactory for most applications.

For greater RSSI accuracy, the AD9363 uses a gain step calibration algorithm. Running this calibration does not change the actual gain of the receive path but instead only affects RSSI. LNA gain varies over frequency and the difference in gain from one step to another varies as well. The AD9363 stores gain steps as maximum LNA gain, and differences from this maximum LNA gain are stored in an indirectly addressed internal table accessed by Register 0x140 through Register 0x144. Maximum LNA gain occurs when the LNA gain index = 3.

In combination with an external single tone provided at the system input, the algorithm measures the actual gain steps to 0.25 dB precision and creates error terms that are added to the calculated RSSI value. Error terms are calculated for each LNA and mixer gain step. Each system runs this calibration as part of its factory test routine so that RSSI is optimized for each unit. The test fixture reads the resulting error terms out of the AD9363 and stores them in nonvolatile baseband processor memory. In the field during initialization, the baseband processor writes the error terms back into the AD9363.

The first step, performed only once, is to determine the optimum single-tone amplitude. Provide a single tone within the channel bandwidth and monitor the received data. Adjust the tone amplitude until the received data is within a few dB of full scale but not overloading. This is the single-tone amplitude used during factory test. The calibration steps are as follows:

1. Initialize the AD9363, making sure that the baseband dc and RF dc calibrations run as part of this routine. In addition, make sure that baseband dc tracking is turned on.
2. Put the AD9363 into the alert state.
3. Table 35 shows the register values to use, depending on the LO frequency used. For the next steps that program the step values, use the values from Table 35.
4. Program the directly addressable register values, as shown in Table 36.
5. Program the LNA gain step words into the internal table (see Table 37).
6. Turn on the external single tone at the amplitude determined previously and inject it into Rx1.
7. Run the calibration by setting Bit D3 in Register 0x016.
8. The calibration completes when Bit D3 in Register 0x016 clears.
9. Read the LNA and mixer error terms as shown in Table 38 into nonvolatile memory.

Table 35. Gain Step Calibration Register Values vs. LO Frequency

LO Frequency Range (MHz)	Step Description	Step Value (dB)	Register Value (Hex)	Variable in Table 36, Table 37, and Table 39
600 to 1300	Maximum LNA gain	24	C0	Xx
	LNA gain difference word for Index 0	23	2E	Aa
	LNA gain difference word for Index 1	8	10	Bb
	LNA gain difference word for Index 2	3	6	Cc
	LNA gain difference word for Index 3	0	0	Dd

LO Frequency Range (MHz)	Step Description	Step Value (dB)	Register Value (Hex)	Variable in Table 36, Table 37, and Table 39
1300 to 3300	Maximum LNA gain	24	C0	Xx
	LNA gain difference word for Index 0	22	2C	Aa
	LNA gain difference word for Index 1	8	10	Bb
	LNA gain difference word for Index 2	3	6	Cc
	LNA gain difference word for Index 3	0	0	Dd
2700 to 3800	Maximum LNA gain	23	B8	Xx
	LNA gain difference word for Index 0	22	2C	Aa
	LNA gain difference word for Index 1	8	10	Bb
	LNA gain difference word for Index 2	3	6	Cc
	LNA gain difference word for Index 3	0	0	Dd

Table 36. Configure LNA Gain Step Parameters

Line Number	Command	Address/Data	Comment
1	SPI write	0x145,0F	Set maximum mixer gain index (always 0x0F)
2	SPI write	0x148,0E	Maximum measurement time
3	SPI write	0x147,3F	Maximum settling time
4	SPI write	0x158,0D	Default RSSI measurement mode
5	SPI write	0x150,0E	Maximum RSSI measurement time
6	SPI write	0x15D,xx	Maximum LNA Gain (from Table 35)

Table 37. Programming the LNA Gain Steps into the Internal Table

Command	Address/Data	Comment
SPI write	143,61	Write R1 and R2 internal LNA tables and start clock
SPI write	140,00	LNA index
SPI write	141,aa	LNA gain step from Table 35
SPI write	143,63	Write data
Wait	3 μ s	Wait for data to fully write to internal table
SPI write	140,01	LNA index
SPI write	141,bb	LNA gain step from Table 35
SPI write	143,63	Write data
Wait	3 μ s	Wait for data to fully write to internal table
SPI write	140,02	LNA index
SPI write	141,cc	LNA gain step from Table 35
SPI write	143,63	Write data
Wait	3 μ s	Wait for data to fully write to internal table
SPI write	140,03	LNA index
SPI write	141,dd	LNA gain step from Table 35
SPI write	143,63	Write data
Wait	3 μ s	Wait for data to fully write to internal table
SPI write	143,01	Clear write bit
SPI write	143,00	Stop clock

Table 38. Reading Gain Step Error Words from the AD9363

Line No.	Command	Address/Data	Comment
1	SPI write	143,30	Set up to read LNA error words from Rx1.
2	SPI write	140,00	Set LNA index address to 0.
3	SPI read	142	Read LNA error for Index 0. Store in nonvolatile table.
4	Repeat Step 2 and Step 3 for three remaining LNA indices		
5	SPI write	143,20	Set up to read mixer error words from Rx1.
6	SPI write	140,00	Set mixer index address to 0.
7	SPI read	142	Read mixer error for Index 0. Store in nonvolatile table.
8	Repeat Step 6 and Step 7 for 14 remaining mixer indices		
9	SPI write	143,00	Put calibration register back to default.

Programming Gain Step Errors in the Field

During initialization (while the transceiver is in the alert or wait states), program the two configuration registers as shown in Table 39 (xx is the value from Table 35).

Table 39. Configuration Registers

Line No.	Command	Address/Data	Comment
1	SPI write	145,0F	Set maximum mixer gain index (always 0x0F)
2	SPI write	15D,xx	Maximum LNA gain (from Table 35)

Program the indirectly addressable LNA gain difference words exactly as in Step 5. Finally, program the error words back into the [AD9363](#) as described in Table 40.

In the processes and scripts shown previously, Rx1 is calibrated and then the error word results are programmed into Rx1 and Rx2. The resulting RSSI errors are expected to be within approximately 0.5 dB for Rx2 when using Rx1 error words. For maximum accuracy, calibrate each receiver independently with error words saved to nonvolatile memory for each receiver. When programming in the field, program the words into the internal tables for each receiver separately.

Table 40. Programming Gain Step Errors into the [AD9363](#) in the Field

Line No.	Command	Address/Data	Comment
1	SPI write	143,61	Set up to write Rx1 and Rx2, start clock.
2	SPI write	140,00	Set LNA index address to 0
3	SPI write	141,ff	Write LNA Index 0 error word from nonvolatile memory
4	SPI write	143,65	Write data into Address 0
5	Repeat Step 2 to Step 4 for three remaining LNA indices		
6	SPI write	143,61	Set up to write Rx1 and Rx2, start clock
7	SPI write	140,00	Set mixer index address to 0
8	SPI write	141,gg	Write Mixer Index 0 error word from nonvolatile memory
9	SPI write	143,69	Write data into Address 0
10	Repeat Step 7 and Step 9 for 14 remaining mixer indices		
11	SPI write	143,00	Stop clock

TRANSMIT POWER CONTROL

TRANSMIT POWER CONTROL OVERVIEW

The [AD9363](#) transceiver uses an accurate and efficient method of transmit power control (TPC) that involves a minimum of interaction with the baseband processor. This section shows how to set up the registers for the various modes and how to use transmit power control during normal operation.

Tx ATTENUATION WORDS

A single 9-bit word controls the attenuation of a particular transmitter path. The internal lookup table is 360 entries deep and the overall transmit path attenuation step size is 0.25 dB/LSB across the entire table. An attenuation word of zero results in 0 dB of attenuation. The value of 359 (decimal) results in an

overall attenuation of 89.75 dB. The lookup table is hard coded into the [AD9363](#) and is not programmable.

ATTENUATION WORD UPDATE OPTIONS

The baseband processor can write attenuation words at any time using the `AD9361_SET_TX_ATTENUATION` function. There are two choices for when the new attenuation word is implemented. The default mode implements the attenuation as soon as the function is executed. The other option is to write the new attenuation word, but require the [AD9363](#) go through an alert cycle before the word is implemented.

Additionally, setting the select Tx1 and Tx2 bit (Register 0x079, Bit D6) causes the [AD9363](#) to use the Tx1 attenuation word for both transmitters. The bit is normally cleared.

Tx POWER MONITOR

Tx POWER MONITOR OVERVIEW

This section describes the Tx power monitor (TPM) circuit operation and features. TPM is available in TDD mode only because it uses the inactive receiver to perform power measurements during transmit. This feature is very useful as a transmit power detector with more than 66 dB of linear dynamic range (the linear range can be extended to more than 80 dB as shown later in this section).

The AD9363 has two TPM inputs, TX_MON1 (Pin M5) and TX_MON2 (Pin A5). The maximum input signal level is 4 dBm continuous wave (CW) referenced to 50 Ω . Note that, when not using the inputs, tie them to ground.

This section explains how to set up transmit control registers and how to use TPC in normal operation.

Tx POWER MONITOR DESCRIPTION

One of the many features of the AD9363 is its ability to measure the level of a received signal accurately, resulting in an RSSI reading that is available to the system. Recognizing that, in TDD systems, the receiver and the transmitter are not operating

simultaneously, the AD9363 provides the ability to reuse the receiver circuitry by multiplexing the power detector into the receive path. The receiver RSSI circuitry is then turned on during the transmit burst and results in accurate Tx RSSI measurements. See Figure 27 for a transmit power monitor circuit block diagram in a typical TDD system diagram.

Because the Tx signal is high level (with respect to an Rx signal), it is multiplexed into the receiver chain after the LNA. The receiver circuitry reuses the results in an accurate, wide dynamic range measurement utilizing the existing (and otherwise idle) circuitry. The measurement is an rms level that has a configurable time measurement window and returns results in Tx RSSI units with 0.25 dB/LSB resolution in $-dBFS$ units over a more than 66 dB of detector dynamic range.

The measurement starts as the device is moved into Tx mode by the enable state machine. The measurement can be performed once after the enable state machine enters the Tx state or the measurement can be done continuously until the enable state machine exits the Tx state.

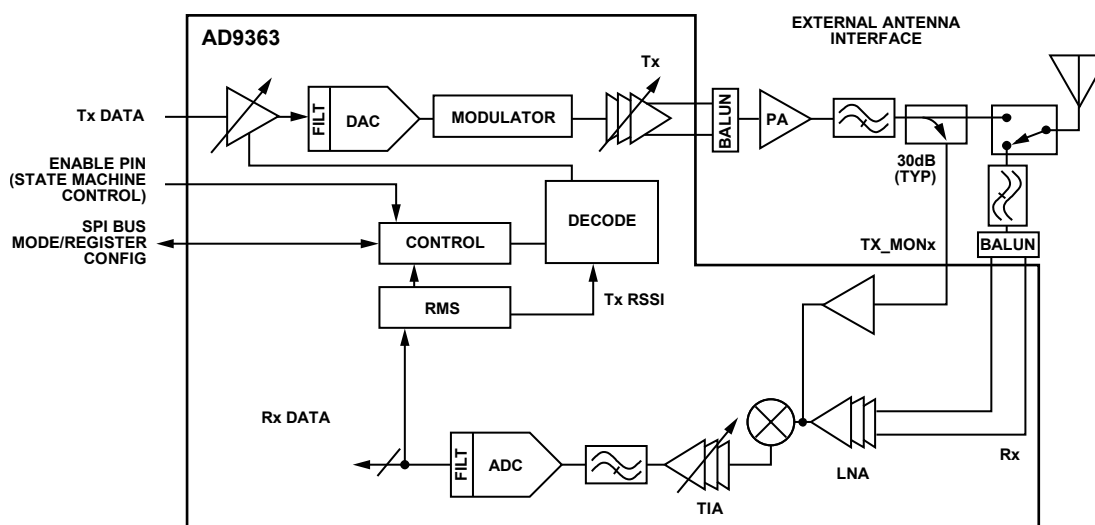


Figure 27. Tx Power Monitor Circuit Block Diagram

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INPUT MATCHING/ATTENUATION NETWORK

The TX_MONx inputs require a matching/attenuation network to provide matching to the driving source (typically a 50 Ω coupler output) and to scale the input signal. Place matching components, R1 to R3 and C1, as close as possible to the AD9363. The TX_MONx inputs are dc biased and the C1 capacitor is an ac coupling capacitor to ac couple the Tx_MONx input. R2 is a damping resistor to minimize series resonance comprised of on-chip inductance and capacitance. The best way to determine the optimum value for R2 is to empirically tune it for desired transmit power monitor frequency response. Use proper transmission line design techniques to design the signal path (TL1) from the Tx output coupler to the input of the transmit power monitor. The higher the frequency of operation, the more critical this path becomes in terms of loss and signal reflections.

Figure 28 shows a measured transmit power monitor frequency response using the matching circuit and component values in Figure 30. The frequency response is optimized for a 2.3 GHz frequency of operation.

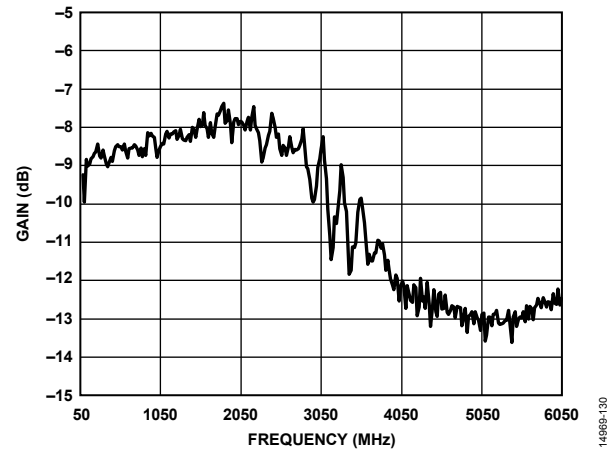


Figure 28. TPM Frequency Response

Tx POWER MONITOR GAIN CONTROL

The TPM total gain is composed of two gains: front-end gain (Tx monitor TIA gain) and Rx low-pass filter gain (GBBF), as described in Table 41. The TPM front-end gain is set by the Tx Monitor 1 configuration and Tx Monitor 2 configuration registers (Register 0x070, Bits[D1:D0] and Register 0x071, Bits[D1:D0], respectively). The Tx monitor TIA gain values are shown in Table 41. In addition to the two gains, Table 41 also includes minimum and maximum TPM input signal levels and associated SNR.

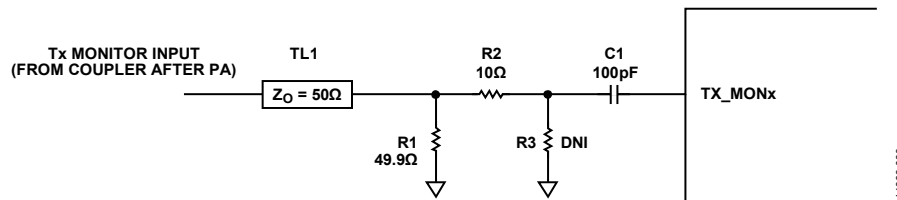


Figure 29. TPM Matching/Attenuation Input Network

Table 41. TPM Gain and Dynamic Range¹

Tx Monitor Gain[1:0]	Tx Monitor Gain (dB)	GBBF (dB)	Input Power (P _{IN}) Maximum (dBm)	P _{IN} Minimum (dBm)	SNR (dB) ²
00	Open				
01	0	0	4	-62.7	67
		30	-25.7	-70.1	44
10	6	0	-2.2	-68.6	67
		30	-31.7	-75.8	44
11	9.5	0	-5.7	-72.1	66
		30	-35.2	-78.9	44

¹ A blank cell in this table means not applicable.

² Bandwidth = 10 MHz for SNR calculation.

Figure 31 shows a block diagram of the Tx power monitor (TPM) signal chain. Note that the LO signal used to downconvert the TPM input signal is Tx LO.

Receive low-pass filter gain, GBBF, is set by register values Tx monitor low gain and Tx monitor high gain (Register 0x067, Bits[D4:D0] and Register 0x068, Bits[D4:D0], respectively). These values set the receive low-pass filter gain index in the 0 dB to 24 dB range. TPM gain mode, low or high, is determined by a threshold in the Tx attenuation threshold register (Register 0x078, Bits[D7:D0]). If the Tx attenuation value (Register 0x073 and Register 0x074) is equal to or less than the threshold, the low gain index value is used and if the value is greater than the threshold, the high gain index is used in the receive path. The TIA gain is automatically set high or low by the AD9363. Tx RSSI1 and Tx RSSI2 values in Register 0x06B, Register 0x06C, and Register 0x06D are compensated for gain changes.

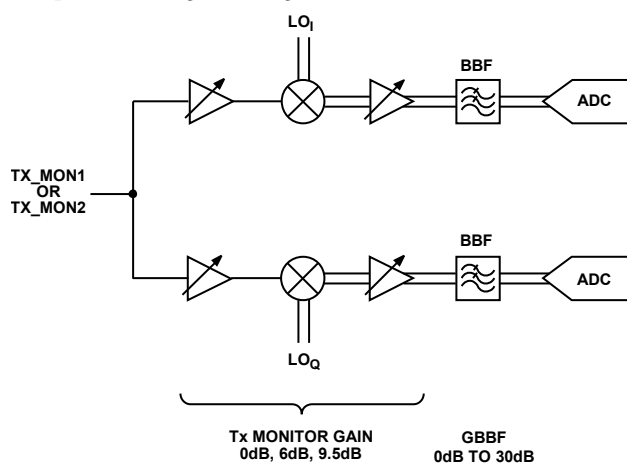


Figure 30. TPM Gain Distribution Circuit

TPM DYNAMIC RANGE

The TPM dynamic range can be maximized on the top end by minimizing the total TPM gain, that is, Tx monitor gain = 0 dB and GBBF = 0 dB. The upper range of the input signal is 4 dBm in that case (the upper range of the input signal can be increased to 9 dBm by forcing the TIA feedback resistor value to 1.75 kΩ by setting Bit D6 and Bit D7 in Register 0x1DC and Bit D0 and Bit D2 in Register 0x1DB). Maximizing total TPM gain, that is, Tx monitor gain = 9.5 dB and GBBF = 30 dB minimizes the total input referred noise, thereby increasing the lower range of the input signal to -78.9 dBm. The resulting total dynamic range can be as high as 82.8 dB by following the previously described gain control and making the gain switch threshold occur at -35.2 dBm input signal level.

Figure 32 shows a linear dynamic range of about 70 dB that can be achieved for three different input signal ranges with the Tx monitor gain set to 0 dB, 6 dB, or 9.5 dB and GBBF = 0 dB (see Table 41 for the input signal level ranges that correspond with these three different gain settings. This approach uses the same Tx monitor gain and GBBF gain settings across the whole attenuation range.



Figure 31. TPM Frequency Response

EXAMPLE OF Tx MONITOR CONFIGURATION AND MEASUREMENT OF TPM TRANSFER FUNCTION

The following example is based on measured results using a direct connection from the Tx1 output to the Tx monitor input on an evaluation board. The goal of the example is to show how to use the AD9363 TPM and an advanced application to extend the dynamic range of TPM. The frequency of operation = 2300 MHz and the transmitted signal = 1 MHz CW signal.

TPM can be enabled in multichip sync and Tx monitor control, using Bits[D6:D5] in Register 0x001, and in TPM mode enable using Bit D5 and Bit D7 in Register 0x06E. The preferred way to enable TPM is to set Bit D7 and Bit D5 in Register 0x06E. The user must also clear Bit D2 and Bit D3 in the analog power-down override register (Register 0x057) because TPM is powered down by default.

To maximize SNR, set the Tx monitor track bit in Register 0x067, Bit D5, which minimizes dc offset in the Tx monitor signal path.

The resulting measured TPM transfer characteristics are shown in Figure 33. The dashed line is uncompensated for the Tx monitor TIA gain change at the threshold and it shows a transition at 37 dB Tx attenuation (this corresponds to a threshold setting of 0x94 in Register 0x078). Below the threshold, Tx monitor gain is 0 dB and GBBF is 0 dB. Above the threshold, Tx monitor gain is 9.5 dB and GBBF is 0 dB. The compensated characteristic (solid line in Figure 33) is a gain compensated version of the dashed line. The resulting linear dynamic range is 76 dB, which is about 10 dB greater than the 66 dB dynamic range achievable with a single gain setting.

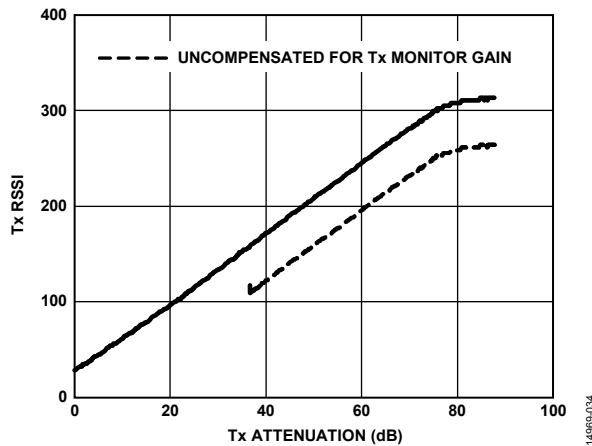


Figure 32. Tx Monitor (Tx RSSI) vs. Tx Attenuation

As Figure 33 shows, the TPM TIA gain is not compensated by the Tx RSSI algorithm. The 9.5 dB compensation that results in the solid line occurs in the baseband processor.

TPM TEST MODE

It is possible to output TPM I/Q data at the Rx data port in TDD mode in the Tx state. This may be useful in some applications.

The enable Rx data port bit for calibration (Register 0x014, Bit D7) must be set and TPM enabled in Register 0x06E to be in this test mode.

RF PORT INTERFACE

RF PORT INTERFACE OVERVIEW

The purpose of this section is to define the expected [AD9363](#) port impedance values and potential impedance matching techniques.

The [AD9363](#) has two independent receive paths and two independent transmit paths. Each receive path has three (A, B, and C) LNA inputs and each transmit path has two (A and B) Tx outputs. The LNA inputs and Tx outputs require external impedance matching networks. The receiver LNA input ports can be used in either single-ended mode or differential mode. The transmitter output ports can be used in differential mode only.

It is critical to ensure that these interface work properly to achieve performance levels specified in the [AD9363](#) data sheet. The main considerations are as follows:

- Rx interface type: single-ended or differential.
- The device to be interfaced, such as, filter, balun, transmit/receive (T/R) switch, external LNA, or external power amplifier: Short to ground at dc.
- Rx LNA maximum (no damage) input power (2.5 dBm peak, single-ended, lossless match, 50 Ω source).
- Rx LNA input port dc voltage level (~ 0.6 V dc).
- Tx output port bias (1.3 V dc at 75 mA per side at the maximum output power).
- Board design, such as reference planes, transmission lines, and impedance matching.

Rx SIGNAL PATH INTERFACE

The [AD9363](#) LNA devices (1A, 1B, 1C, 2A, 2B, 2C) are functional for the full 70 MHz to 6.0 GHz receive frequency range. When operating at or below 3 GHz, any LNA input port provides optimal performance. When operating above 3 GHz, utilize the Rx1A and Rx2A LNA input ports for optimal performance.

All three LNAs provide differential inputs that can also be configured as single-ended inputs (either side of the differential input can be used as a single-ended input). It is recommended that the LNA inputs be configured in differential mode to achieve best noise figure and even order distortion (IP2) performance. The LNA input pins have dc bias (~ 0.6 V dc) present on them and may need to be ac-coupled depending on the common-mode voltage level of the external circuit. The maximum safe input level is 2.5 dBm peak (single-ended, ideal match, 50 Ω source). Figure 34 shows the basic single-ended and differential interface configurations. Note that matching networks are usually required to achieve optimum performance.

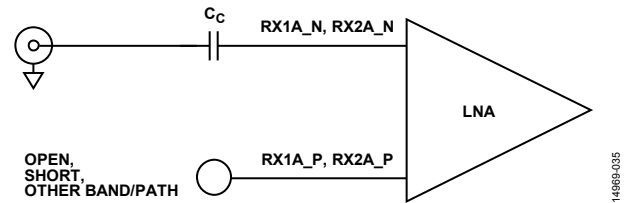


Figure 33. [AD9363](#) Rx Input Interface Circuit—Single-Ended Interface to the Negative Side of the Differential Input

Given a single-ended operation mode, a positive side connection is delineated by the _P at the end of the Rx input port name and a negative side connection is delineated by the _N at the end of the Rx input port name.

The Rx differential input impedance varies over frequency and is shown in Figure 38 through Figure 47. The reference plane for this data is the [AD9363](#) ball pads. Note that Z_o within the graph marker sections is 50 Ω .

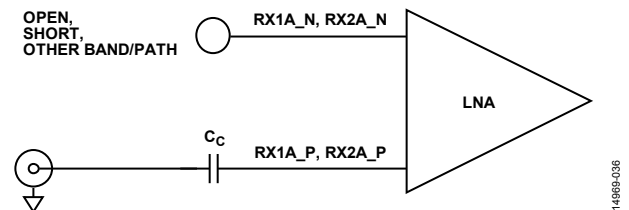


Figure 34. [AD9363](#) Rx Input Interface Circuits—Single-Ended Interface to the Positive Side of the Differential Input

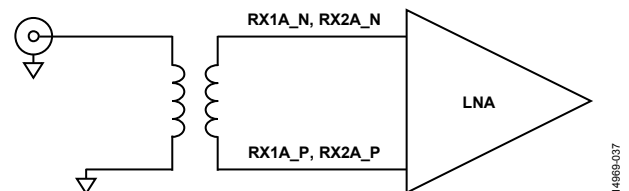


Figure 35. [AD9363](#) Rx Input Interface Circuits—Differential Interface Using a Transformer

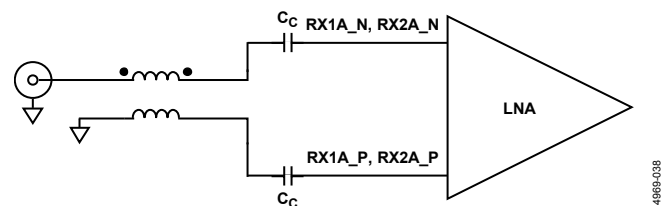


Figure 36. [AD9363](#) Rx Input Interface Circuits—Differential Interface Using a Transmission Line Balun

Rx1A AND Rx2A SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

Rx1A AND Rx2A SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

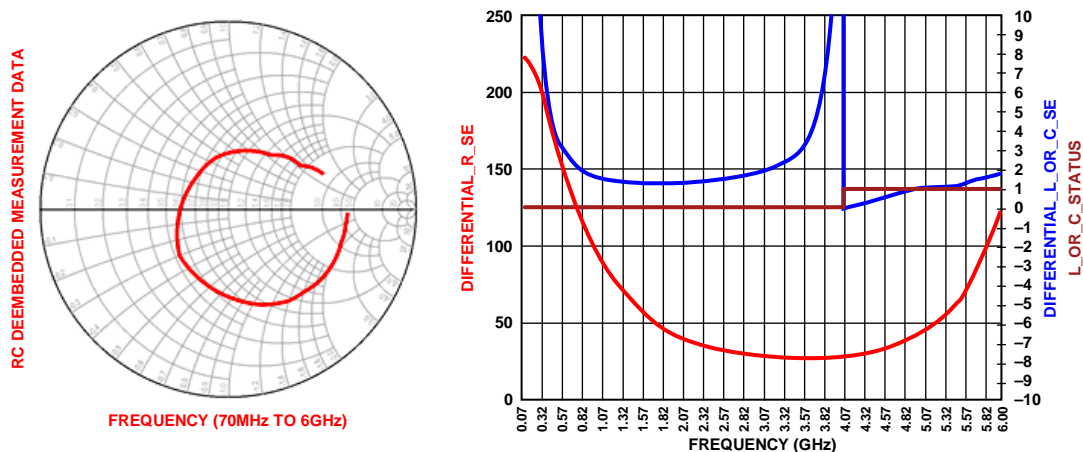


Figure 37. AD9363 Rx1A and Rx2A Input Differential Impedance

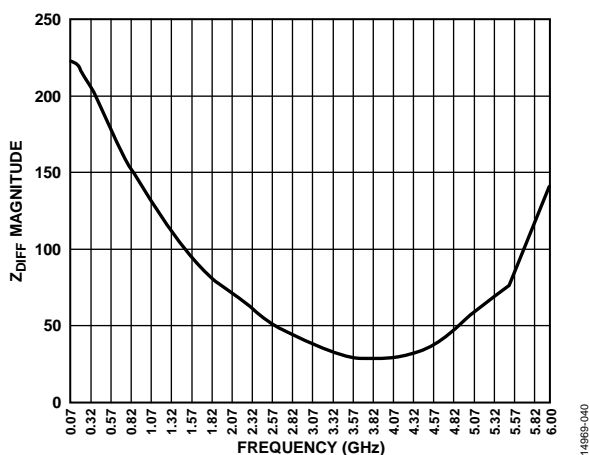


Figure 38. AD9363 Rx1A and Rx2A Input Differential Impedance Magnitude

Rx1B SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

Rx1B SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

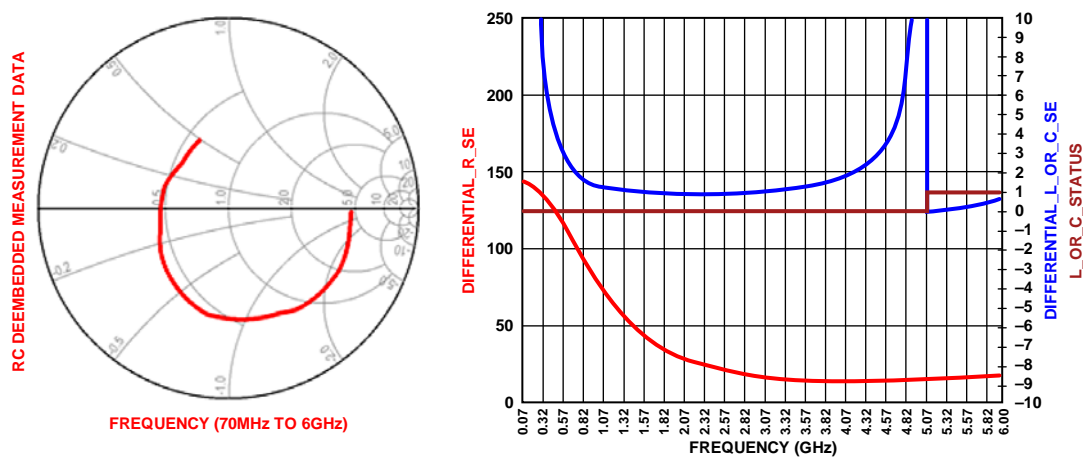


Figure 39. AD9363 Rx1B Input Differential Impedance

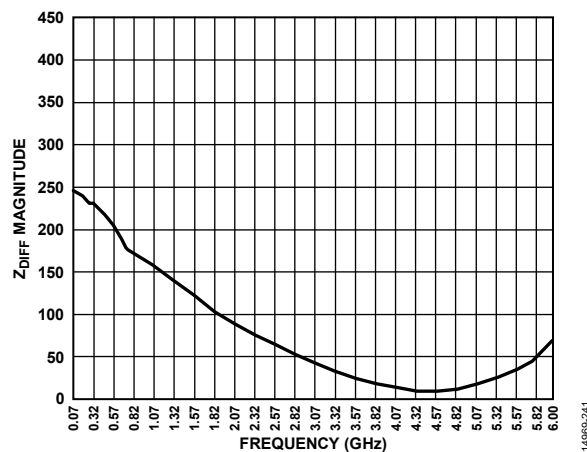


Figure 40. AD9363 Rx1B Input Differential Impedance Magnitude

Rx1C SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

Rx1C SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

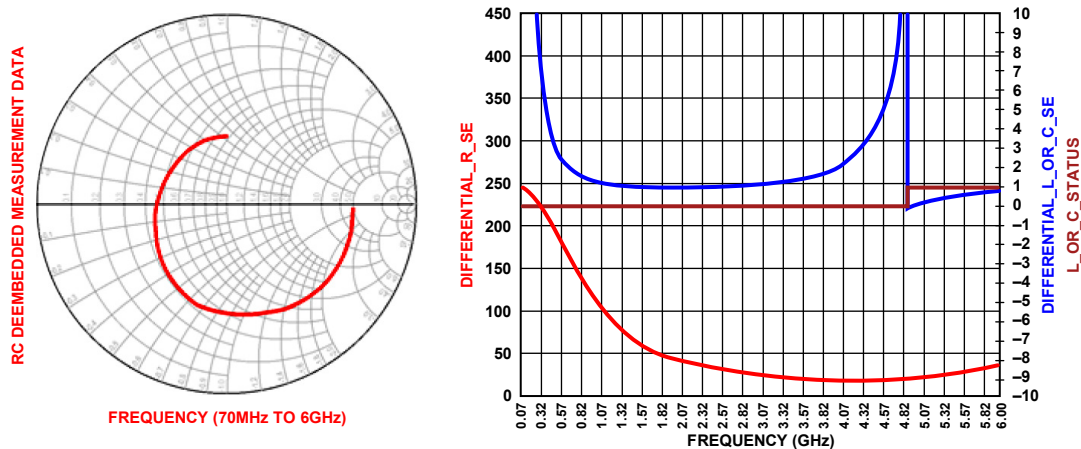


Figure 41. AD9363 Rx1C Input Differential Impedance

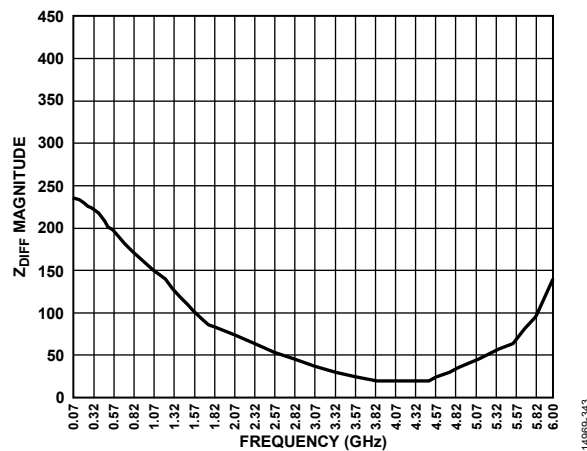
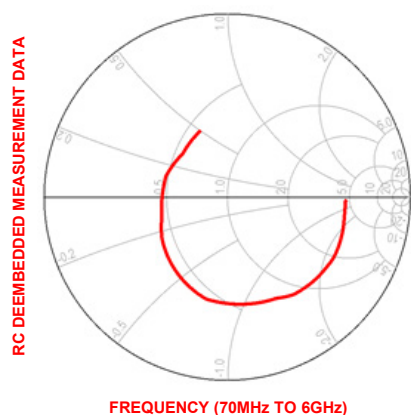


Figure 42. AD9363 Rx1C Input Differential Impedance Magnitude

Rx2B SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE



Rx2B SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

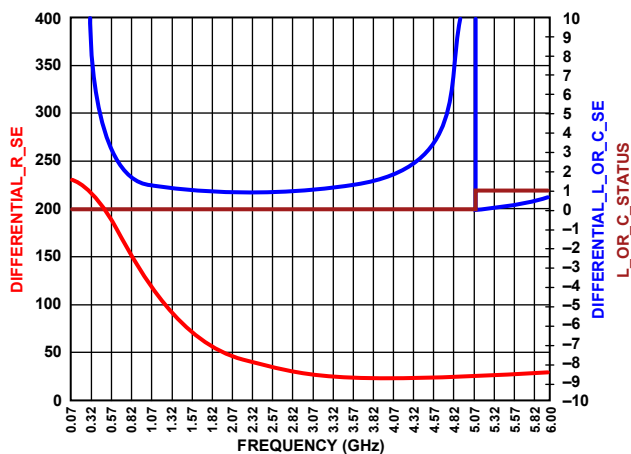


Figure 43. AD9363 Rx2B Input Differential Impedance

Rx2C SERIES EQUIVALENT DIFFERENTIAL IMPEDANCE

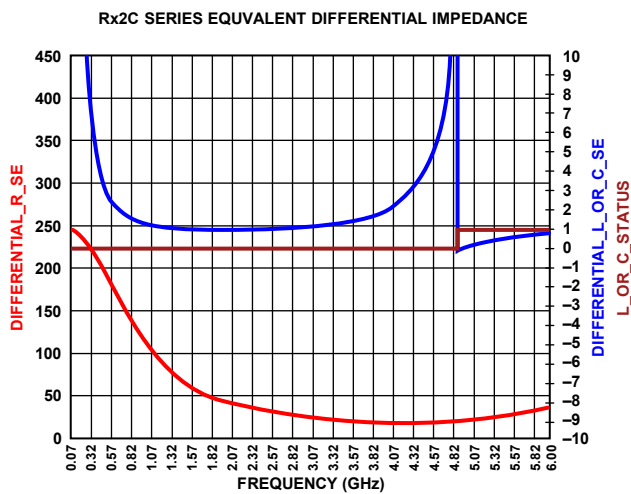
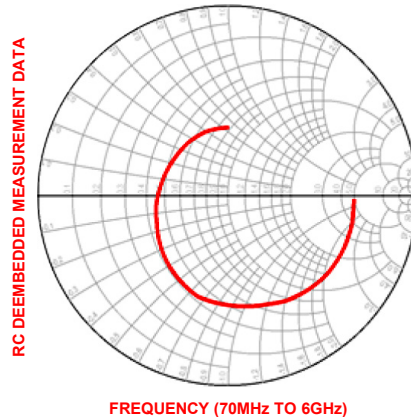


Figure 44. AD9363 Rx2C Input Differential Impedance

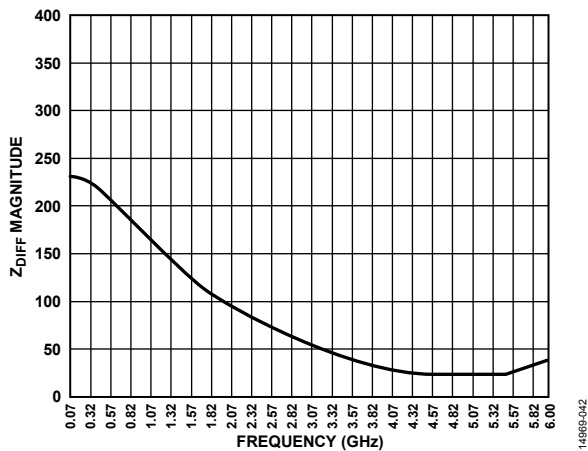


Figure 45. AD9363 Rx2B Input Differential Impedance Magnitude

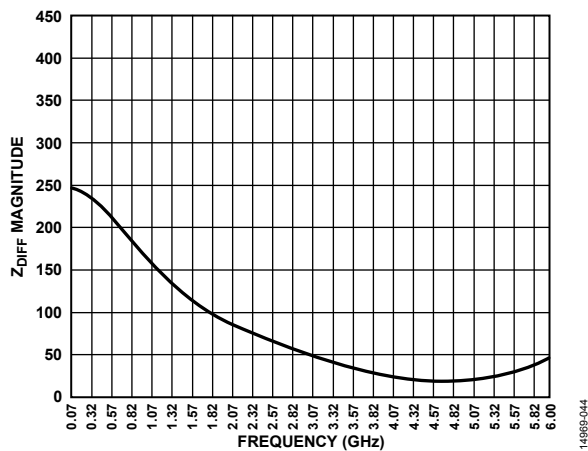


Figure 46. AD9363 Rx2C Input Differential Impedance Magnitude

From a design flexibility viewpoint, the following Rx path impedance matching strategy is preferred:

- Place a differential matching network between the balun/filter and the LNA input port.
- Place a single-ended matching network on the balun/filter input port.

The best matching network topology is application dependent. The examples within this section are simpler narrow-band cases. As the matching bandwidth increases, the required number of matching sections increases.

The LNA input ports have a dc voltage on them. A short to ground at dc is to be avoided. Figure 47 defines the general-purpose matching topology.

The balun/filter single-ended port is impedance matched with a simple PII network. The balun/filter differential port is impedance matched with either a dc blocked differential PII network or a dc blocked differential T network.

The dc blocked differential T network is represented by the smaller box in Figure 47. The dc blocked differential PII network is represented by the larger box in Figure 47.

The main advantages of the dc blocked differential PII network topology are a relatively wide impedance matching bandwidth (up to 830 MHz) and impedance matching

Topology selection flexibility. The main disadvantage is a higher number of SMD components.

The main advantage of the dc blocked differential T network topology is a lower SMD component count. The main disadvantage is the impedance matching bandwidth may be up to 5% smaller than the dc blocked differential PII topology.

Tx SIGNAL PATH INTERFACE

The AD9363 transmit path covers a full 70 MHz to 6.0 GHz transmit frequency range and the two Tx outputs exhibit similar performance. The Tx outputs are differential and require an external output bias. These outputs must be biased to 1.3 V dc supply voltage (nominal) using either chokes (wire wound inductors) or a transformer center tap connection. Each side of the differential output draws ≈ 75 mA of dc bias current at full output power. It is important to select components with low dc resistance (R_{DCR}) to minimize voltage drop (ΔV) across the

series parasitic resistance element (see R_{DCR} (marked red) resistor symbol in Figure 48).

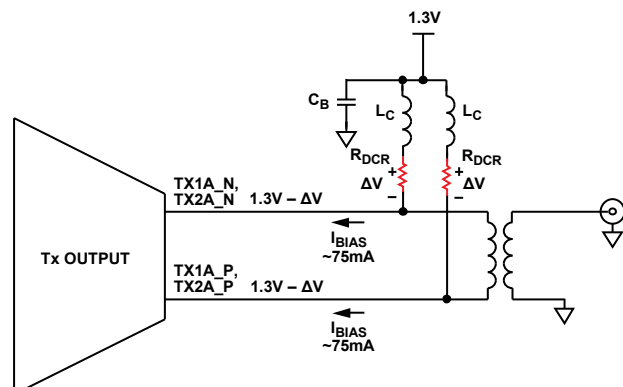


Figure 47. AD9363 Tx Output DC Biasing Using Chokes

As the ΔV voltage drop increases, the Tx buffer RF performance (OP1dB, maximum output power) degrades. Select choke inductance (LC) such that the choke impedance is high enough relative to the load impedance so that it does not affect the frequency response. The Tx outputs must be ac-coupled in most applications due to the presence of 1.3 V dc supply bias voltage. The approach in Figure 49 is preferred because there are fewer parasitics and the component count is lower.

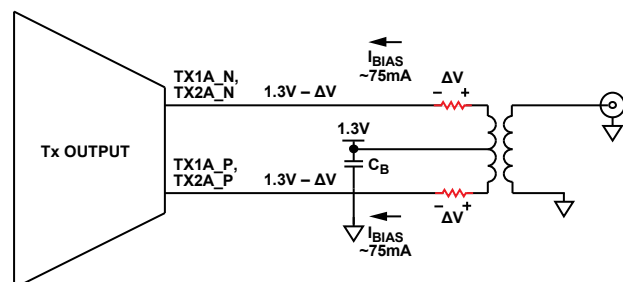


Figure 48. AD9363 Tx Output DC Biasing Using Center Tapped Transformer

The Tx differential output port is a medium signal device. Therefore, impedance matching is based on load-pull techniques, similar to a power amplifier. The goal is to provide a Tx output differential load impedance that represents the best compromise between the maximum output power delivered and the highest possible third-order linearity (OIP3).

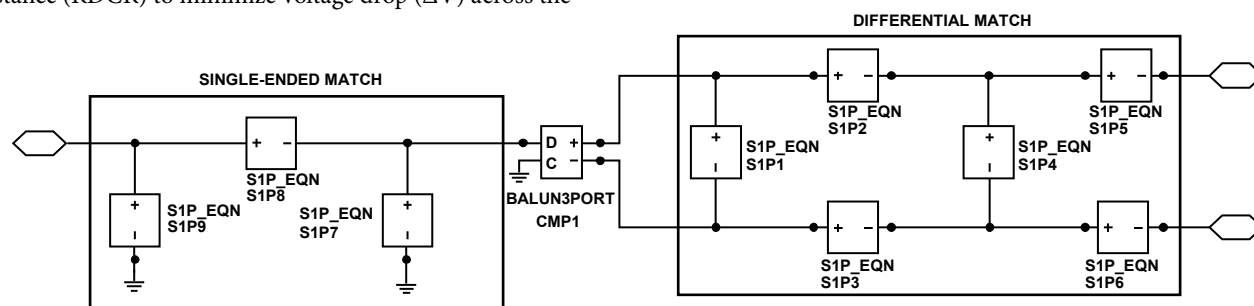


Figure 49. AD9363 Rx Input General-Purpose Impedance Matching Topology

Load pull-based impedance matching is simple. The focus is on developing the preferred load impedance at the Tx output ball pads. This matching technique is quite different from the small signal techniques utilized for the Rx input.

- Load-pull: design the matching network for the preferred load impedance at the Tx output pads.
- Small signal: design the matching network for maximum power transfer (TG is the transducer gain).

Based on present load-pull data, the preferred Tx output differential load impedance is 50 Ω .

- The reference plane is the Tx output ball pads.
- The fundamental power is inversely proportional to the real part of the load impedance.
- The OIP3 is inversely proportional to the real part of the load impedance.
- The OIP3 is higher for capacitive loads as compared to inductive loads. If residual impedance matching errors exist, it is better to err with a capacitive termination rather than an inductive termination.

Figure 51 to Figure 54 show the basic differential Tx output interface configurations. Note that matching networks (balun single-ended port) are often required to achieve optimum performance.

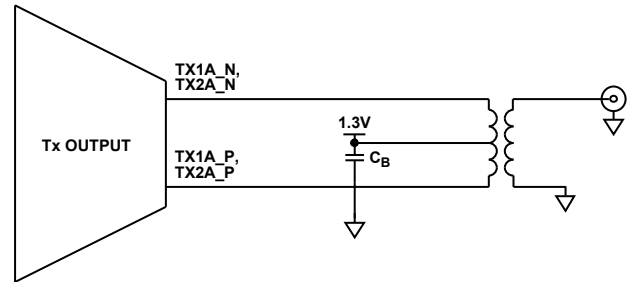


Figure 50. AD9363 Tx Output Differential Interface Configuration—Center Tap DC Feed

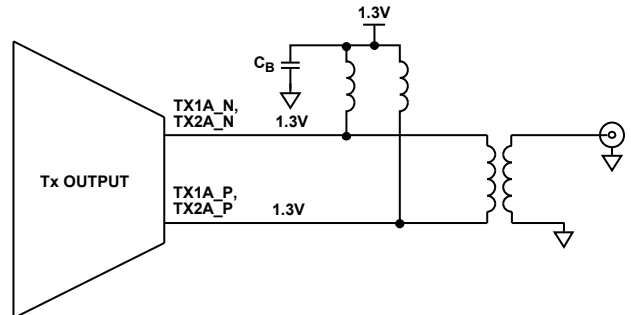


Figure 51. AD9363 Tx Output Differential Interface Configuration—Balun Differential to 50 Ω , Single-Ended

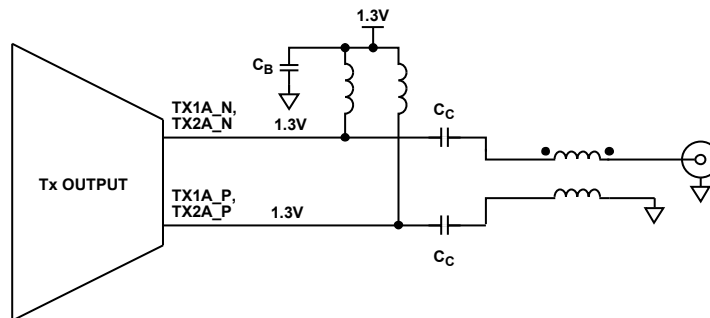


Figure 52. AD9363 Tx Output Differential Interface Configuration

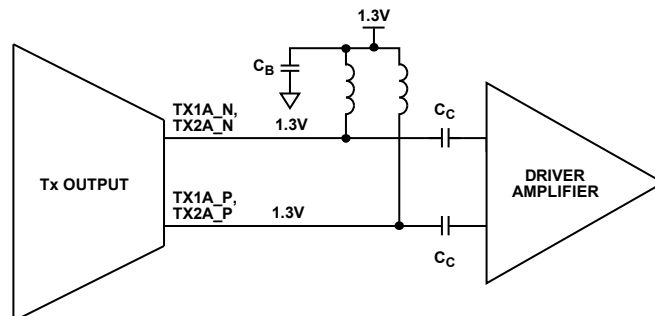


Figure 53. AD9363 Tx Output Differential Interface Configuration—Differential Gain Stage

FACTORY CALIBRATIONS

FACTORY CALIBRATIONS OVERVIEW

Factory calibrations are necessary to limit the amount of variation seen across a large quantity of circuit boards. Some calibrations are used to increase the accuracy of the [AD9363](#) device, while others are needed to calibrate nonlinearities of external components in the RF front end. The factory calibrations described in Table 42 are suggested calibrations. The number of calibration points for a specific design is dependent on the temperature stability and linearity of the RF components. The actual factory calibrations necessary might vary from Table 42 depending on the accuracy and performance of the desired system.

Table 42. Suggested Factory Calibrations

No.	Factory Calibration
1	Tx RSSI (Tx monitor)
2	Rx RSSI
3	Rx LNA gain step error
4	Tx power out vs. Tx attenuation
5	Tx power out vs. frequency

Tx RSSI (Tx MONITOR)

If the power detector is used, at minimum, a single-point Tx RSSI measurement must be made to correlate the absolute output power after the power amplifier to the Tx RSSI value reported by the [AD9363](#) device. Typically, a coupler is used to sample the power after the power amplifier back into the Tx monitor input of the [AD9363](#) device. During this measurement, transmit a typical burst. A signal with constant power (such as a preamble) gives the most accurate results. After a single-point measurement is measured, the Tx RSSI for other Tx power out levels can be calculated with the assumption that the Tx path is linear, the power detector path is linear, and all external RF components in the path are operating in their linear regions. If the system requires a higher precision of power control, multiple points across the [AD9363](#) Tx attenuation range and carrier frequency range can be measured during this factory calibration to generate a matrix of Tx RSSI correction values.

Complete the factory calibration using the corresponding transmitter on the [AD9363](#) device to transmit a known reference signal while the Tx RSSI is read across the SPI port for each desired output power point. Refer to the Tx Power Monitor section for detailed information on this process and the different power control modes.

Rx RSSI

The RSSI measurement occurs after the Rx gain is set (manual gain)/frozen (AGC). For the power measurement to be meaningful to the baseband processor, the RSSI code must be related to an absolute Rx input level (dBm) during factory calibration. Depending on the RSSI accuracy desired, this calibration can be a signal point calibration at a single frequency and input power level, or can consist of a matrix of frequencies and input power levels. It is recommended that the calibration signal be a typical burst of the associated standard.

For each receiver, there are two different RSSI readback registers. One register stores the first power measurement (RSSI preamble). The second register updates the power measurement at the symbol rate (RSSI symbol). If a calibration signal has a preamble or symbol with constant power, the RSSI is more accurate and repeatable. For more details, see the Received Signal Strength Indicator (RSSI) section. The `AD9361_RSSI_SETUP` function configures the RSSI measurement. The [AD9363](#) automatically takes into account the Rx gain step used and factors it into the RSSI value. For improved RSSI accuracy over frequency, run the Rx LNA gain step calibration before the RSSI factory calibration.

Rx LNA GAIN STEP CALIBRATION

The gain of the LNA and mixer stages inside the [AD9363](#) varies over temperature and frequency. This calibration is a one time factory calibration that measures the gain step error for the LNA and mixer to reduce the error of the Rx RSSI measurement. In the field, the baseband processor writes the error-corrected expected gain steps into the [AD9363](#) for the current frequency used. This process improves Rx RSSI accuracy and linearity. Complete this procedure before calibrating the Rx RSSI. The Rx LNA gain step calibration is only necessary if using the Rx RSSI feature, and more detail on this calibration can be found in the Received Signal Strength Indicator (RSSI) section.

Tx POWER OUTPUT vs. Tx ATTENUATION AND Tx POWER OUTPUT vs. CARRIER FREQUENCY

Complete a factory calibration such that the output power of the system is known. Depending on the linearity of the RF components chosen, a single-point calibration may be sufficient. If higher accuracy is desired, a matrix of carrier frequencies and [AD9363](#) Tx attenuation points may be evaluated to measure the Tx power output. This factory calibration prevents the output power from exceeding regulatory limits. This calibration also checks for transmit mask compliance and transmit emission limits (ACLR).

CONTROL OUTPUT

CONTROL OUTPUT OVERVIEW

The [AD9363](#) provides real-time status information on up to eight dedicated pins. Information, such as when calibrations are running and the state of the overload detectors in the receive signal path, are just a few of the many options available. This section describes the signals and their behavior in detail and describes how to program the registers so that the desired signals are available on the appropriate pins. This section also provides information about how a baseband processor can use the signals in an application. The control outputs are configured using the `AD9361_CTRL_OUTS_SETUP` function.

As shown in Table 44, the control output signals are mapped as a table. The control output pointer selects the row (address) that is sent to the output pins and the bits in control output enable individually select which output pins are active. The [AD9363](#) holds low any pins that are not enabled.

Some internal signals are available on more than one combination of control output pointer and control output enable. For example, to enable a control output that indicates that the Rx1 gain has changed, set the control output pointer register to 0x08 and set the control output enable register to 0x10. The same signal is also available by setting control output pointer to 0x05 and

control output enable to 0x40 or, alternatively, with control output pointer set to 0x1E and control output enable set to 0x04. Any one of these options is valid.

The baseband processor can only monitor the signals in one row at a time because the control output pointer register can only have a single value loaded at any given time. Thus, selecting one row over the other depends on which other signals the baseband processor must monitor simultaneously. From the example, if the baseband processor must also know when the auxiliary ADC word is valid, only the option of setting control output pointer to 0x1E allows this combination of the two signals. In this case, the control output enable register must be set to 0x05. The baseband processor can also set more of the bits in the control output enable register, even if it does not monitor those signals.

Some of the signals are helpful in a production system whereas some others are useful for debug. In either case, Analog Devices recommends connecting the [AD9363](#) control outputs to baseband processor inputs on the baseband processor so that the baseband processor can monitor real-time conditions in the [AD9363](#).

Table 43. Control Output Bit Descriptions

Register Address	Register Name	Bit D7	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0	Default	R/W
0x035	Control output pointer	Control output pointer[7:0]								0x00	R/W
0x036	Control output enable	Enable Control Output 7	Enable Control Output 6	Enable Control Output 5	Enable Control Output 4	Enable Control Output 3	Enable Control Output 2	Enable Control Output 1	Enable Control Output 0	0xFF	R/W

Table 44. Control Output Table

Register 0x035	Bit D7	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0
00	Calibration done	Tx charge pump calibration done	Rx charge pump calibration done	Rx baseband filter tuning done	Tx baseband filter tuning done	Gain step calibration busy	Rx synthesizer VCO calibration busy	Tx synthesizer VCO calibration busy
01	Tx RF PLL lock	Rx RF PLL lock	Baseband PLL lock	0	0	0	0	0
02	Baseband dc calibration busy	RF dc calibration busy	Channel 1 Rx quad calibration busy	Channel 1 Tx quad calibration busy	Channel 2 Rx quad calibration busy	Channel 2 Tx quad calibration busy	Gain step calibration busy	Tx monitor calibration busy
03	Channel 1 ADC low power	Channel 1 large LMT overage	Channel 1 large ADC overage	Channel 1 small ADC overage	Channel 2 low power	Channel 2 large LMT overage	Channel 2 large ADC overage	Channel 2 small ADC overage
04	Channel 2 Rx gain[6]	Channel 2 Rx gain[5]	Channel 2 Rx gain[4]	Channel 2 Rx gain[3]	Channel 2 Rx gain[2]	Channel 2 large LMT overage	Channel 2 large ADC overage	Channel 2 gain lock
05	Channel 2 gain change	Channel 1 Gain change	Channel 2 low power	Channel 2 large LMT overage	Channel 2 large ADC overage	Channel 2 gain lock	Channel 2 energy lost	Channel 2 stronger signal
06	Channel 1 low power	Channel 1 large LMT overage	Channel 1 large ADC overage	Channel 1 Rx gain[6]	Channel 1 Rx gain[5]	Channel 1 Rx gain[4]	Channel 1 Rx gain[3]	Channel 1 Rx gain[2]
07	Channel 1 low power	Channel 1 large LMT overage	Channel 1 large ADC overage	Channel 1 small ADC overage	Channel 1 AGC small[2]	Channel 1 AGC small[1]	Channel 1 AGC small[0]	Channel 1 gain lock

Register 0x035	Bit D7	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0
08	Channel 1 stronger signal	Channel 1 gain lock	Channel 1 energy lost	Channel 1 gain change	Channel 2 stronger signal	Channel 2 gain lock	Channel 2 energy lost	Channel 2 gain change
09	Rx on	Channel 1 RSSI preamble ready	Channel 1 RSSI symbol ready	Tx on	Channel 2 RSSI preamble ready	Channel 2 RSSI symbol ready	Not used	Not used
0A	Channel 1 Tx INT3 overflow	Channel 1 Tx HB3 overflow	Channel 1 Tx HB2 overflow	Channel 1 Tx QEC overflow	Channel 1 Tx HB1 overflow	Channel 1 Tx FIR overflow	Channel 1 Rx FIR overflow	Not used
0B	Calibration sequence state[3]	Calibration sequence state[2]	Calibration sequence state[1]	Calibration sequence state[0]	ENSM[3]	ENSM[2]	ENSM[1]	ENSM[0]
0C	Channel 1 energy lost	Channel 1 reset peak detect	Channel 2 energy lost	Channel 2 reset peak detect	Gain freeze	Channel 1 digital saturation	Channel 2 digital saturation	Not used
0D	Channel 1 Tx quad calibration status[1]	Channel 1 Tx quad calibration status[0]	Channel 1 Tx quad calibration done	RF dc calibration busy	Channel 2 Tx quad calibration status[1]	Channel 2 Tx quad calibration status[0]	Channel 2 Tx quad calibration done	Not used
0E	Not used	Not used	Not used	Baseband dc calibration busy	Not used	Not used	Not used	Not used
0F	Channel 1 AGC state[2]	Channel 1 AGC state[1]	Channel 1 AGC state[0]	Channel 1 reset peak detect	Channel 2 reset peak detect	Channel 1 RF dc calibration state[1]	Channel 1 RF dc calibration state[0]	Not used
10	Channel 2 AGC state[2]	Channel 2 AGC state[1]	Channel 2 AGC state[0]	Channel 2 enable RSSI	Channel 1 enable RSSI	Channel 2 RF dc calibration state[1]	Channel 2 RF dc calibration state[0]	Not used
11	Auxiliary ADC output[11]	Auxiliary ADC output[10]	Auxiliary ADC output[9]	Auxiliary ADC output[8]	Auxiliary ADC output[7]	Auxiliary ADC output[6]	Auxiliary ADC output[5]	Auxiliary ADC output[4]
12	Channel 1 filter power ready	Channel 1 gain lock	Channel 1 energy lost	Channel 1 stronger signal	Channel 1 ADC power ready	Channel 1/Channel 2 AGC state[2]	Channel 1/Channel 2 AGC state[1]	Channel 1/Channel 2 AGC state[0]
13	Channel 2 filter power ready	Channel 2 gain lock	Channel 2 energy lost	Channel 2 stronger signal	Channel 2 ADC power ready	Channel 2 AGC state[2]	Channel 2 AGC state[1]	Channel 2 AGC state[02]
14	Channel 2 Tx Int3 overflow	Channel 2 Tx HB3 overflow	Channel 2 Tx HB2 overflow	Channel 2 Tx QEC overflow	Channel 2 Tx HB1 overflow	Channel 2 Tx FIR overflow	Channel 2 Rx FIR overflow	0
15	Channel 1 SOI present	Channel 1 update dc RF	Channel 1 measure dc RF	Channel 1 dc track count reached	0	0	0	0
16	Channel 1 gain lock	Channel 1 Rx gain[6]	Channel 1 Rx gain[5]	Channel 1 Rx gain[4]	Channel 1 Rx gain[3]	Channel 1 Rx gain[2]	Channel 1 Rx gain[1]	Channel 1 Rx gain[0]
17	Channel 2 gain lock	Channel 2 Rx gain[6]	Channel 2 Rx gain[5]	Channel 2 Rx gain[4]	Channel 2 Rx gain[3]	Channel 2 Rx gain[2]	Channel 2 Rx gain[1]	Channel 2 Rx gain[0]
18	Channel 2 SOI present	Channel 2 update dc RF	Channel 2 measure dc RF	Channel 2 dc track count reached	Channel 2 enable decimate power	Channel 2 enable ADC power	Channel 1 enable decimate power	Channel 1 enable ADC power
19	Rx synthesizer charge pump calibration[3]	Rx synthesizer charge pump calibration[2]	Rx synthesizer charge pump calibration[1]	Rx synthesizer charge pump calibration[0]	Tx synthesizer charge pump calibration[3]	Tx synthesizer charge pump calibration[2]	Tx synthesizer charge pump calibration[1]	Tx synthesizer charge pump calibration[0]
1A	Rx synthesizer VCO tuning[8]	Rx synthesizer VCO ALC[6]	Rx synthesizer VCO ALC[5]	Rx synthesizer VCO ALC[4]	Rx synthesizer VCO ALC[3]	Rx synthesizer VCO ALC[2]	Rx synthesizer VCO ALC[1]	Rx synthesizer VCO ALC[0]
1B	Tx synthesizer VCO tuning[8]	Tx synthesizer VCO ALC[6]	Tx synthesizer VCO ALC[5]	Tx synthesizer VCO ALC[4]	Tx synthesizer VCO ALC[3]	Tx synthesizer VCO ALC[2]	Tx synthesizer VCO ALC[1]	Tx synthesizer VCO ALC[0]
1C	Rx synthesizer VCO tuning[7]	Rx synthesizer VCO tuning[6]	Rx synthesizer VCO tuning[5]	Rx synthesizer VCO tuning[4]	Rx synthesizer VCO tuning[3]	Rx synthesizer VCO tuning[2]	Rx synthesizer VCO tuning[1]	Rx synthesizer VCO tuning[0]
1D	Tx synthesizer VCO tuning[7]	Tx synthesizer VCO tuning[6]	Tx synthesizer VCO tuning[5]	Tx synthesizer VCO tuning[4]	Tx synthesizer VCO tuning[3]	Tx synthesizer VCO tuning[2]	Tx synthesizer VCO tuning[1]	Tx synthesizer VCO tuning[0]
1E	Channel 1 low threshold exceeded	Channel 1 high threshold exceeded	Channel 1 gain update counter expired	Channel 1 AGC state[1]	Channel 1 AGC state[0]	Channel 1 gain change	Temperature sense valid	Auxiliary ADC valid
1F	Channel 2 low threshold exceeded	Channel 2 high threshold exceeded	Channel 2 gain update counter expired	Channel 2 AGC small[1]	Channel 2 AGC small[0]	Channel 2 gain change	Not used	Not used

DESCRIPTION OF CONTROL OUTPUT SIGNALS

Any control output options not listed in the following sections are undefined. For example, if the control output pointer register is set to 0x0E, the logic level of Control Output 0 is undefined and it is not listed in the following description section.

After the baseband processor initiates a calibration on the [AD9363](#), the baseband processor must not execute additional code until the calibration completes. There are three methods to meet this requirement:

- The baseband processor can wait until the longest time that the calibration could take to run.
- The baseband processor can poll the bit used to initiate the calibration or it can poll a lock bit for VCO calibrations.
- The baseband processor can monitor various control output signals that inform the baseband processor in real time when the calibration completes.

REGISTER 0x035 = 0x00 (CALIBRATION BUSY AND DONE)

Control Output 7 (Calibration Done)

When the [AD9363](#) powers up into the sleep state, this signal is low. The signal responds only to the RF dc, baseband dc, Tx quadrature, Rx quadrature, and gain step calibrations. After one of these calibrations completes, the calibration done signal transitions high. From that point, while any of the previously listed calibrations runs, calibration done is low, returning high at the completion of the calibration. If several bits in the calibration control register are set simultaneously, the calibration state machine runs the calibrations automatically in a particular order. Only after all calibrations previously listed are complete does the calibration done signal transition high.

Control Output 6 (Tx Charge Pump Calibration Done)

When the [AD9363](#) powers up into the sleep state, this signal is low. It transitions high after a Tx charge pump calibration completes. If this signal is already high, it transitions and stays low during the charge pump calibration and transition high after the calibration completes.

Control Output 5 (Rx Charge Pump Calibration Done)

This signal is the same as the signal described in the Control Output 6 (Tx Charge Pump Calibration Done) section, but it applies to the Rx charge pump calibration.

Control Output 4 (Rx Baseband Filter Tuning Done)

This signal is normally high. This signal is low only when the Rx baseband filter calibration runs.

Control Output 3 (Tx Baseband Filter Tuning Done)

This signal is normally high. This signal is low only when the Tx baseband filter calibration runs.

Control Output 2 (Gain Step Calibration Busy)

This signal is normally low. This signal is high only when the gain step calibration runs.

Control Output 1 (Rx Synthesizer VCO Calibration Busy)

This signal is normally low. This signal is high only when the Rx RF VCO calibration runs.

Control Output 0 (Tx Synthesizer VCO Calibration Busy)

This signal is normally low. This signal is high only when the Rx RF VCO calibration runs.

REGISTER 0x035 = 0x01 (PLL LOCK)

Control Output 7 (Tx RF PLL Lock)

This signal reflects the state of the Tx RF PLL lock detect circuit. If the lock detect mode is continuous, then this control output signal is high when the RF PLL is locked and low otherwise (including when a calibration runs). If the lock detect mode is run once, then this bit indicates the status of the lock detect circuit every time the frequency integer word is written (causing a VCO calibration to occur) but after that occurs, the lock detect circuit stops monitoring the state of the RF PLL.

Control Output 6 (Rx RF PLL Lock)

This signal is the same as the signal described in the Control Output 7 (Tx RF PLL Lock) section but applies to the Rx RF PLL.

Control Output 5 (Baseband PLL Lock)

This signal is high when the baseband PLL is locked; otherwise, this signal is low.

Control Output 4 Through Control Output 0

This signal is always low.

REGISTER 0x035 = 0x02 (CALIBRATION BUSY)

Control Output 7 (Baseband DC Calibration Busy)

This signal is normally low. This signal is high only when the baseband dc calibration runs.

Control Output 6 (RF DC Calibration Busy)

This signal is normally low. This signal is high only when the RF dc calibration runs.

Control Output 5 (Channel 1 Rx Quadrature Calibration Busy)

This signal is normally low. This signal is high only when the Rx1 quadrature calibration runs.

Control Output 4 (Channel 1 Tx Quadrature Calibration Busy)

This signal is normally low. This signal is high only when the Tx1 quadrature calibration runs.

Control Output 3 (Channel 2 Rx Quadrature Calibration Busy)

This signal is normally low. This signal is high only when the Rx2 quadrature calibration runs.

Control Output 2 (Channel 2 Tx Quadrature Calibration Busy)

This signal is normally low. This signal is high only when the Tx2 quadrature calibration runs.

Control Output 1 (Gain Step Calibration Busy)

This signal is normally low. This signal is high only when the gain step calibration runs.

Control Output 0 (Tx Monitor Calibration Busy)

This signal is normally low. This signal is high only when the Tx monitor calibration runs.

REGISTER 0x035 = 0x03 (Rx GAIN CONTROL)**Control Output 7 (Channel 1 ADC Low Power)**

The Channel 1 ADC low power signal is used in the fast AGC and the MGC modes. This signal is high when a low power condition exists in the [AD9363](#).

Control Output 6 (Channel 1 Large LMT Overage)

The Channel 1 large LMT overage signal transitions high when a large LMT overload occurs. The signal remains high until the gain changes. After a gain change, the signal transitions low even if the input signal exceeds the threshold because the gain control holds the LMT detect in reset until the peak wait time counter expires. If an overload still occurs, this control output transitions high again.

Control Output 5 (Channel 1 Large ADC Overage)

The Channel 1 large ADC overage signal transitions high when a large ADC overload occurs. The signal remains high until the gain changes. After a gain change, the signal transitions low even if the ADC overload still occurs because the gain control holds the ADC detect in reset until the peak wait time counter expires. If an overload still occurs, this control output transitions high again.

Control Output 4 (Channel 1 Small ADC Overage)

The Channel 1 small ADC overage signal transitions high when a small ADC overload occurs. The signal remains high until the gain changes. After a gain change, the signal transitions low even if the ADC overload still occurs because the gain control holds the ADC detect in reset until the peak wait time counter expires. If an overload still occurs, this control output transitions high again.

Control Output 3 (Channel 2 Low Power)

This signal operates the same as the signal described in the Control Output 7 (Channel 1 ADC Low Power) section, but applies to Rx2.

Control Output 2 (Channel 2 Large LMT Overage)

This signal operates the same as the signal described in the Control Output 6 (Channel 1 Large LMT Overage) section, but applies to Rx2.

Control Output 1 (Channel 2 Large ADC Overage)

This signal operates the same as the signal described in the Control Output 5 (Channel 1 Large ADC Overage) section, but applies to Rx2.

Control Output 0 (Channel 2 Small ADC Overage)

This signal operates the same as the signal described in the Control Output 4 (Channel 1 Small ADC Overage) section but applies to Rx2.

REGISTER 0x035 = 0x04 (Rx GAIN CONTROL)**Control Output 7 Through Control Output 3 (Channel 2 Rx Gain[6:2])**

These control outputs represent the most significant five bits of the gain index pointer for Rx2. For a split table, these bits represent the most significant five bits of the LMT gain index.

Control Output 2 (Channel 2 Large LMT Overage)

See the Control Output 2 (Channel 2 Large LMT Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 1 (Channel 2 Large ADC Overage)

See the Control Output 1 (Channel 2 Large ADC Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 0 (Channel 2 Gain Lock)

This signal applies only to fast AGC mode. This signal is high if the AGC locks the gain; otherwise, this signal is low.

REGISTER 0x035 = 0x05 (Rx GAIN CONTROL)**Control Output 7 (Channel 2 Gain Change)**

This signal is normally low; it pulses high when the Rx2 gain changes. The internal clock rates of the [AD9363](#) determine the duration of the pulse. For the standard LTE 10 MHz profile, the duration is approximately 30 ns.

Control Output 6 (Channel 1 Gain Change)

This signal is the same as the signal described in the Control Output 7 (Channel 2 Gain Change) section, but applies to Rx1.

Control Output 5 (Channel 2 Low Power)

See the Control Output 3 (Channel 2 Low Power) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 4 (Channel 2 Large LMT Overage)

See the Control Output 2 (Channel 2 Large LMT Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 3 (Channel 2 Large ADC Overage)

See the Control Output 1 (Channel 2 Large ADC Overage) section.

Control Output 2 (Channel 2 Gain Lock)

This signal is the same as the signal described in the Control Output 0 (Channel 2 Gain Lock) section (see the Register 0x035 = 0x04 (Rx Gain Control) section).

Control Output 1 (Channel 2 Energy Lost)

This signal is normally low and applies only to the fast AGC. It transitions high when the energy lost condition occurs and stays high for as long as the condition is true.

Control Output 0 (Channel 2 Stronger Signal)

This signal is normally low and applies only to the fast AGC. It transitions high when the stronger signal condition occurs and stays high for as long as the condition is true.

REGISTER 0x035 = 0x06 (Rx GAIN CONTROL)**Control Output 7 (Channel 1 ADC Low Power)**

See the Control Output 7 (Channel 1 ADC Low Power) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 6 (Channel 1 Large LMT Overage)

See the Control Output 6 (Channel 1 Large LMT Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 5 (Channel 1 Large ADC Overage)

See the Control Output 5 (Channel 1 Large ADC Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 4 Through Control Output 0 (Channel 1 Rx Gain [6:2])

This signal is the same as the signal described in the Control Output 7 Through Control Output 3 (Channel 2 Rx Gain [6:2]) section (see the Register 0x035 = 0x04 (Rx Gain Control) section), but applies to Rx1.

REGISTER 0x035 = 0x07 (Rx GAIN CONTROL)**Control Output 7 (Channel 1 ADC Low Power)**

See the Control Output 7 (Channel 1 ADC Low Power) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 6 (Channel 1 Large LMT Overage)

See the Control Output 6 (Channel 1 Large LMT Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 5 (Channel 1 Large ADC Overage)

See the Control Output 5 (Channel 1 Large ADC Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 4 (Channel 1 Small ADC Overage)

See the Control Output 4 (Channel 1 Small ADC Overage) section in the Register 0x035 = 0x03 (Rx Gain Control) section.

Control Output 3 Through Control Output 1 (Channel 1 AGC, Small [2:0])

These control outputs correspond to the slow and fast AGC state machines. Note that in slow AGC mode, there are only four states (State 0 through State 3); therefore, the MSB does not go high in this mode.

Control Output 0 (Channel 1 Gain Lock)

This signal is the same as the signal described in the Control Output 0 (Channel 2 Gain Lock) section (see the Register 0x035 = 0x04 (Rx Gain Control) section), but applies to Rx1.

REGISTER 0x035 = 0x08 (Rx GAIN CONTROL)**Control Output 7 (Channel 1 Stronger Signal)**

This signal is the same as the signal described in the Control Output 0 (Channel 2 Stronger Signal) section (see the Register 0x035 = 0x05 (Rx Gain Control) section), but applies to Rx1.

Control Output 6 (Channel 1 Gain Lock)

See the Control Output 0 (Channel 1 Gain Lock) section in the Register 0x035 = 0x07 (Rx Gain Control) section.

Control Output 5 (Channel 1 Energy Lost)

This signal is the same as the signal described in the Control Output 1 (Channel 2 Energy Lost) section (see the Register 0x035 = 0x05 (Rx Gain Control) section), but applies to Rx1.

Control Output 4 (Channel 1 Gain Change)

See the Control Output 6 (Channel 1 Gain Change) section in the Register 0x035 = 0x05 (Rx Gain Control) section.

Control Output 3 (Channel 2 Stronger Signal)

See the Control Output 0 (Channel 2 Stronger Signal) section in the Register 0x035 = 0x05 (Rx Gain Control) section.

Control Output 2 (Channel 2 Gain Lock)

See the Control Output 0 (Channel 2 Gain Lock) section in the Register 0x035 = 0x04 (Rx Gain Control) section.

Control Output 1 (Channel 2 Energy Lost)

See the Control Output 1 (Channel 2 Energy Lost) section in the Register 0x035 = 0x05 (Rx Gain Control) section.

Control Output 0 (Channel 2 Gain Change)

See the Control Output 7 (Channel 2 Gain Change) section in the Register 0x035 = 0x05 (Rx Gain Control) section.

REGISTER 0x035 = 0x09 (Rx ON, Tx ON, RSSI)**Control Output 7 (Rx On)**

This signal is high when the receiver signal path is enabled. For this enablement to occur, at least one receiver must be enabled in Register 0x003. In addition, the [AD9363](#) must be in the receive state (for TDD enable state machine) or the FDD state (for FDD enable state machine). If the FDD external control enable bit is set, then in addition to being in the FDD state, the baseband processor must turn on one or both receivers via the ENABLE pin.

Control Output 6 (Channel 1 RSSI Preamble Ready)

This signal is high when the RSSI preamble word is valid. After the preamble word becomes valid, it stays valid until some event (controlled by the RSSI mode select bits) causes the RSSI algorithm to restart. If the AD9363 is in the receive state and the preamble word is valid, the preamble word remains valid, even if the AD9363 is moved to the alert or Tx states.

If the RSSI algorithm is set to restart when the AD9363 enters Rx mode and the AD9363 moves from alert to the Rx or FDD state, this signal transitions low while the new preamble word is calculated and then it transitions high when it is valid.

If the RSSI algorithm is set to restart when the fast AGC locks the gain, the preamble updates only if the enable state machine moves into the Rx state and then locks the gain. It does not update if the enable state machine is already in the Rx (or FDD) state. Gain changes in slow AGC mode never update the preamble.

Control Output 5 (Channel 1 RSSI Symbol Ready)

This signal pulses high when the Rx1 RSSI symbol value is updated. The AD9363 internal clock rates determine the pulse duration. For the standard LTE 10 MHz profile, the duration is approximately 60 ns.

Control Output 4 (Tx On)

This signal is high when the transmit signal path is enabled. For this enablement to occur, at least one transmitter must be enabled. In addition, the AD9363 must be in the transmit state (for TDD enable state machine) or the FDD state (for FDD enable state machine). If the external control enable bit is set, then in addition to being in the FDD state, the baseband processor must turn on one or both transmitters via the TXNRX pin.

Control Output 3 (Channel 2 RSSI Preamble Ready)

This signal is the same as the Control Output 6 signal described in this section, but applies to Rx2.

Control Output 2 (Channel 2 RSSI Symbol Ready)

This signal is the same as the Control Output 5 signal described in this section, but applies to Rx2.

REGISTER 0x035 = 0x0A (DIGITAL OVERFLOW)**Control Output 7 (Channel 1 Tx Interpolation Filter 3 Overflow)**

This signal is high if the Tx Interpolation Filter 3 overflows. If the overflow condition stops, the signal goes low.

Control Output 6 (Channel 1 Tx HB3 Overflow)

This signal is high if the Tx HB3 filter overflows. If the overflow condition stops, the signal goes low.

Control Output 5 (Channel 1 Tx HB2 Overflow)

This signal is high if the Tx HB2 filter overflows. If the overflow condition stops, the signal goes low.

Control Output 4 (Channel 1 Tx QEC Overflow)

This signal is high if the Tx QEC algorithm overflows. If the overflow condition stops, the signal goes low.

Control Output 3 (Channel 1 Tx HB1 Overflow)

This signal is high if the Tx HB1 filter overflows. If the overflow condition stops, the signal goes low.

Control Output 2 (Channel 1 Tx FIR Overflow)

This signal is high if the Tx FIR filter overflows. If the overflow condition stops, the signal goes low.

Control Output 1 (Channel 1 Rx FIR Overflow)

This signal is high if the Rx FIR filter overflows. If the overflow condition stops, the signal goes low.

REGISTER 0x035 = 0x0B (CALIBRATION AND ENSM STATES)**Control Output 7 Through Control Output 4 (Calibration Sequence State [3:0])**

These four control outputs represent the state of the calibration state machine. For example, while a baseband dc calibration is running, the state of the calibration state machine is 0x2. In this case, only Control Output 5 is high.

Control Output 3 Through Control Output 0 (ENSM[3:0])

These four control outputs represent the state of the enable state machine. For example, in the alert state, the enable state machine is in State 5; therefore, Control Output 2 and Control Output 0 are high.

REGISTER 0x035 = 0x0C (GAIN CONTROL)**Control Output 7 (Channel 1 Energy Lost)**

See the Control Output 5 (Channel 1 Energy Lost) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 6 (Channel 1 Reset Peak Detect)

This signal applies to all Rx gain control modes. This signal is high when the gain control circuit holds the peak detectors in the reset state.

Control Output 5 (Channel 2 Energy Lost)

See the Control Output 1 (Channel 2 Energy Lost) section in the Register 0x035 = 0x05 (Rx Gain Control) section.

Control Output 4 (Channel 2 Reset Peak Detect)

This signal is the same as the Control Output 6 signal described in this section, but applies to Rx2.

Control Output 3 (Gain Freeze)

If the gain is frozen, this signal is high; otherwise, it is low. Frozen gain indicates that one or more bits are set that prevent the gain from unlocking, even if a case such as a peak overload occurs. Gain only freezes after lock.

Control Output 2 (Channel 1 Digital Saturation)

This signal is normally low. If this signal is high, this indicates that a digital overload is occurring or has occurred. After the signal goes high, the gain must change for the signal to transition low. If the gain changes but the overload condition persists, the signal still transitions and stays low while the AD9363 holds the peak detectors in the reset state for a duration set by the peak overload wait time. The signal then transitions high after the peak detectors exit the reset state.

Control Output 1 (Channel 2 Digital Saturation)

This signal is the same as the Control Output 2 signal described in this section, but applies to Rx2.

REGISTER 0x035 = 0x0D (Tx QUADRATURE AND RF DC CALIBRATION STATUS)**Control Output 7 and Control Output 6 (Channel 1 Tx Quadrature Calibration Status [1:0])**

These control outputs display the status of the Tx quadrature calibration state machine, stepping through State 0 through State 3 as the calibration runs. It returns to State 0 when the calibration completes.

Control Output 5 (Channel 1 Tx Quadrature Calibration Done)

This signal pulses high when the Tx quadrature calibration finishes. The AD9363 digital clock rates determine the pulse duration. For the LTE 10 MHz standard customer software profile, the signal pulses high for approximately 480 ns.

Control Output 4 (RF DC Calibration Busy)

This signal transitions high while the RF dc calibration runs, then transitions low.

Control Output 3 and Control Output 2 (Channel 2 Tx Quadrature Calibration Status [1:0])

This signal is the same as the Control Output 7 and Control Output 6 signal described in this section, but applies to Tx2.

Control Output 1 (Channel 2 Tx Quadrature Calibration Done)

This signal is the same as the Control Output 5 signal described in this section, but applies to Tx2.

REGISTER 0x035 = 0x0E (Rx QUADRATURE AND BASEBAND DC CALIBRATION STATUS)**Control Output 4 (Baseband DC Calibration Busy)**

This signal is high when the baseband dc calibration runs. If only the baseband dc calibration is run, then the signal is high once time only. If an RF calibration only runs or if a baseband dc calibration is run followed by an RF dc calibration, the signal is high for the baseband dc calibration and then it pulses high again during the RF dc calibration.

REGISTER 0x035 = 0x0F (GAIN CONTROL)**Control Output 7 Through Control Output 5 (Channel 1 AGC State [2:0])**

See the Control Output 3 Through Control Output 1 (Channel 1 AGC, Small [2:0]) section in the Register 0x035 = 0x07 (Rx Gain Control) section.

Control Output 4 (Channel 1 Reset Peak Detect)

See the Control Output 6 (Channel 1 Reset Peak Detect) section in the Register 0x035 = 0x0C (Gain Control) section.

Control Output 3 (Channel 2 Reset Peak Detect)

See the Control Output 4 (Channel 2 Reset Peak Detect) section in the Register 0x035 = 0x0C (Gain Control) section.

Control Output 2 and Control Output 1 (Channel 1 RF DC Calibration State [1:0])

These signals represent the state of the Rx1 RF dc calibration state machine.

REGISTER 0x035 = 0x10 (GAIN CONTROL AND RSSI)**Control Output 7 Through Control Output 5 (Channel 2 AGC State [2:0])**

This signal is the same as the signal described in the Control Output 7 Through Control Output 5 (Channel 1 AGC State [2:0]) section (see the Register 0x035 = 0x0F (Gain Control) section), but applies to Rx2.

Control Output 4 (Channel 2 Enable RSSI)

This signal is high when the RSSI word is valid; otherwise, this signal is low.

Control Output 3 (Channel 1 Enable RSSI)

This signal is the same as the Control Output 4 signal described in this section, but applies to Rx1.

Control Output 2 and Control Output 1 (Channel 2 RF DC Calibration State [1:0])

This signal is the same as the signal described in the Control Output 2 and Control Output 1 (Channel 1 RF DC Calibration State [1:0]) section (see the Register 0x035 = 0x0F (Gain Control) section), but applies to Rx2.

REGISTER 0x035 = 0x11 (AUXILIARY ADC DIGITAL OUTPUT)**Control Output 7 Through Control Output 0 (Auxiliary ADC Output [11:4])**

These bits are the most significant 8 bits of the auxiliary ADC digital word.

REGISTER 0x035 = 0x12 (GAIN CONTROL, POWER WORD READY)**Control Output 7 (Channel 1 Filter Power Ready)**

This signal pulses high when the power measurement using the HB1 or FIR outputs is valid. The time the signal remains high is dependent on the internal clock rates of the [AD9363](#). For the standard customer software LTE 10 MHz profile, the signal is high for approximately 65 ns.

Control Output 6 (Channel 1 Gain Lock)

See the Control Output 6 (Channel 1 Gain Lock) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 5 (Channel 1 Energy Lost)

See the Control Output 5 (Channel 1 Energy Lost) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 4 (Channel 1 Stronger Signal)

See the Control Output 7 (Channel 1 Stronger Signal) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 3 (Channel 1 ADC Power Ready)

If ADC power is used for AGC power measurements, this signal pulses high when a new power word is ready. The [AD9363](#) internal clock rates determine the pulse durations. The interval between updates is set by the weight of the ADC power multipliers (see Equation 20).

Control Output 2 Through Control Output 0 (Channel 1 AGC State [2:0])

See the Control Output 3 Through Control Output 1 (Channel 1 AGC, Small [2:0]) section in the Register 0x035 = 0x07 (Rx Gain Control) section.

REGISTER 0x035 = 0x13 (GAIN CONTROL, POWER WORD READY)**Control Output 7 (Channel 2 Filter Power Ready)**

This signal is the same as the signal described in the Control Output 7 (Channel 1 Filter Power Ready) section (see the Register 0x035 = 0x12 (Gain Control, Power Word Ready) section), but applies to Rx2.

Control Output 6 (Channel 2 Gain Lock)

This signal is the same as the signal described in the Control Output 2 (Channel 2 Gain Lock) section (see the Register 0x035 = 0x08 (Rx Gain Control) section).

Control Output 5 (Channel 2 Energy Lost)

See the Control Output 1 (Channel 2 Energy Lost) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 4 (Channel 2 Stronger Signal)

See the Control Output 3 (Channel 2 Stronger Signal) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 3 (Channel 2 ADC Power Ready)

This signal is the same as the signal described in the Control Output 3 (Channel 1 ADC Power Ready) section (see the Register 0x035 = 0x12 (Gain Control, Power Word Ready) section), but applies to Rx2.

Control Output 2 Through Control Output 0 (Channel 2 AGC State [2:0])

This signal is the same as the signal described in the Control Output 2 Through Control Output 0 (Channel 1 AGC State [2:0]) section (see the Register 0x035 = 0x12 (Gain Control, Power Word Ready) section), but applies to Rx2.

REGISTER 0x035 = 0x14 (DIGITAL OVERFLOW)**Control Output 7 (Channel 2 Tx Interpolation Filter 3 Overflow)**

This signal is the same as the signal described in the Control Output 7 (Channel 1 Tx Interpolation Filter 3 Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 6 (Channel 2 Tx HB3 Overflow)

This signal is the same as the signal described in the Control Output 6 (Channel 1 Tx HB3 Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 5 (Channel 2 Tx HB2 Overflow)

This signal is the same as the signal described in the Control Output 5 (Channel 1 Tx HB2 Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 4 (Channel 2 Tx QEC Overflow)

This signal is the same as the signal described in the Control Output 4 (Channel 1 Tx QEC Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 3 (Channel 2 Tx HB1 Overflow)

This signal is the same as the signal described in the Control Output 3 (Channel 1 Tx HB1 Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 2 (Channel 2 Tx FIR Overflow)

This signal is the same as the signal described in the Control Output 2 (Channel 1 Tx FIR Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 1 (Channel 2 Rx FIR Overflow)

This signal is the same as the signal described in the Control Output 1 (Channel 1 Rx FIR Overflow) section (see the Register 0x035 = 0x0A (Digital Overflow) section), but applies to Tx2.

Control Output 0

This signal is always zero.

REGISTER 0x035 = 0x15 (DC OFFSET TRACKING)**Control Output 7 (Channel 1 SOI Present)**

This signal is high when the digital signal power exceeds the RF dc offset SOI threshold. In MGC mode, this is always true. For AGC modes, this signal goes low when the gain updates. The pulse low occurs each time the gain update counter expires (for slow AGC mode) or when Control Input 2 transitions high (for hybrid mode). The time duration of the low pulse is dependent on the [AD9363](#) internal clock rates. For the standard LTE 10 MHz profile, the duration is approximately 400 ns. In fast AGC mode, the signal goes low while the AGC moves through its states. When the gain locks, the signal transitions high when the digital signal level exceeds the SOI threshold.

Control Output 6 (Channel 1 Update DC RF)

This signal pulses high when the RF dc offset word updates. The duration of the pulse is dependent on the [AD9363](#) internal clock rates. For the standard LTE 10 MHz profile, the pulse is approximately 30 ns.

Control Output 5 (Channel 1 Measure DC RF)

This signal is high when the RF dc offset is actively being calculated and when the correction words are generated. New correction words are only applied at times set by the dc offset update. In any gain control mode, if the gain changes, this signal is low, indicating that the RF dc offset algorithm is waiting for the gain to finish changing before calculating new correction words.

Control Output 4 (Channel 1 DC Track Count Reached)

This signal pulses high when the RF dc tracking count is reached. This event signals that the correction word can update with a new value. The value is not applied until an event occurs, as specified in the dc offset update. The [AD9363](#) internal clock rates determine the duration of the pulse. For the standard LTE 10 MHz profile, the pulse is approximately 30 ns.

Control Output 3 Through Control Output 0

This signal is always zero.

REGISTER 0x035 = 0x16 (GAIN CONTROL)**Control Output 7 (Channel 1 Gain Lock)**

See the Control Output 6 (Channel 1 Gain Lock) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 6 Through Control Output 0 (Channel 1 Rx Gain [6:0])

These signals represent the gain index of Rx1, but only apply to the AGC modes. For the full gain table mode, this is the index of the full gain table. For the split gain table mode, this index is for the LMT table. The baseband processor must read the index of the LPF table using SPI reads.

REGISTER 0x035 = 0x17 (GAIN CONTROL)**Control Output 7 (Channel 2 Gain Lock)**

See the Control Output 2 (Channel 2 Gain Lock) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 6 Through Control Output 0 (Channel 2 Rx Gain [6:0])

This signal is the same as the signal described in the Control Output 6 Through Control Output 0 (Channel 1 Rx Gain [6:0]) section (see the Register 0x035 = 0x16 (Gain Control) section), but applies to Rx2.

REGISTER 0x035 = 0x18 (DC OFFSET TRACKING, POWER WORD READY)**Control Output 7 (Channel 2 SOI Present)**

This signal is the same as the signal described in the Control Output 7 (Channel 1 SOI Present) section (see the Register 0x035 = 0x15 (DC Offset Tracking) section), but applies to Rx2.

Control Output 6 (Channel 2 Update DC RF)

This signal is the same as the signal described in the Control Output 6 (Channel 1 Update DC RF) section (see the Register 0x035 = 0x15 (DC Offset Tracking) section), but applies to Rx2.

Control Output 5 (Channel 2 Measure DC RF)

This signal is the same as the signal described in the Control Output 5 (Channel 1 Measure DC RF) section (see the Register 0x035 = 0x15 (DC Offset Tracking) section), but applies to Rx2.

Control Output 4 (Channel 2 DC Track Count Reached)

This signal is the same as the signal described in the Control Output 4 (Channel 1 DC Track Count Reached) section (see the Register 0x035 = 0x15 (DC Offset Tracking) section), but applies to Rx2.

Control Output 3 (Channel 2 Enable Decimation Power)

This signal is high when the Rx2 decimated power word is valid. In manual gain mode, this is always true. In the AGC modes, the signal pulses low when the gain changes, indicating that the decimated power word is not correct while the gain is changing. The time that the signal is held low depends on the gain control mode and the [AD9363](#) internal clock rates but is generally in the hundreds of nanoseconds. For example, for the slow AGC mode and the standard LTE 10 MHz customer software profile, the signal is low for approximately 400 ns.

Control Output 2 (Channel 2 Enable ADC Power)

This signal operates in the same manner as Control Output 3 described in this section, but applies to the ADC power measurement for Channel 2.

Control Output 1 (Channel 1 Enable Decimation Power)

This signal operates in the same manner as Control Output 3 described in this section, but applies to Rx1.

Control Output 0 (Channel 1 Enable ADC Power)

This signal operates in the same manner as Control Output 2 described in this section, but applies to Rx1.

REGISTER 0x035 = 0x19 (CHARGE PUMP CALIBRATION STATES)***Control Output 7 Through Control Output 4 (Rx Synthesizer Charge Pump Calibration [3:0])***

These signals represent the state of the receiver charge pump calibration state machine. Most of the calibration time (10 sec of milliseconds) is spent in State 1. Near the end of the calibration, the state machine jumps to State 8 and then, approximately 10 ms later, it steps through State 0 through State 8 in approximately 200 μ s, remaining in State 8 after the calibration.

Control Output 3 Through Control Output 0 (Tx Synthesizer Charge Pump Calibration [3:0])

These signals represent the state of the transmitter charge pump calibration state machine. However, the response of these signals is different than the Rx charge pump calibration bits in Control Output 7 through Control Output 4 (described in this section). For the Tx charge pump calibration, the control outputs step through State 0 through State 8 in approximately 200 μ s, and remain in State 8 after the calibration completes.

REGISTER 0x035 = 0x1A (Rx VCO AND ALC CALIBRATION STATES)***Control Output 7 (Rx Synthesizer VCO Tuning [8])***

The Rx synthesizer VCO tuning algorithm uses a state machine, the state of which is represented by 9 bits. This is the most significant bit of the state. See the Control Output 7 Through Control Output 0 (Rx Synthesizer VCO Tuning [7:0]) section in the Register 0x035 = 0x1C (Rx VCO Calibration States) section for the lower 8 bits.

Control Output 6 Through Control Output 0 (Rx Synthesizer VCO ALC [6:0])

The Rx synthesizer VCO tuning algorithm incorporates an automatic level control (ALC) calibration to fine tune the VCO level. These signals represent the state of the ALC state machine as it calibrates.

REGISTER 0x035 = 0x1B (Tx VCO AND ALC CALIBRATION STATES)***Control Output 7 (Tx Synthesizer VCO Tuning [8])***

This signal is the same as the signal described in the Control Output 7 (Rx Synthesizer VCO Tuning [8]) section (see the Register 0x035 = 0x1A (Rx VCO and ALC Calibration States) section), but applies to the Tx synthesizer.

Control Output 6 Through Control Output 0 (Tx Synthesizer VCO ALC [6:0])

This signal is the same as the signal described in the Control Output 6 Through Control Output 0 (Rx Synthesizer VCO ALC [6:0]) section (see the Register 0x035 = 0x1A (Rx VCO and ALC Calibration States) section), but applies to the Tx synthesizer.

REGISTER 0x035 = 0x1C (Rx VCO CALIBRATION STATES)***Control Output 7 Through Control Output 0 (Rx Synthesizer VCO Tuning [7:0])***

These are the lower eight bits of the Rx synthesizer VCO tuning state machine. See the Control Output 7 (Rx Synthesizer VCO Tuning [8]) section in the Register 0x035 = 0x1A (Rx VCO and ALC Calibration States) section.

REGISTER 0x035 = 0x1D (Tx VCO CALIBRATION STATES)***Control Output 7 Through Control Output 0 (Tx Synthesizer VCO Tuning [7:0])***

These bits are the same as those described in the Register 0x035 = 0x1C (Rx VCO Calibration States) section, but they apply to the Tx synthesizer VCO tuning state machine.

REGISTER 0x035 = 0x1E (GAIN CONTROL, TEMPERATURE SENSE VALID, AUXILIARY ADC VALID)***Control Output 7 (Channel 1 Low Threshold Exceeded)***

This signal only applies to slow AGC mode. If the signal power drops below the inner low threshold, this signal goes high until the measured power is no longer lower than the threshold. When this condition occurs, the slow AGC adjusts the gain in an attempt to keep the signal power between the two inner thresholds. After the gain changes (and assuming that the signal power is now within the inner thresholds), this signal remains high until a new power measurement completes. Thus, it can be hundreds of microseconds or longer before this signal transitions low, even though the gain change already occurred.

Control Output 6 (Channel 1 High Threshold Exceeded)

This signal is similar to Control Output 7 (described in this section), but applies to the inner high threshold of the slow AGC.

Control Output 5 (Channel 1 Gain Update Count Expired)

This signal pulses high when the slow AGC gain update counter expires. The length of the pulse depends on the AD9363 internal clock rates. For the standard LTE 10 MHz customer software profile, the signal is high for approximately 40 ns.

Control Output 4 and Control Output 3 (Channel 1 AGC State [1:0])

See the Control Output 7 Through Control Output 5 (Channel 1 AGC State [2:0]) section in the Register 0x035 = 0x0F (Gain Control) section.

Control Output 2 (Channel 1 Gain Change)

See the Control Output 4 (Channel 1 Gain Change) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

Control Output 1 (Temperature Sensor Valid)

This signal changes state when the temperature sensor word is valid. The baseband processor can manually start a temperature measurement, or it can set up the [AD9363](#) for periodic measurements. For periodic measurements, this control output signal is a square wave with a period equal to double the measurement time interval.

Control Output 0 (Auxiliary ADC Valid)

If the auxiliary ADC is enabled, this signal changes state when the auxiliary ADC word in Register 0x01E and Register 0x01F is valid. This signal is a square wave with a period equal to twice the update time of the auxiliary ADC.

REGISTER 0x035 = 0x1F (GAIN CONTROL)**Control Output 7 (Channel 2 Low Threshold Exceeded)**

This signal is the same as the signal described in the Control Output 7 (Channel 1 Low Threshold Exceeded) section (see the Register 0x035 = 0x1E (Gain Control, Temperature Sense Valid, Auxiliary ADC Valid) section), but applies to Rx2.

Control Output 6 (Channel 2 High Threshold Exceeded)

This signal is the same as the signal described in the Control Output 6 (Channel 1 High Threshold Exceeded) section (see the Register 0x035 = 0x1E (Gain Control, Temperature Sense Valid, Auxiliary ADC Valid) section), but applies to Rx2.

Control Output 5 (Channel 2 Gain Update Counter Expired)

This signal is the same as the signal described in the Control Output 5 (Channel 1 Gain Update Count Expired) (see the Register 0x035 = 0x1E (Gain Control, Temperature Sense Valid, Auxiliary ADC Valid) section), but applies to Rx2.

Control Output 4 and Control Output 3 (Channel 2 AGC Small[1:0])

See the Control Output 7 Through Control Output 5 (Channel 2 AGC State [2:0]) section in the Register 0x035 = 0x10 (Gain Control and RSSI) section.

Control Output 2 (Channel 2 Gain Change)

See the Control Output 0 (Channel 2 Gain Change) section in the Register 0x035 = 0x08 (Rx Gain Control) section.

AUXILIARY ADCs, AUXILIARY DACs, GPOs, AND TEMPERATURE SENSOR

AUXILIARY ADCs, AUXILIARY DACs, GPOs, AND TEMPERATURE SENSOR OVERVIEW

This section describes operation of the auxiliary features available in the AD9363. These features simplify system tasks and lower overall system cost. These features include two 10-bit auxiliary DACs, one 12-bit auxiliary ADC, an internal temperature sensor, and four general-purpose (GPO) output pins.

Auxiliary DACs

The two auxiliary DACs are 10-bit, general-purpose DACs. Each DAC is capable of sourcing 10 mA. For stability, place a 0.1 μ F capacitor on the output of each auxiliary DAC. SPI writes enable the auxiliary DAC. The auxiliary DAC may be set for manual operation or set to automatically toggle during TDD operation to reduce control required from the baseband processor. The auxiliary DAC is configured using the AD9361_AUXDAC_SETUP function. By default, the auxiliary DACs are disabled when the device is first powered up.

In certain applications, it is desirable to delay the auxiliary DAC transition after the enable signal transitions. Each auxiliary DAC has its own receive and transmit mode delay setting in Register 0x30 through Register 0x33. Each LSB equals approximately 1 μ s. Register 0x3A must be set based on the reference clock to program a 1 μ s delay. Set Bits[D6:D0] to the number of reference clock cycles per μ s minus one. Figure 54 shows the auxiliary DAC code vs. the output voltage for four different reference voltage settings for AUXDAC1.

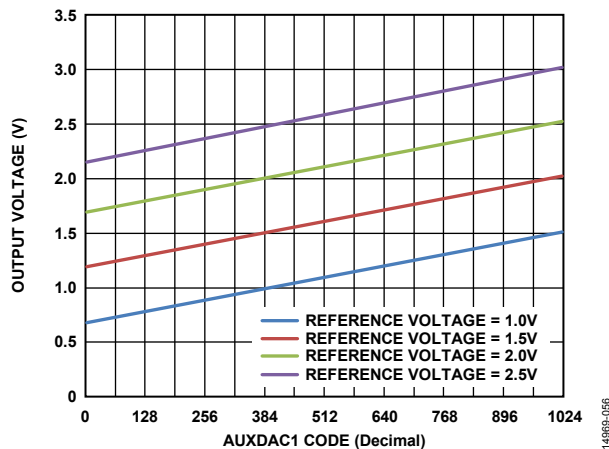


Figure 54. Auxiliary DAC Output Voltage vs. AUXDAC1 Code

AUXILIARY ADC

The auxiliary ADC is a 12-bit auxiliary converter with an input level range of 0 V to 1.3 V with an adjustable conversion time. Configure the auxiliary ADC using the AD9361_AUXADC_SETUP function. The auxiliary ADC allows monitoring of desired voltages, such as a power amplifier power detector or an external temperature sensor. A small value capacitor (680 pF) can be placed on the AUXADCx pin to improve noise performance. The AD9363 also includes an internal temperature sensor that can be measured using the auxiliary ADC. Note that the

auxiliary ADC can only be used to measure either the internal temperature or the voltage on the AUXADCx pin at a time.

Figure 56 shows the auxiliary ADC code vs. input voltage. The auxiliary ADC is turned off by default. The auxiliary ADC clock is generated by dividing the baseband PLL frequency. Equation 21 and Equation 22 determine the auxiliary ADC clock frequency and the decimation rates.

$$\text{Auxiliary ADC Clock Frequency} = \frac{\text{Baseband PLL Frequency}}{1 + \text{Auxiliary ADC Clock Divider}[5:0]} \quad (21)$$

$$\text{Auxiliary ADC Decimation} = 256 \times 2^{\text{Auxiliary ADC Decimation}[2:0]} \quad (22)$$

The auxiliary ADC output is read from Register 0x1E, Bits[D7:D0] and Register 0x1F, Bits[D3:D0]. To capture the voltage on the AUXADCx pin, route the decimation filter clock on the CTRL_OUT0 pin. To select the auxiliary ADC decimation clock on the CTRL_OUT0 pin, write Register 0x35 to Register 0x1E. Data from Register 0x1E, Bits[D7:D0] and Register 0x1F, Bits[D3:D0] can be latched on the falling edge or on the rising edge of the decimation clock exiting the CTRL_OUT0 pin. The SPI reads must occur before the edge on the control out signal toggles again.

The register settings used during the ramp test shown in Figure 55 are shown in Table 45.

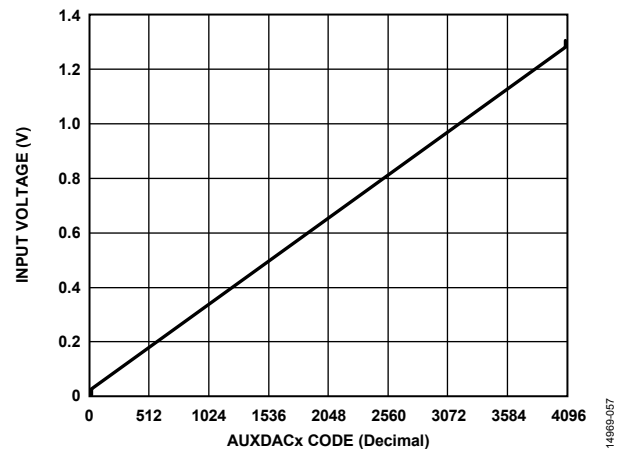


Figure 55. Input Voltage vs. Auxiliary ADC (AUXDACx) Code

Table 45. Example Code for Auxiliary ADC Setup Using the SPI Write Command

Address	Data	Comment
0x00F	0x4	Set the temperature sensor decimation to 4096
0x01C	0x63	Set the auxiliary ADC clock frequency to baseband PLL/36
0x01D	0x0	Enable auxiliary ADC and set decimation to 256
0x035	0x1E	Select auxiliary ADC valid on Control Output 2
0x036	0xFF	Enable all control output pins

INTERNAL TEMPERATURE SENSOR

The auxiliary ADC can be used to measure the internal temperature of the device under test (DUT). To measure the temperature sensor, use the AD9361_AUXDAC_SETUP function to configure the device in temperature sensor mode, and then use the AD9361_GET_TEMP function to conduct a reading. The temperature word has a slope of approximately 1.14 LSB/°C. A single-point factory or bench calibration is required to equate absolute temperature to the temperature word.

Bits[D2:D0] in Register 0x0F set the decimation rate for the auxiliary ADC in temperature sensor mode, per Equation 23.

$$\text{Temperature Sensor Decimation} = 256 \times 2^{\text{Temperature Sensor Decimation}[2:0]} \quad (23)$$

For temperature measurement, the clock frequency of the auxiliary ADC is set to the frequency of the baseband PLL divided by 64. Bits[D7:D1] in Register 0x0D set the rate at which the temperature sensor periodically takes temperature readings, per Equation 24.

$$\text{Calculation Time (sec)} = \frac{\text{Measurement Time Interval}[6:0] \times 2^{29}}{\text{Baseband PLL Clock Frequency(Hz)}} \quad (24)$$

If temperature measurements are to be performed manually (Bit D0 in Register 0x0D is clear), then the measurements start when Bit D0 in Register 0x0C (start temperature reading) is set. Data from Register 0x0E can be latched into the baseband processor on the toggle of the temperature sensor valid signal, Bit D1 in Register 0x0C. Route this signal out on the CTRL_OUT1 pin by writing 0x36 to Register 0x03.

Figure 56 shows the temperature sweep of the AD9363 while reading the internal temperature sensor. Table 46 specifies the register settings used to generate the internal temperature sensor graph plotted in Figure 56

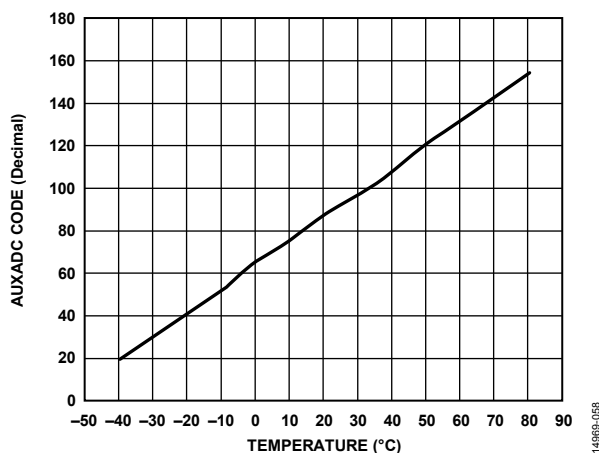


Figure 56. Auxiliary ADC Measuring Internal Temperature Sensor

Table 46. Example Code for Temperature Sensor Setup Using the SPI Write Command

Address	Data	Comment
0x00B	0x0	Set the temperature sensor offset to 0
0x00C	0xF	Temperature sensor is set in manual mode
0x00D	0x0	Calculation time is set to 0 sec
0x00F	0x0	Set the temperature sensor decimation to 256
0x01D	0x1	Disable the AUXADC pin voltage measurement
0x035	0x1E	Select temperature sensor valid on Control Output 1
0x036	0xFF	Enable all control output pins

GENERAL-PURPOSE OUTPUT (GPO) CONTROL

The AD9363 has four GPO pins that can be setup using the AD9361_GPO_SETUP function. The GPOs commonly control antenna switches or the LNA enable. There are two options for controlling the GPOs: manual and automatic. The manual method uses SPI writes from the baseband processor. The automatic method slaves the GPOs to the enable state machine.

When using external LNAs, the AD9363 can optionally slave GPO_0 and GPO_1 off the receive gain tables to control LNA gain on each of the two receivers. The supply voltage to the GPOs comes from a pin, VDD_GPO (Pin B8), on the AD9363 with a nominal supply voltage range of 1.3 V to 3.3 V. Setting Bit D4 in Register 0x026 puts the GPOs in manual control mode. Use the upper nibble (four bits) of Register 0x027 as the GPO logic level controls. GPO_3 uses Bit D7, GPO_2 uses Bit D6, GPO_1 uses Bit D5, GPO_0 uses Bit D4. In this mode, the lower nibble of Register 0x26 is ignored.

GPO Autotoggle

When initializing the GPOs for enable state machine control, set the initial states of the GPOs in the lower nibble of Register 0x27, with GPO_0 corresponding to Bit D0, GPO_1 corresponding to Bit D1, GPO_2 corresponding to Bit D2, and GPO_3 corresponding to Bit D3. Register 0x20 contains the bits that determine how the GPOs respond to state changes from alert.

The upper nibble controls what GPO pins change states when moving to Rx mode, and the lower nibble controls what GPO_x pins change states in Tx mode. For example, set Register 0x26, Register 0x27, and Register 0x20 as follows:

- Register 0x26 = 0x00 (enable state machine control enabled).
- Register 0x27 = 0xFF (initialize all GPO pins to 1).
- Register 0x20 = 0x24 (toggle the GPO_1 pin in Rx mode and GPO_2 in Tx mode).

Using these settings, when the device enters the alert state, all GPO pins become high. When the device enters Tx mode, only the GPO_2 pin toggles low. When the device enters Rx mode, the GPO_1 pin toggles low. This is a typical scenario for a transmit/receive (T/R) switch with differential control.

Some applications require inserting a delay between when the DUT state transitions and when the GPO pin toggles. To accommodate these needs, there are GPO registers that can be programmed to the required delay. Register 0x28 through Register 0x2B set the delay from an enable state machine (ENSM) state change from alert to receive, whereas Register 0x02C through Register 0x02F set the delay from an ENSM state change from alert to transmit. Each LSB is 1 μ s.

The delay settings work only when the TXNRX pin and the ENABLE pin control the state machine. The delay settings do not work when the SPI is used to control the state machine. Depending on the reference clock, program Register 0x3A for a resolution of 1 μ s/LSB. Set Bits[D6:D0] to the number of reference clock cycles per μ s minus one. In FDD mode, the Tx

enable and Tx delays are applied and the Rx enable and Rx delays are ignored.

Figure 57 shows the timing of the GPOs and AUXDAC1 (based on the code written in Table 46) when the device transitions from alert to receive. The pink trace shows when the ENABLE pin is toggled. Note that after 10 μ s, GPO_0 (blue trace) and GPO_1 (yellow trace) change states and AUXDACx (green trace) begins ramping up to the desired voltage.

GPO Voltage Level, Drive Strength

The VDD_GPO pin (Pin B8), which has a voltage range of 1.3 V to 3.3 V, sets the output high logic level of the GPO. The off resistance of the GPO_x pins is 15 Ω . The on resistance of the GPO_x pins is 32 Ω .

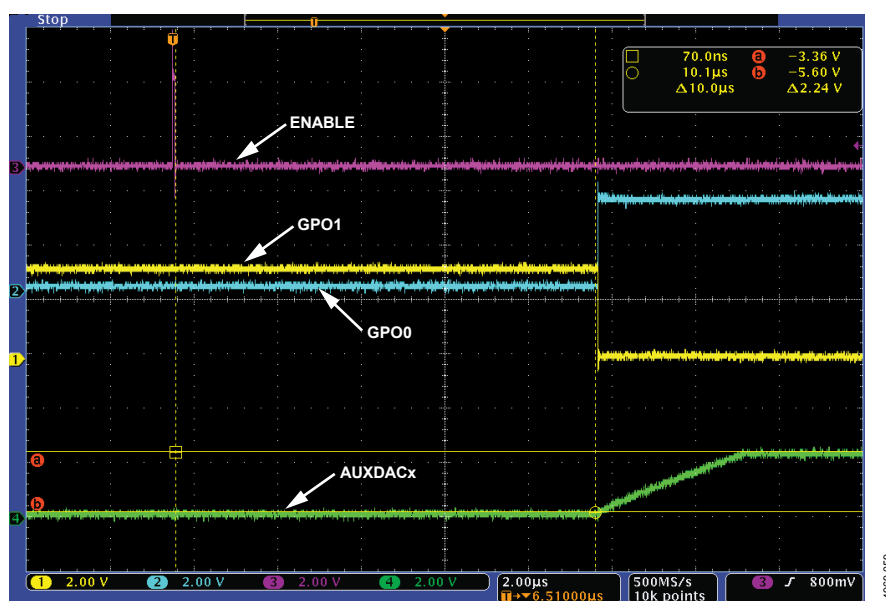


Figure 57. GPO/Auxiliary DAC Toggle: Alert to Rx

DIGITAL INTERFACE SPECIFICATION

DIGITAL INTERFACE SPECIFICATION OVERVIEW

This section defines the parallel data ports and the SPI that enable the transfer of data and control/status information between the [AD9363](#) and a baseband processor. Figure 59 shows these interfaces and provides a high level view of how the [AD9363](#) and baseband processor are used in a broadband wireless system.

The data interface operates in one of two modes: standard CMOS-compatible mode or low voltage differential signal (LVDS)-compatible mode. Each interface possesses unique characteristics described in the following sections.

When CMOS mode is used,

- Single-ended CMOS logic compatibility is maintained.
- Either one or both data ports can be used. Using two ports allows higher data throughput.
- Both FDD and TDD operation are supported with one or two data ports.

When LVDS mode is used,

- Data port signaling is differential LVDS, allowing up to 12 inch PCB traces or connector interconnects between the [AD9363](#) and the baseband processor.
- Only the data port (including clocking and other associated timing signals) is LVDS compatible.
- Both FDD and TDD operations are supported.

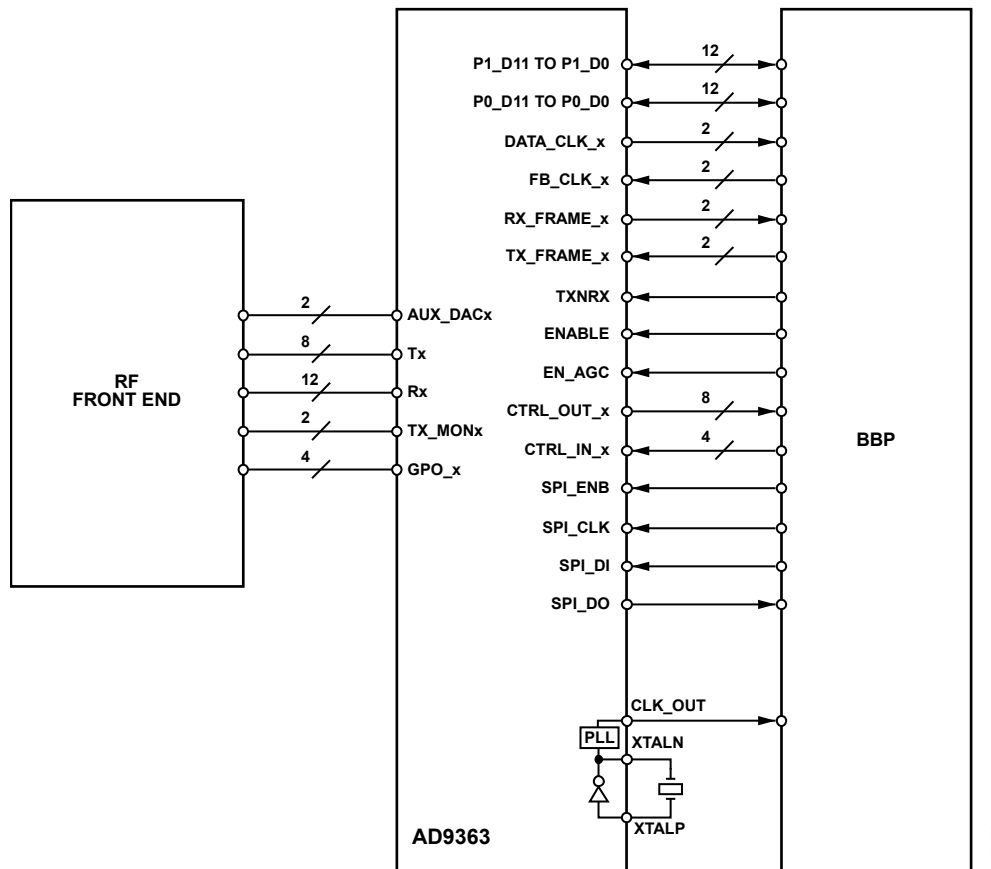


Figure 58. [AD9363](#) Interface

SYNCHRONIZATION VERIFICATION

This section describes operation of the [AD9363](#) datapath in CMOS mode. In this mode, the [AD9363](#) datapath interface can use either or both parallel data ports to transfer data samples between the [AD9363](#) and the baseband processor. The bus transfers are controlled using simple hardware handshake signaling. The two ports can be operated in either FDD mode or bidirectional TDD mode.

In FDD mode, half of the bits transmit data and the other half receive data simultaneously. In TDD mode, the transmit data and receive data are alternately transferred between the [AD9363](#) and the baseband processor on the same pins during different time slots. For applications that do not require fast effective data rates, a single port can be used to minimize connections to the [AD9363](#). The datapath interface consists of the signals described in the following sections.

P0_D11 to P0_D0 and P1_D11 to P1_D0

Both Port 0 (P0_Dx) and Port 1 (P1_Dx) have a 12-bit parallel data bus (Px_D11 to Px_D0, referred to as D[11:0]) that transfers data between the baseband processor and the [AD9363](#). Each bus is identical to the other in size and function, so D[11:0] is used to refer to either Port 0 or Port 1. These buses can be configured as transmit only, receive only, or bidirectional.

DATA_CLK Signal

The DATA_CLK signal is provided to the baseband processor as a master clock for the Rx datapath. In CMOS mode, it is generated internally and output on the DATA_CLK_P pin (DATA_CLK_N is left unconnected). The same clock is used for Port 0, Port 1, or both ports, depending on the data bus configuration. The baseband processor uses this master clock as the timing reference for the interface data transfers and for the baseband data processing. The DATA_CLK signal provides source synchronous timing with dual edge capture (DDR) or single rising edge capture (SDR) data transfer during a receive operation.

The DATA_CLK signal frequency generated depends on the system architecture (such as, number of RF channels, degree of oversampling, and bandwidth mode).

FB_CLK Signal

FB_CLK is a feedback (looped back) version of the DATA_CLK signal driven from the baseband processor to the FB_CLK_P pin in CMOS mode (FB_CLK_N is left unconnected). FB_CLK allows source synchronous timing with rising edge capture for the burst control signals (TX_FRAME, ENABLE, and TXNRX). FB_CLK also provides source synchronous timing with dual edge capture (DDR) or single rising edge capture (SDR) for D[11:0] data signals during Tx bursts (both Port 0 and Port 1). Note that FB_CLK must be a feedback version of DATA_CLK (exact same frequency and duty cycle), but there is no phase relationship requirement between the two clock signals.

RX_FRAME Signal

The RX_FRAME signal is driven by the [AD9363](#) to identify valid data for the Rx datapath (both Port 0 and Port 1). A high transition indicates the beginning of the frame. RX_FRAME can be set to be a single high transition at the beginning of a burst and stay high throughout the burst, or it can be set to be a pulse train that has a rising edge at the beginning of each frame (50% duty cycle). In CMOS mode, this signal is output from the RX_FRAME_P pin (RX_FRAME_N can be left unconnected).

TX_FRAME Signal

TX_FRAME is driven by the baseband processor to identify valid data for the Tx datapath (both Port 0 and Port 1). A high transition indicates the beginning of the frame. The baseband processor can set TX_FRAME to be a single high transition at the beginning of a burst that stays high throughout the burst, or it can set TX_FRAME to a pulse train that has a rising edge at the beginning of each frame (50% duty cycle). The [AD9363](#) accepts either format. In CMOS mode, this signal is input to the TX_FRAME_P pin (TX_FRAME_N is tied to ground).

The [AD9363](#) transmits null data (all zeros) until the first TX_FRAME indicates valid data. This is a useful feature when the Tx path completes a transmit operation in FDD independent mode and the datapath is not automatically flushed. In this case, the TX_FRAME pin can be held low to complete the data flushing operation. See the Enable State Machine (ENSM) Guide section for more details.

Note that the interface requires both the RX_FRAME and TX_FRAME signals to function properly.

ENABLE

ENABLE is driven from the baseband processor to the [AD9363](#) to provide data transfer burst control (along with TXNRX) in TDD mode. ENABLE is asserted by the baseband processor for a minimum of a single DATA_CLK cycle to indicate the start of each burst. It is subsequently asserted a second time for a minimum of a single DATA_CLK cycle to indicate the end of each burst.

The [AD9363](#) internally tracks the sequence of ENABLE pulses to interpret each pulse correctly as either the start or finish of each burst. The ENABLE signal also can be configured in level mode, in which an edge transition (not pulses) determines when the ENSM moves between states. The level sampled on TXNRX during each ENABLE start event controls the bus direction in TDD mode. The start and finish latencies (between the ENABLE pulses being sampled by the [AD9363](#) and the presence of the first and last valid data samples on the bus) vary depending on the datapath configuration. The RX_FRAME and TX_FRAME signals are used to determine valid data by the baseband processor and the [AD9363](#), respectively. The FB_CLK signal is used to sample this input.

In FDD mode, the ENABLE signal serves as the single control input to determine the state of the ENSM. There is also an alternative FDD mode in which the ENABLE signal can be redefined as Rx on, a direct hardware control input to the ENSM that controls the Rx function. In this mode (called FDD independent control mode), the baseband processor independently controls the Rx function, which can result in power consumption savings.

TXNRX

TXNRX is driven from the baseband processor to the AD9363 and provides data transfer burst control (along with ENABLE) when the data bus is in TDD mode. When ENABLE is sampled high by the AD9363 to start a burst, the level on TXNRX is also sampled to determine the data direction. In TDD mode, TXNRX sampled high indicates a transmit burst and TXNRX sampled low indicates a receive burst.

The TXNRX signal level must be maintained throughout a data transfer burst (a valid logic level). The TXNRX signal may be established any number of cycles (≥ 0) before the ENABLE start pulse is sampled, and it may be changed any number of cycles (≥ 0) after the ENABLE finish pulse is sampled. It is important

to note that the TXNRX signal can only change state while the ENSM is in the ALERT state because the TXNRX signal powers up and powers down the synthesizers directly in TDD mode.

In normal FDD mode, the TXNRX signal is ignored but must be held at a valid logic level. There is also an alternative FDD mode in which the TXNRX signal can be redefined as Tx on, a direct hardware control input to the ENSM that controls the Tx function. In this mode (called FDD independent control mode), the baseband processor independently controls the Tx function, which can result in power consumption savings.

CMOS Maximum Clock Rates and Signal Bandwidths

The data listed in Table 47 compares the maximum data clock rates and maximum RF signal bandwidths in the different allowable operating modes for the CMOS data bus configuration. Maximum RF bandwidths are listed for two cases: sampling using the minimum sample rate that avoids aliasing, and sampling using $2\times$ oversampling. Details of each mode are given in subsequent sections. The maximum DATA_CLK rate is limited to 61.44 MHz, so the data rates are limited by this factor and the 56 MHz maximum analog filter bandwidth.

Table 47. Maximum Data Rates (SDR and DDR) and Signal Bandwidths

Operating Mode	1R1T Configurations						1R2T/2R1T/2R2T Configurations					
	Maximum Data Rate (Combined I and Q Words)		Maximum RF Channel Signal Bandwidth				Maximum Data Rate (Combined I and Q Words)		Maximum RF Channel Signal Bandwidth (Per Channel)			
			Using Minimum Sample Frequency		Using 2× Oversampling				Using Minimum Sample Frequency		Using 2× Oversampling	
	SDR (MSPS)	DDR (MSPS)	SDR Bus (MHz)	DDR Bus (MHz)	SDR Bus (MHz)	DDR Bus (MHz)	SDR (MSPS)	DDR (MSPS)	SDR Bus (MHz)	DDR Bus (MHz)	SDR Bus (MHz)	DDR Bus (MHz)
Single Port												
Half Duplex	30.72	61.44	30.72	56 ¹	15.36	30.72	15.36	30.72	15.36	30.72	7.68	15.36
Full Duplex	15.36	30.72	15.36	30.72	7.68	15.36	7.68	15.36	7.68	15.36	3.84	7.68
Dual Port												
Half Duplex	61.44	122.88	56 ¹	56 ¹	30.72	56 ¹	30.72	61.44	30.72	56 ¹	15.36	30.72
Full Duplex	30.72	61.44	30.72	56 ¹	15.36	30.72	15.36	30.72	15.36	30.72	7.68	15.36

¹ Limited by the analog filter bandwidth.

SINGLE-PORT, HALF DUPLEX MODE (CMOS)

Single-port, half duplex mode is used in applications requiring TDD operation and data rates of less than 61.44 MHz. In this mode, the bus is used in a bidirectional manner so that data can be received or transmitted on the same lines. This mode can be used with all receiver-transmitter configurations (1R1T, 2R1T, 1R2T, and 2R2T) and is typically employed when there is limited printed circuit board (PCB) space or the baseband processor has only a single data bus port available.

The bus can be operated as either single data rate (SDR) or dual data rate (DDR) in this configuration. In this mode, the enabled port is multiplexed between transmit and receive operation and the unused port is disabled. The enabled port is determined by the swap ports bit in SPI Register 0x012. Figure 60 shows the connections between the AD9363 and the baseband processor for this mode of operation.

During an Rx burst, D[11:0] is driven by the AD9363 such that the setup and hold times between DATA_CLK_x and Px_D11 to Px_D0 arriving allow the baseband processor to use DATA_CLK_x to capture the data. Similarly, during a Tx burst, Px_D11 to Px_D0 is driven by the baseband processor such that the

setup and hold times between FB_CLK_x and Px_D11 to Px_D0 allow the AD9363 to use FB_CLK_x to capture the data.

A data transfer starts when the ENABLE signal pulses (or goes high); the end of the data transfer is marked but another pulse on the ENABLE line (or when it returns to low). The direction of the data transfer is determined by the TXNRX signal. When this signal is low and the enable state machine is in the Rx or FDD state, the bus is configured in the receive direction (data transferred from AD9363 to the baseband processor). When TXNRX is driven high and the enable state machine has moved out of the Rx or FDD state, the enable state machine changes the bus to the transmit direction (data transferred from the baseband processor to the AD9363).

The RX_FRAME and TX_FRAME signals indicate the beginning of a set (frame) of data samples. The RX_FRAME signal can be set to occur once at the beginning of the burst (one high transition only) for each data transfer, or to have a rising edge at the beginning of each frame and repeat with a 50% duty cycle until the data transfer is complete. Similarly, TX_FRAME accepts either format from the baseband processor.

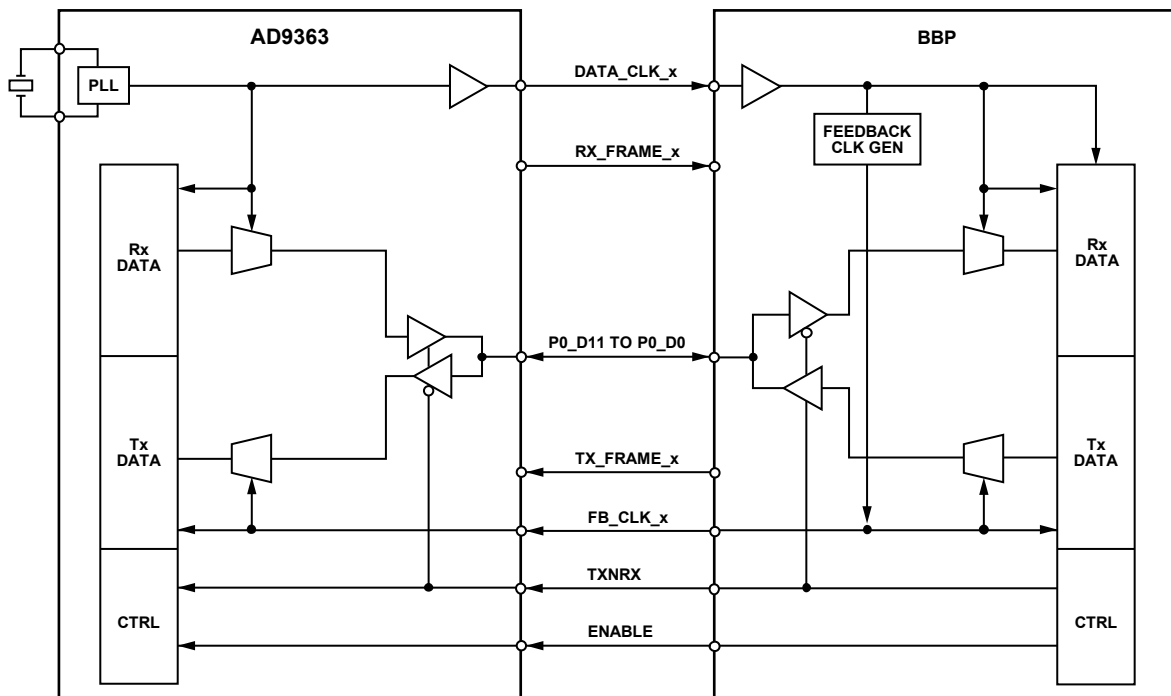


Figure 59. Single-Port TDD Mode Bus Configuration

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During a transmit burst, the baseband processor drives the data values on P0_D11 to P0_D0 using the FB_CLK and TX_FRAME signals. During a Rx burst, the AD9363 drives the data values on P0_D11 to P0_D0 using the DATA_CLK and RX_FRAME signals.

The data samples are carried in twos complement format, with Bit D11 as the numerically most significant bit and Bit D0 as the least significant bit. Thus, the most positive sample value is 0x7FF and the most negative value is 0x800. In this mode, the I and Q data samples are time interleaved on the data bus. For a single RF path in each direction (a 1R1T system), the I and Q samples are carried in a 2-way interleave—I, Q, I, Q, ..., and so on.

For a system utilizing two Rx/Tx channels, the I and Q samples from RF Channel 1 and Channel 2 are carried in a 4-way interleave—I1, Q1, I2, Q2, I1, Q1, I2, Q2, ..., and so on.

For a system with a 2R1T or 1R2T configuration, the clock frequencies, sample periods, and data capture timing are the same as if configured for a 2R2T system. However, in the path with only a single channel used, the I-Q pair of the disabled channel in each data group is unused. These unused slots are ignored by the AD9363. For example, in a 2R1T system with only Tx Channel 1 used, the transmit burst has two unused slots as follows: I, Q, X, X, I, Q, X, X, ..., and so on.

The unused X slots may be filled with arbitrary data values by the baseband processor. Such values can be fixed constant

values, or the preceding data sample values can be repeated to reduce the bus switching factor and, therefore, power consumption.

SINGLE-PORT TDD FUNCTIONAL TIMING (CMOS)

The timing diagrams in Figure 61 and Figure 62 show the relationship among the bus signals in single-port TDD mode. These diagrams show an example of timing for both SDR and DDR modes of operation. For all subsequent sections in this section, only DDR timing is shown.

Figure 61 and Figure 62 also include the timing diagrams for the 1R1T scenario where the 2R2T timing bit is set, forcing the data transfer format to be the same as the 2R2T case. This mode is useful for single-port systems that may need to switch between single-channel and multichannel operation, but cannot change their data transfer format. The 2R2T bit has no effect if the device is not configured in 1R1T mode.

Note that the TX_FRAME signal and Tx data must be transmitted such that they meet the setup and hold requirements relative to FB_CLK. In addition to the 1R1T and 2R2T scenarios, 1R2T and 2R1T configurations show that their timing is identical to the 2R2T configuration. Behavior with different combinations of receiver and transmitter channels in other modes also follows the 2R2T timing behavior; therefore, for all subsequent sections in this reference manual, these plots are omitted from the figures.

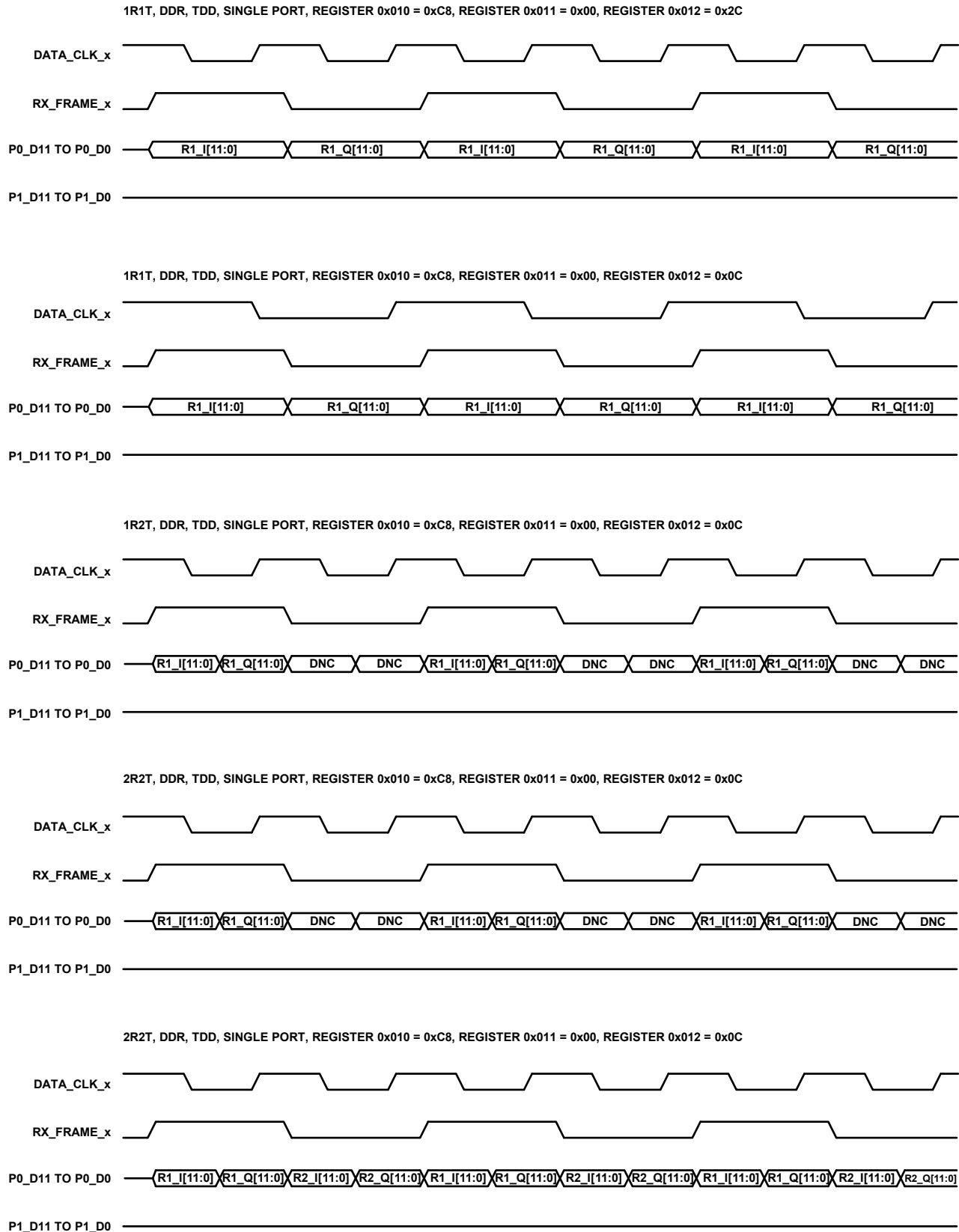


Figure 60. Receiver Datapath, Single-Port TDD (DNC Means Don't Care)

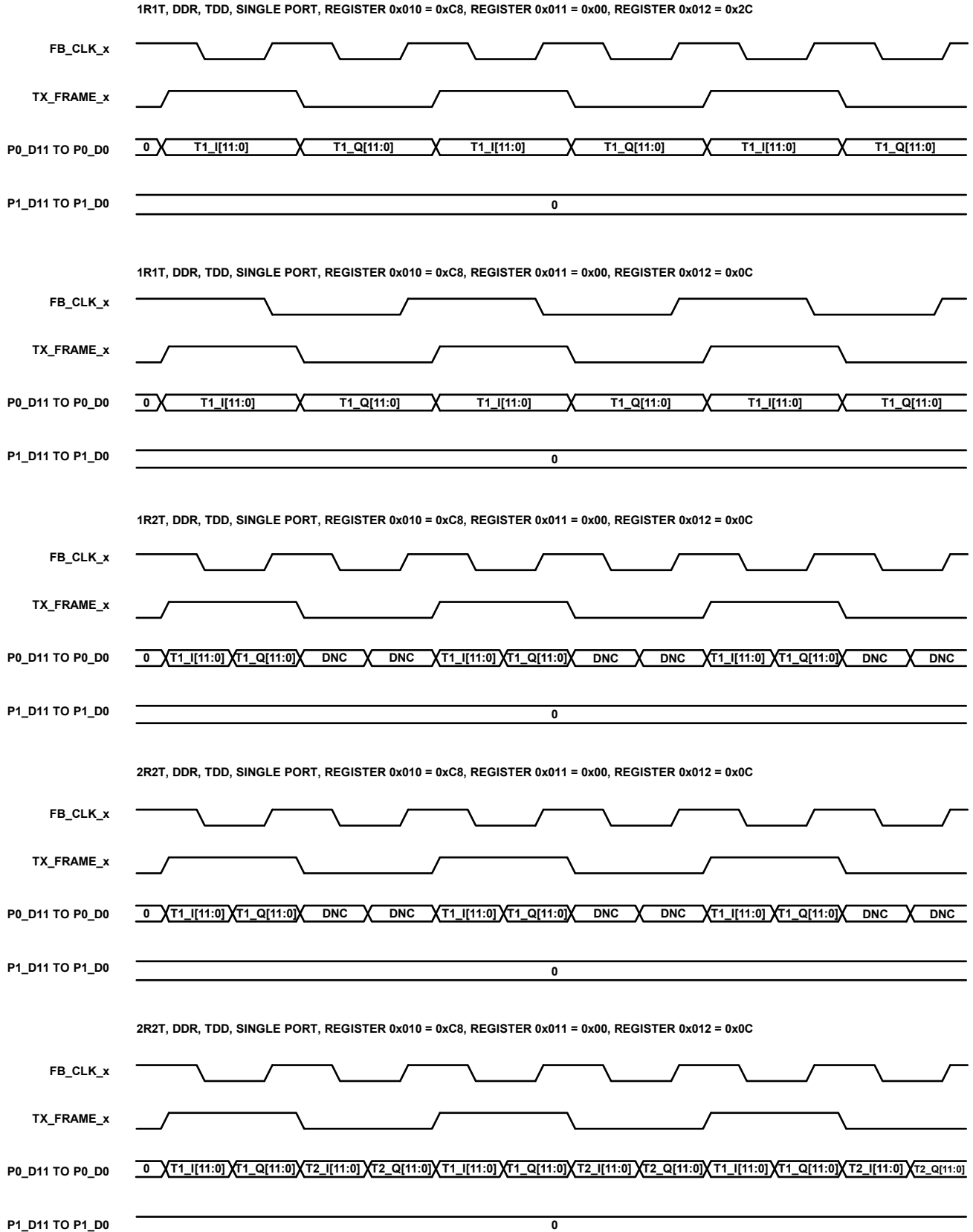


Figure 61. Transmitter Datapath, Single-Port TDD (DNC Means Don't Care)

SINGLE-PORT, FULL DUPLEX MODE (CMOS)

Single-port, full duplex mode is used in applications requiring FDD operation and data rates less than 30.72 MHz. In this mode, the bus is split in half with six bits dedicated to Rx data and six bits dedicated to Tx data. This mode can be used with all receiver and transmitter configurations. The bus can be operated as either SDR or DDR in this configuration. In this example, only Port 0 is enabled and the data bus is split into separate sub buses.

Each subbus operates simultaneously allowing full duplex of transmit and receive data between the baseband processor and the [AD9363](#). Because the bus must complete twice as many data transfers for full duplex mode, the data bus must operate at twice the speed of the TDD mode to achieve the same transmit and receive data rates (as each are running concurrently in full duplex). Figure 62 shows the connections between the [AD9363](#) and the baseband processor for this mode of operation.

Transmit data is driven on P0_D11 to P0_D6 by the baseband processor such that the setup and hold times between FB_CLK_x and P0_D11 to P0_D6 allow the [AD9363](#) to use FB_CLK_x to capture the data. Receive data is driven on P0_D5 to P0_D0 by the [AD9363](#) such that the setup and hold times between DATA_CLK_x and P0_D5 to P0_D0 arriving at the baseband processor enable the baseband processor to use DATA_CLK_x to capture the data. A pulse on the ENABLE pin (or a rising edge) triggers the beginning of data transfer, and another pulse (or falling edge) signifies the end of data transfer.

The RX_FRAME and TX_FRAME signals indicate the beginning of a set (frame) of data samples. The RX_FRAME signal can be set to occur once at the beginning of the burst (one high transition only) for each data transfer or to have a rising edge at the beginning of each frame and repeat with a 50% duty cycle until the data transfer is complete. Similarly, the TX_FRAME signal accepts either format from the baseband processor.

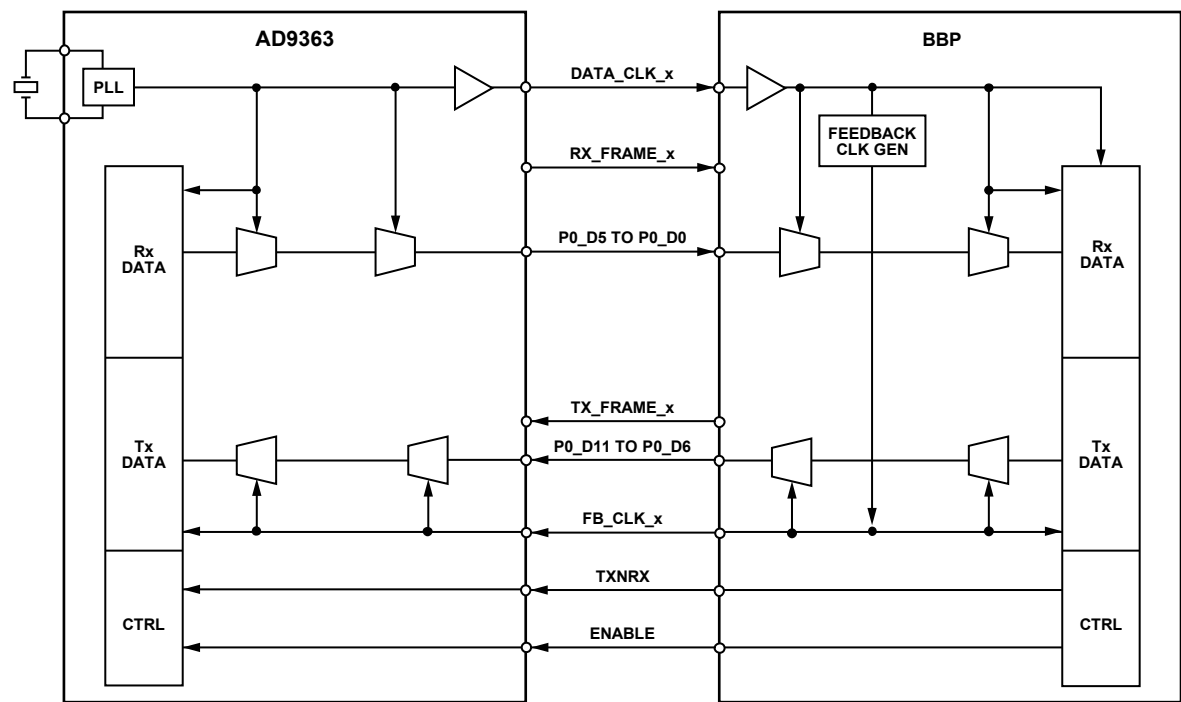
The transmit data samples are carried in twos complement format, with the first 6-bit byte (P0_D[11:6]) containing the MSBs and the second 6-bit byte (P0_D[5:0]) containing the LSBs. P0_D11 is the numerically most significant bit and P0_D6 is the least significant bit. The receive data samples are also carried in twos complement format, with the first 6-bit byte (P0_D5 to P0_D0) containing the MSBs and the second 6-bit byte (P0_D5 to P0_D0) containing the LSBs. P0_D5 is the numerically most significant bit and P0_D0 is the least significant bit. In both cases, the most positive sample value is 0x7FE, with the first byte being 0x1F and the second byte being 0x3F. The most negative value is 0x800, with the first byte being 0x20 and the second byte being 0x00.

In this mode, the I and Q data samples are time interleaved on the data bus. For a single RF path in each direction (a 1R1T system), the data is carried in a four-way interleave, as follows: I MSB, Q MSB, I LSB, Q LSB, ..., and so on.

For a system with two active Rx/Tx channels, the I and Q samples from RF Channel 1 and Channel 2 are carried in an eight-way interleave, as follows: I1 MSB, Q1 MSB, I1 LSB, Q1 LSB, I2 MSB, Q2 MSB, I2 LSB, Q2 LSB, ..., and so on.

For a system with a 2R1T or a 1R2T configuration, the clock frequencies, sample periods, and data capture timing are the same as if configured for a 2R2T system. However, in the path with only a single channel used, the I-Q pair of the disabled channels in each data group is unused. These unused slots are ignored by the [AD9363](#). As an example, for a 2R1T system using Transmit Channel 1, the transmit burst has four unused slots, as follows: I1 MSB, Q1 MSB, I1 LSB, Q1 LSB, X, X, X, X, ..., and so on.

The unused X slots can be filled with arbitrary data values by the baseband processor. Such values can be constant values, or the preceding data sample values can be repeated to reduce the bus switching factor and, therefore, power consumption.



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Figure 62. Single-Port, Full Duplex Mode

SINGLE-PORT FDD FUNCTIONAL TIMING (CMOS)

The timing diagrams in Figure 63 and Figure 64 show the relationship among the bus signals in single-port FDD mode. Note that, because 2R1T and 1R2T systems follow the 2R2T timing diagrams, they are omitted from Figure 63 and Figure 64.

DUAL-PORT, HALF DUPLEX MODE (CMOS)

Dual-port, half duplex mode is used in applications requiring TDD operation and data rates up to 122.88 MHz. In this mode, both data ports are used, with Port 0 assigned to I data and Port 1 assigned to Q data. The ports operate bidirectionally in this mode, and data direction is determined by which channel is active: transmit or receive.

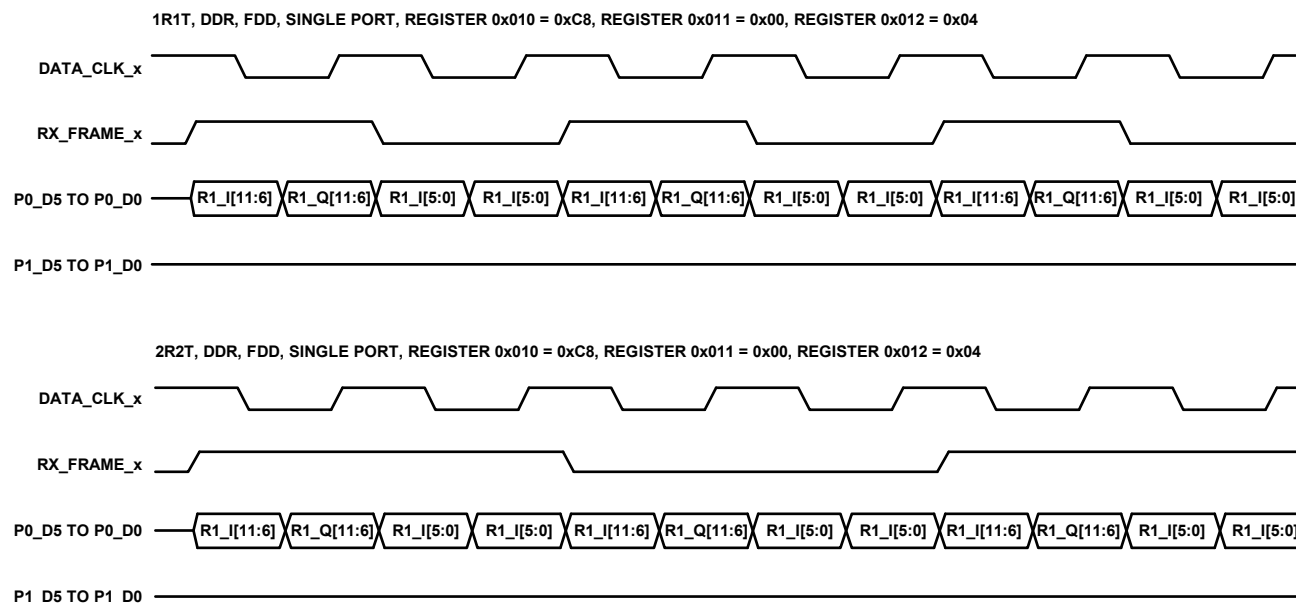


Figure 63. Receive Datapath, Single-Port FDD

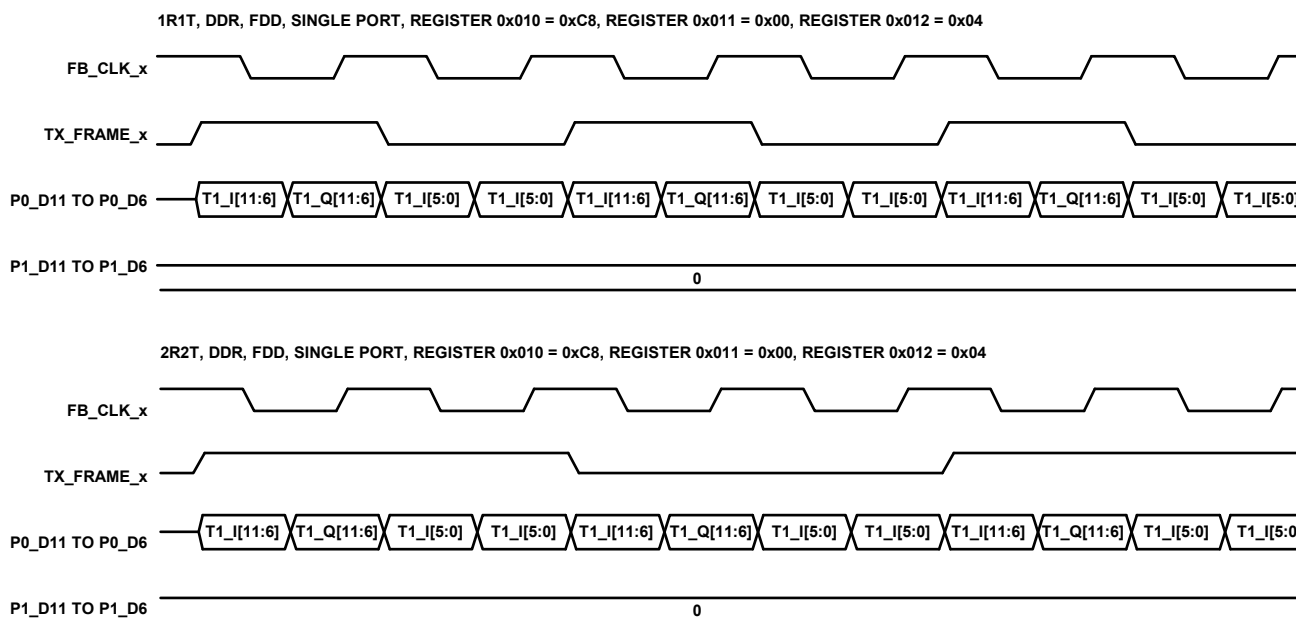


Figure 64. Transmit Datapath, Single-Port FDD

Each bus can be operated as either SDR or DDR in this configuration. This mode can be used with all receiver and transmitter configurations. Figure 65 shows the connections between the AD9363 and the baseband processor for this mode of operation.

During an Rx burst, both ports are driven by the AD9363 such that the setup and hold times between DATA_CLK_x and each data sample arriving at the baseband processor enable the baseband processor to use DATA_CLK_x to capture the data. A data transfer starts when the ENABLE signal pulses (or goes high), and the end of the data transfer is marked but another pulse on the ENABLE line (or when it returns low).

The direction of data transfer is determined by the TXNRX signal. When this signal is low and the AD9363 is in the FDD state or the Rx state, the enable state machine configures the bus in the receive direction (data is transferred from the AD9363 to the baseband processor). All other states result in the bus being set to high impedance. When TXNRX is driven high, the enable state machine changes the bus to the transmit direction (data is transferred from the baseband processor to the AD9363). During a transmit burst, both ports (P0_D11 to P0_D0 and P1_D11 to P1_D0) are driven by the baseband processor such that the setup and hold times between FB_CLK_x and each P_x_D_x allow the AD9363 to use FB_CLK_x to capture the data.

The RX_FRAME and TX_FRAME signals indicate the beginning of a set (frame) of data samples. The RX_FRAME signal can be set to occur once at the beginning of the burst (one high transition only) or to have a rising edge at the beginning of each frame and have a 50% duty cycle. Similarly, TX_FRAME accepts either format from the baseband processor.

The data samples are carried in two's complement format, with Bit D11 being the numerically most significant bit and Bit D0 being the least significant bit. The most positive sample value is 0x7FF and the most negative value is 0x800. For a single RF path in each direction (that is, a 1R1T system), the I and Q samples are separated with I data on P0_D11 to P0_D0, and Q data on P1_D11 to P1_D0, as follows:

- Port 0: I, I, I, ..., and so on.
- Port 1: Q, Q, Q, ..., and so on.

For a system with two active Rx channels, the I and Q samples from RF Path 1 and RF Path 2 are carried in a two-way interleave with I samples on Port 0 and Q samples on Port 1.

- Port 0: I1, I2, I1, I2, ..., and so on.
- Port 1: Q1, Q2, Q1, Q2, ..., and so on.

For a system with a 2R1T or a 1R2T configuration, the clock frequencies, sample periods, and data capture timing are the same as if configured for a 2R2T system. However, in the path with only a single channel used, the I-Q pair in each data group of the disabled channel is unused. As an example, for a 2R1T system with only the Tx Channel 1 used, the Tx burst has two unused slots, as follows:

- Port 0: I₁, X, I₁, X, ..., and so on.
- Port 1: Q₁, X, Q₁, X, ..., and so on.

The unused X slots can be filled with arbitrary data values by the baseband processor. Such values can be either constant values, or the preceding data sample values can be repeated to reduce the bus switching factor and, therefore, power consumption.

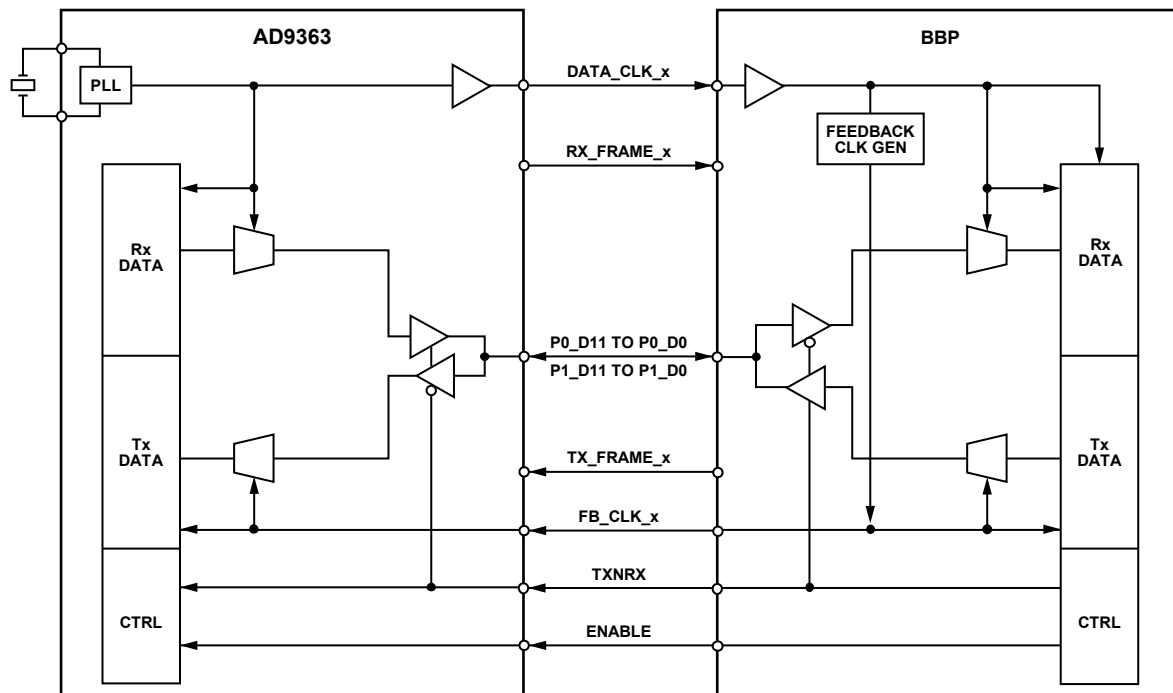


Figure 65. Dual-Port TDD Mode

DUAL-PORT TDD FUNCTIONAL TIMING (CMOS)

The timing diagrams in Figure 66 and Figure 67 show the relationship among the bus signals in dual-port TDD mode. Note that, because 2R1T and 1R2T systems follow the 2R2T timing diagrams, they are omitted from Figure 66 and Figure 67.

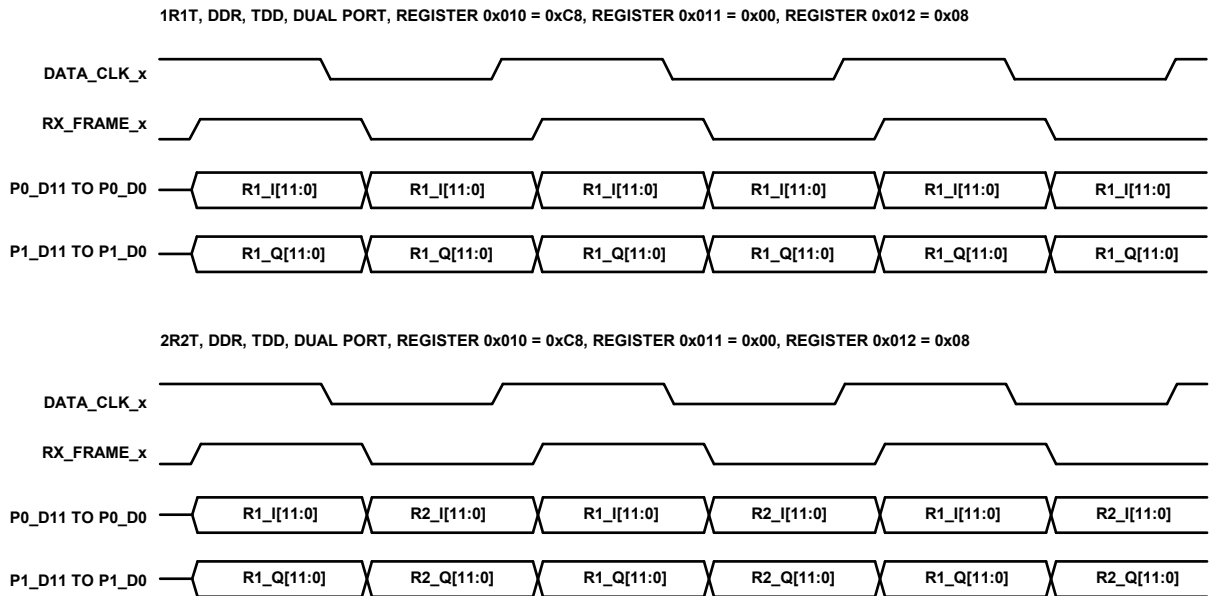


Figure 66. Receiver Datapath, Dual-Port TDD

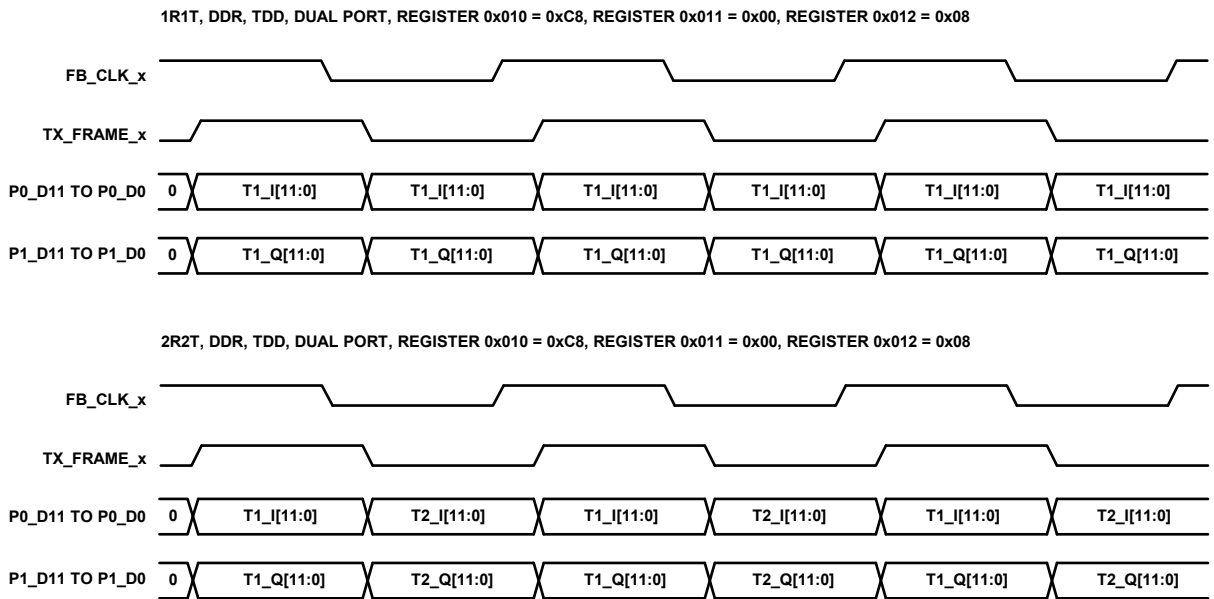


Figure 67. Transmitter Datapath, Dual-Port TDD

DUAL-PORT, FULL DUPLEX MODE (CMOS)

Dual-port, full duplex mode (full port) is used in applications requiring FDD operation and data rates less than 61.44 MHz. In this mode, both data ports are used, with Port 0 assigned to receive data and Port 1 assigned to transmit data. Each bus operates simultaneously, allowing full duplex transfer of Tx and Rx data between the baseband processor and the AD9363. For this mode, each data bus must operate at twice the speed of the dual-port TDD mode to achieve the same Tx and Rx data rates because each bus is running concurrently in full duplex mode. Each bus can be operated as either SDR or DDR in this configuration. This mode can be used with all receiver and transmitter configurations. Figure 68 shows the connections between the AD9363 and the baseband processor for this mode of operation.

Transmit data is driven on P1_D11 to P1_D0 by the baseband processor such that the setup and hold times between FB_CLK_x and data allow the AD9363 to use FB_CLK_x to capture the data. Receive data is driven on P0_D11 to P0_D0 by the AD9363 such that the setup and hold times between DATA_CLK_x and data arriving at the baseband processor enable the baseband processor to use DATA_CLK_x to capture the data. A pulse on the ENABLE pin (or a rising edge) triggers the beginning of data transfer, and another pulse (or falling edge) signifies the end of data transfer.

The RX_FRAME and TX_FRAME signals indicate the beginning of a set (frame) of data samples. RX_FRAME can be set to occur once at the beginning of the burst (one high transition only) for each data transfer, or it can be set to have a rising edge at the beginning of each frame and repeat with a 50% duty cycle until the data transfer is complete. Similarly,

TX_FRAME accepts either format from the baseband processor.

The Tx data samples are carried in twos complement format. P1_D11 is the numerically most significant bit and P1_D0 is the least significant bit. The Rx data samples are also carried in twos complement format. P0_D11 is the numerically most significant bit and P0_D0 is the least significant bit. In both cases, the most positive sample value is 0x7FF and the most negative value is 0x800.

The I and Q data samples are carried on the same data bus in each direction. For a single RF path in each direction, the data is carried as follows: Port x: I, Q, I, Q, I, Q, ..., and so on.

For a system with two Rx/Tx channels, the I and Q samples from RF Channel 1 and Channel 2 are carried as follows: Port x: I1, Q1, I2, Q2, ..., and so on.

For a system with a 2R1T or a 1R2T configuration, the clock frequencies, sample periods, and data capture timing are the same as when configured for a 2R2T system. However, in the path with only a single channel used, the I-Q pair of the disabled channel in each data group is unused. These unused slots are ignored by the AD9363. For example, for a 2R1T system using Tx Channel 1, the Tx burst has two unused slots, as follows: Port 1: I1, Q1, X, X, ..., and so on.

The unused X slots can be filled with arbitrary data values by the baseband processor. Such values can be either constant values, or the preceding data sample values can be repeated to reduce the bus switching factor and, therefore, power consumption.

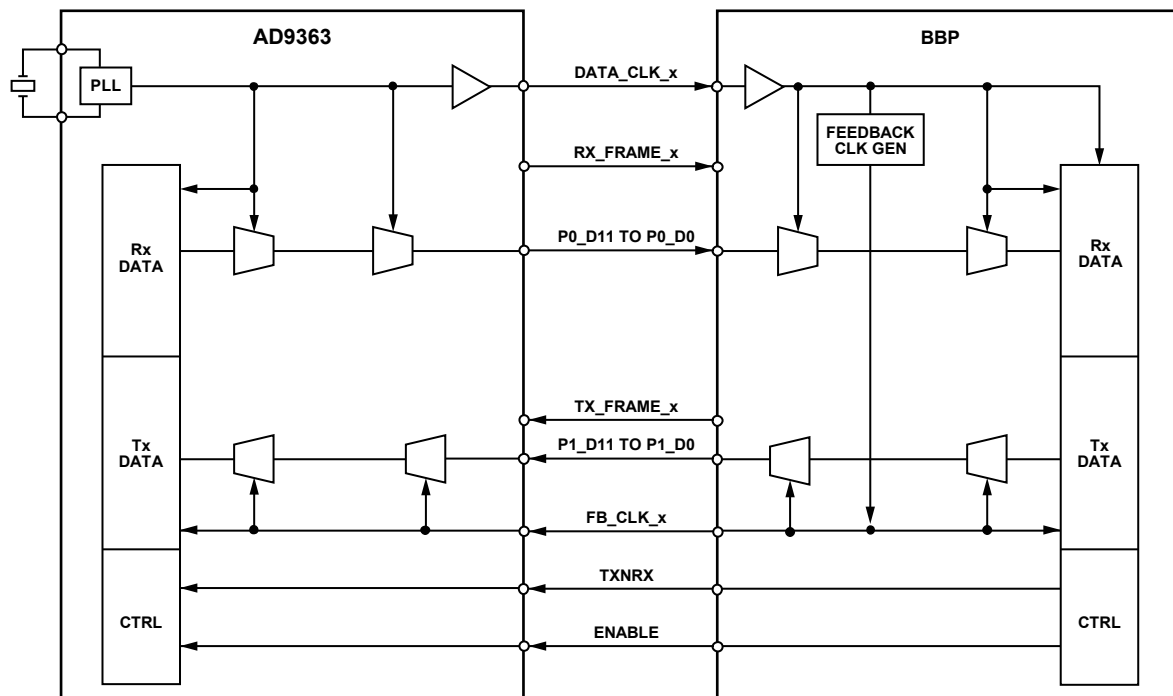


Figure 68. Dual-Port, Full Duplex Mode (Full Port)

DUAL-PORT FDD FUNCTIONAL TIMING (CMOS)

The timing diagrams in Figure 69 and Figure 70 show the relationship among the bus signals in dual-port full duplex mode. Note that because 2R1T and 1R2T systems follow the 2R2T timing diagrams, they are omitted from Figure 69 and Figure 70.

DATA BUS IDLE AND TURNAROUND PERIODS (CMOS)

The P0_D11 to P0_D0 and P1_D11 to P1_D0 bus signals are usually actively driven by the baseband processor or by the [AD9363](#). During any idle periods, the data bus values are ignored by both components. Both ports, however, must have valid logic levels even when they are unused.

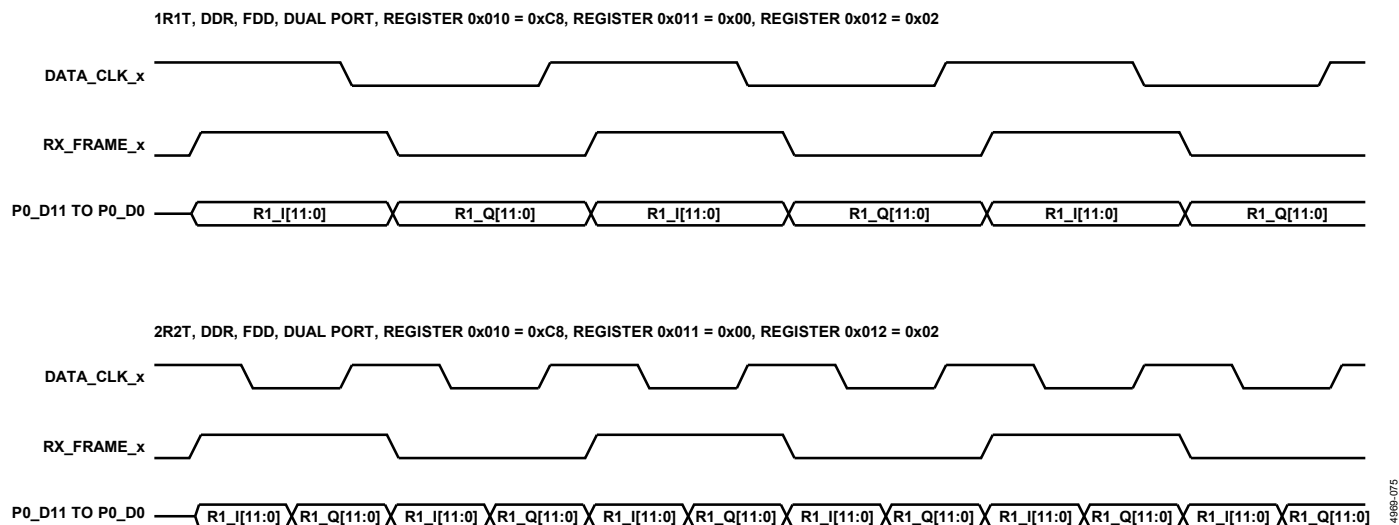


Figure 69. Receiver Datapath, Dual-Port FDD (Full Port)

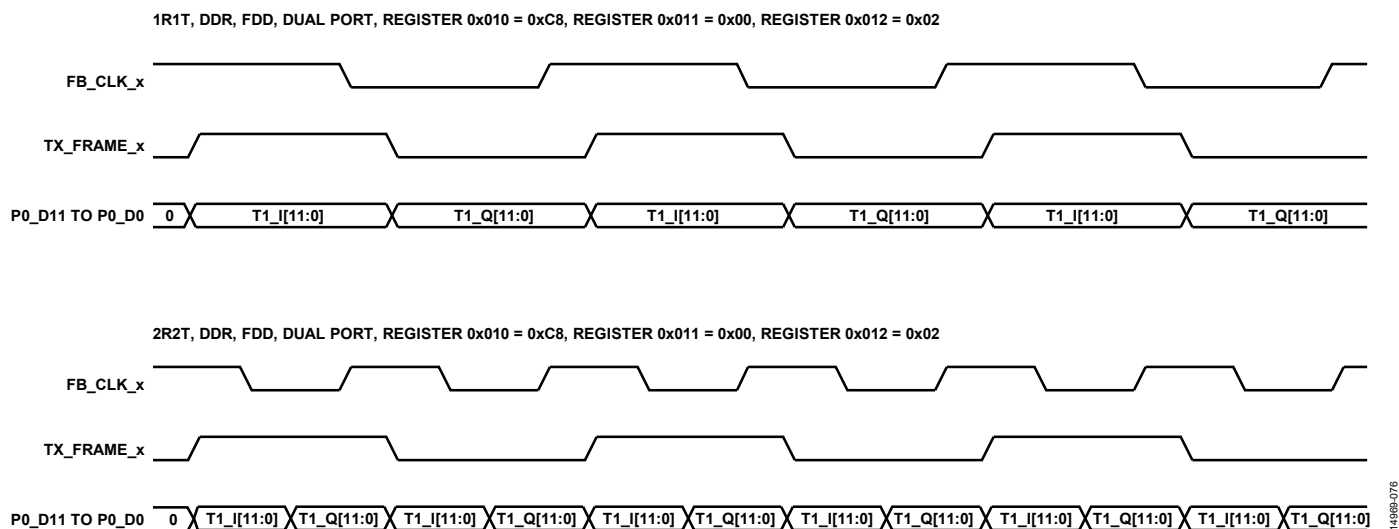


Figure 70. Transmit Datapath, Dual-Port FDD (Full Port)

DATAPATH TIMING PARAMETERS (CMOS)

The timing parameters in Table 48 provide guidance when interfacing the [AD9363](#) to a baseband processor. Figure 71 shows the relationship between the data clocks and the hardware control inputs. Figure 72 shows the relationship among all other parameters.

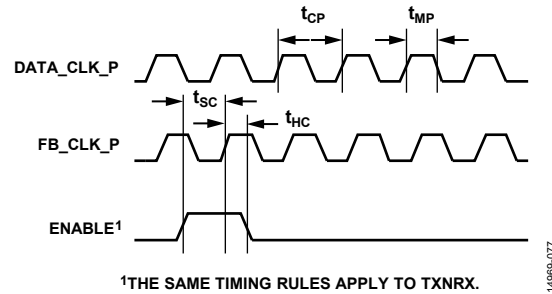


Figure 71. Data Port Timing Parameter Diagrams—Data Reference Clocks and Hardware Control Inputs (CMOS Bus Configuration)

Table 48. Datapath Timing Constraint Values

Parameter	Min	Max	Description
t_{CP}	16.276 ns		DATA_CLK_x cycle time (clock period)
t_{MP}	45% of t_{CP}	55% of t_{CP}	DATA_CLK_x and FB_CLK_x high and/or low minimum pulse width (including effects of duty cycle distortion, period jitter, cycle to cycle jitter, and half period jitter)
t_{SC}	1 ns		Control signal setup time to FB_CLK_x at the AD9363 inputs (ENABLE, TXNRX)
t_{HC}	0 ns		Control signal hold time from FB_CLK_x at the AD9363 inputs (ENABLE, TXNRX)
t_{STx}	1 ns		Tx data setup time to FB_CLK_x at the AD9363 inputs
t_{HTx}	0 ns		Tx data hold time from FB_CLK_x at the AD9363 inputs
t_{DDR_x}	0 ns	1.5 ns	Rx data delay from DATA_CLK_x to the D11 to D0 outputs; 1.8 V supply
		1.2 ns	Rx data delay from DATA_CLK_x to the D11 to D0 outputs (2.5 V supply)
t_{DDDV}	0 ns	1.0 ns	Rx data delay from DATA_CLK_x to RX_FRAME
t_{ENPW}	t_{CP}		ENABLE pulse width (edge detected by FB_CLK_x)
$t_{TXNRXPW}$	t_{CP}		TXNRX pulse width (edge detected by FB_CLK_x)
$t_{TXNRXSU}$	0 ns		TXNRX setup time to ENABLE
t_{RPRE}	$2 \times t_{CP}$		Time at which the baseband processor stops driving D11 to D0 before a receive burst, TDD
t_{RPST}	$2 \times t_{CP}$		Time at which the baseband processor starts driving D11 to D0 after a receive burst, TDD

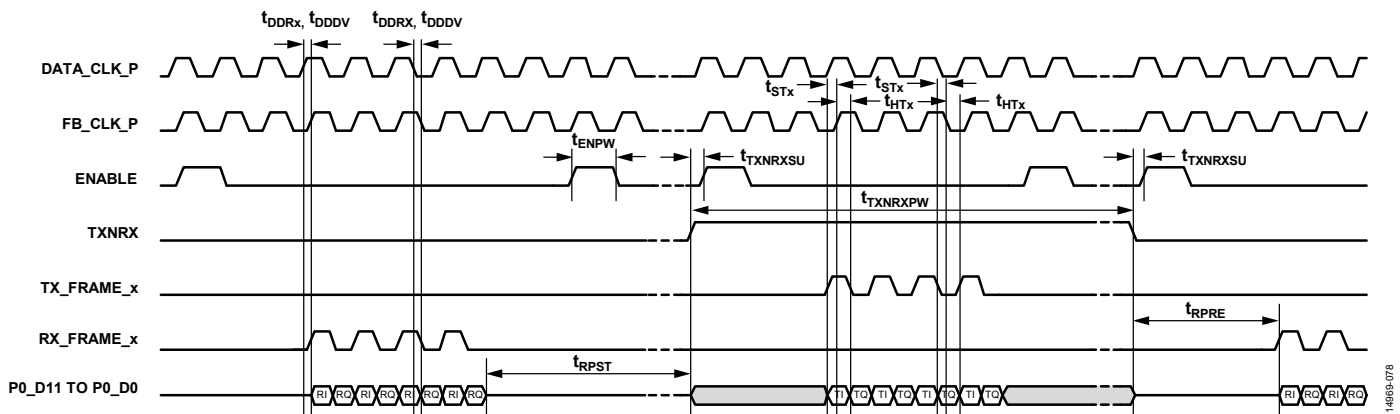


Figure 72. Data Port Timing Parameter Diagrams, CMOS Bus Configuration (Single Port, DDR, and TDD Operation)

LVDS MODE DATAPATH AND CLOCK SIGNALS

The following information describes operation of the [AD9363](#) datapath in low voltage differential signal (LVDS) mode (ANSI-644 compatible). The [AD9363](#) datapath interface uses parallel data buses (Port 0 and Port 1) to transfer data samples between the [AD9363](#) and the baseband processor. The bus transfers are controlled using simple hardware handshake signaling. In LVDS mode, both buses are used with differential LVDS signaling.

The [AD9363](#) LVDS interface facilitates connecting to custom ASICs and FPGAs that have LVDS capability. LVDS interfaces are typically used when a system requires superior switching performance in noisy environments and higher data rates than a standard CMOS interface can provide. When using LVDS mode, it is recommended to keep all trace lengths no longer than 12 inches and to keep differential traces close together and at equal lengths.

LVDS MODE DATAPATH SIGNALS

The datapath interface consists of the DATA_CLK signal and the FB_CLK signal.

DATA_CLK

DATA_CLK is a differential LVDS signal generated in the [AD9363](#) and provided to the baseband processor as a master clock for the Rx datapath. The baseband processor uses this master clock as the timing reference for the interface data transfers and for the baseband processing of the data samples.

DATA_CLK provides source synchronous timing with DDR operation for the RX_D5_x to RX_D0_x signals during receive operation. SDR is not available in LVDS mode.

The frequency of DATA_CLK depends on the system architecture, including the number of RF channels, the degree of oversampling, and the bandwidth mode. This frequency is set via SPI writes to the [AD9363](#).

DATA_CLK can be stopped by the [AD9363](#) (in response to a SPI transaction from the baseband processor) during interface idle periods to reduce power consumption. If DATA_CLK is disabled, the transition to and from the nontoggling state must obey the electrical layer requirements for clean signal transitions, and a valid level must be driven by the [AD9363](#) at all times.

FB_CLK

FB_CLK is a differential LVDS signal driven from the baseband processor and is a feedback (loop back) version of DATA_CLK. FB_CLK provides source synchronous timing with dual edge capture for Tx_D[5:0] signals during Tx bursts.

FB_CLK can be stopped by the baseband processor during interface idle periods to reduce power consumption. If so, the transitions to and from the nontoggling state must obey the electrical layer requirements for clean signal transitions, and a valid level must be driven by the baseband processor at all times.

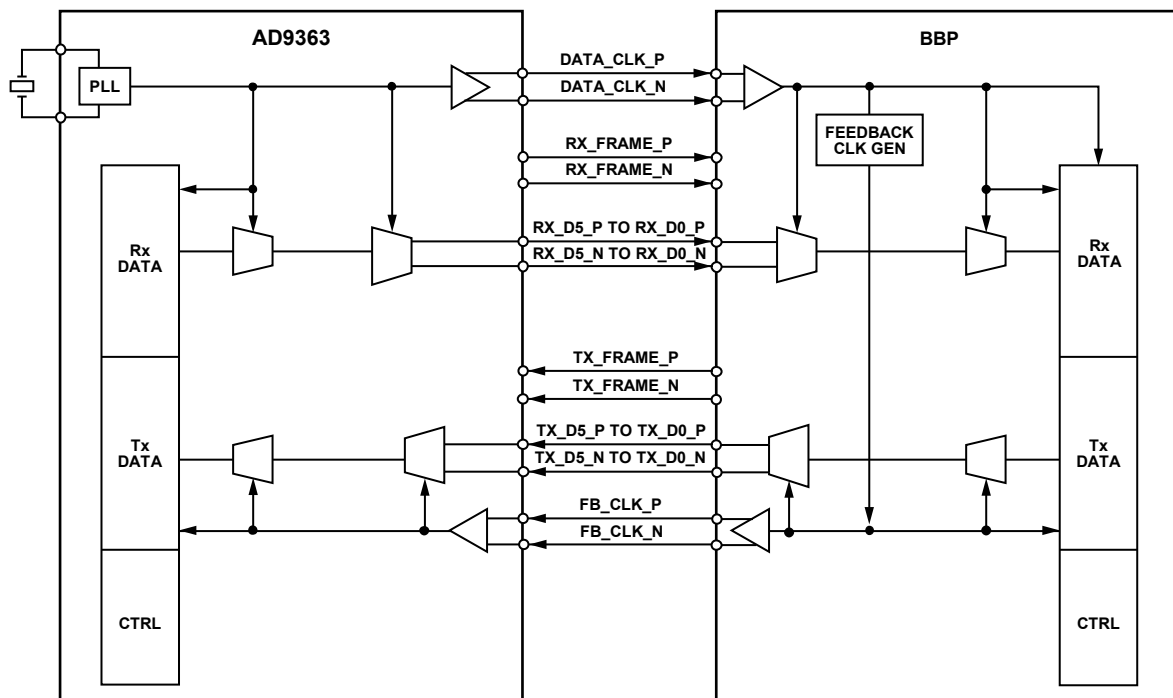


Figure 73. [AD9363](#) Datapath, LVDS Mode

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RX_FRAME

RX_FRAME is a differential LVDS signal driven from the AD9363 and provided to the baseband processor to frame the data samples provided by the AD9363. A high transition on this signal indicates the beginning of the frame. RX_FRAME can be set to be a single high transition at the beginning of a burst and can stay high throughout the burst, or it can be set to be a pulse train that has a rising edge at the beginning of each frame (50% duty cycle).

RX_D5_x to RX_D0_x

RX_D5_x to RX_D0_x is a differential LVDS data bus consisting of six differential pairs. It is driven from the AD9363 to the baseband processor with received data. Data is transmitted on this bus in pairs of data words to create a 12-bit data bus.

TX_FRAME

TX_FRAME is a differential LVDS signal driven from the baseband processor and provided to the AD9363 to frame the data samples provided by the baseband processor. A high transition indicates the beginning of the frame. TX_FRAME can accept a single high transition at the beginning of a burst that stays high throughout the burst, or a pulse train that has a rising edge at the beginning of each frame (50% duty cycle).

The AD9363 transmits null data (all zeros) until the first TX_FRAME indicates valid data. This is a useful feature when the Tx path completes a transmit operation in FDD independent mode and the datapath is not automatically flushed. In this case, the TX_FRAME pin can be held low to complete the data flushing operation. See the Enable State Machine (ENSM) Guide section for more details.

Note that both RX_FRAME and TX_FRAME are required signals for the interface to function properly.

TX_D5_x to TX_D0_x

TX_D5_x to TX_D0_x is a differential LVDS data bus consisting of six differential pairs. It is driven from the baseband processor to the AD9363 with data to be output through the transmitter. Data is transmitted on this bus in pairs of data words to create a 12-bit data bus.

ENABLE

ENABLE is driven from the baseband processor to the AD9363 to provide data transfer burst control (along with TXNRX) in TDD mode. ENABLE is asserted by the baseband processor for a minimum of a single DATA_CLK_x cycle to indicate the start of each burst. It is subsequently asserted a second time for a minimum of a single DATA_CLK_x cycle to indicate the end of each burst.

The AD9363 internally tracks the sequence of ENABLE pulses to interpret each pulse correctly as either the start or finish of each burst. The ENABLE signal can also be configured in level mode, in which the state of the signal (not pulses) determines when the enable state machine moves between states. In LVDS mode, the data ports are always active. In TDD mode, both the baseband processor and the AD9363 ignore data in the inactive direction. The start and finish latencies (between the ENABLE pulses being sampled by the AD9363 and the presence of the first and last valid data samples on the bus) vary depending on the datapath configuration. Use the RX_FRAME signal and the TX_FRAME signal to determine valid data by the baseband processor and the AD9363, respectively. Use the FB_CLK signal to sample this input.

In FDD mode, the ENABLE signal serves as the single control input to determine the state of the enable state machine. There is also an alternative FDD mode in which the ENABLE signal can be redefined as Rx on, a direct hardware control input to the enable state machine that controls the Rx function. In this mode (called FDD independent control mode), the baseband processor independently controls the Rx function, which can result in power consumption savings.

TXNRX

TXNRX is driven from the baseband processor to the AD9363 and provides data transfer burst control (along with ENABLE) when the enable state machine is in TDD mode. When ENABLE is sampled high by the AD9363 to start a burst, the level on TXNRX is also sampled to determine the data direction. In TDD mode, TXNRX sampled high indicates a transmit burst and TXNRX sampled low indicates a receive burst.

The TXNRX signal level must be maintained throughout a data transfer burst (a valid logic level). The TXNRX signal may be established any number of cycles (≥ 0) before the ENABLE start pulse is sampled, and it may be changed any number of cycles (≥ 0) after the ENABLE finish pulse is sampled. It is important to note that the TXNRX signal can only change state while the enable state machine is in the alert state because the TXNRX rising and falling edges power up and power down the corresponding synthesizers directly in TDD mode.

In normal FDD mode, the TXNRX signal is ignored but must be held at a valid logic level. There is also an alternative FDD mode in which the TXNRX signal can be redefined as Tx on, a direct hardware control input to the enable state machine that controls the Tx function. In this mode, called FDD independent control mode, the baseband processor independently controls the Tx function, which results in power consumption savings.

LVDS MAXIMUM CLOCK RATES AND SIGNAL BANDWIDTHS

The data listed in Table 49 compares the maximum data clock rates and signal bandwidths in the different allowable operating modes for the LVDS data bus configuration. Maximum RF bandwidths are listed for two cases: sampling using the minimum sample rate that avoids aliasing, and sampling using 2× over-sampling. Details of each mode are given in subsequent sections. The maximum data clock rate is increased to 245.76 MHz in LVDS mode. This clock and the 56 MHz maximum analog filter bandwidth limit RF channel signal bandwidth. Note that the data bus timing is identical for TDD and FDD modes because each path (transmit and receive) has a dedicated bus.

DUAL-PORT, FULL DUPLEX MODE (LVDS)

Dual-port, full duplex LVDS mode is enabled by writing an SPI register. In this mode, both Port 0 and Port 1 are enabled as LVDS signals and the data buses (D[11:0]) are split into separate sub-buses (RX_D5_x to RX_D0_x and TX_D5_x to TX_D0_x). Each subbus operates simultaneously, allowing full duplex of transmit and receive data between the baseband processor and the AD9363.

Transmit data (TX_D5_x to TX_D0_x), FB_CLK_x, and TX_FRAME_x are driven by the baseband processor such that the setup and hold times between FB_CLK_x, TX_D5_x to TX_D0_x, and TX_FRAME_x allow the AD9363 to use FB_CLK_x to capture TX_D5_x to TX_D0_x and TX_FRAME_x. The data samples on the TX_D5_x to TX_D0_x bus are framed by the TX_FRAME_x signal, as shown in the timing diagrams. The transmit data samples are carried in twos complement format, with the first 6-bit word in each data packet containing the MSBs and the second 6-bit word containing the LSBs. The most positive sample value is 0x7FF, with the first word being 0x1F and the second word being 0x3F, and the most negative value is 0x800, with the first word being 0x20 and the second word being 0x00. TX_D5_x is the most significant bit and TX_D0_x is the least significant bit in each word.

Receive data (RX_D5_x to RX_D0_x), DATA_CLK_x, and RX_FRAME_x are driven by the AD9363 such that the setup and hold times between DATA_CLK_x, RX_D5_x to RX_D0_x, and RX_FRAME_x allow the baseband processor to use DATA_CLK_x to capture RX_D5_x to RX_D0_x and RX_FRAME_x. The data samples on the RX_D5_x to RX_D0_x bus are framed by the RX_FRAME_x signal, as shown in the timing diagrams.

The receive data samples are carried in twos complement format, with the first 6-bit word in each data packet containing the MSBs and the second 6-bit word containing the LSBs. This means the most positive sample value is 0x7FF, with the first word being 0x1F and the second word being 0x3F, and the most negative value is 0x800, with the first word being 0x20 and the second word being 0x00. RX_D5_x is the most significant bit and D[0] as the least significant bit in each word.

Note that, as in CMOS mode, FB_CLK_x must be generated from DATA_CLK_x so that it retains the same frequency and duty cycle. There is no phase relationship requirement between the two clock signals.

As mentioned previously, the I and Q data samples are time interleaved on each data bus. For a 1R1T system, the I and Q samples are carried in a 4-way interleave as follows: I MSB, Q MSB, I LSB, Q LSB, ..., and so on.

For this case, the TX_FRAME_x and RX_FRAME_x signals are coincident with data switching. Each signal is in a high state for I MSB and Q MSB, and a low state for I LSB and Q LSB when 50% duty cycle framing is enabled. These signals then switch high again with I MSB to indicate the start of a new frame.

For a 2R2T system, the I and Q samples from RF Path 1 and RF Path 2 are carried in an 8-way interleave as follows: I1 MSB, Q1 MSB, I1 LSB, Q1 LSB, I2 MSB, Q2 MSB, I2 LSB, Q2 LSB, ..., and so on.

For this case, the TX_FRAME_x and RX_FRAME_x signals are coincident with data switching. Each is in a high state for I1 MSB, Q1 MSB, I1 LSB, Q1 LSB, and a low state for I2 MSB, Q2 MSB, I2 LSB, and Q2 LSB when 50% duty cycle framing is enabled. These signals then switch high again with I1 MSB to indicate the start of a new frame.

For a system with a 2R1T or a 1R2T configuration, the clock frequencies, bus transfer rates and sample periods, and data capture timing are the same as if configured for a 2R2T system. However, in the path with only a single channel used, the I-Q pair in each data group of the disabled channel is unused. These unused slots are ignored by the AD9363. As an example, for a 2R1T system using Tx Channel 1, the transmit burst has four unused slots: I1 MSB, Q1 MSB, I1 LSB, Q1 LSB, X, X, X, X, ..., and so on. For this case, the TX_FRAME and RX_FRAME signals are coincident with data switching and high for I1 MSB, Q1 MSB, I1 LSB, Q1 LSB, and then low for unused slots.

Table 49. Maximum LVDS Data Rates and Signal Bandwidths

Operating Mode	1R1T Configurations			1R2T/2R1T/2R2T Configurations		
	Maximum Data Rate (Combined I and Q Words)	Maximum RF Channel Signal Bandwidth		Maximum Data Rate (Combined I and Q Words)	Maximum RF Channel Signal Bandwidth (MHz) Per Channel	
		Using Minimum Sample Frequency	Using 2× Oversampling		Using Minimum Sample Frequency	Using 2× Oversampling
Dual-Port, Full Duplex	61.44	56 ¹	56 ¹	61.44	56 ¹	30.72

¹ Limited by the analog filter bandwidth.

These signals then switch high again with I1 MSB to indicate the start of a new frame. The unused X slots can be filled with arbitrary data values by the baseband processor. Such values can be either constant values, or the preceding data sample values can be repeated to reduce the bus switching factor and, therefore, power consumption.

DATAPATH FUNCTIONAL TIMING (LVDS)

The timing diagrams in Figure 74 and Figure 75 show the relationship among the bus signals in dual-port FDD LVDS mode. The differential data in the timing diagrams include solid and dashed lines to show the differential nature of the data lines. Solid lines for the positive leg match solid lines for the negative leg of the differential pair, and dashed lines for the positive leg pair with dashed lines for the negative leg. Note that because

2R1T and 1R2T systems follow the 2R2T timing diagrams, they are omitted from Figure 74 and Figure 75. The following bits are not supported in LVDS mode:

- Swap ports. In LVDS mode, Port 0 is Tx and Port 1 is Rx. This configuration cannot be changed.
- Single port mode. Both ports are enabled in LVDS mode.
- FDD full port; not supported in LVDS mode.
- FDD alternate word order; not supported in LVDS mode.
- FDD swap bits; not supported in LVDS mode.

DATAPATH TIMING PARAMETERS (LVDS)

Table 50 lists the timing constraints for the LVDS data buses.

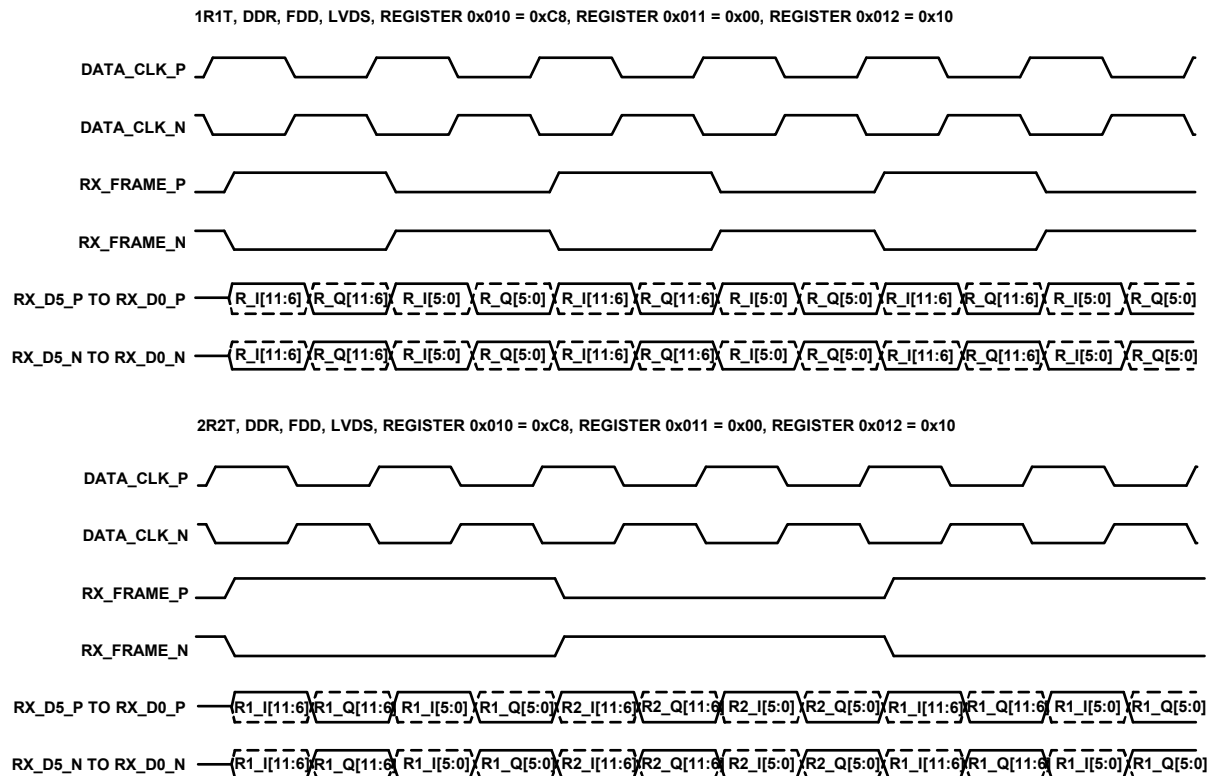


Table 50. Datapath Timing Constraint Values, LVDS Mode

Parameter	Min	Max	Unit	Description
t_{CP}	4.069		ns	DATA_CLK_x cycle time (clock period)
t_{MP}	45	55	% of t_{CP}	DATA_CLK_x and FB_CLK_x high and/or low minimum pulse width (including effects of duty cycle distortion, period jitter, cycle to cycle jitter, and half period jitter)
t_{STx}	1		ns	TX_D5_x to TX_D0_x, TX_FRAME_x setup time to FB_CLK_x falling edge at the AD9363 inputs
t_{HTx}	0		ns	TX_D5_x to TX_D0_x, TX_FRAME_x hold time from FB_CLK_x falling edge at the AD9363 inputs
t_{DDRx}	0.25	1.25	ns	Delay from DATA_CLK_x to RX_D5_x to RX_D0_x outputs
t_{DDV}	0.25	1.25	ns	Delay from DATA_CLK_x to RX_FRAME_x

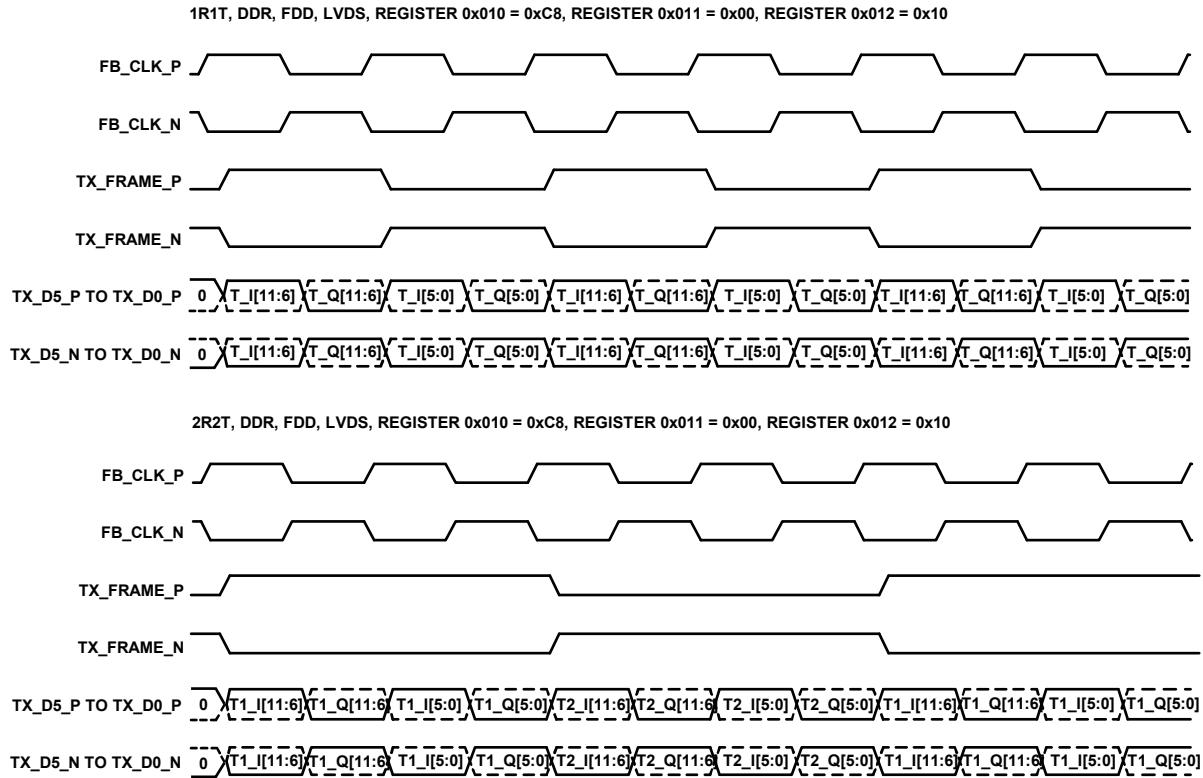
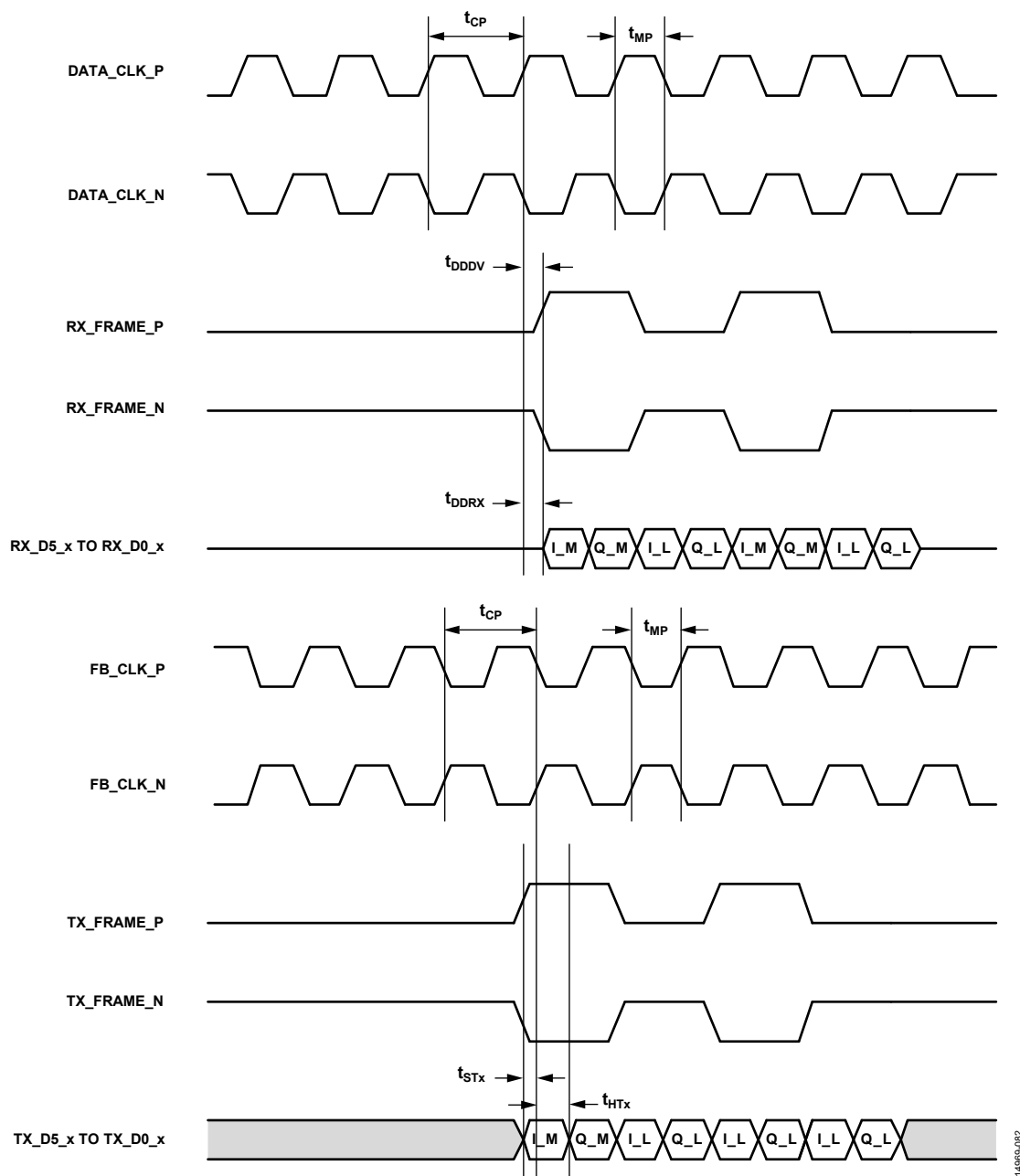


Figure 75. Transmit Datapath, LVDS

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Figure 76. Data Port Timing Parameter Diagrams—LVDS Bus Configuration

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI bus provides the mechanism for all digital control of the [AD9363](#). Each SPI register is 8 bits wide, and each register contains control bits, status monitors, or other settings that control all functions of the device. The following sections explain the specifics of this interface.

SPI Functional Layer

Configure the SPI bus by setting the bit values in the SPI configuration register. This register is symmetrical; that is, Bit D6 is equivalent to Bit D1, and Bit D5 is equivalent to Bit D2 (Bit D4 and Bit D3 are unused). The device powers up in its default mode (MSB first addressing), but can accept an LSB first write to the SPI configuration register because of this symmetry. The symmetrical bits are ORed together; therefore, setting one bit sets both bits in the pair. The bit order is MSB first when Bit D5 and Bit D2 are left clear, while the bit order is swapped to LSB first when these bits are set. After the bits are properly configured, all subsequent register writes must follow the selected format.

The bus is configured as a 4-wire interface by default. If Bit D6 and Bit D1 are set, the SPI bus is configured as a 3-wire interface. Bit D7 and Bit D0 asynchronously reset all registers to their default values when set, and these bits must be cleared before other registers can be changed.

Each SPI bus signal is described in the following sections.

SPI_ENB

SPI_ENB is the bus enable signal driven from the baseband processor to the [AD9363](#). SPI_ENB is driven low before the first SPI_CLK rising edge and is normally driven high again after the last SPI_CLK falling edge. The [AD9363](#) ignores the clock and data signals while SPI_ENB is high. If the [AD9363](#) is the only device on the SPI bus, SPI_ENB can be tied low.

The SPI_DO and SPI_DI pins transition to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until SPI_ENB is reactivated low.

SPI_CLK

SPI_CLK is the interface reference clock driven by the baseband processor to the [AD9363](#). It is only active while SPI_ENB is low. The maximum SPI_CLK frequency is 50 MHz.

SPI_DI, SPI_DO, and SPI_DIO

When configured as a 4-wire bus, the SPI uses two data signals: SPI_DI and SPI_DO. SPI_DI is the data input line driven from the baseband processor to the [AD9363](#) and SPI_DO is the data output from the [AD9363](#) to the baseband processor in this configuration. When configured as a 3-wire bus, SPI_DI is used as a bidirectional data signal that both receives and transmits serial data. In 3-wire configuration, this signal is referred to as SPI_DIO to distinguish between the two configurations.

The data signals are launched on the rising edge of SPI_CLK and sampled on the falling edge of SPI_CLK by both the baseband processor and the [AD9363](#). SPI_DI (or SPI_DIO) carries the control field from baseband processor to the [AD9363](#) during all transactions and the write data fields during a write transaction. SPI_DO (or SPI_DIO) carries the returning read data fields from the [AD9363](#) to the baseband processor during a read transaction.

The [AD9363](#) does not provide any weak pull-ups or pull-downs on these pins. When SPI_DO is inactive, it is floated in a high impedance state. If a valid logic state on SPI_DO is required at all times, add an external weak pull-up/pull-down on the PCB.

SPI Data Transfer Protocol

The [AD9363](#) SPI is a flexible, synchronous serial communications bus allowing seamless interfacing to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The control field width for the [AD9363](#) is limited to 16-bit only, and multibyte I/O operation is allowed. The [AD9363](#) cannot be used to control other devices on the bus—it only operates as a slave.

There are two phases to a communication cycle. Phase 1 is the control cycle, which is the writing of a control word into the [AD9363](#). The control word provides the [AD9363](#) serial port controller with information regarding the data field transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 control field defines whether the upcoming data transfer is read or write. It also defines the register address being accessed.

Phase 1 Instruction Format

The 16-bit control field contains the following information:

MSB	D14	D13	D12	D11	D10	D9:D0
W/Rb	NB2	NB1	NB0	X	X	A[9:0]

- W/Rb—Bit 15 of the instruction word determines whether a read or write data transfer occurs after the instruction byte write. Logic high indicates a write operation; logic zero indicates a read operation.
- NB2, NB1, NB0—Bits[14:12] of the instruction word specify the number of bytes transferred during Phase 2 of the I/O operation. Table 51 details the number of bytes transferred during Phase 2 for each NB[2:0] combination.

Table 51. Phase 2 Byte Transfer

NB2, NB1, NB0	Description
000	Transfer 1 byte
001	Transfer 2 bytes
010	Transfer 3 bytes
011	Transfer 4 bytes
100	Transfer 5 bytes
101	Transfer 6 bytes
110	Transfer 7 bytes
111	Transfer 8 bytes

- [D11:D10]—Bits[11:10] of the instruction word are unused.
- [D9:D0]—Bits[9:0] specify the starting byte address for the data transfer during Phase 2 of the I/O operation.

All byte addresses, both starting and internally generated addresses, are assumed to be valid. That is, if an invalid address (undefined register) is accessed, the I/O operation continues as if the address space are valid. For write operations, the written bits are discarded, and read operations result in Logic 0s at the output.

Single-Byte Data Transfer

When NB2, NB1, and NB0 are all zero, a single-byte data transfer is selected. In this scenario, the next eight bits to follow the address bits contain the data being written to or read from the [AD9363](#) register. After the final bit is transferred, the data signals return to their idle states and the SPI_ENB signal goes high to end the communication session.

Multibyte Data Transfer

When NB2, NB1, and NB0 are all nonzero, a multibyte data transfer is selected. The format and ordering of the data to be transferred in this mode depend on whether the device is configured for LSB first or MSB first data transfer.

For multibyte data transfers in LSB mode, the user writes an instruction byte that includes the register address of the least significant byte. The SPI internal byte address generator increments for each byte required in the multibyte communication cycle. Data is written in least to most significant order as the byte addresses are also generated in least to most significant order.

For multibyte data transfers in MSB mode, the user writes an instruction word that includes the register address of the most significant byte. The serial port internal byte address generator decrements for each byte required by the multibyte communication cycle. Data is written in most to least significant order because the byte addresses are generated in most to least significant order.

Example: MSB First, Multibyte Transfer

To complete a 4-byte write, starting at Register 0x02A in MSB first format, apply an instruction word of 1_011_000000101010 (binary). This instruction directs the [AD9363](#) SPI controller to perform a write transfer of four bytes with the starting byte address of 0x02A. After the first data byte is written, the internal byte address generation logic decrements to 0x029, which is the destination of the second byte. After the second byte is written, the internal byte address generation logic decrements to 0x028, which is the destination of the third byte. After the third byte is written, the internal byte address generation logic decrements to 0x027, which is the destination of the last byte. After the fourth byte is written, the I/O communication cycle is complete and the next 16 falling clock cycles on SPI_CLK are utilized to clock in the next instruction word. If no further communication is needed, the data signals return to their idle states, SPI_CLK goes low, and the SPI_ENB signal goes high to end the communication session.

Example: LSB First, Multibyte Transfer

To complete a 4-byte write, starting at Register 0x02A in LSB first format, apply an instruction word of 010101000000_110_1 (binary). This instruction directs the [AD9363](#) SPI controller to perform a write transfer of four bytes with the starting byte address of 0x02A. After the first data byte is written, the internal byte address generation logic increments to 0x02B, which is the destination of the second byte. After the second byte is written, the internal byte address generation logic increments to 0x02C, which is the destination of the third byte.

After the third byte is written, the internal byte address generation logic increments to 0x02D, which is the destination of the last byte. After the fourth byte is written, the I/O communication cycle is complete and the next 16 falling clock cycles on SPI_CLK are used to clock in the next instruction word. If no further communication is required, the data signals return to their idle states, SPI_CLK goes low, and the SPI_ENB signal goes high to end the communication session.

Timing Diagrams

The following diagrams in Figure 77 and Figure 78 detail the SPI bus waveforms for a single-register write operation and a single-register read operation, respectively. In the first figure, the value of 0x55 is written to Register 0x15A. In the second value, Register 0x15A is read and the value returned by the device is 0x55.

When the same operations are performed with a 3-wire bus, the SPI_DO line in Figure 77 is eliminated, and the SPI_DI and SPI_DO lines in Figure 78 are combined on the SPI_DI line.

Table 52 lists the timing specifications for the SPI bus. The relationship between these parameters is shown in Figure 79. This diagram shows a 3-wire SPI bus timing diagram with these parameters marked. Note that this is a single read operation; therefore, the bus ready parameter after the data is driven from the AD9363 is not shown in the diagram.

Table 52. SPI Bus Timing Constraint Values

Parameter	Min	Max	Description
t_{CP}	20 ns		SPI_CLK cycle time (clock period)
t_{MP}	9 ns		SPI_CLK pulse width
t_{SC}	1 ns		SPI_ENB setup time to first SPI_CLK rising edge
t_{HC}	0 ns		Last SPI_CLK falling edge to SPI_ENB hold
t_S	2 ns		SPI_DI data input setup time to SPI_CLK
t_H	1 ns		SPI_DI data input hold time to SPI_CLK
t_{CO}	3 ns	8 ns	SPI_CLK rising edge to output data delay (3-wire or 4-wire mode)
t_{HZM}	t_H	$t_{CO}(\text{max})$	Bus turnaround time after baseband processor drives the last address bit
t_{HZS}	0 ns	$t_{CO}(\text{max})$	Bus turnaround time after the AD9363 drives the last data bit

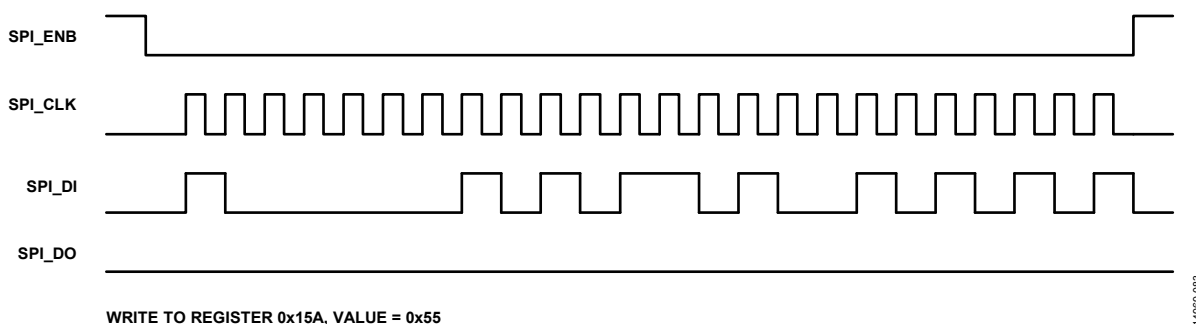


Figure 77. Nominal Timing Diagram, SPI Write

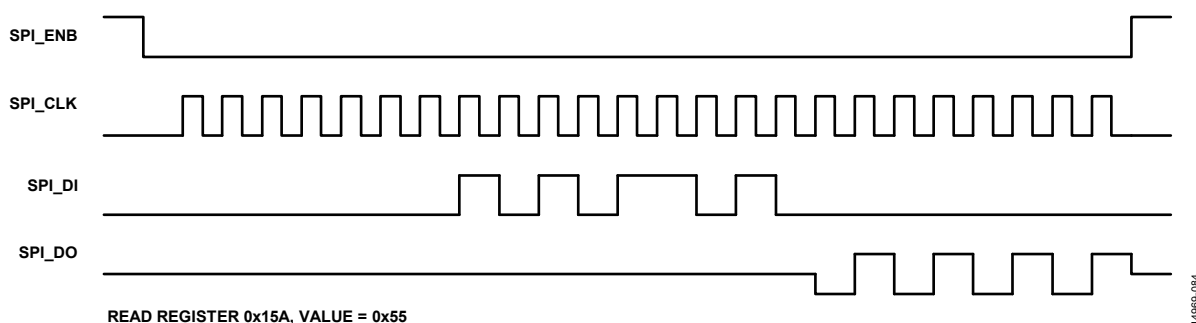


Figure 78. Nominal Timing Diagram, SPI Read

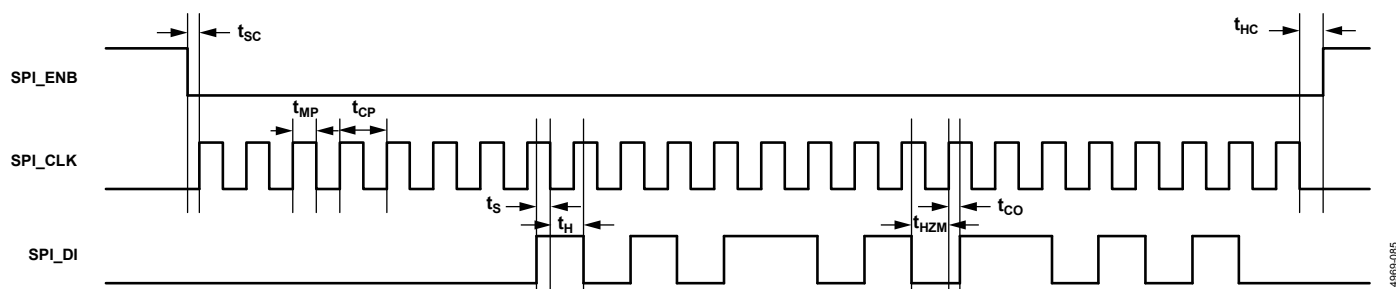


Figure 79. 3-Wire SPI Timing with Parameter Labels, SPI Read

ADDITIONAL INTERFACE SIGNALS

CLOCK_OUT

CLOCK_OUT is an output signal designed to be used as a master clock source for the baseband processor. This output can be programmed to be a buffered version of the input clock or a multiple of the Rx datapath ADC clock. Note that the clock frequency must always be less than 61.44 MHz.

CTRL_IN3 to CTRL_IN0

The CTRL_INx pins are four programmable input signals used for real time control Rx gain settings as described in the Gain Control section.

CTRL_IN2 can also be used to provide hardware control in the receiver AGC hybrid mode. In this mode, gain changes occur when the baseband processor pulls the CTRL_IN2 pin high. This allows the baseband processor to directly control the time that the gain setting changes.

CTRL_OUT7 to CTRL_OUT0

The CTRL_OUTx pins are eight programmable digital output signals used for real time processing. These outputs include internally generated functions and status bits such as PLL lock, calibration complete, and AGC functions.

EN_AGC

EN_AGC is an input signal that provides real time control of when the AGC is active. When pulled high, the EN_AGC pin forces the AGC to unlock so that adjustments to the gain setting can be made. If the EN_AGC pin is not used, then the gain lock delay bit must be set high.

GPO3 to GPO0

The GPO_x pins are digital outputs that can be configured to monitor the status of the ENSM or serve as general-purpose logic outputs. These pins are especially useful for biasing a connected power amplifier or controlling front-end switches used in TDD systems. See the General-Purpose Output (GPO) Control section for more details.

RESET

RESET is an input signal allowing asynchronous hardware reset of the [AD9363](#). A logic low applied to this pin resets the device (all SPI registers are reset to default settings and the device is placed in sleep mode). Hold the RESET line low for at least 1 μ s, and do not program the device for at least 1 μ s after the RESET line is taken back high.

POWER SUPPLY AND LAYOUT GUIDE

POWER SUPPLY AND LAYOUT GUIDE OVERVIEW

Due to the increased complexity of the [AD9363](#) and the high pin count, PCB layout is important to get the best performance. This section provides a checklist of issues to look for and how to work on them. The goal of this section is help achieve the best performance from the [AD9363](#) while reducing board layout effort. This section assumes that the reader is a RF engineer who understands RF PCB layout and has an understanding of RF transmission lines. This section discusses the following issues and provides guidelines for system designers to obtain the best performance from the [AD9363](#):

- PCB material and stack up selection
- RF transmission line layout
- Fan out and trace space layout guidelines
- Special components placement and routing guidelines
- Power management and system noise considerations
- Power distribution to all the different power domains

PCB MATERIAL AND STACK UP SELECTION

Figure 80 shows the stack up used for the [AD9363](#) customer evaluation boards. The top and the bottom layers are Rogers 4003 with an 8 mil dielectric. The remaining layers are FR4-370 HR.

The board design uses the Rogers laminate for the top and the bottom layers for its low loss tangent at high frequencies.

The ground planes under the Rogers laminate (Layer 2 and Layer 9) are the reference planes for the transmission lines routed on the outer surfaces. These layers are solid copper plane without any splits under the RF traces. Layer 2 and Layer 9 are crucial to maintaining the RF signal integrity and, therefore, the [AD9363](#) performance.

Layer 3 and Layer 8 contain the 1.3 V analog supply, the 3.3 V GPO_x supply, and the 1.8 V VDD_INTERFACE supply. To keep the RF section of the [AD9363](#) isolated from the fast transients of the digital section, the digital lines from the [AD9363](#) are on inner Layer 5 and Layer 6. The RF traces on the outer layers must be controlled impedance to obtain the best performance from the [AD9363](#).

All inner layers in this board use 1 ounce copper. The outer layers use 1.5 ounce copper so that the RF traces are less prone to peeling. Ground planes on this board are full copper floods with no splits except for vias and through-hole components. The ground planes must route entirely to the edge of the PCB under the SMAs to maintain signal launch integrity.

Power planes, however, can be pulled back from the board edge to decrease the risk of shorting from the board edge.

OVERALL THICKNESS =		0.062	±10%	ROGERS 4003 (DK = 3.38)			
		370 HR (DK = 4.1)					
		<u>DIELECTRIC</u>	<u>COPPER</u>	<u>TARGET IMPEDANCE</u>	<u>LINE/SPACE</u>	<u>CALC</u>	
R4003	1	0.008	SIGNAL	1.5	50Ω ± 10% 100 DIFFERENTIAL ± 10%	0.0155 0.008/0.006	50.1 100.0
	2	0.003	GND	1			
NEW LAYER	3	0.003	PWR	1	OZ		
	4	0.0046	GND	1	OZ		
370 HR	5	0.008	SIGNAL	1	50Ω ± 10% 100 DIFFERENTIAL ± 10%	0.0049 0.0038/0.0062	50.0 100.2
	6	0.008	SIGNAL	1			
NEW LAYER	7	0.0046	GND	1	OZ		
	8	0.003	PWR	1	OZ		
R4003	9	0.003	GND	1	OZ		
	10	0.008	SIGNAL	1.5	50Ω ± 10% 100 DIFFERENTIAL ± 10%	0.0155 0.008/0.006	50.1 100.0
		0.0606	FINAL THICKNESS (AFTER PLATING)				

Figure 80. [AD9363](#) Customer Evaluation Board Stack Up

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RF TRANSMISSION LINE LAYOUT

The [AD9363](#) evaluation boards use micro strip lines for all RF traces. The critical Rx and Tx lines route on the top side of the board. It is not recommended to use vias to route RF traces. The differential lines from the balun secondary to the Rx and Tx balls must be as short as possible.

Ensure that the length of the single-ended transmission line is short to minimize the effects of parasitic coupling. Because the receiver front end is dc biased internally, the differential side of the balun is ac-coupled. The system designer can optimize the RF performance with a proper selection of the balun and the ac coupling capacitors. The Tx monitor traces, external LO traces, and the external clock traces may require matching components as well, to ensure best performance.

All the previous RF signals mentioned must have a solid ground reference under them. Do not run any of the critical traces over a section of the reference plane that is discontinuous. The ground flood on the reference layer must extend all the way to the edge of the board. This ensures good signal integrity for the SMA launch.

See the RF Port Interface section for more information on the RF matching issues associated with the [AD9363](#).

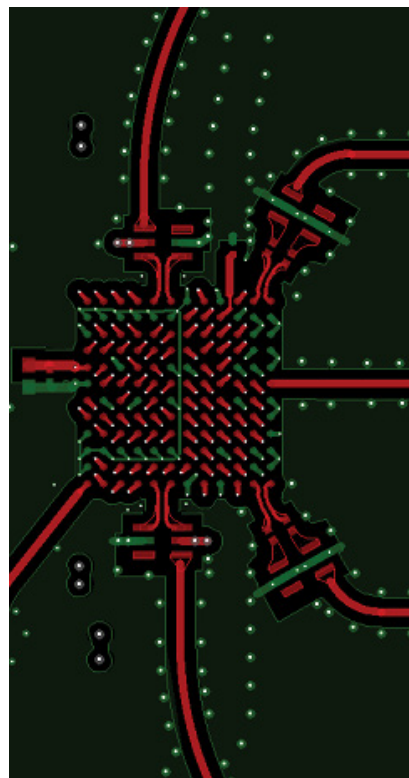


Figure 81. RF Match Structures on Rx and Tx on FM Comms 2 Board

FAN OUT AND TRACE SPACE GUIDELINES

The AD9363 is in a 10 mm × 10 mm, 144-pin BGA package. The pitch between the balls is 0.8 mm. This small pitch makes it impractical to route all signals on a single layer. RF balls are on the outer edges of the AD9363 package. This helps in routing the critical signals without a fan out via. The digital signals are buried in the inner layers of the board. The digital balls corresponding to the Rx data port are buried on one signal layer and those corresponding to the Tx data port are buried on a different signal layer. The AD9363 evaluation boards use a 10-mil pin escape trace from the BGA land pad and drop the

digital signals on the inner layers by using a 6 mil via with a 12 mil keep out. The spacing between the BGA lands to the pin escape via is 22 mils. After the signal is on the inner layers, a 4.9 mil trace (50 Ω) connects the signal to the FPGA. The recommended BGA land size is 14 mils.

Only one signal trace is routed between adjacent BGA land pads and between pin escape vias on the inner layers. Routing two traces between adjacent BGA land pads and pin escape vias by reducing the BGA land pad width and trace pad space design rules reduces overall board manufacturing and assembly reliability. Figure 82 shows the fan out scheme evaluation board.

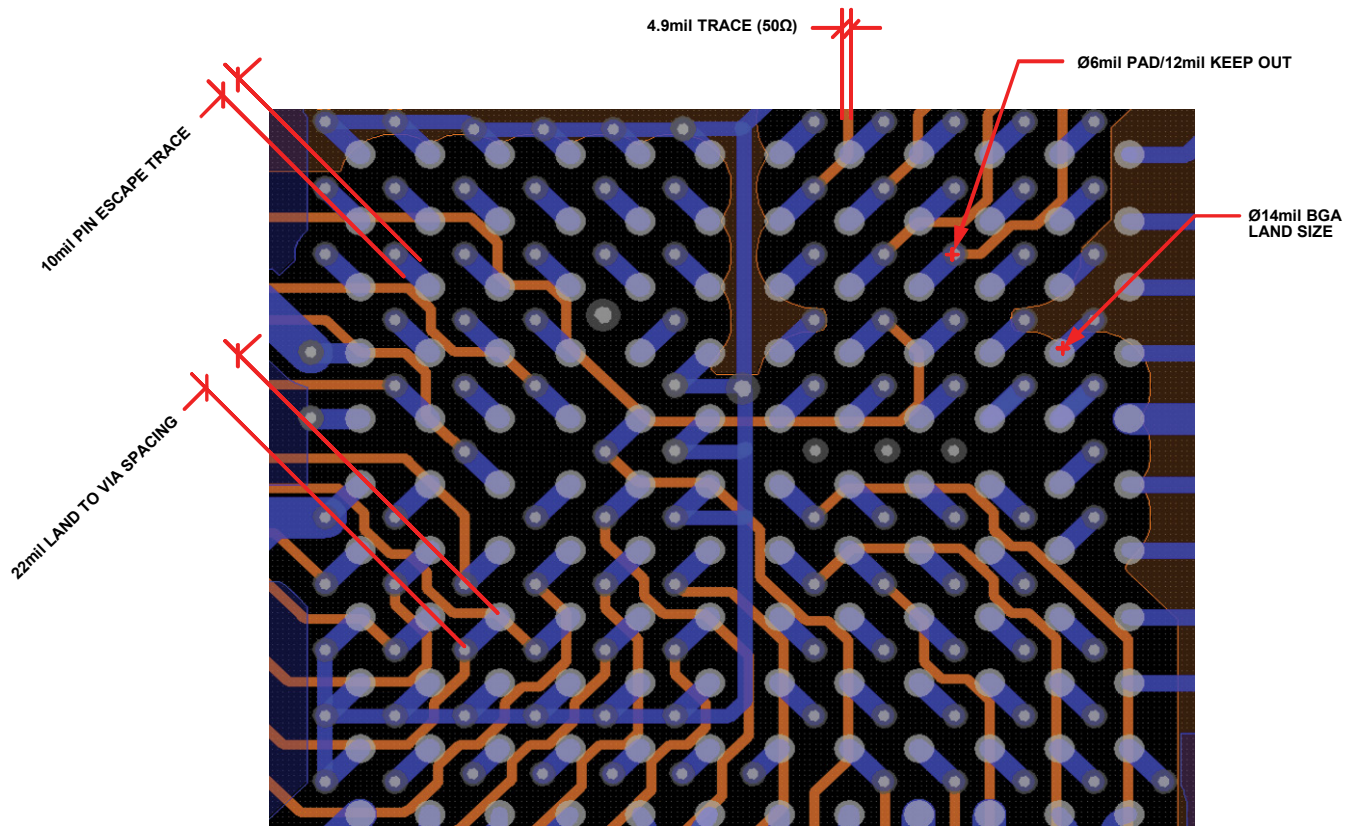


Figure 82. 0.8 mm Pitch BGA Via Fan Out

COMPONENT PLACEMENT AND ROUTING GUIDELINES

The [AD9363](#) transceiver requires few external components to function, but there are certain external components that are critical to the proper functioning of the part. This section provides a checklist for properly placing and routing some of those critical signals and components.

- The receiver/transmitter baluns and the matching circuits affect the overall RF performance of the [AD9363](#). Therefore, be certain to optimize the component selection and placement. See the RF Port Interface section for more information.
- Pull the TEST/ENABLE ball (C4) to ground for proper functioning. When this ball is not grounded, the [AD9363](#) does not function.
- Pull the RESET ball (Pin K5) high with a 10 k Ω resistor to VDD_INTERFACE (Pin H12) for proper functioning. To reset the device, pull the RESET ball low.
- Connect a 14.3 k Ω resistor to the RBIAS ball (Pin L4). This resistor must have a 1% tolerance.
- If using an external clock, connect the clock to the XTALN ball (Pin M12) via an ac coupling capacitor. Ensure that the external clock peak-to-peak amplitude does not exceed 1.3 V.
- The Rx and the Tx external LO balls on the [AD9363](#) are internally dc biased. If these balls are used, connect a series coupling capacitor to the ball. If the Rx and Tx external LO balls are not used, connect them to ground.
- 1 Ω resistor in series to the bypass capacitor on the TX_VCO_LDO_OUT (Pin B11) and RX_VCO_LDO_OUT (Pin G2) is required. A capacitor that has a 1 Ω ESR can replace this series combination of a resistor and capacitor.
- The VDDA1P1_TX_VCO (Pin A11) must be shorted to the TX_VCO_LDO_OUT (Pin B11) ball only.
- The VDDA1P1_RX_VCO (Pin G3) must be shorted to RX_VCO_LDO_OUT (Pin G2) ball only.

- The Tx monitor balls also require a matching network. If the Tx monitor is not used, then connect Ball A5 and Ball M5 to ground. For more information, see the Tx Power Monitor section.
- There must be at least a 0.1 μ F bypass capacitor near each power supply ball.
- Install 10 μ F bypass capacitor on the VDDA1P3_RX_SYNTH (Pin J3) and VDDA1P3_TX_SYNTH (Pin K3) ball.
- Install a 10 μ F capacitor near the Tx balun dc feed.

POWER MANAGEMENT AND SYSTEM NOISE CONSIDERATIONS

The [AD9363](#) has three different power domains on the chip. 1.3 V is the main power domain that powers the major part of the chip. The VDD_INTERFACE supply is a separate power domain. The input voltage on the VDD_INTERFACE can range from 1.2 V to 2.5 V. This voltage controls the voltage levels of the digital interface of the [AD9363](#). To operate the digital interface in LVDS mode, supply 1.8 V or 2.5 V to the VDD_INTERFACE supply. The input voltage to VDD_GPO ball can range from 1.3 V to 3.3 V. The VDD_GPO must rise as fast or faster than the 1.3 V supply domain.

All the different power domains have different power supply noise rejection characteristics (PSRR). There are certain supplies on the part that are more sensitive to noise than others are. These supplies must be decoupled properly to achieve the best performance from the [AD9363](#). The noise considerations for the 1.3 V analog supply are vital whereas the noise considerations for the VDD_INTERFACE supply and the VDD_GPO are less critical.

Table 53 lists the Rx error vector magnitude (EVM) and Tx EVM degradation when a ripple voltage is injected on the 1.3 V analog supply. In this experiment, the LO is set to 700 MHz and the reference clock is at 19.2 MHz with the RF PLL doubled. The Tx attenuation setting is set to 10 dB. In this experiment, ripple voltage is added on the 1.3 V dc supply with the help of a bias tee. This combination powers all the 1.3 V analog supply domains. The lower frequency ripple is more detrimental to the device performance. For this reason, the low frequency noise must be reduced on the platform that integrates the [AD9363](#).

Table 53. 1.3 V Analog Supply Noise Sensitivities

Noise Frequency	Ripple Voltage	Rx EVM (10 MHz LTE)	Tx EVM (10 MHz LTE)
Not applicable	0 mV	−37.782 dB	−37.462 dB
40 kHz	16 mV	−24.886 dB	−28.619 dB
300 kHz	22 mV	−35.254 dB	−35.517 dB
500 kHz	52 mV	−36.254 dB	−35.517 dB
1 MHz	>50 mV	−37.501 dB	−36.95 dB
5 MHz	>50 mV	−37.749 dB	−36.927 dB

Using an LDO to Power Up the 1.3 V Analog Supply on the AD9363

The evaluation boards power the 1.3 V analog supply of the AD9363 with an LDO. The selection of the LDO is important not only from a power management perspective but also from a performance perspective. An LDO with poor PSRR degrades the RF performance of the device. An LDO with poor noise characteristics introduces noise in the receiver spectrum as well as in the transmitter spectrum.

Figure 83 shows the close in noise spectrum of the ADP1755 when used to power the 1.3 V analog supply. This spectrum shows a clean and a low noise floor that is beneficial to achieving the best performance from the AD9363. Any spurs or noise from the power supply within a 1 MHz span appears on the local oscillator frequency and manifests itself as transmitter phase noise. Similarly, it also affects the receiver down conversion performance.

Using a Switching Regulator to Power Up the 1.3 V Analog Supply on the AD9363

Using a switching regulator to power the AD9363 provides efficiency that is easily transferrable to an overall cost reduction. A switching regulator can power the 1.3 V analog power supply of the AD9363. However, choosing the right switching regulator is crucial to getting the best performance from the AD9363. During the selection process, the following characteristics of the switching regulator are important: noise floor, output noise spectrum, switching frequency, slew rate, and maximum output capacitance.

Noise Floor

It is beneficial to have a switching regulator with a low noise floor. The noise floor characteristics of the switching regulator change with the load. The noise floor is typically worse when the regulator is not loaded but turned on. 1/f noise affects the low frequency performance of the regulator.

At higher frequencies, the switching action of the regulator introduces noise at the switching frequencies and its harmonics; in addition, rapid transitions of the switching frequency may excite the parasitic capacitance of the regulation circuit and create high frequency oscillations, in this respect layout and passive component selection are also important to minimize the noise generated by the switching regulator.

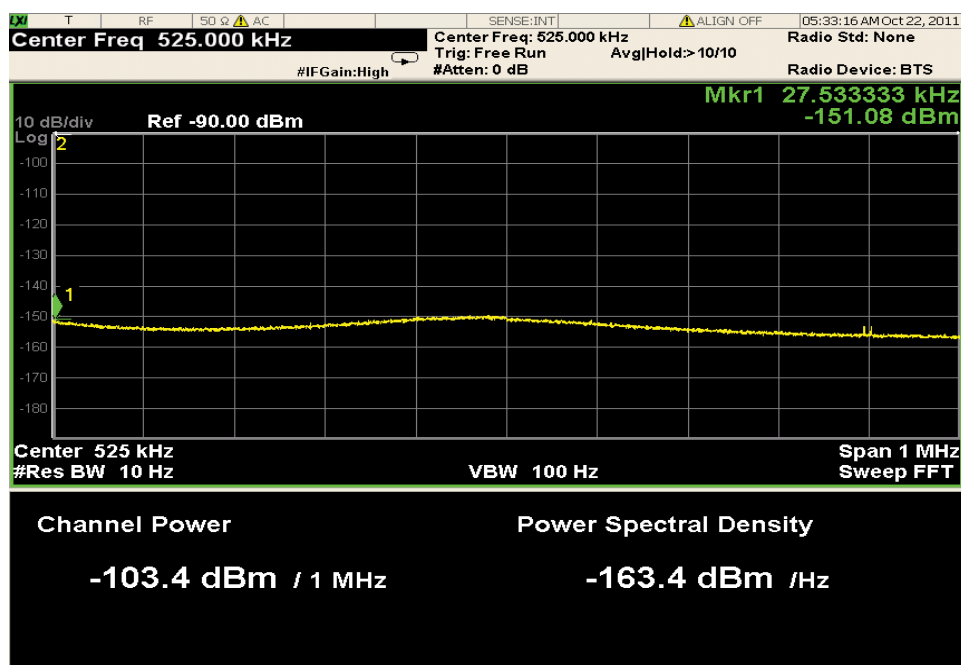


Figure 83. Noise Floor of the ADP1755 Powering the 1.3 V Analog Plane

Output Noise Spectrum

Figure 84 shows the output spectrum of the [ADP5040](#) switching regulator up to 1 MHz. This span is important, as the [AD9363](#) is more sensitive to low frequency noise than it is to high frequency noise. Switcher noise greater than 1 MHz is also important. Some switching regulators can have large multiples of the switching frequency with many sidebands. These spurs generated by the switcher can couple into other power supplies or RF balls.

Switching Frequency

The switching frequency of the switching regulator is also an important characteristic to consider. Therefore, choose a regulator with a switching frequency greater than 1 MHz. Since the switching frequency of [ADP5040](#) is 3 MHz, it is relatively quiet ranging from 100 Hz to 500 kHz.

Slew Rate

The slew rate of the regulator is important to control the rise time and fall times of the switching edges. A switcher regulator with a high slew rate is preferred as this reduces low frequency sidebands that can fall below 1 MHz.

Maximum Output Capacitance

In switching regulators with limitation for the maximum allowable output capacitance, it is important to consider the effects over the lowest frequency that can be decoupled from the power supply noise. Two main factors affect the transient response of a switching regulator: the output capacitor ESR and the regulator loop bandwidth. To improve the transient response, it is preferable to add capacitors in parallel instead of using one larger output capacitor. This is to reduce the total ESR. Increasing the output capacitance value also changes the regulator loop characteristics and the phase margin, small phase margin yields to an under-damped system where oscillation occurs after a transient. If the phase margin is too large, then the system becomes over damped where the response to transients is slow. Transient performance considerations are in the Rx LO Frequency Deviations Due to Power Supply Transients section.

Figure 84 shows the 1 MHz noise spectrum of the [ADP5040](#). In this screenshot, the [ADP5040](#) is powering up the 1.3 V analog power plane with the [AD9363](#) in FDD mode.

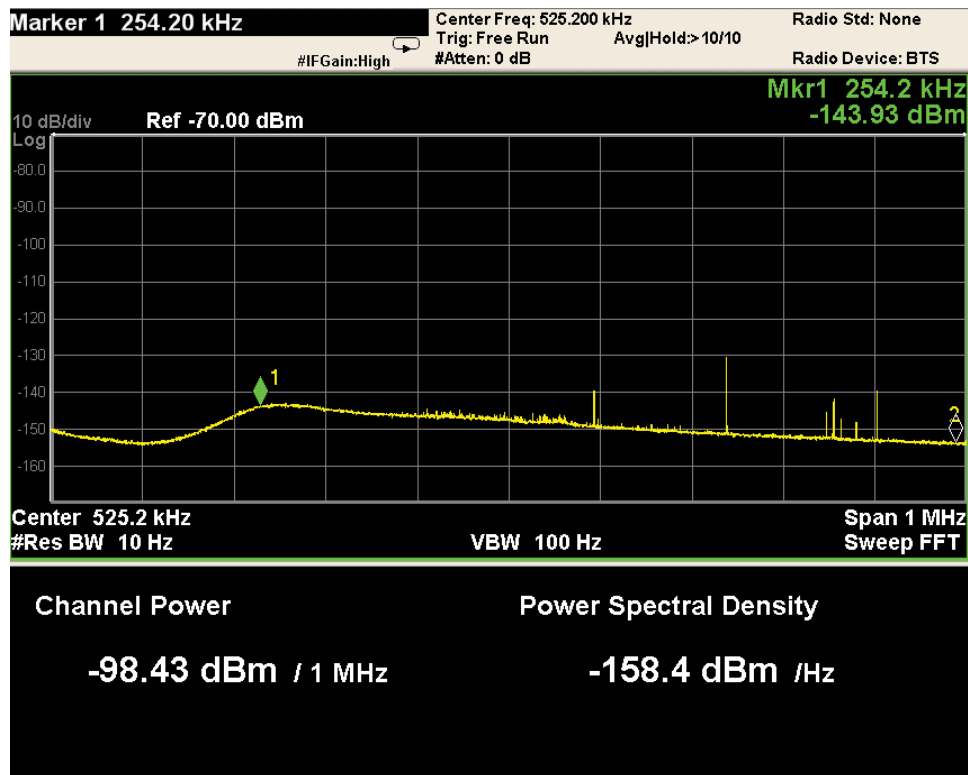


Figure 84. Noise Floor at the Buck Output of the [ADP5040](#) Powering the 1.3 V Analog Plane (the [AD9363](#) is in the FDD State)

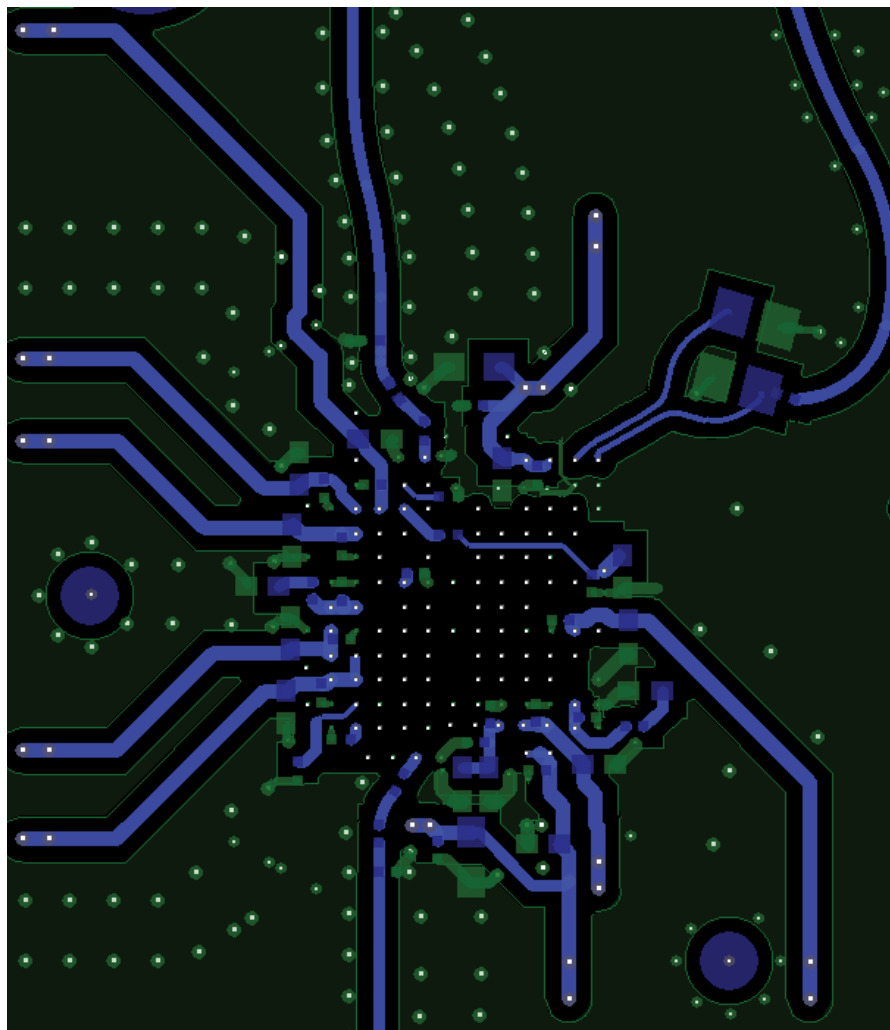
Power Distributions For Different Power Supply Domains

The AD9363 has 17 power supply balls. These balls power up different circuits on the part. Table 54 shows the ball number, the ball name, the recommended routing technique for that ball from the main 1.3 V analog supply plane and a brief description of the block it powers up in the chip. In some cases, one finger

is used to power up two to three 1.3 V power supply balls while in some cases there are some power supply balls that have a finger just for themselves. Table 54 shows which power supply balls have their own fingers and which balls are tied together and share one finger. Fingers provide isolation for the concerned 1.3 V power supply balls. Figure 85 shows this structure.

Table 54. Power Supply Pins on the AD9363

Pin No.	Mnemonic	Recommending Routing	Description
A11	VDDA1P1_TX_VCO	Short to B11 with 1 μ F bypass capacitor, 1 Ω series resistance	Powers supply for Tx VCO in the chip
B8	VDD_GPO	GPO_x pull-up voltage (1.3 V to 3.3 V)	Power supply for the GPO_x balls
B9	VDDA1P3_TX_LO	1.3 V separate trace to common supply point	Power supply for Tx LO generator and LO divider
B10	VDDA1P3_TX_VCO_LDO	Short to B9	Power supply for the Tx VCO LDO
B11	X_VCO_LDO_OUT	Short to A11	Output of the Tx VCO LDO to power the Tx VCO on the chip
D2	VDDA1P3_RX_RF	Short to D3	Power supply for the Rx LNAs and the mixer stages
D3	VDDA1P3_RX_TX	Short to E3	Power supply for Tx low-pass filter, Tx monitor, Rx transimpedance amplifier, Rx low-pass filter, auxiliary DAC
E2	VDDA1P3_RX_LO	Short to F2	Power supply for Rx LO generator and LO divider
E3	VDDA1P3_TX_LO_BUFFER	1.3 V separate trace to common supply point	Power supply to the Tx LO buffer that goes to the up converter
F2	VDDA1P3_RX_VCO_LDO	1.3 V separate trace to common supply point	Power supply input for the Rx VCO LDO
F12	VDDD1P3_DIG	1.3 V separate trace to common supply point	Powers the digital core
G2	RX_VCO_LDO_OUT	Short to G3	Output of the Rx VCO LDO to power the Rx VCO LDO in the chip
G3	VDDA1P1_RX_VCO	Short to G2 with 1 μ F bypass capacitor 1 Ω series resistance	Power supply for the Rx VCO on the chip
H12	VDD_INTERFACE	Interface pull-up voltage (1.3 V to 2.5 V)	Powers the digital interface of the chip
J3	VDDA1P3_RX_SYNTN	1.3 V separate trace to common supply point	Powers the charge pump, Σ - Δ modulator, and the VCO calibration block of the Rx synthesizer
K3	VDDA1P3_TX_SYNTN	1.3 V separate trace to common supply point	Powers the charge pump, Σ - Δ modulator, and the VCO calibration block of the Tx synthesizer
K4	VDDA1P3_BB	1.3 V separate trace to common supply point	Powers the Tx DACs, Rx ADCs, and auxiliary ADC
M7, M8	TX1A_P, TX1A_N	Vertical interconnect access (VIA) directly to 1.3 V plane	Provides power to the Tx output on the Tx1A_P and Tx1A_N pins, and the Tx1B_P and Tx1B_N pins
A7, A8	TX2A_N, TX2A_P	VIA directly to 1.3 V plane	Provides power to the Tx output on the Tx2A_P and Tx2A_N pins, and the Tx2B_P and Tx2B_N pins



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Figure 85. Power Supply Fingers

Rx and Tx Synthesizer Supplies

The power supply noise rejection on the VDDA1P3_RX_SYNTH and VDDA1P3_TX_SYNTH power domains is very low. This means that any noise ripple on these balls affects the synthesizer performance. The supply noise on the synthesizers degrades the phase noise. For the best performance in the FDD mode, VDDA1P3_RX_SYNTH, VDDA1P3_TX_SYNTH, VDDA1P3_RX_LO, VDDA1P3_RX_VCO_LDO, VDDA1P3_TX_LO, and VDDA1P3_TX_VCO_LDO can be powered up with a separate low noise LDO. This also helps mitigate the effects of transients on the 1.3 V analog supply. The evaluation board uses this power design.

Tx Balun DC Feed Supplies

Each transmitter requires 150 mA of current supplied by the dc feed of the balun. To reduce switching transients when attenuation settings change, the balun dc feed must be powered directly by the 1.3 V plane. A 10 μ F capacitor and a 0.1 μ F capacitor are helpful on the dc feed pin to eliminate spurs on the Tx spectrum and dampen the transients.

Rx LO FREQUENCY DEVIATIONS DUE TO POWER SUPPLY TRANSIENTS

The AD9363 is a transceiver that can operate in TDD or in FDD mode. In FDD mode, there is a need to dynamically change the transmit power when the receivers are on and receiving data. This means that the load that the device presents to the power supply changes, giving rise to transients on the power supply line. The amplitude and the response time of these transients depend on board layout and the regulator used to supply power. These power supply transients are detrimental to the receiver performance until the transient dies down.

Figure 86 shows the instantaneous deviation in the Rx VCO frequency due to a voltage transient on the 1.3 V supply. This experiment included the AD9363 in the FDD state. The Channel 1 spectrum in Figure 86 is the Rx VCO leakage from the Rx pin when the Rx LO is 800 MHz. Channel 2 is an FM demodulation of Channel 1, meaning that Channel 2 shows the instantaneous changes in VCO frequency. The spectrum analyzer is triggered on the TXNRX signal that turns the transmitter on or off. This environment simulates the worst case VCO frequency deviation that can occur on the Rx synthesizer.

The blue trace in Figure 87 shows the voltage transient on the 1.3 V line when the transmitters turn on. The magenta trace is the V_{TUNE} voltage of the Tx VCO that is probed on the Tx external LO line and the green trace is the V_{TUNE} voltage of the Rx VCO that is probed on the Rx external LO line. The instantaneous frequency deviation shown in Figure 86 is a direct cause of the instantaneous change in the V_{TUNE} voltage. The screenshots in Figure 86 and Figure 87 were taken simultaneously on one trigger. The experiment described previously was performed with the ADP1706 1.3 V LDO powering the 1.3 V supply.

This issue can be mitigated by powering the Rx synthesizer, Tx synthesizer, Rx LO, and Tx LO supplies from a different LDO. This approach helps in isolating the synthesizers from the transients on the 1.3 V supply. Figure 87 shows the frequency kick when the Rx synthesizer, Tx synthesizer, Tx LO, and Rx LO supplies are powered up externally. The frequency kick decreases to one third of its initial amplitude. Figure 88 shows the voltage kick on the 1.3 V supply and the consequent response of V_{TUNE} voltage of the Tx VCO (magenta) and the V_{TUNE} voltage of the Rx VCO (green).

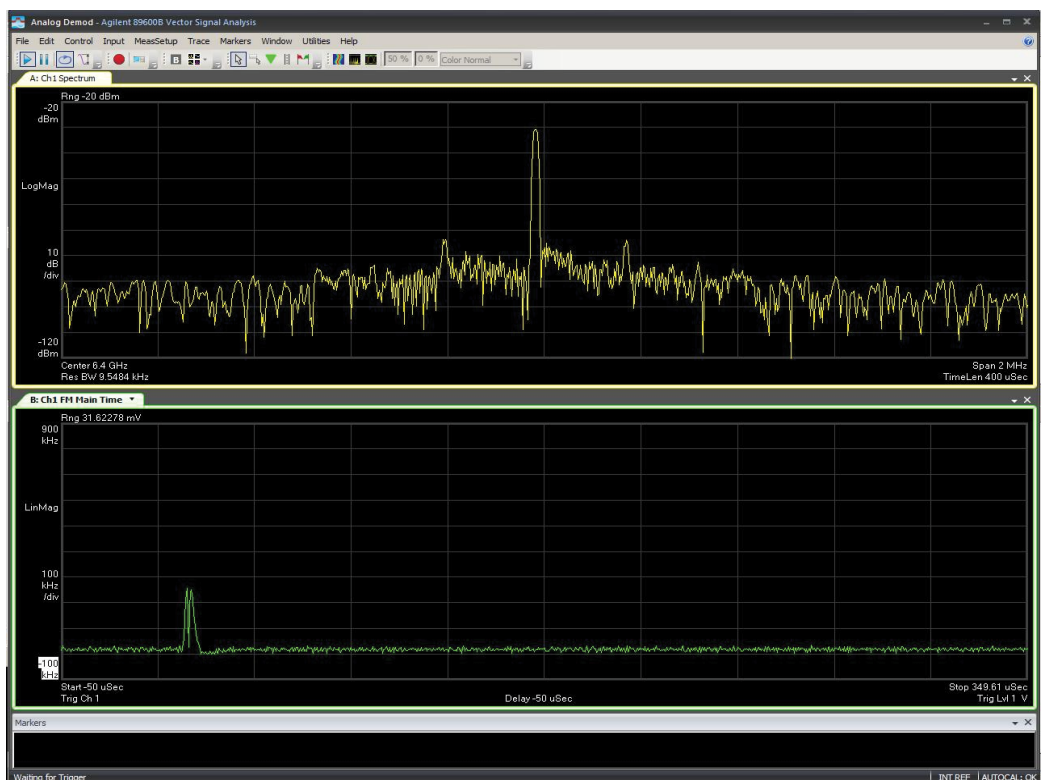


Figure 86. Instantaneous Rx VCO Frequency Deviation Seen Due to a Voltage Transient on the 1.3 V Supply

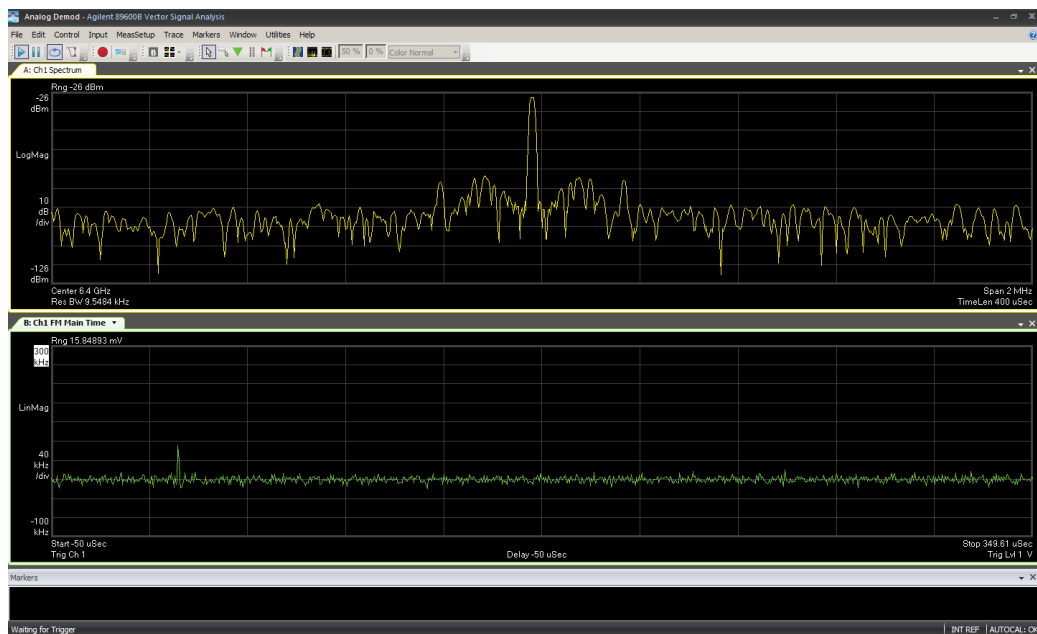
Figure 87. Voltage Transient on the 1.3 V Supply and V_{TUNE} of the Rx and the Tx VCO

Figure 88. Instantaneous Frequency Deviation Seen Due to a Voltage Transient on the 1.3 V Supply; VDDA1P3_RX_SYNTH and VDDA1P3_TX_SYNTH Supplied Externally

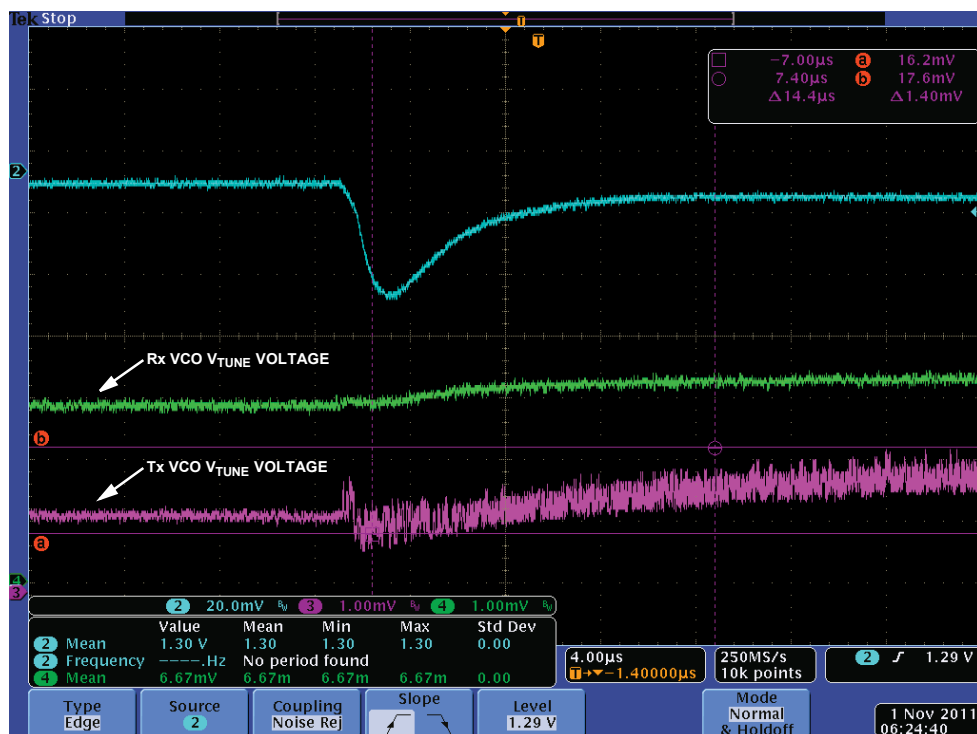


Figure 89. Voltage Transient on the 1.3 V Supply and the V_{TUNE} of the VCO; VDDA1P3_RX_SYNTH and VDDA1P3_TX_SYNTH Supplied Externally

RELATED LINKS

Resource	Description
AD9363	Product page for the AD9363 RF agile transceiver
AD9548	Product page for the AD9548 quad/octal input network clock generator/synchronizer
ADA4851-4	Product page for the ADA4851-4 low cost, high speed, rail-to-rail, output op amp (quad)
ADP1706	Product page for the ADP1706 1 A, low dropout, CMOS linear regulator
ADP1755	Product page for the ADP1755 1.2 A low V_{IN} , adjustable V_{OUT} , LDO linear regulator
ADP5040	Product page for the ADP5040 micro PMU with 1.2 A buck regulator and two 300 mA LDOs



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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