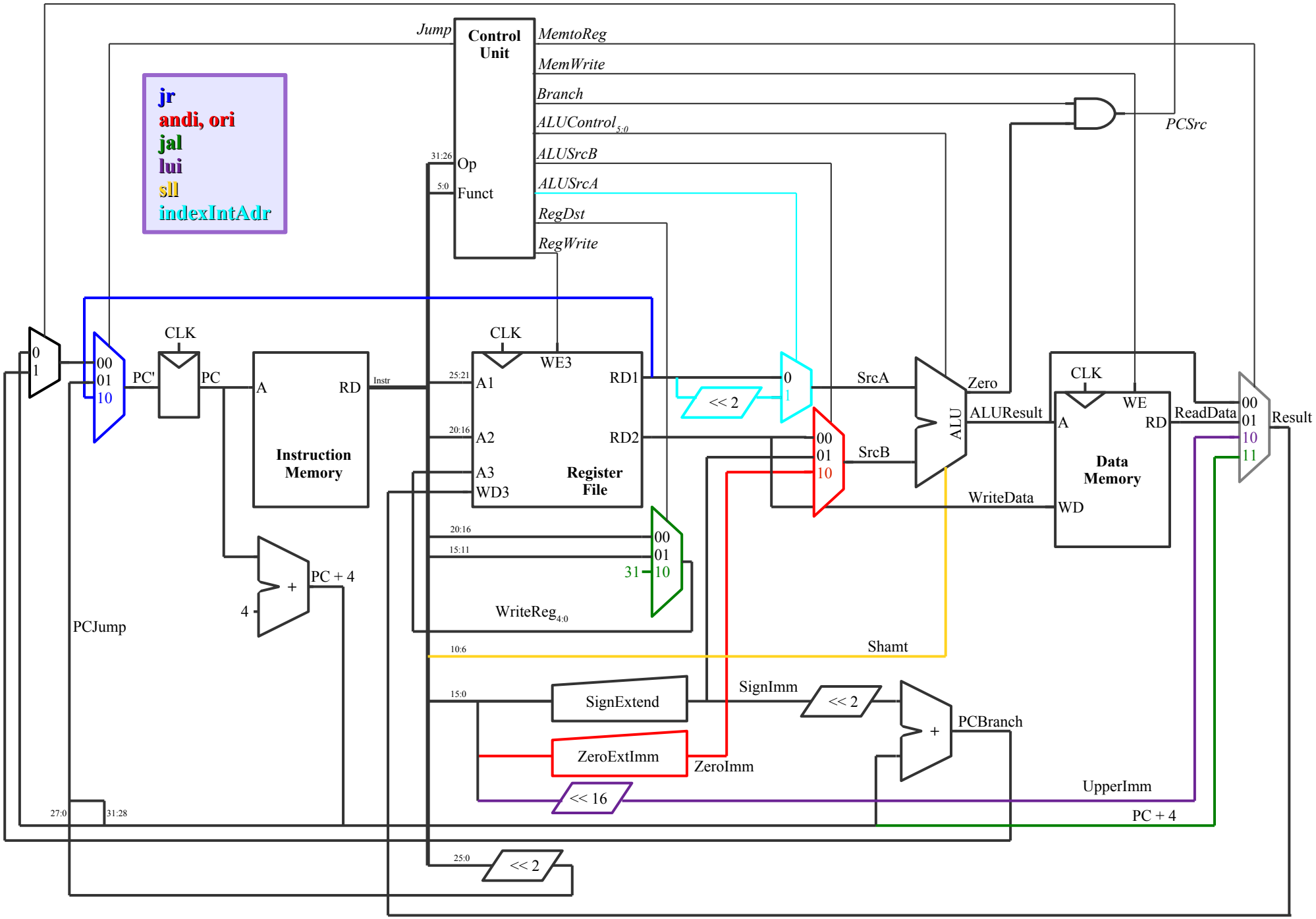
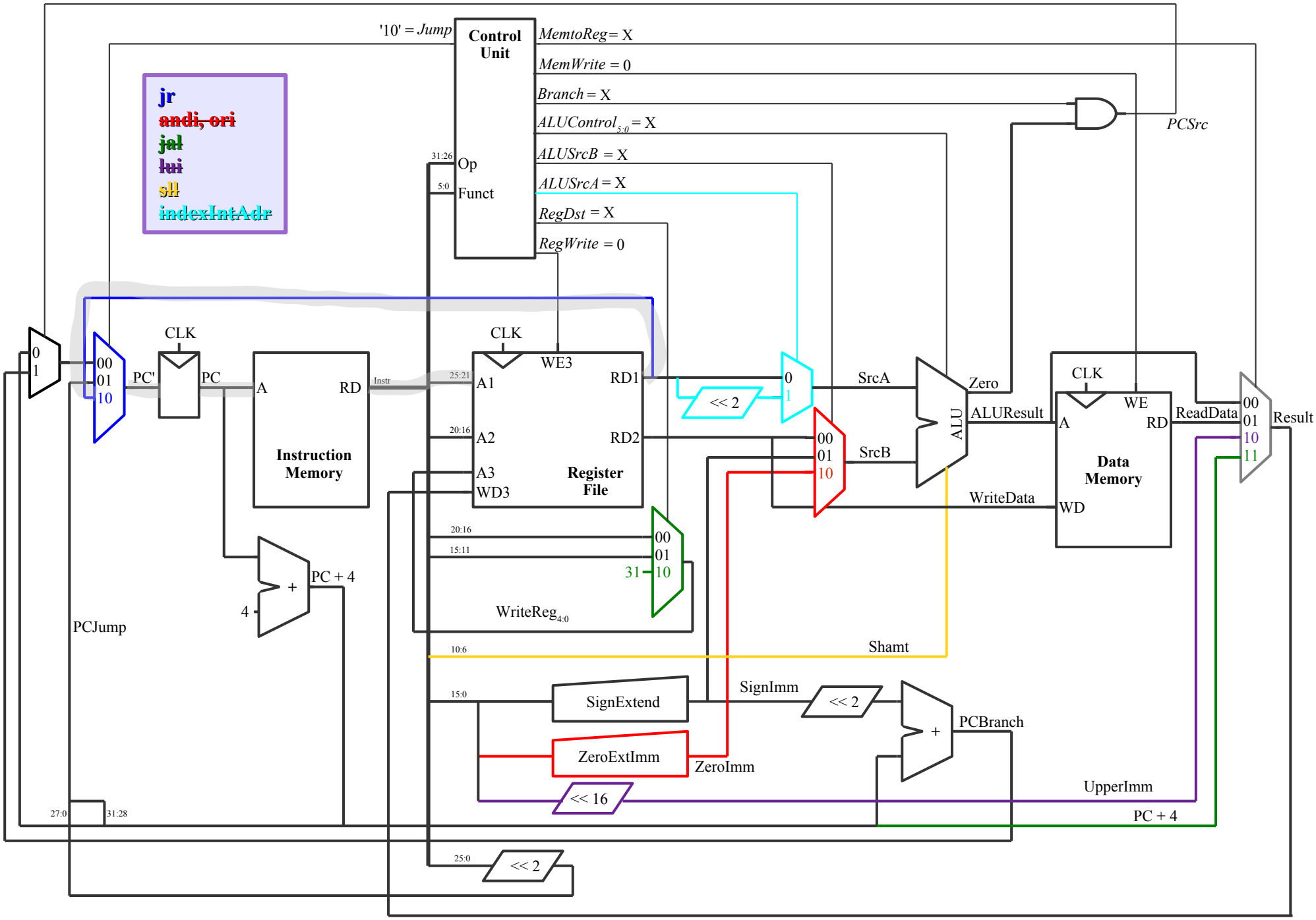

jr
andi, ori
jal
lui
sll
indexIntAdr
Jump
Control Unit
MemtoReg
MemWrite
Branch
ALUControl5:0
ALUSrcB
ALUSrcA
RegDst
RegWrite
PCSrc
31:26
Op
5:0
Funct
0
1
00
01
10
PC'
CLK
PC
A
RD
Instr
Instruction Memory
25:21
20:16
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
<< 2
SrcA
SrcB
ALU
Zero
ALUResult
WriteData
CLK
WE
A
RD
WD
Data Memory
ReadData
Result
11
PC + 4
4
+
PCJump
20:16
15:11
31
WriteReg4:0
10:6
Shamt
15:0
SignExtend
SignImm
PCBranch
ZeroExtImm
ZeroImm
<< 16
UpperImm
27:0
31:28
25:0

jr : PC = [rs]

R :

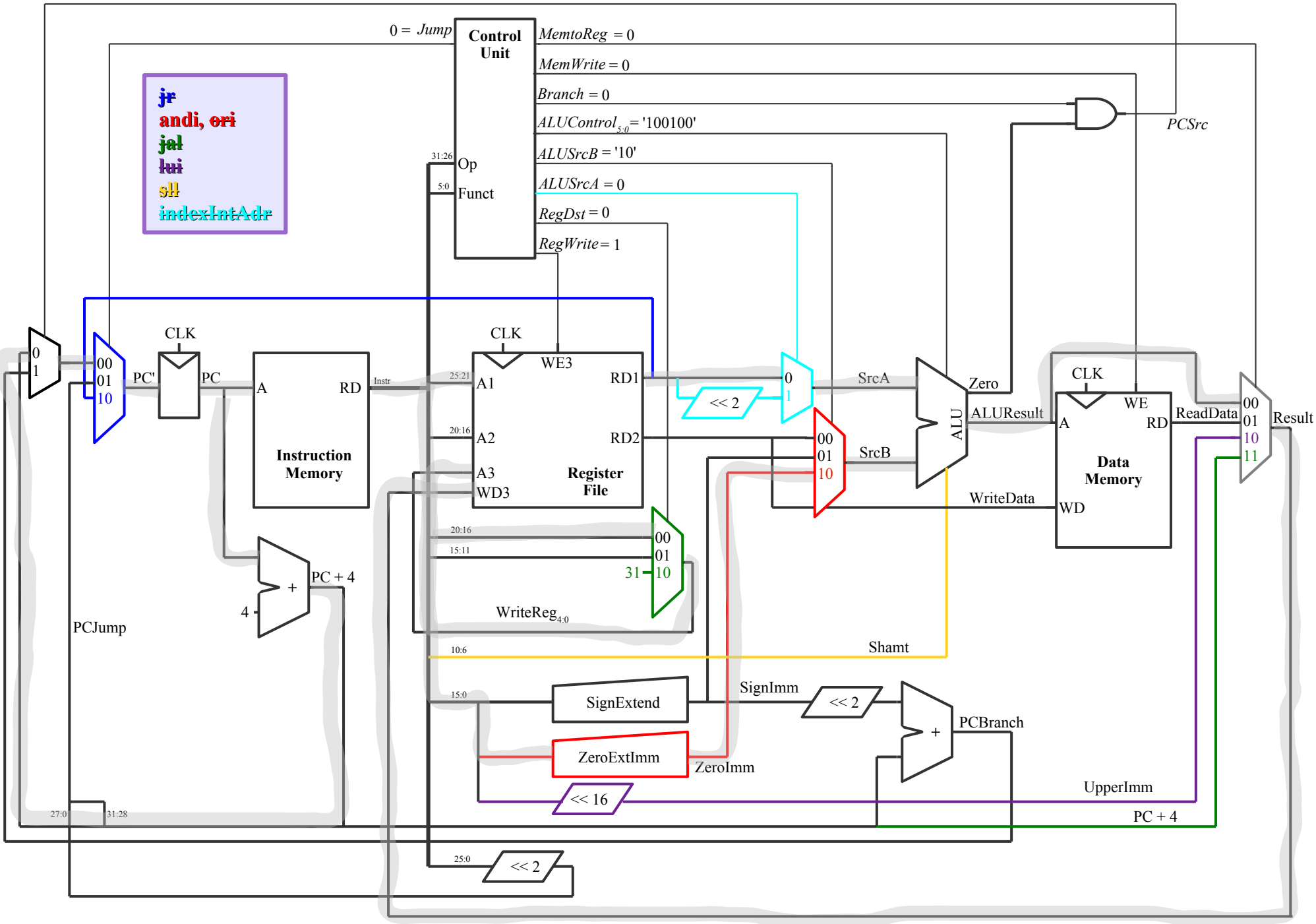
opcode	rs	rt	rd	shamt	funct
31 26	25 21	20 16	15 11	10 6	5 0



andi : [rt] = [rs] & ZeroImm

I :

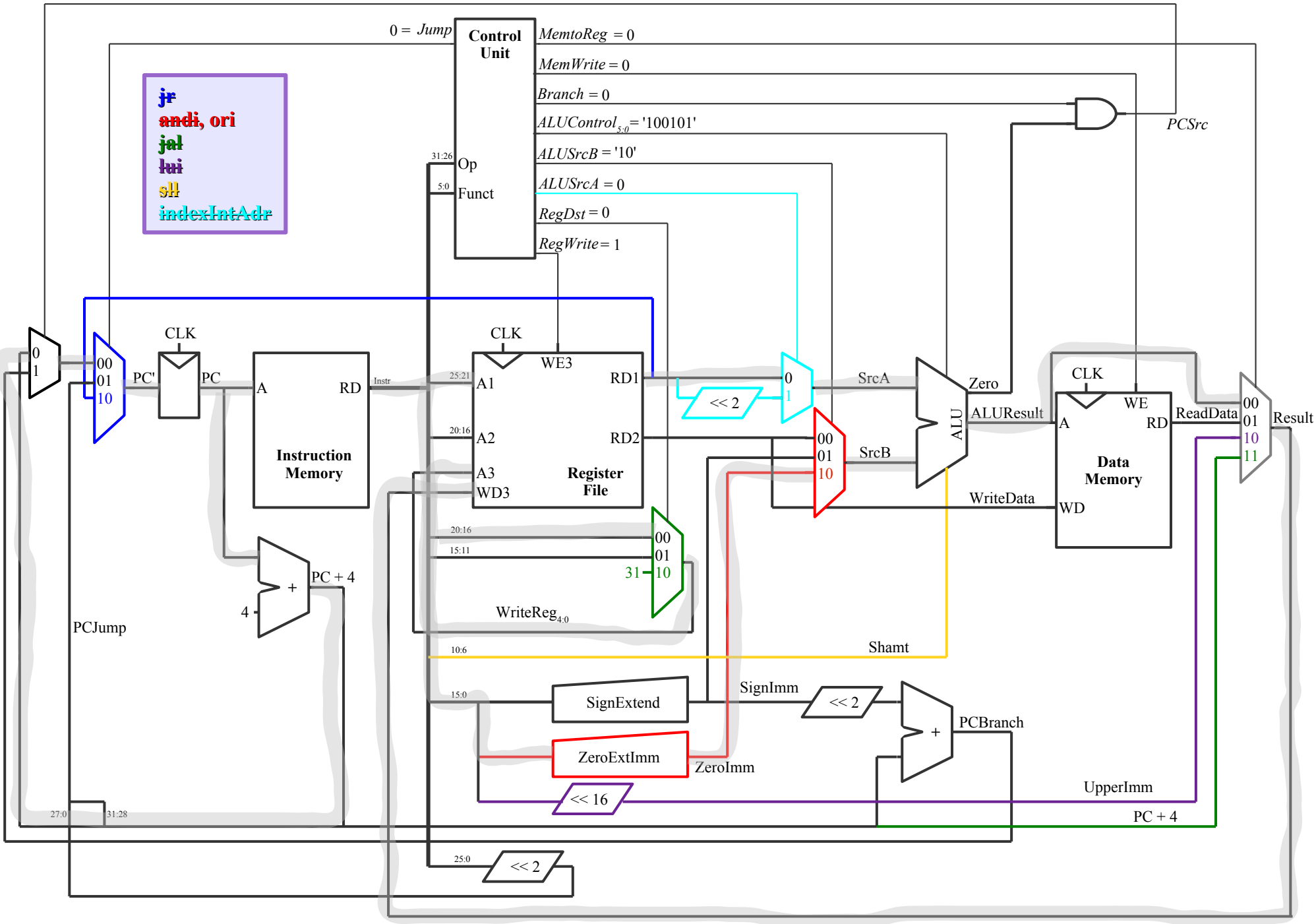
opcode	rs	rt	immediate
31 26	25 21	20 16	15 0



ori : [rt] = [rs] | ZeroImm

I :

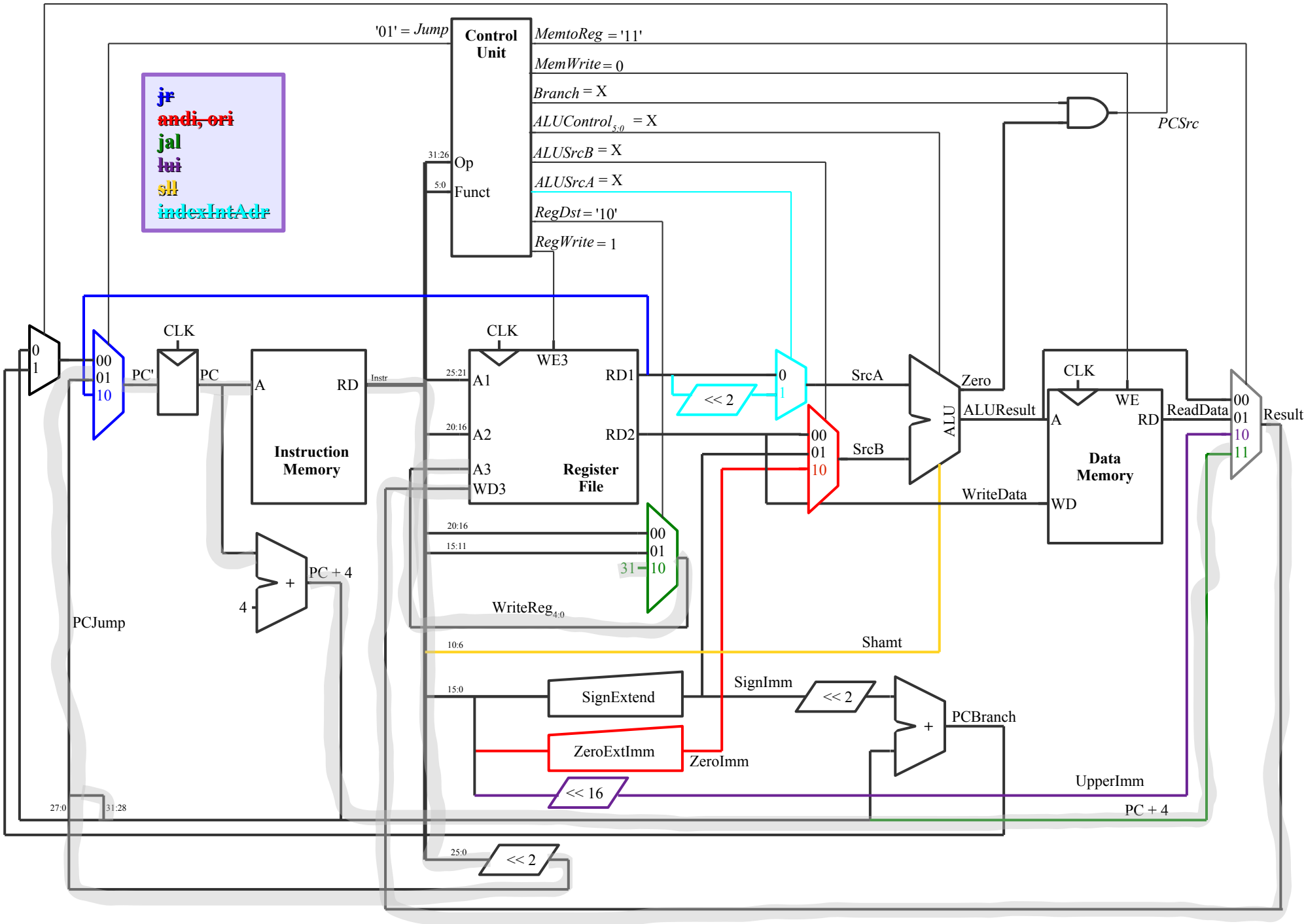
opcode	rs	rt	immediate
31 26	25 21	20 16	15 0



`jal : [$ra] = PC + 4, PC = PCJump`

J :

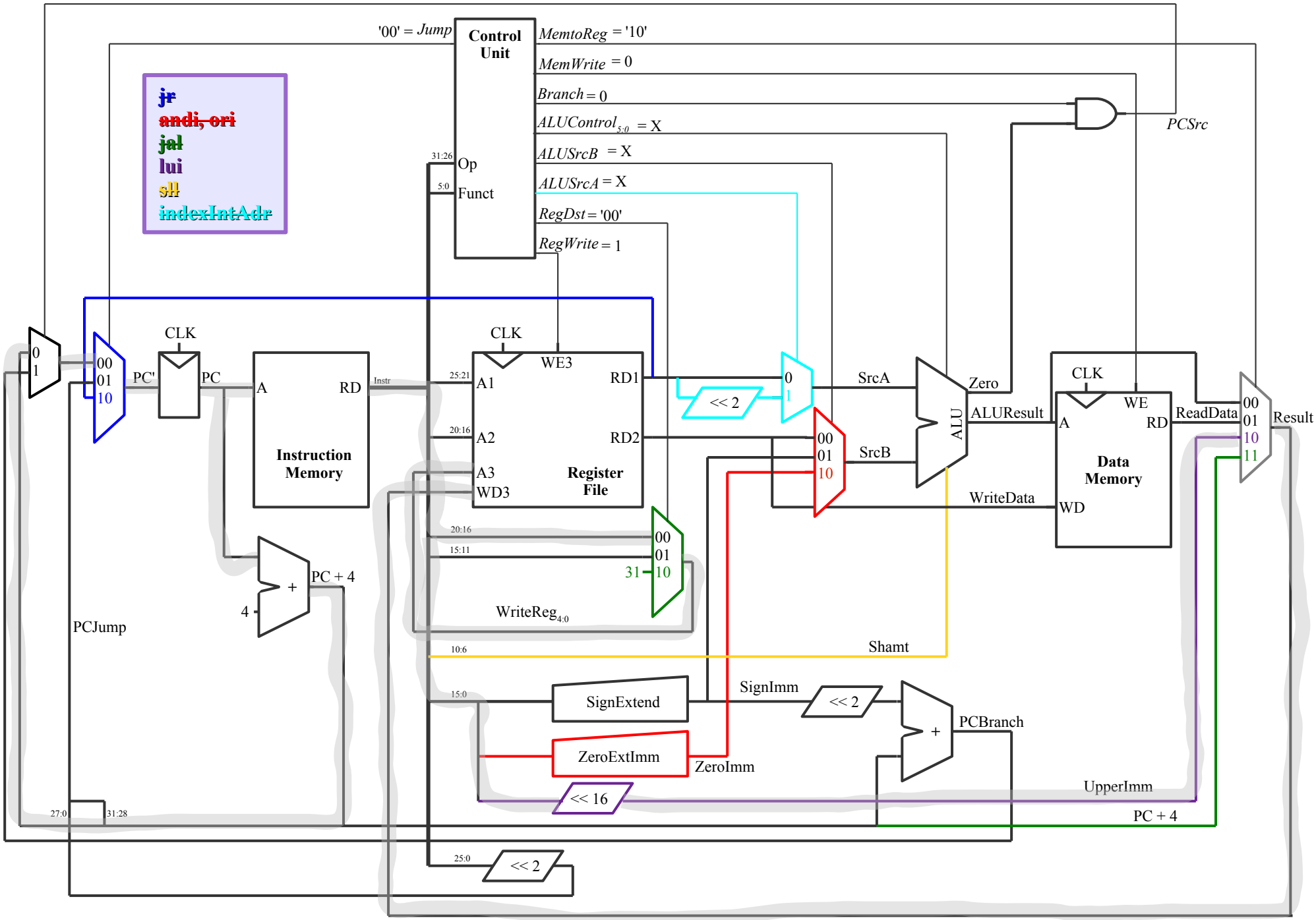
opcode	address
31 26	25 0



```
lui : [rt] = {imm, 16'b0}
```

I :

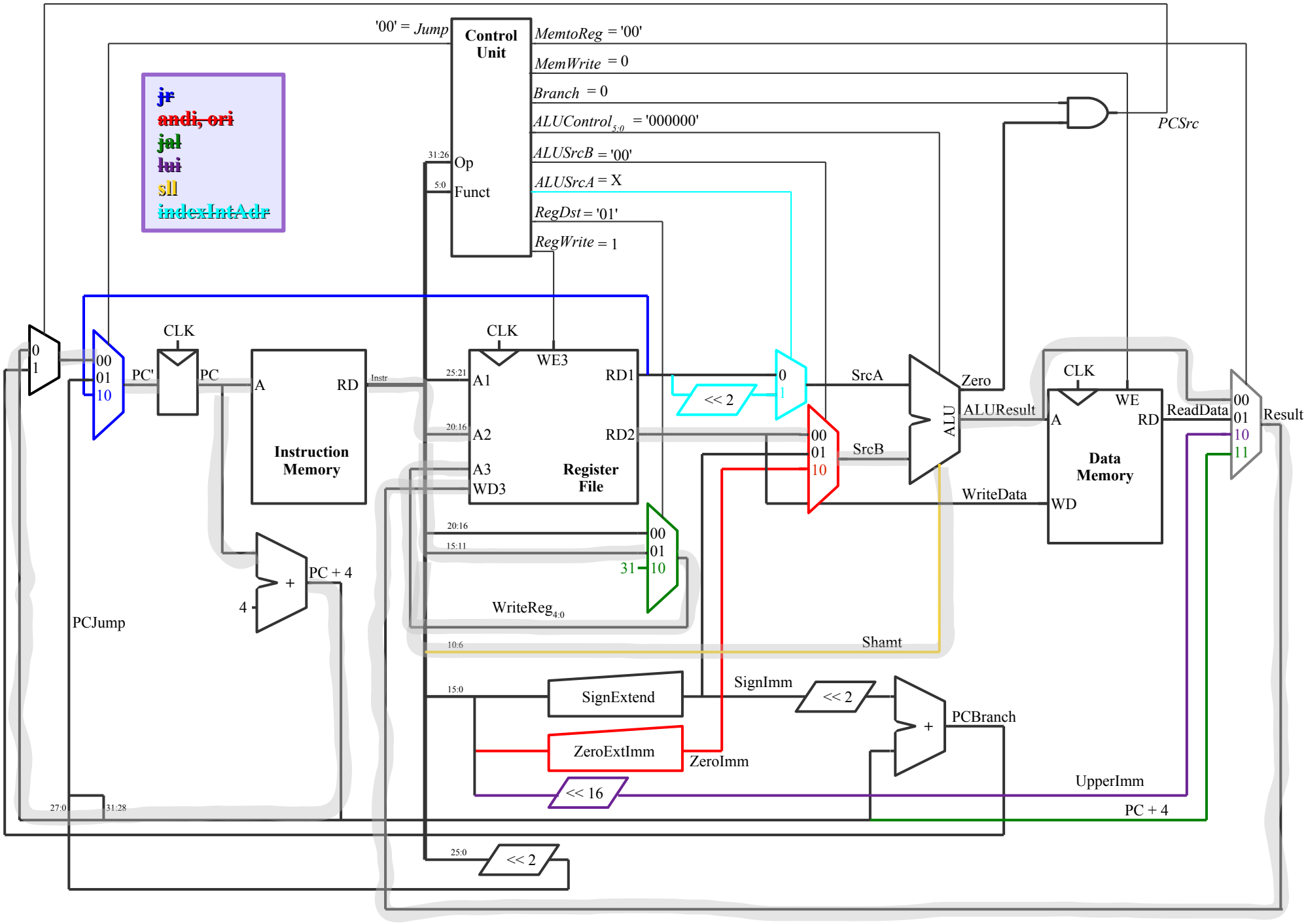
opcode	rs	rt	immediate
31 26	25 21	20 16	15 0



```
sll : [rd] = [rt] << shamt
```

R :

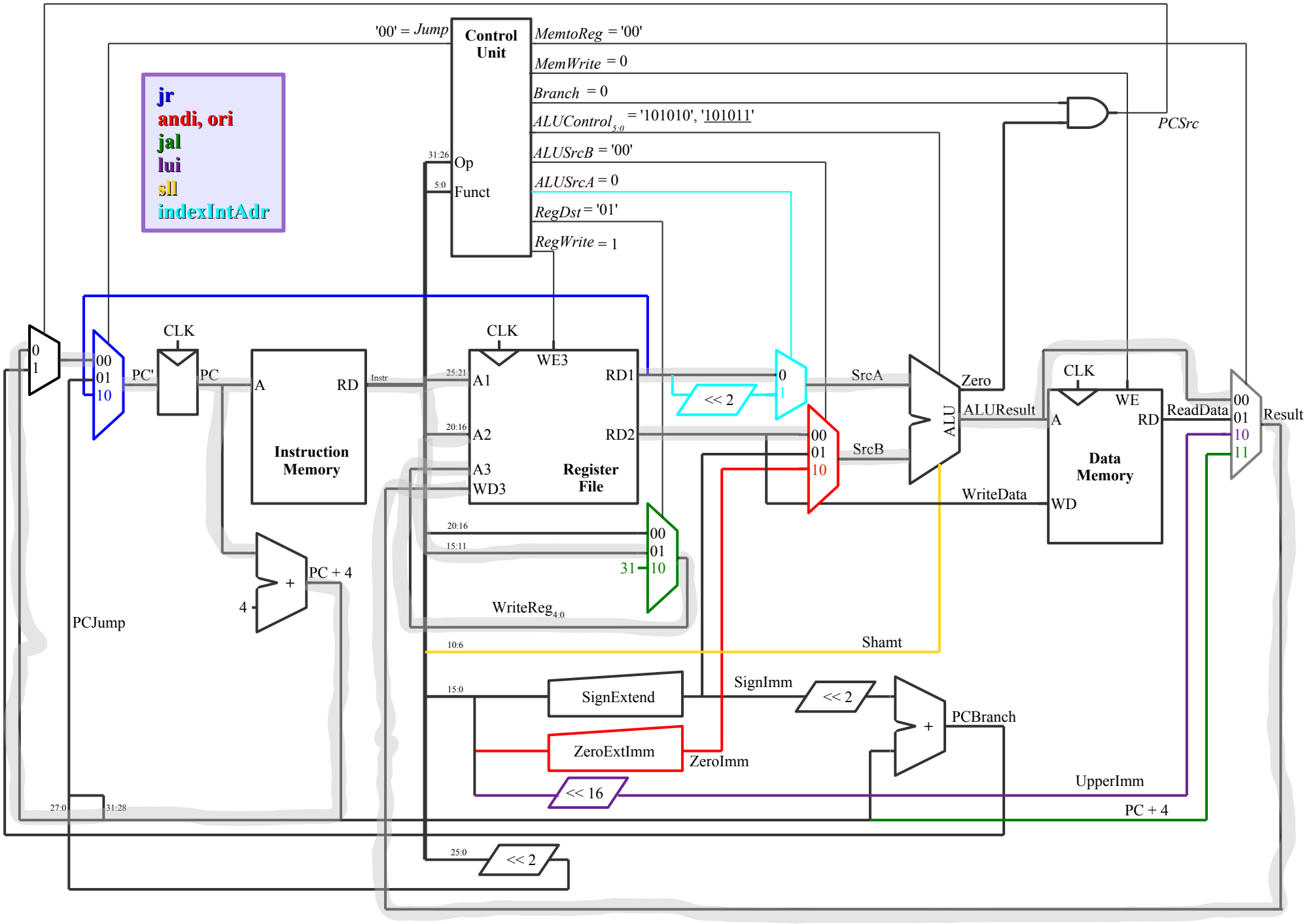
opcode	rs	rt	rd	shamt	funct
31 26	25 21	20 16	15 11	10 6	5 0



slt,sltu : [rd] = ([rs]<[rt]) ? 1:0

R :

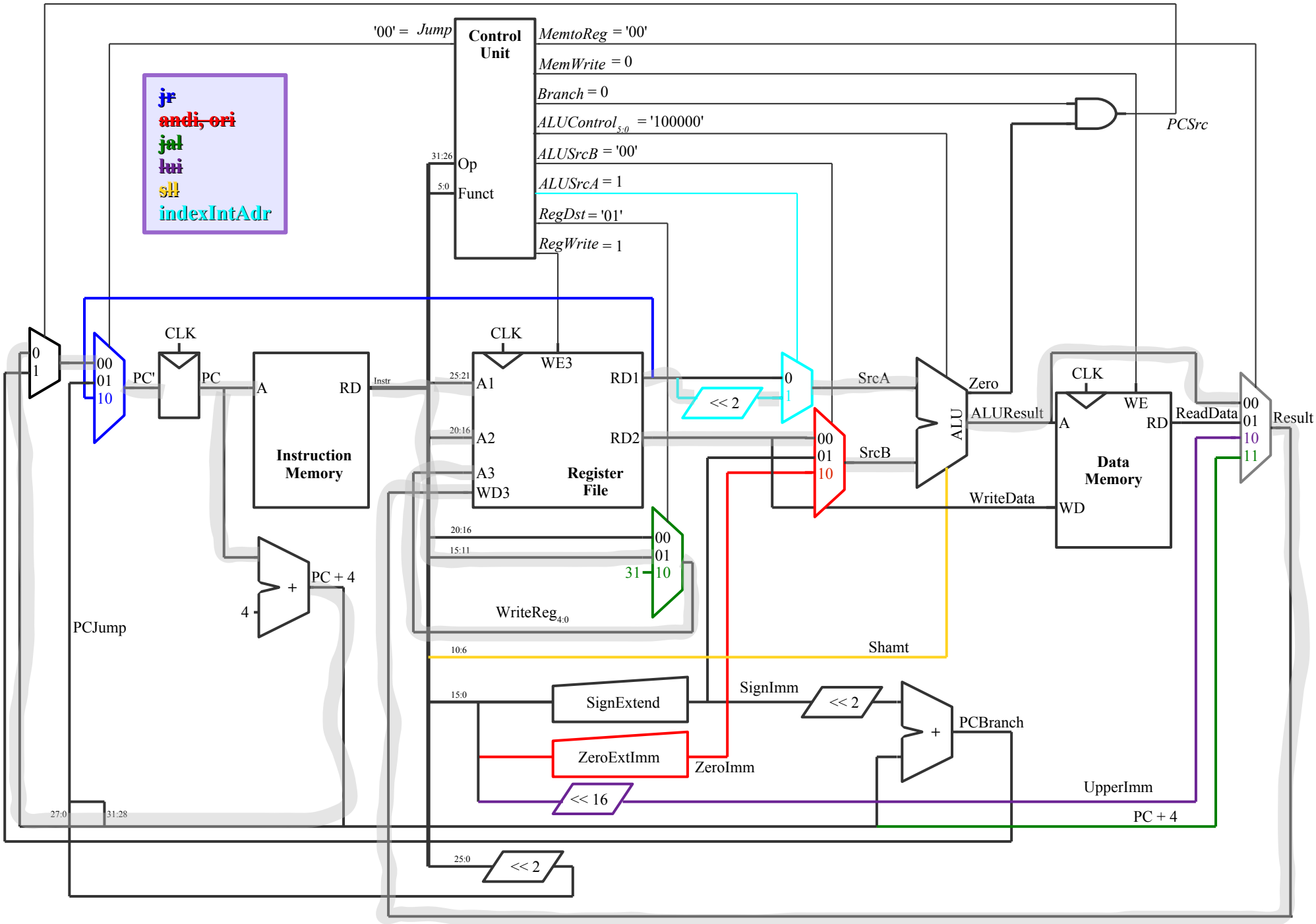
opcode	rs	rt	rd	shamt	funct
31 26	25 21	20 16	15 11	10 6	5 0



indexIntAdr : [rd] = [rs]*4 + [rt]

R' :

opcode	rs	rt	rd	shamt	funct
31 26	25 21	20 16	15 11	10 6	5 0



Instr	$Op_{31:26}$	$F_{5:0}$	RegWrite	RegDst	AluSrcA	AluSrcB	AluCtrl	Branch	MemWrite	MemtoReg	Jump
R-type	000000	Voir tab	1	01	0	00	Voir Tab	0	0	00	00
lw	100011	100000	1	00	0	01	100000	0	0	01	00
sw	101011	100000	0	XX	0	01	100000	0	1	XX	00
beq	000100	100010	0	XX	0	00	100010	1	0	XX	00
j	000010	XXXXXX	0	XX	X	XX	XXXXXX	X	0	XX	01
addi	001000	100000	1	00	0	01	100000	0	0	00	00
jr	000000	001000	0	XX	X	XX	XXXXXX	X	0	XX	10
andi	001100	XXXXXX	1	00	0	10	100100	0	0	00	00
ori	001101	XXXXXX	1	00	0	10	100101	0	0	00	00
jal	000011	XXXXXX	1	10	X	XX	XXXXXX	X	0	11	01
lui	001111	XXXXXX	1	00	X	XX	XXXXXX	0	0	10	00
sll	000000	000000	1	01	X	00	000000	0	0	00	00
sltu	000000	101011	1	01	0	00	101011	0	0	00	00
slt	000000	101010	1	01	0	00	101010	0	0	00	00
indexIntAdr	010001	XXXXXX	1	01	1	00	100000	0	0	00	00