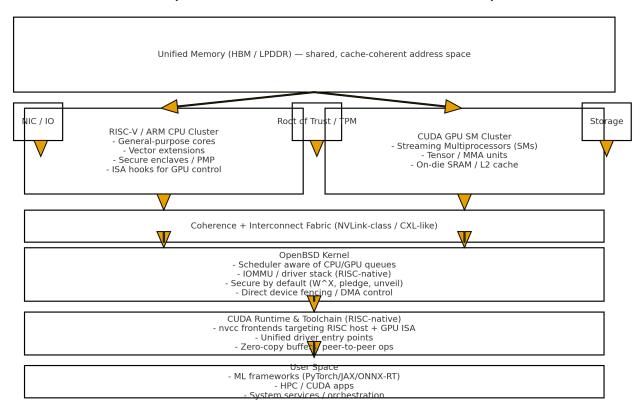
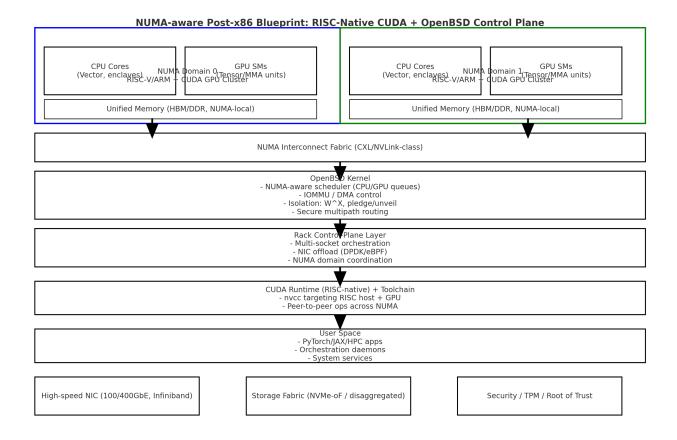
## Post■x86 Blueprint: RISC■Native CUDA + OpenBSD

## Single**■**socket unified design

Post-x86 Blueprint: RISC-Native CUDA on Fused CPU+GPU with OpenBSD



NUMA■aware rack■scale design



This document presents two architecture blueprints: - A clean, single die fused CPU+GPU RISC native CUDA stack with OpenBSD. - An extended, NUMA wave rack scale design with multipath control plane. Together, they outline a credible post x86 future for AI/HPC infrastructure.