ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 322E

COMPUTER ARCHITECTURE
ASSIGNMENT 3

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STUDENT:

NAME : ABDULKADİR

SURNAME : PAZAR

NUMBER : 150180028

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Question 1

Percentage of Data Transfer Time

Percentage of data transfer time can be calculated as:

$$\frac{740\text{ns} \cdot 2\text{MB}}{2\text{bytes}} = \frac{740 \cdot 10^{-9} \cdot 2 \cdot 10^{6}\text{bytes}}{2\text{bytes}} = 0.74 = \%74$$

Question 2

a)

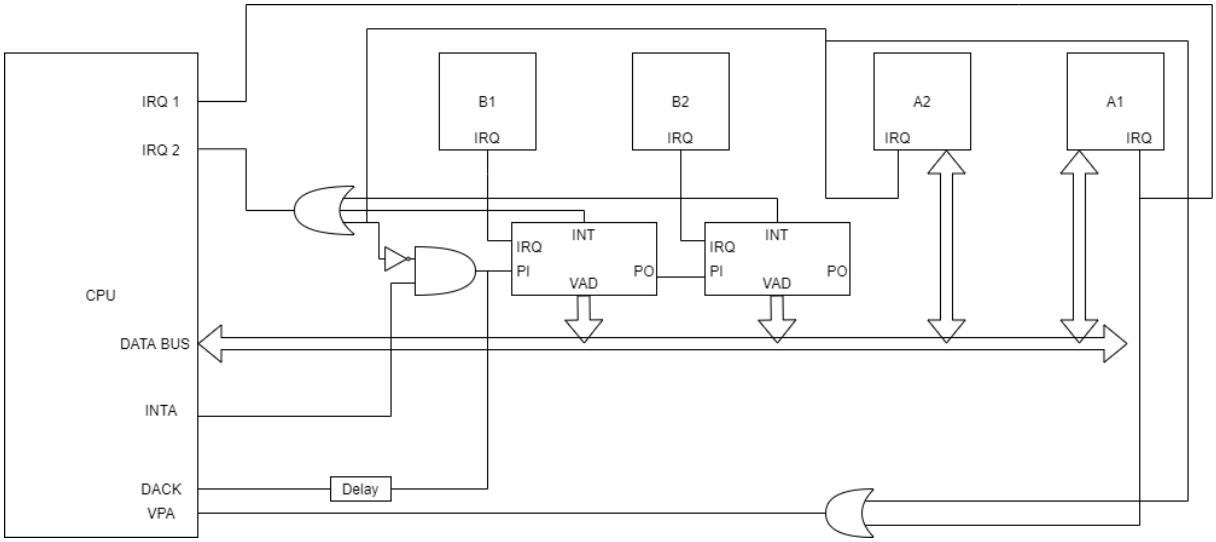

Figure 1: Design of the System

In my design of the system, I connected IRQ of A1 to IRQ1 input as it has the highest precedence. I connected other devices to IRQ2 input using an OR gate with inputs as IRQ of A2, INT of priority 1 of daisy chain and, INT of priority 2 of daisy chain. To read from B devices, we need DACK of CPU to be 1. For that I connected the PI input of priority 1 box of the daisy chain. This input signal is the AND of $\overline{\text{IRQA2}}$ and INTA signal which will be 1 when INTA=1 and A2 has no interrupt request. For the A devices, I connected them to the data bus to be able to clear interrupt requests. DACK is 0 whenever PI of priority 1 box is 0 as to not read the interrupts. And their IRQs are connected to VPA as they work in autovectored mode.

b)

- IRQ A2 makes IRQ 2 input of CPU 1.
- VPA becomes 1 as IRQ A2 is 1.
- Since PI of priority 1 of daisy chain is 0 because $\overline{\text{IRQA2}}$ is connected to the AND gate, VAD is not sent to the data bus as register is disabled.
- After IRQ A2 is removed after the software action, PI of priority 1 of daisy chain becomes 1. After a delay, DACK input becomes 1.
- Since PI became 1, PO becomes 1 but VAD register is disabled as B1 didn't send a request.
- PI of priority 2 becomes 1, this in turn makes VAD register enabled as both PI and IRQ B2 is 1.
- VAD register is sent to the data bus and INT is sent to the IRQ2 input of the CPU.