ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 322E

COMPUTER ARCHITECTURE
ASSIGNMENT 4

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Question 1

TIME	CPU	DMAC1	DMAC2	DMAC3	DMAC4
0-40	IF	REQUEST	REQUEST	REQUEST	REQUEST
40-140	OR,EX	1st word			
140-640			All 5 words		
640-740		2nd word			
740-1240				All 5 words	
1240-1340		**3rd word**			
1340-1440					1st word
1440-1540		4th word			
1540-1640					2nd word
1640-1740		5th word			
1740-1840					3rd word
1840-1870	**OW**				
1870-1970					4th word
1970-2010	IF				
2010-2110	OR,EX				**5th word**

- Data transfer takes 100 ns (memory access time + I/O interface access time).
- at C = 20ns, when CPU is in the IF stage, all 4 DMACs attempt to start the transfer.
- Between 40-140 ns, CPU can complete OR and EX stages since it doesn't access the memory while $DMAC_1$ transfers the first word since it has highest precedence.
- Since $DMAC_1$ works in cycle stealing mode, it releases the bus to $DMAC_2$. $DMAC_2$ completes the transfer of all 5 words between 140-640 ns since it works in burst mode.
- $DMAC_1$ takes control of the bus, transfers 2nd word between 640-740 ns and releases the bus to $DMAC_3$.
- $DMAC_3$ completes the transfer of all 5 words between 740-1240 ns since it works in burst mode.
- **$DMAC_1$ takes control of the bus, transfers 3rd word between 1240-1340 ns and releases the bus to $DMAC_4$.**

- $DMAC_4$ transfers 1st word between 1340-1440 ns and gives control to $DMAC_1$ since it works in cycle stealing mode.
- $DMAC_1$ transfers 4th word between 1440-1540 ns and gives control to $DMAC_4$ since it works in cycle stealing mode.
- $DMAC_4$ transfers 2nd word between 1540-1640 ns and gives control to $DMAC_1$ since it works in cycle stealing mode.
- $DMAC_1$ transfers 5th word between 1640-1740 ns and gives control to $DMAC_4$ since it works in cycle stealing mode.
- $DMAC_4$ transfers 3rd word between 1740-1840 ns and gives control to the CPU since it works in cycle stealing mode.
- **CPU completes OW stage between 1840-1870 ns and gives bus to $DMAC_4$.**
- $DMAC_4$ transfers 4th word between 1870-1970 ns and gives control to the CPU since it works in cycle stealing mode.
- CPU completes the IF stage of the next instruction between 1970-2010 ns and releases the bus to $DMAC_4$.
- **In 2010-2110 ns, $DMAC_4$ completes the transfer of 5th word while the CPU completes OR and EX stages.**

a.

As explained above in the first bold bullet point, $DMAC_1$ will complete the transfer of 3rd word at C = 1340 ns.

b.

As explained above in the second bold bullet point, CPU will finish the first instruction at C = 1870 ns.

c.

As explained above in the third bold bullet point, $DMAC_4$ will complete the transfer of 5th word at C = 2110 ns.

Question 2

TIME	CPU	DMAC1	DMAC2	DMAC3	DMAC4
0-40	IF	REQUEST	REQUEST	REQUEST	REQUEST
40-90	OR, EX	1st word			
90-100	EX		All 5 words		
100-340			All 5 words		
340-390		2nd word			
390-640				All 5 words	
640-690		3rd word			
690-940					All 5 words
940-990		4th word			
990-1020	OW				
1020-1070		**5th word**			
1070-1270	IR				
1270-	**ISR**				

- Since DMAC type is fly-by (implicit), data is transferred in 50 ns.
- At 10 ns when CPU is in the IF stage, device IS sends an interrupt request.
- At 20 ns when CPU is still in the IF stage all 4 DMACs attempt to transfer words.
- At 40-90 ns $DMAC_1$ sends the 1st word and releases the bus to $DMAC_2$ since it works in cycle stealing mode while CPU completes OR stage and is at EX stage.
- $DMAC_2$ transfers all 5 words between 90-340 ns since it works in burst mode while CPU completes EX stage at 100 ns.
- $DMAC_1$ takes control of the bus since it has highest precedence and transfers 2nd word between 340-390 ns and releases the bus to $DMAC_3$.
- $DMAC_3$ transfers all 5 words between 390-640 ns since it works in burst mode.
- $DMAC_1$ transfers 3rd word between 640-690 ns and releases the bus to $DMAC_4$ since it works in cycle stealing mode.
- $DMAC_1$ transfers all 5 words between 690-940 ns since it works in burst mode.
- $DMAC_1$ transfers 4th word between 940-990 ns and releases the bus to CPU since it works in cycle stealing mode.

- CPU completes OW stage between 990-1020 ns and releases the bus to $DMAC_1$.
- **$DMAC_1$ transfers the 5th word between 1020-1070 ns and releases the bus to CPU.**
- CPU completes the IR stage since there is an interrupt request between 1070-1270 ns.
- **ISR starts at 1270 ns after the IR stage is completed.**

a.

As explained above in the first bold bullet point, $DMAC_1$ will complete the transfer of all 5 words at C = 1070 ns.

b.

As explained above in the second bold bullet point, ISR will start to run at C = 1270 ns.