ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 322E

COMPUTER ARCHITECTURE
ASSIGNMENT 1

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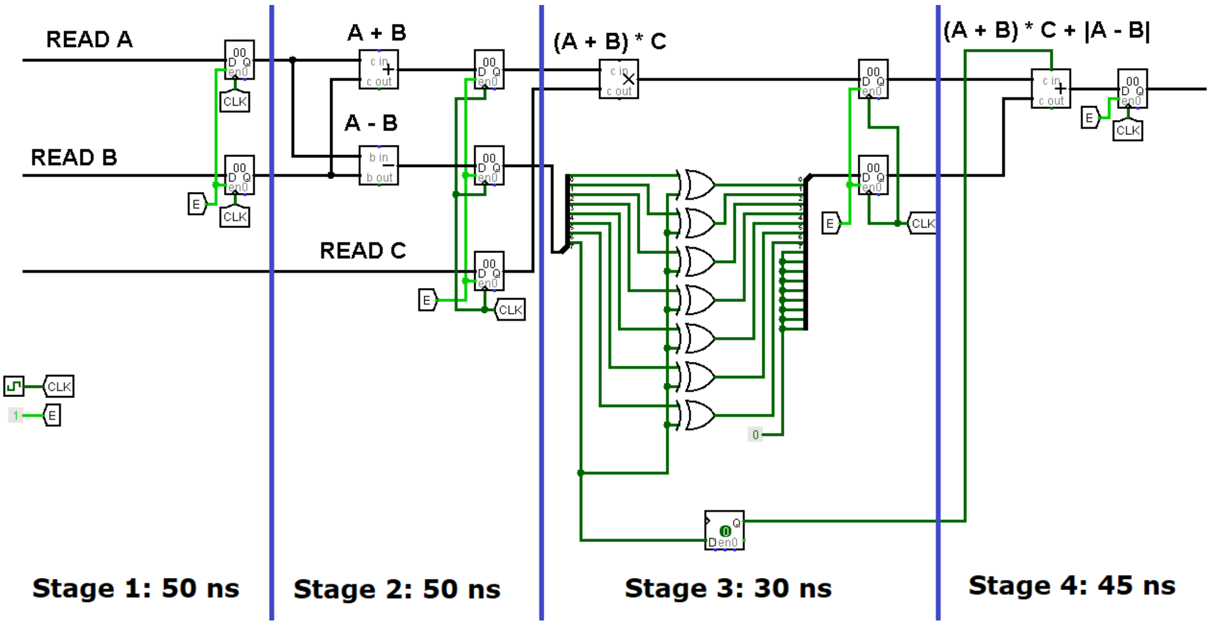
1 Design of The Pipeline Structure



Since memory access is the slowest operation at 50 ns, the sensible thing to do is to keep other stages close to 50 ns. Addition, subtraction and multiplication is done by closed block circuits. $|A - B|$ is calculated using 7 XOR gates. If $A - B$ is positive MSB of the number is 0, XORing the bits with 0 would produce the same bits and it can be passed to the 16-bit adder after sign extension. Adding the MSB, which is 0, at the 16-bit adder does not change the result of the final operation If $A - B$ is negative MSB of the number is 1, XORing the bits with 1 would produce 1's complement of the number. The MSB is passed to the next stage using the D flip-flop because if $A - B$ is negative to achieve the 2's complement we add MSB, which is 1, as carry in to the 16-bit adder circuit.

Input/output lengths of circuits and registers is as follows:

- Pipeline register between Stage 1 and 2: 16 bit in/out
- Adder circuit in Stage 2: 2 8 bit in/8 bit out
- Subtractor circuit in Stage 2: 2 8 bit in/8 bit out
- Pipeline register between Stage 2 and 3: 24 bit in/out
- Multiplication circuit at Stage 3: 2 8 bit in/16 bit out
- XOR gates at Stage 3: 1 bit in/out
- D flip-flop at Stage 3: 1 bit in/out

- Pipeline register between Stage 3 and 4: 32 bit in/out
- Adder circuit in Stage 4: 2 16 bit in/16 bit out
- Pipeline register at the end of Stage 4: 16 bit in/out

2 Cycle Time of The Pipeline

Cycle time is calculated by following formula:

$$\mathrm{t_p = max(\tau_i) + d_r}$$

Where:
$\mathrm{t_p}$: Cycle Time
$\mathrm{max(\tau_i)}$: Maximum Stage Delay
$\mathrm{d_r}$: Register Time Delay

The slowest stages in my design are stages with memory read which have a delay of 50 ns. Pipeline register delays are 5 ns.

$$\mathrm{t_p = 50ns + 5ns = 55ns}$$

3 Execution Time of the First Element

The execution of the first element does not benefit from pipelining. Since cycle time is 55 ns and there are 4 stages, the execution time of the first element is as follows:

$$\mathrm{T_1 = 55ns \cdot 4 = 220ns}$$

4 Speedup of the Pipeline

Delay without pipelining can be calculated by summing the delays of individual stages.

$$\mathrm{t_n = 50ns + 50ns + 30ns + 45ns = 175ns}$$

Formula for Speedup:

$$\mathrm{S = \frac{n \cdot t_n}{(k + n - 1) \cdot t_p}}$$

Where:
n: Number of tasks

$\mathrm{t_n}$: Delay without pipelining

k: Number of stages

$\mathrm{t_p}$: Cycle time

4.1 Infinite Number of Elements

As n approaches infinity speedup will be the ratio of coefficients of n which are $\mathrm{t_n}$ in the numerator and $\mathrm{t_p}$ in the denominator.

$$\lim_{n\to\infty} S = \frac{t_n}{t_p} = \frac{175}{55} = 3.\overline{18}$$

4.2 5 Elements

If the number of elements is finite, we can use the formula for speedup.

$$S = \frac{5 \cdot 175}{(4+5-1)\cdot 55} = \frac{875}{440} = 1.988\overline{63}$$

5 Theoretical Maximum Speedup of the Pipeline

Theoritical maximum speedup can be achieved by dividing the task into equal k parts. If it were possible to divide the main task into k equal small operations and ignore register delays the cycle time would be $\mathrm{t_p} = \frac{\mathrm{t_n}}{\mathrm{k}}$. Since there are 4 stages in my design, theoretical maximum speedup would be $\mathrm{S} = \frac{\mathrm{t_n}}{\mathrm{t_p}} = \mathrm{k} = 4$.