ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 322E

COMPUTER ARCHITECTURE
ASSIGNMENT 2

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Question 1

Space-Time Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
SUB R2, R2, R1	IF	DR	EX	ME	WB																				
NOOP		IF	DR	EX	ME	WB																			
NOOP			IF	DR	EX	ME	WB																		
ADD R1, $03, R3				IF	DR	EX	ME	WB																	
ADD R1, $01, R2					IF	DR	EX	ME	WB																
NOOP						IF	DR	EX	ME	WB															
NOOP							IF	DR	EX	ME	WB														
ADD R2, $10, R5								IF	DR	EX	ME	WB													
SUB R3, $01, R3									IF	DR	EX	ME	WB												
NOOP										IF	DR	EX	ME	WB											
NOOP											IF	DR	EX	ME	WB										
ADD R5, R3, R5												IF	DR	EX	ME	WB									
ADD R4, $01, R4													IF	DR	EX	ME	WB								
SUB R2, $01, R2														IF	DR	EX	ME	WB							
BNZ LOOP															IF	DR	EX	ME	WB						
ADD R5, $10, R5																IF	DR	EX	ME	WB					
NOOP																	IF	DR	EX	ME	WB				
NOOP																		IF	DR	EX	ME	WB			
STL $08(R6), R5																			IF	DR	EX	ME	WB		
SUB R1, R1, R4																				IF	DR	EX	ME	WB	
SUB R1, R1, R3																					IF	DR	EX	ME	WB

Total amount of penalty in clock cycles: 8 clock cycles.

Optimized Software-based Solution

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
SUB R2, R2, R1	IF	DR	EX	ME	WB																
NOOP		IF	DR	EX	ME	WB															
NOOP			IF	DR	EX	ME	WB														
ADD R1, $01, R2				IF	DR	EX	ME	WB													
ADD R1, $03, R3					IF	DR	EX	ME	WB												
NOOP						IF	DR	EX	ME	WB											
ADD R2, $10, R5							IF	DR	EX	ME	WB										
SUB R3, $01, R3								IF	DR	EX	ME	WB									
NOOP									IF	DR	EX	ME	WB								
ADD R4, $01, R4										IF	DR	EX	ME	WB							
ADD R5, R3, R5											IF	DR	EX	ME	WB						
SUB R2, $01, R2												IF	DR	EX	ME	WB					
BNZ LOOP													IF	DR	EX	ME	WB				
ADD R5, $10, R5														IF	DR	EX	ME	WB			
SUB R1, R1, R4															IF	DR	EX	ME	WB		
SUB R1, R1, R3																IF	DR	EX	ME	WB	
STL $08(R6), R5																	IF	DR	EX	ME	WB

We can change the order of some instructions as long as the change does not alter the algorithm of the program or cause new conflict. After optimization, we obtain the space-time diagram above.

Total amount of penalty in clock cycles: 4 clock cycles.