Southern Illinois University, Carbondale  
Department of Electrical, Computer and Bio-Medical Engineering

**PROGRAMMABLE ASIC DESIGN**

**Final Project**

“IMPLEMENTATION OF ANN TO PREDICT HANDWRITTEN DIGITS”

Submitted By:

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December 03,2020

**Introduction:**

The project is initiated with the objective of recognizing the handwritten digits. These digits are represented in pixels in file “digits\_hex.txt” which has a value ranging from –0.5 to 0.5. It is represented by 8-bit fixed point 2’s complementary numbers with 7 fractional bits. There are 64 input layer nodes and 12 hidden layers in between and 10 nodes in output layer.

**Our Implementation:**

We were able to perform weighted sum of previous layer outputs (𝑦 = ΣiN=1 𝑤𝑖 ⋅ 𝑥𝑖 + 𝑏𝑖) and weighted sum was fed to activation function(sigmoid function) 𝑓(𝑦) = 1/ (1+𝑒−𝑦) - 0.5. The output we obtained in our implementation is the 8 bit output of Node **H1.**

B11

H1

W1 3,1

W1 64,1

W1 2,1

W1 1,1

P64

P3

P2

P1

Image Data  
(Pixels)

as

**Milestone 1: Multiplier and Accumulator (MAC) Module Design**

In this design phase, we are going to design a MAC module that perform computation 𝑦 = ΣiN=1 𝑤𝑖 ⋅ 𝑥𝑖 . Since both 𝑤𝑖 and 𝑥𝑖 are 8-bit fixed-point numbers, the final output should have 20 bits. First, we take 8 bit pixel value and weight and multiply those which are again added to another output of multiplication of 8 bit pixel value and weight. This addition is done after multiplication of 8 bit pixel and weight value obtained by splitting 128 bit pixel and weight value in each line of “digits\_hex.txt” and “weights\_hex.txt”.

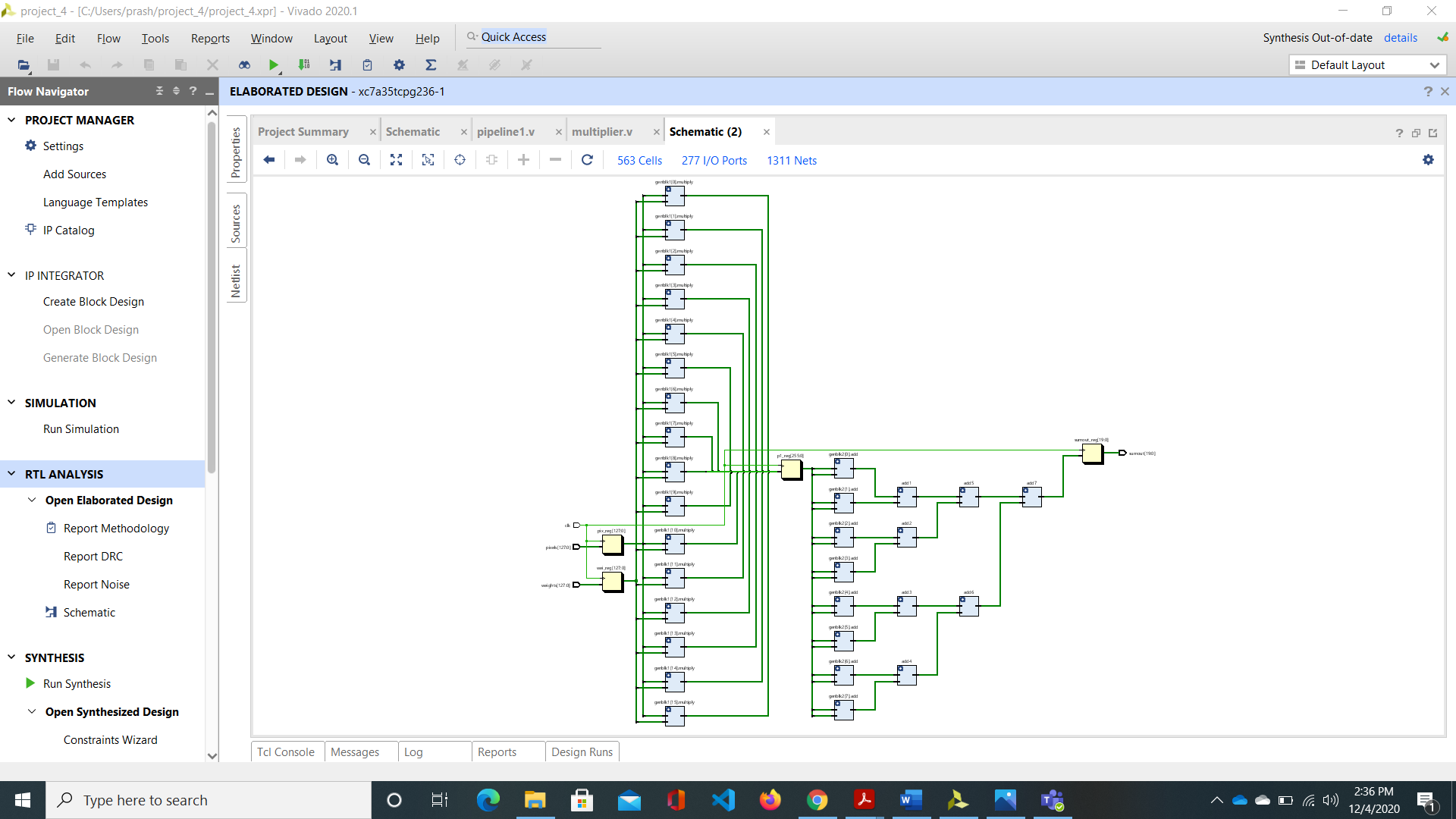
The delay of adder is about 2ns and and delay of multiplier is about 4ns.

Pipeline  
Register

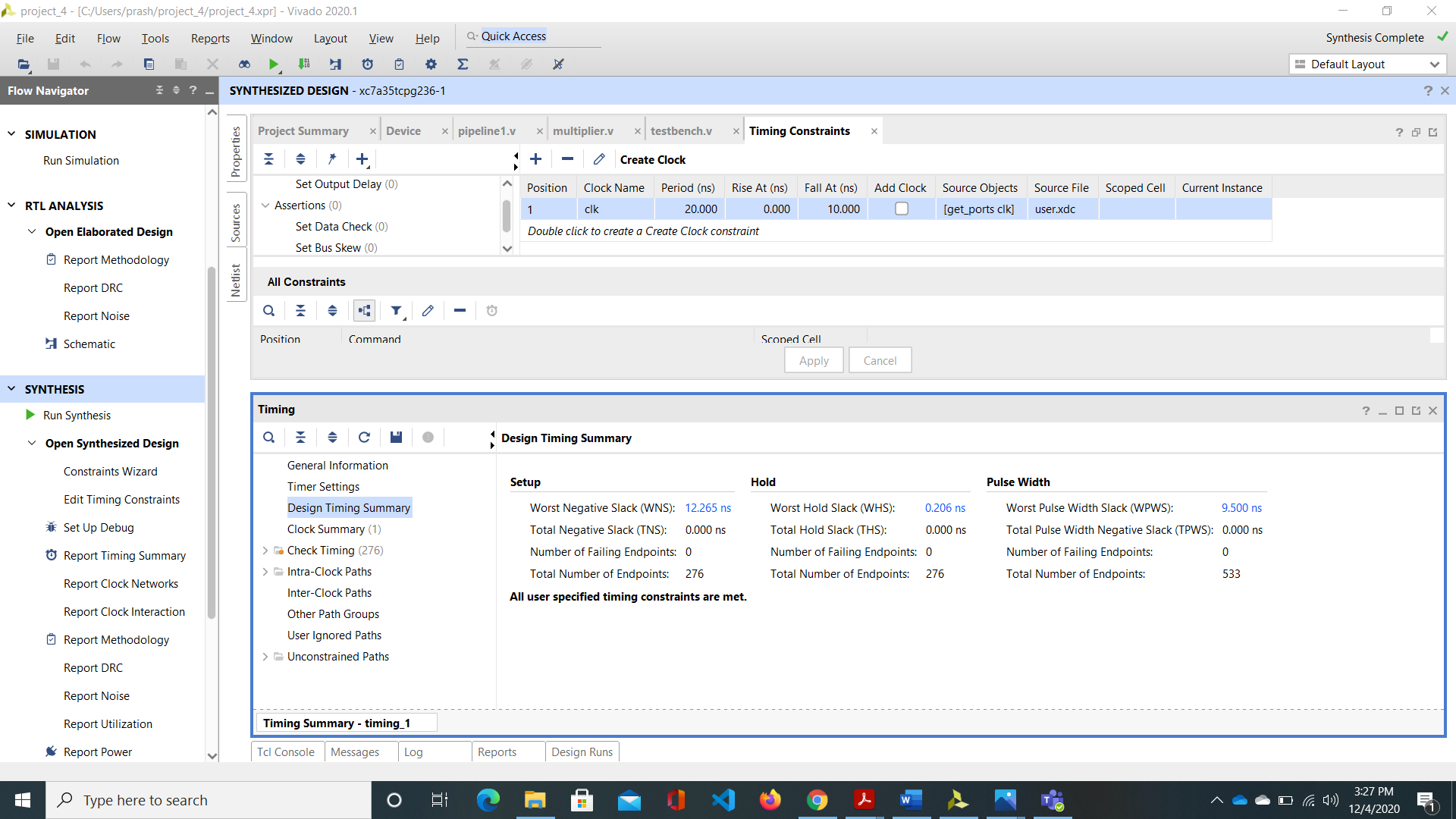
Pipeline  
Register

Pipeline  
Register

**The RTL schematic of MAC Module is**

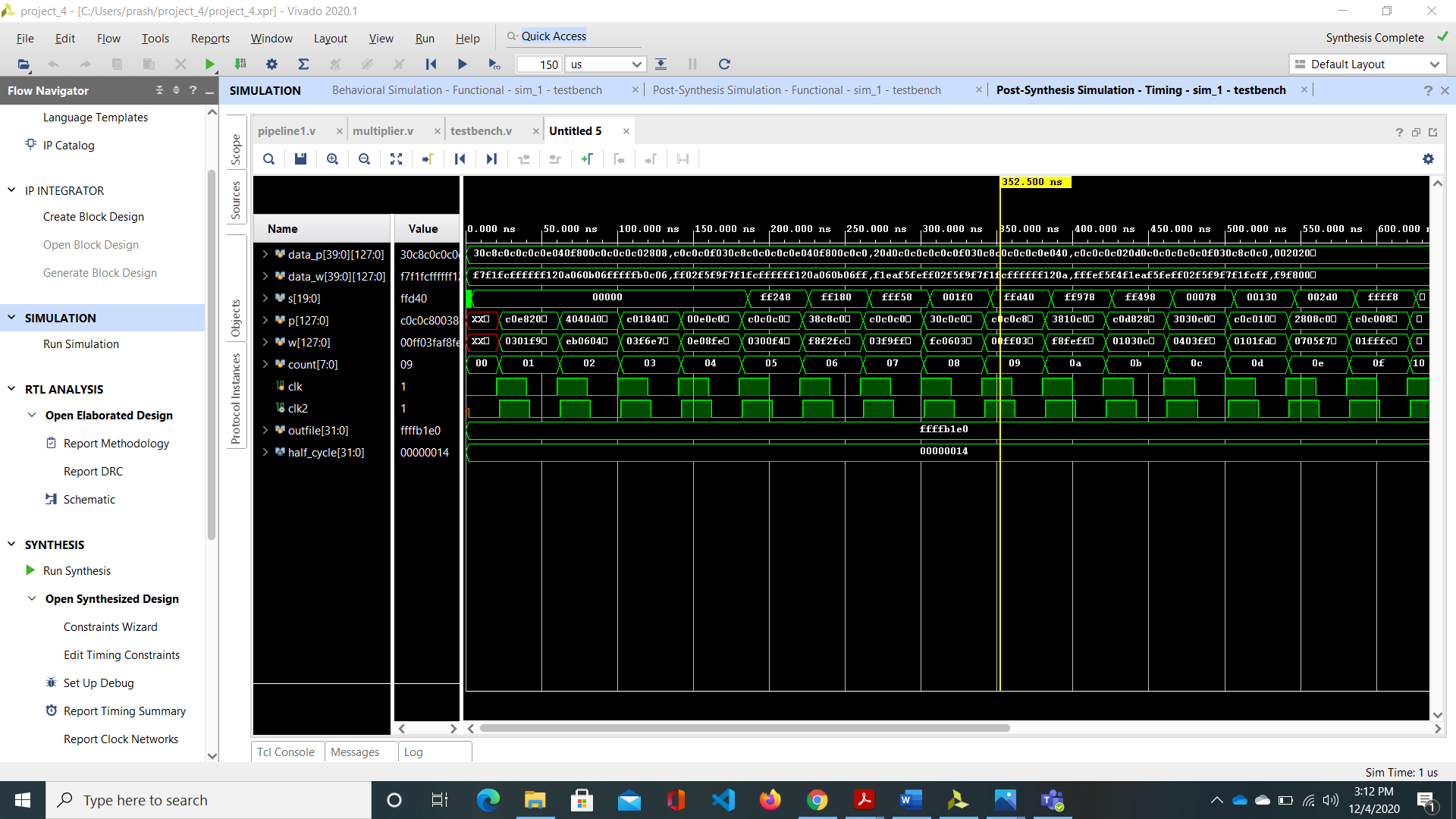


**Timing Report**

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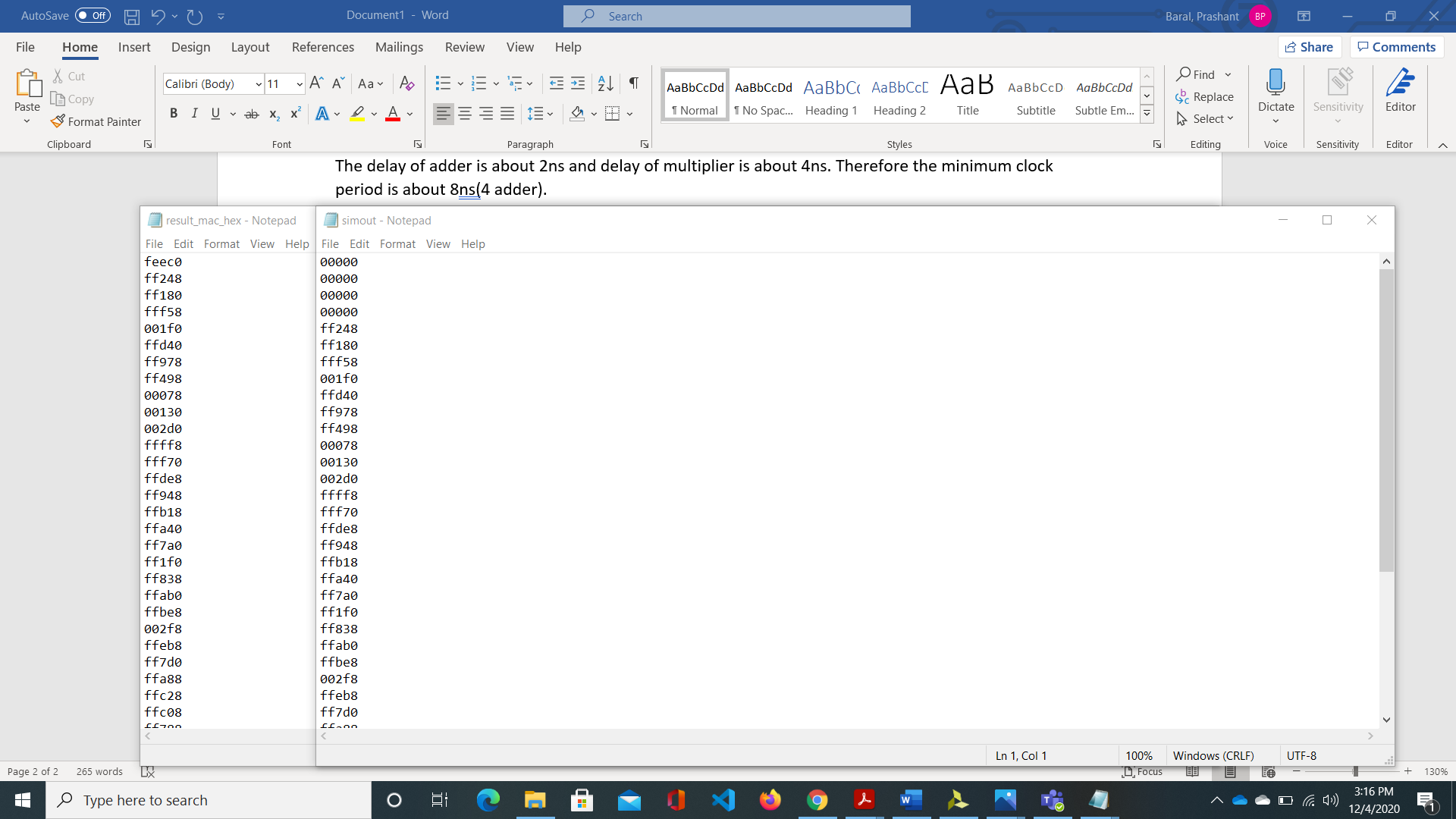
The delay of adder is about 2ns and delay of multiplier is about 4ns. Therefore the minimum clock period is about 8ns(4 adder).

**Post Synthesis Timing Simulation:**

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The output of MAC design

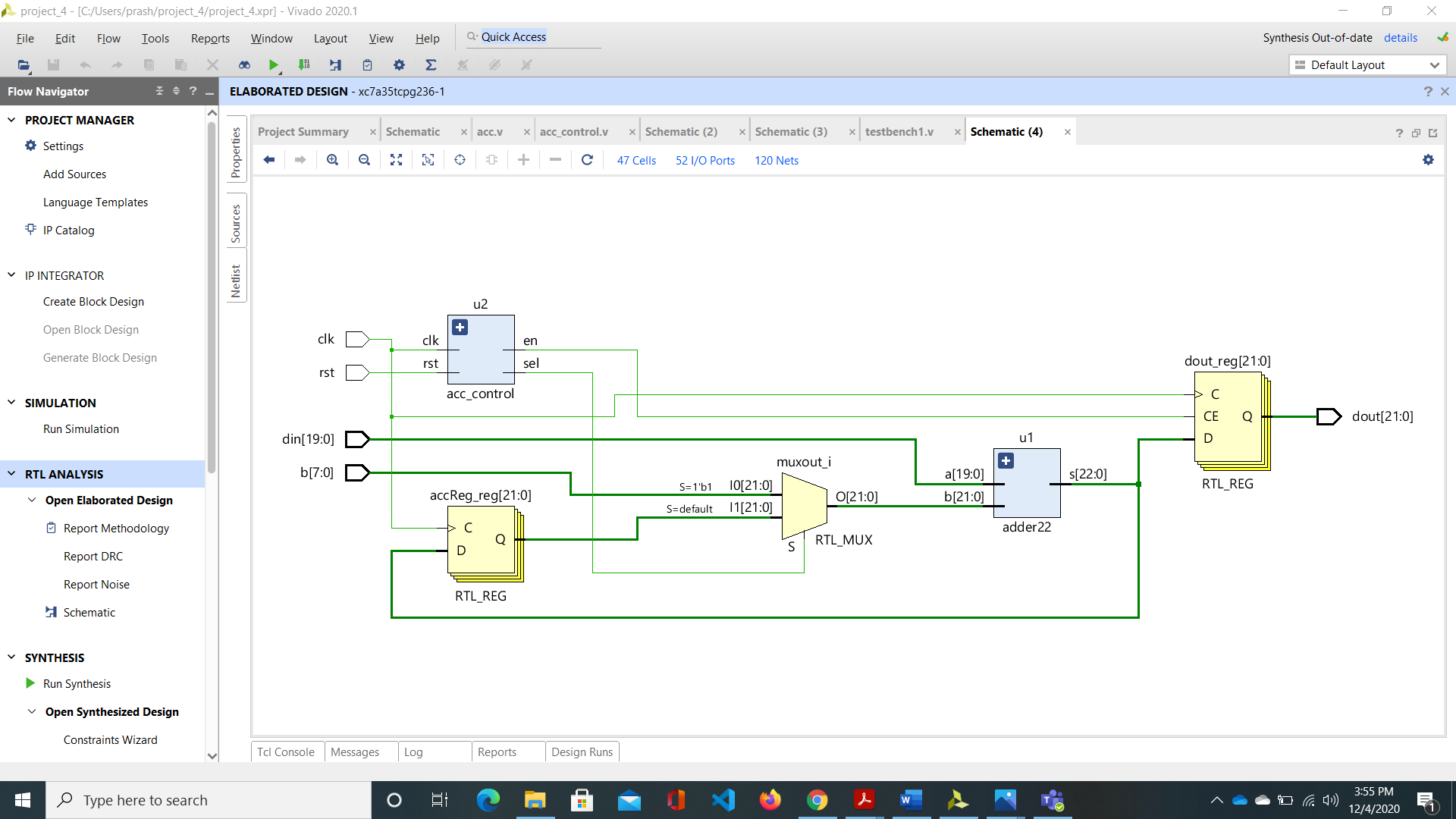
**Comparison of output obtained and expected output**

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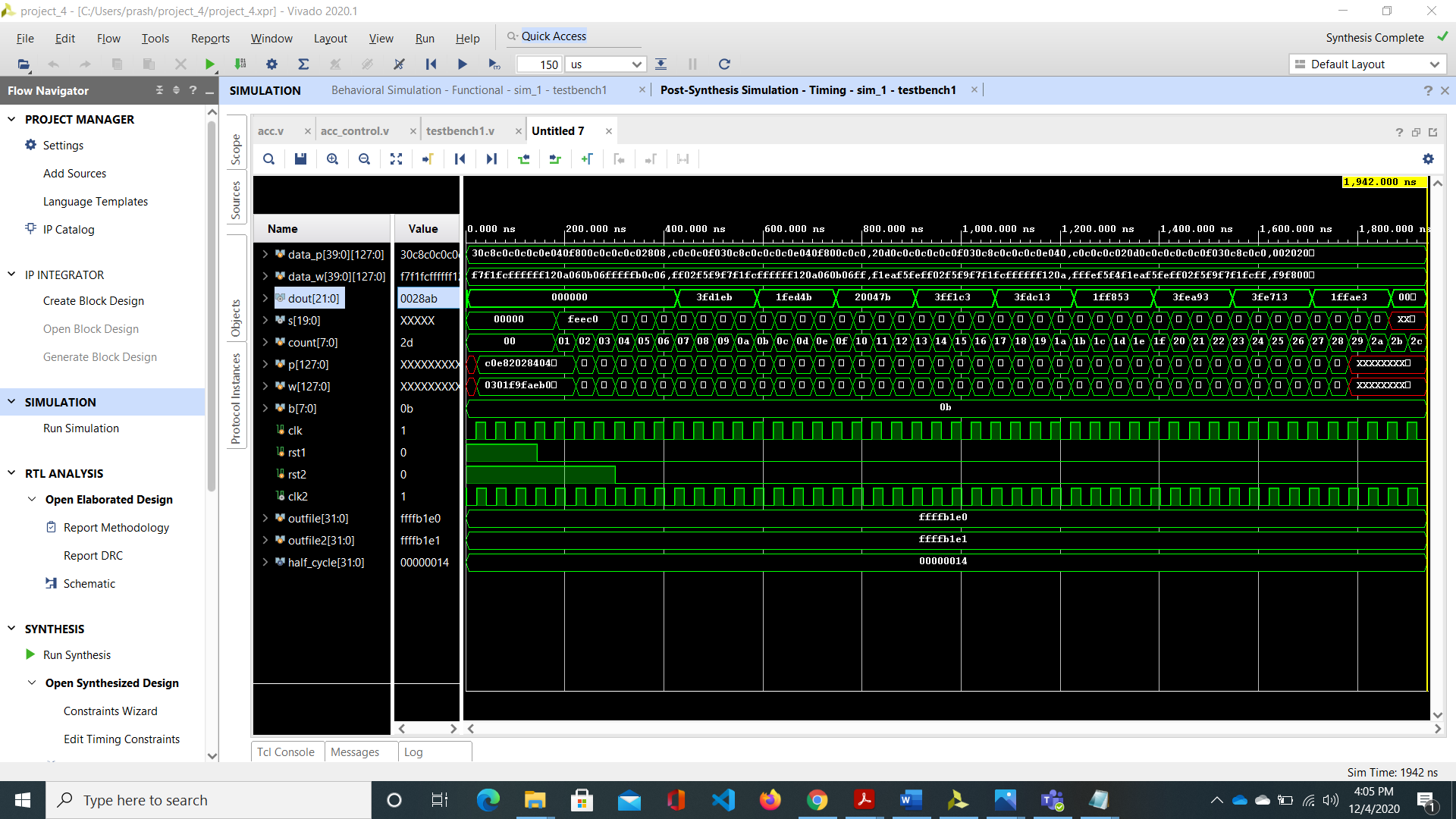
**Milestone 2: Accumulator (ACC) Module Design**

In milestone 1, MAC design performs weighted sum of 16-pixel values but we are using 8x8 bit for representing the image. Therefore, we accumulate the result four times. The result of MAC\_ACC is 22 bit.

**RTL Schematic**

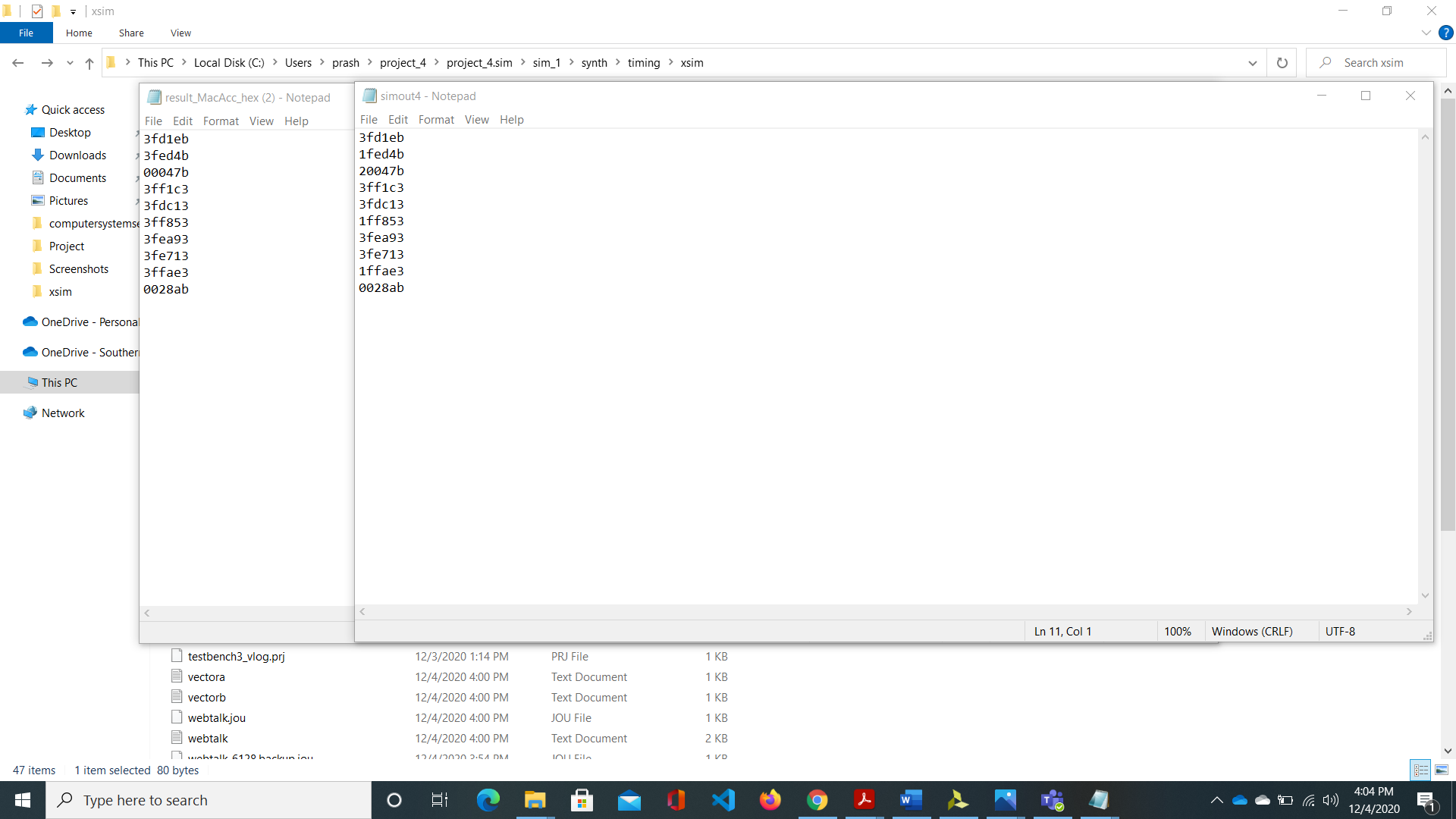
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THE RTL schematic shows the circuit designed for the implementation of function defined in earlier paragraph.

**Post Synthesis Timing Simulation:**

The output of MAC\_ACC design.

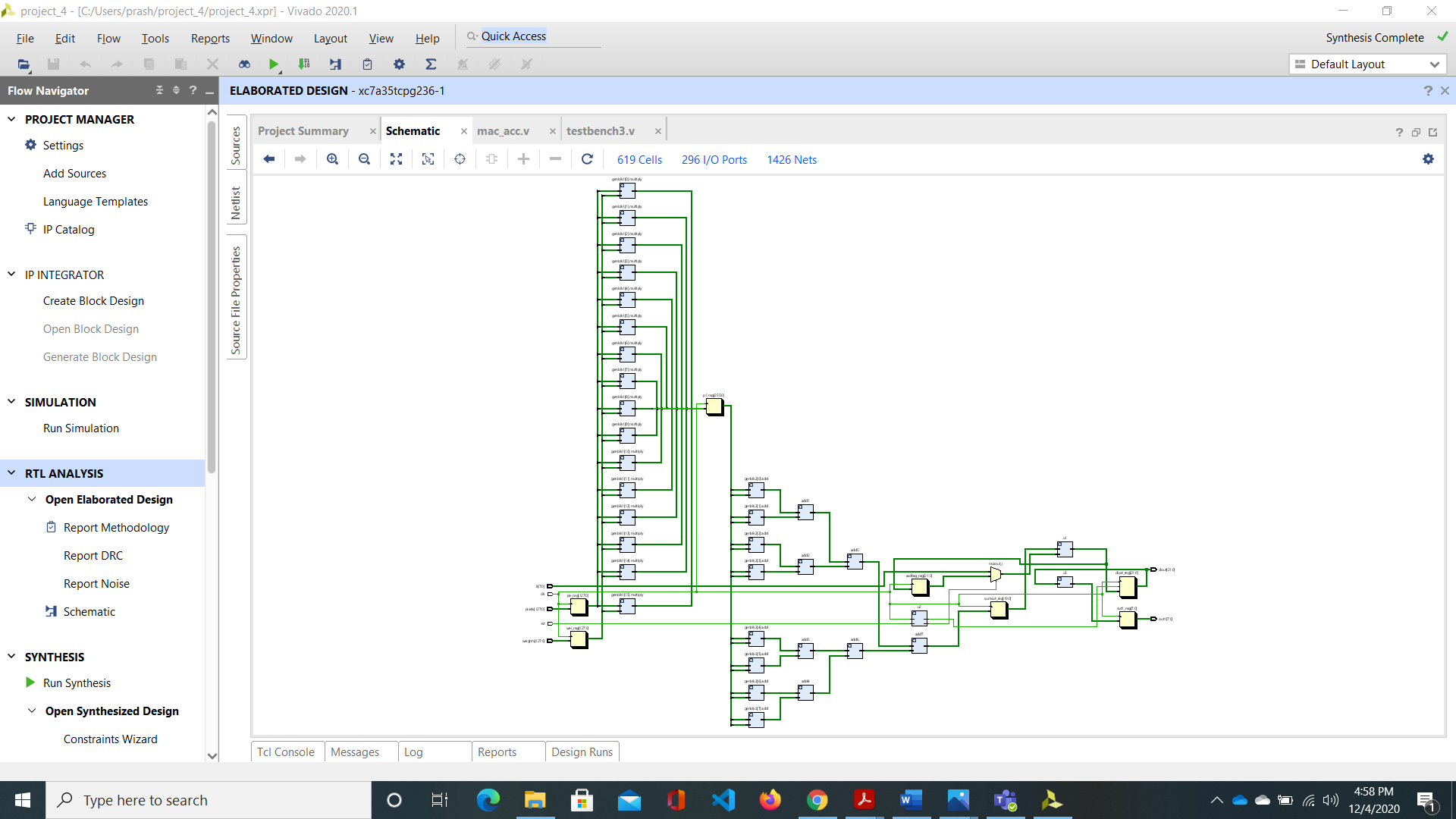
**Comparison of output obtained and expected output**



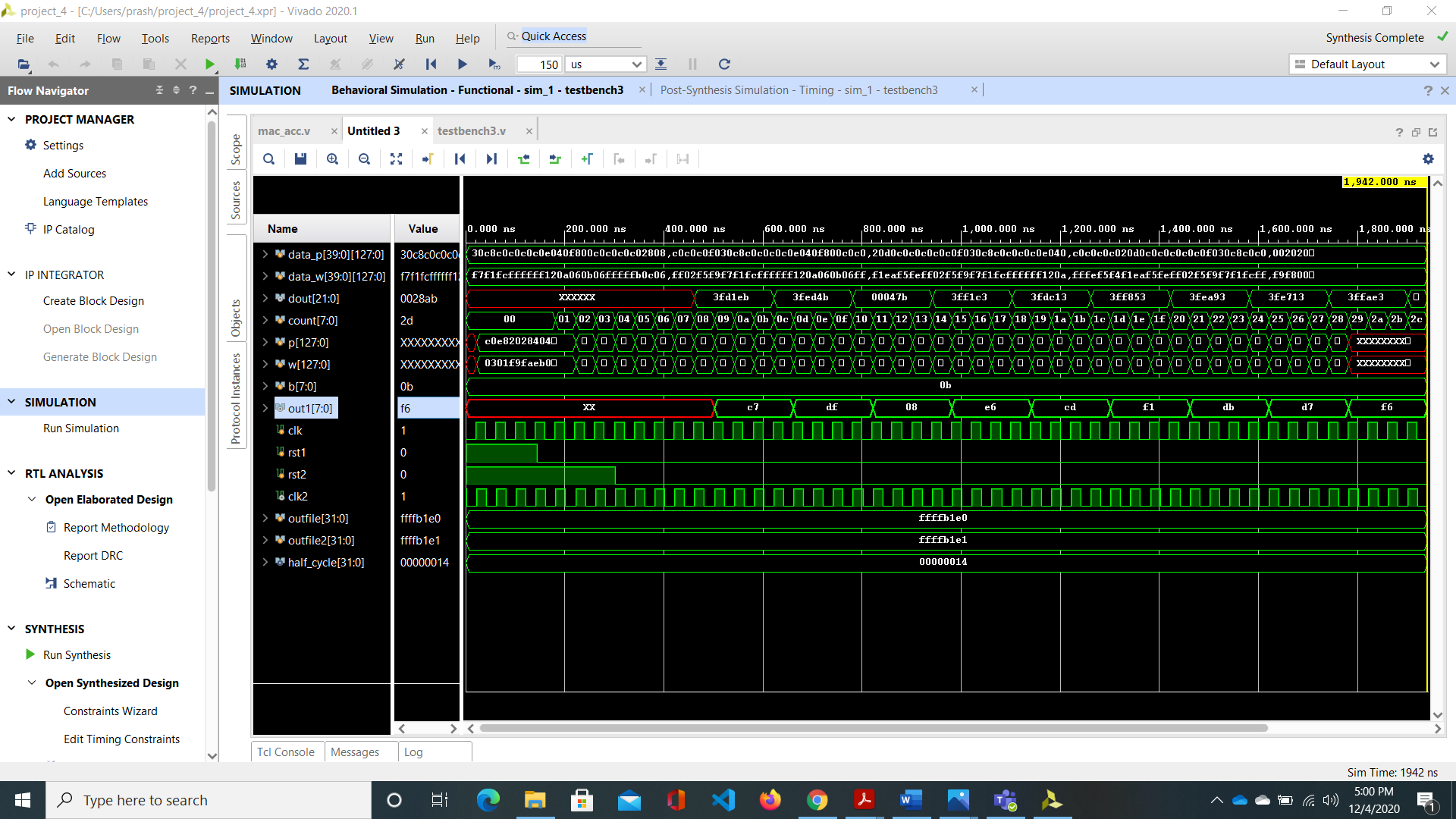
**Milestone 3: Integrating with sigmoid IP block**

In this part, we input 22-bit output of MAC\_ACC to IP wrapper which gives output bit sign, overflow and address of LUT. This LUT is designed such that the value in between -4 and 4 are fed to sigmoid LUT which return the specific output. If input to IP wrapper is greater than 4, the output of sigmoid is the maximum value (4.76) and least value (-4.76) when input to IP wrapper is less than -4.

**RTL Schematic**

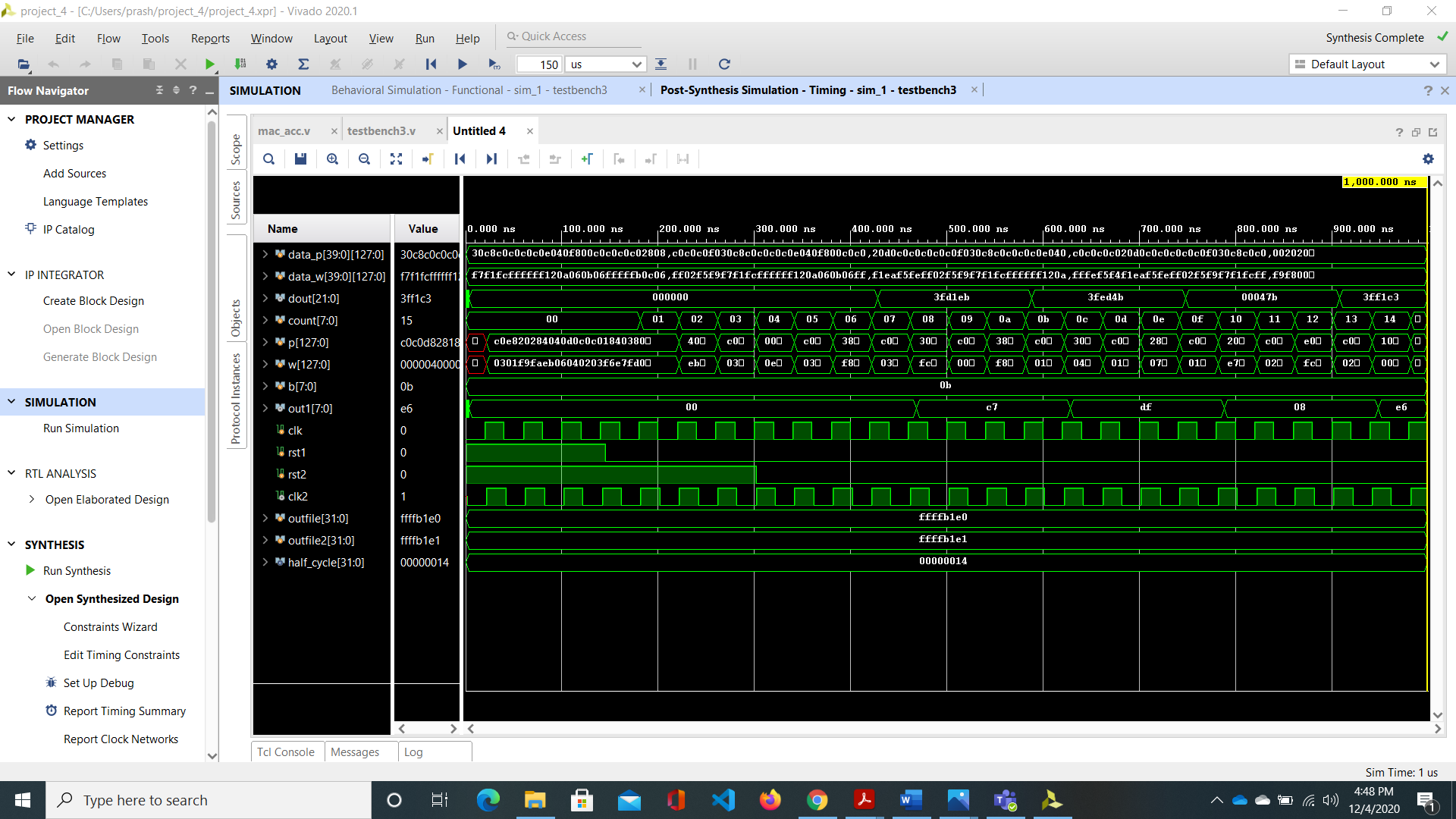
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**Behavioral Simulation**

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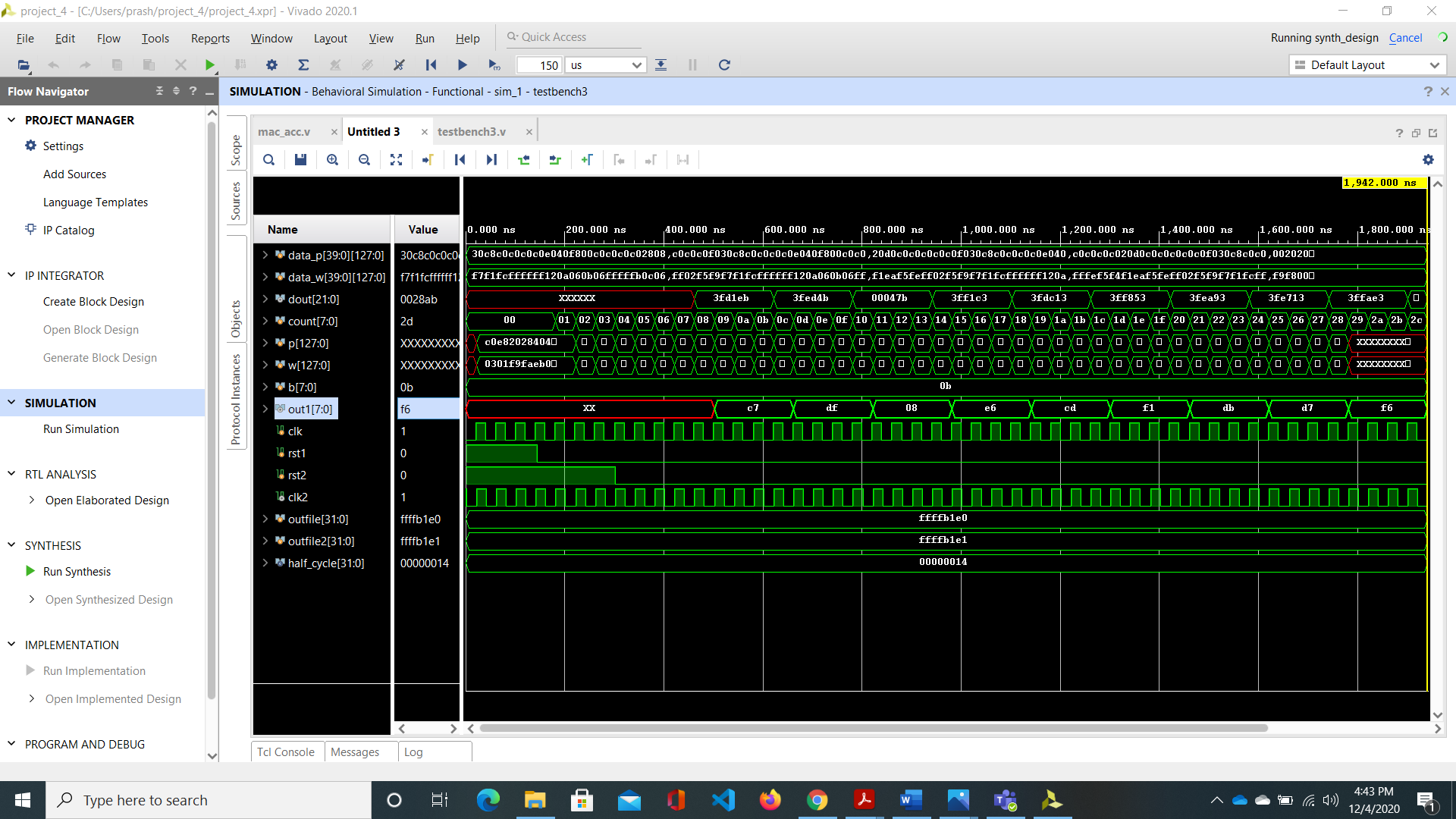
Output of sigmoid function

**Post Synthesis Timing Simulation:**

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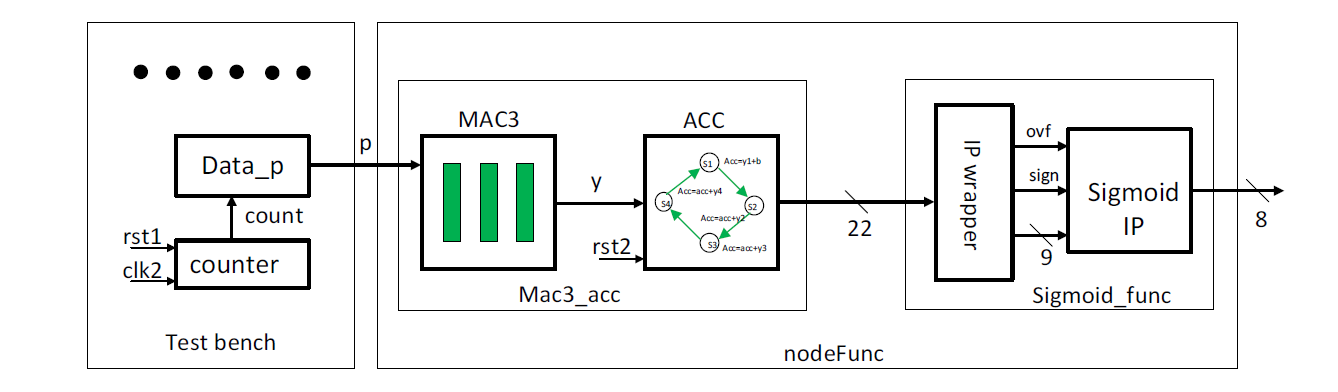
Sigmoid output

**Post Synthesis Functional Simulation:**

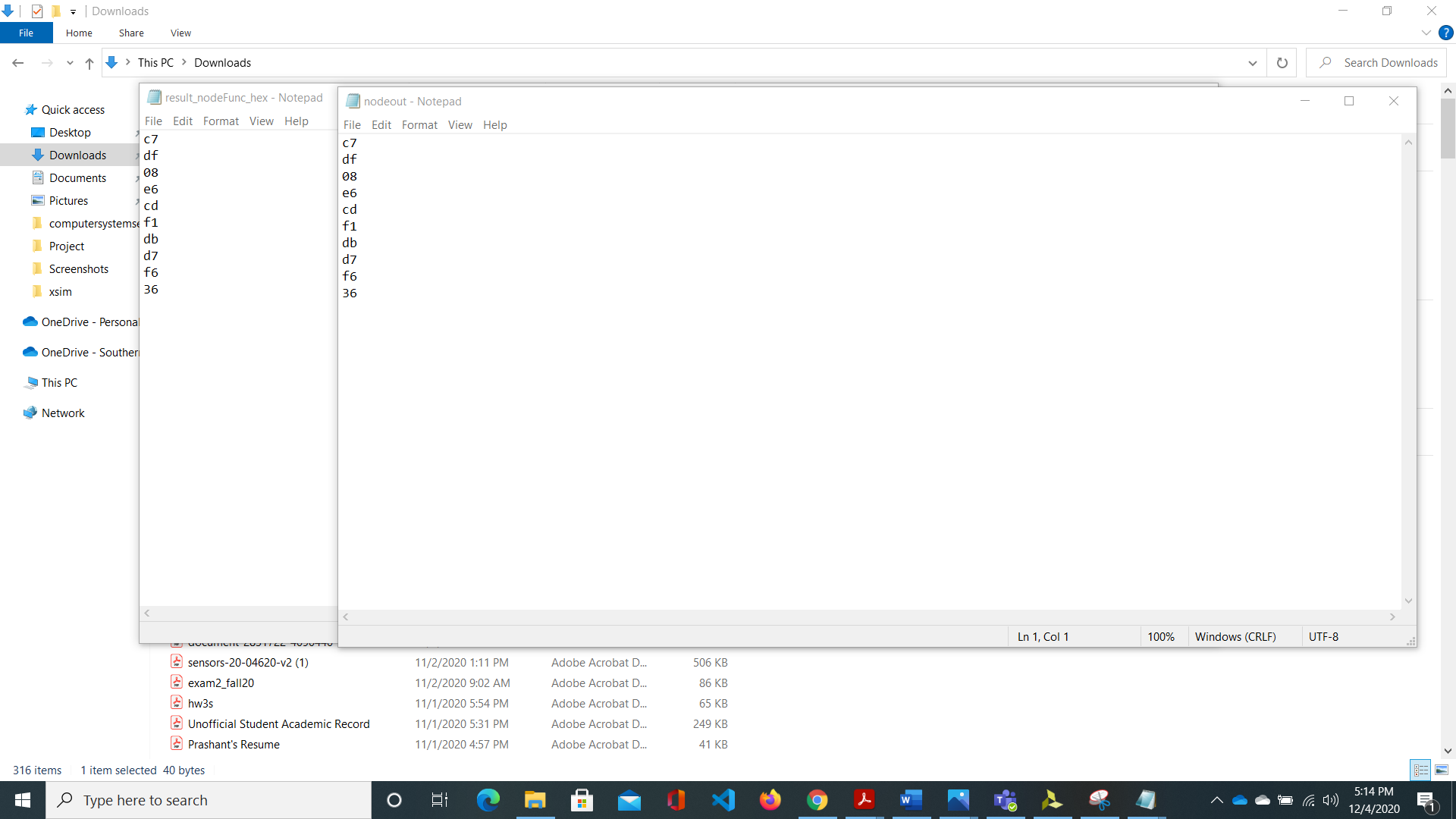
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Sigmoid output

**Diagram representing our implementation**



**Comparison of output obtained and expected output**

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**Design with considerations**

The products by engineers are widely used in modern societies and it affects both positively and negatively in different fields such as public health, safety, welfare, global, cultural, social, environmental factors etc. In our design, we implemented ANN to recognize the handwritten digits.

This design can be very beneficial to the one with impaired vision which contributes towards public health.

Similarly, the same design that we are implementing can be updated in the same FPGA chip by extending the functionalities in our design instead of using different hardware which contributes positively to environmental protection as we are using reusable chip. Instead if we were specific function in specified hardware, for the update we would require the new hardware and we would likely dump it in environment which would help towards environmental degradation.

The design also contributes economically as it is reusable for implementing other functions.