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# A Hardware-aware Heuristic for the Qubit Mapping Problem in the NISQ Era

Siyuan Niu<sup>1</sup>, Adrien Suau<sup>1,2</sup>, Gabriel Staffelbach<sup>2</sup>, and Aida Todri-Sanial<sup>1</sup>

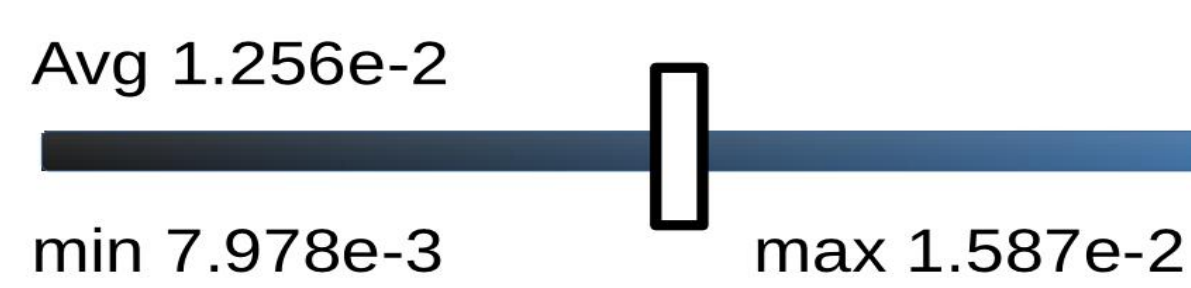
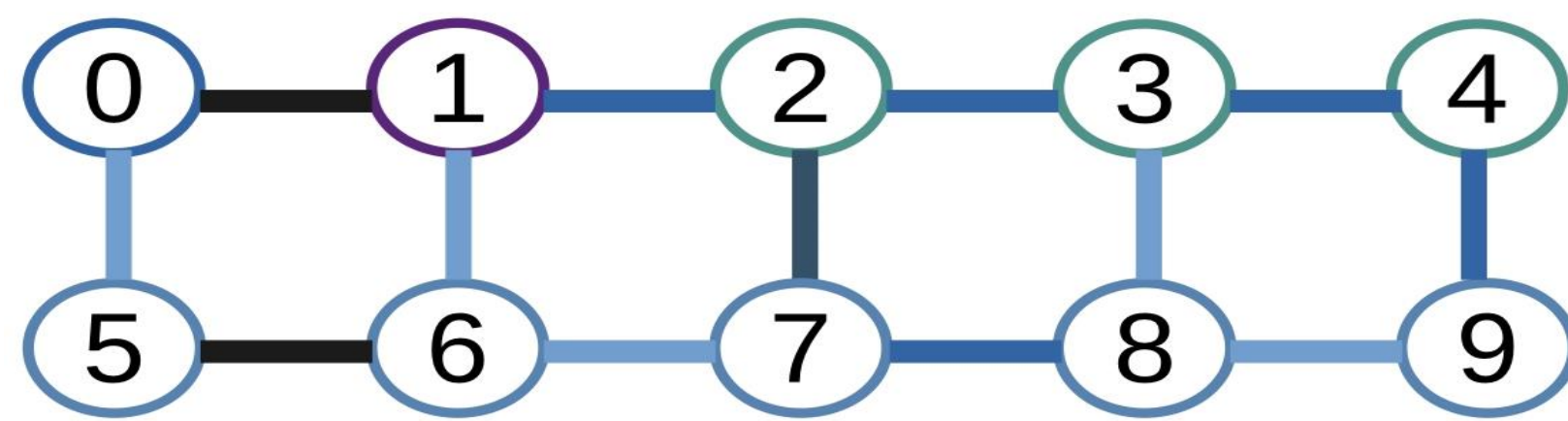
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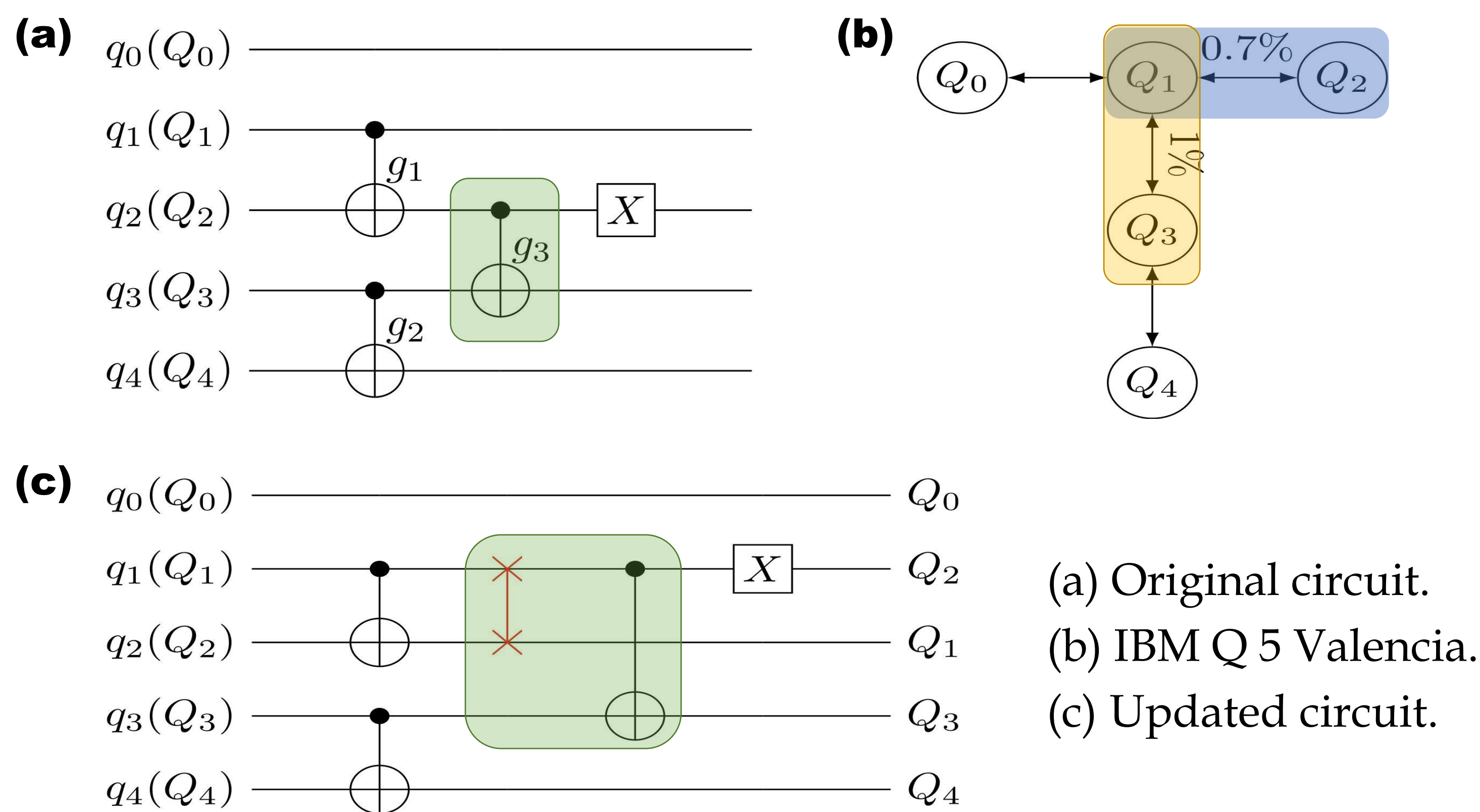


## Introduction



- NISQ devices.
- Connectivity constraint: Nearest-neighbor connections.
- Different physical qubits: various calibration data.
- Qubit mapping problem: Adapting a quantum program to given hardware connectivity.

## Motivation



- Initial mapping
  - $\{q_0 \rightarrow Q_0, q_1 \rightarrow Q_1, q_2 \rightarrow Q_2, q_3 \rightarrow Q_3, q_4 \rightarrow Q_4\}$
- SWAP candidates:
  - $\{q_1, q_2\}$  and  $\{q_1, q_3\}$
- Choose  $\{q_1, q_2\}$  because of the lower error rate.
- Final mapping
  - $\{q_0 \rightarrow Q_0, q_1 \rightarrow Q_2, q_2 \rightarrow Q_1, q_3 \rightarrow Q_3, q_4 \rightarrow Q_4\}$

## Methods

- Hardware-Aware (HA) mapping transition algorithm.
- Cost function

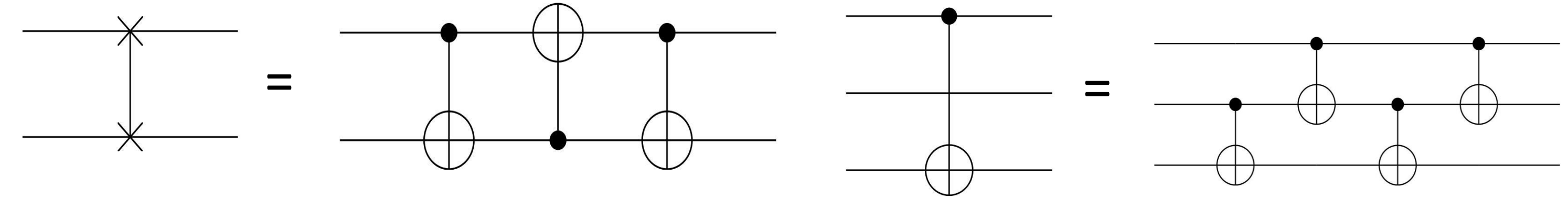
$$H = \frac{1}{|F|} \sum_{g \in F} D[\pi(g, q_1)][\pi(g, q_2)] + W \times \frac{1}{|E|} \sum_{g \in E} D[\pi(g, q_1)][\pi(g, q_2)]$$

- Distance matrix

$$D = \alpha_1 \times S + \alpha_2 \times \varepsilon + \alpha_3 \times T$$

- $S$ : SWAP matrix,  $\varepsilon$ : SWAP error matrix,  $T$ : SWAP execution time matrix

- Selection between SWAP and Bridge gate.



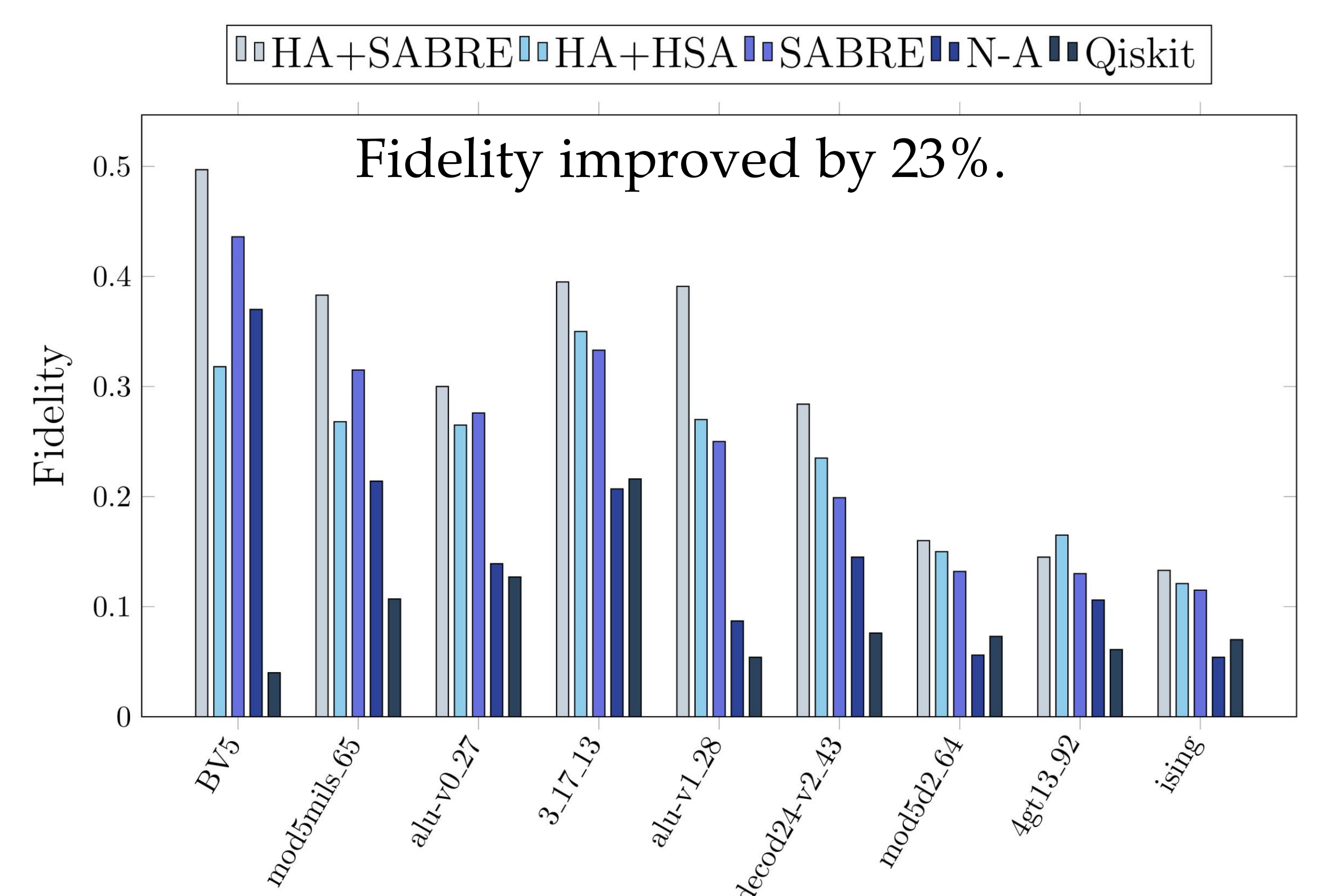
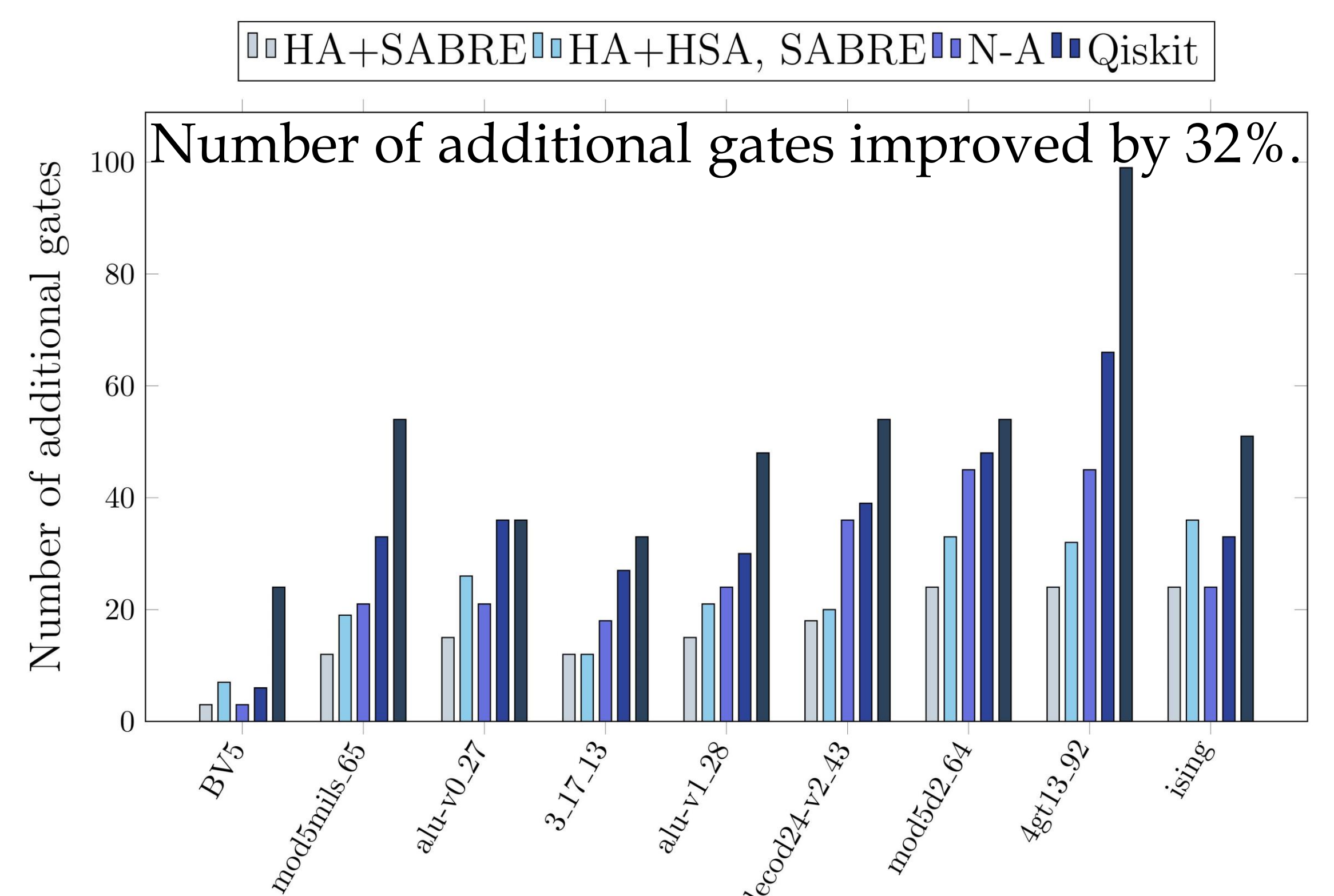
**SWAP gate**

**Bridge gate**

- Hardware-aware Simulated Annealing (HSA) initial mapping.
- Hardware-aware `get_neighbor` method.

## Results

- Comparison of number of additional gates and fidelity on IBM Q 20 Almaden.



## Conclusion

- Map the most used qubit of the mapped circuit to the most connected physical qubit.
- Apply CNOT gates on qubits that are directly connected and with reliable interconnects.
- If a CNOT cannot be applied on two neighbor qubits, apply on two qubits whose distance is two.

