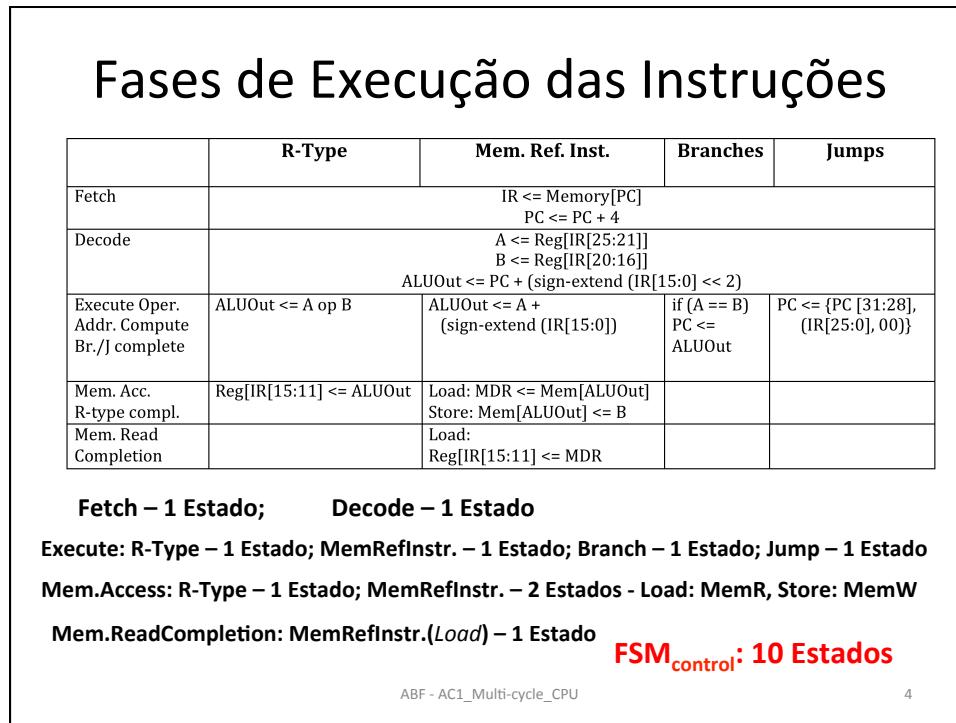
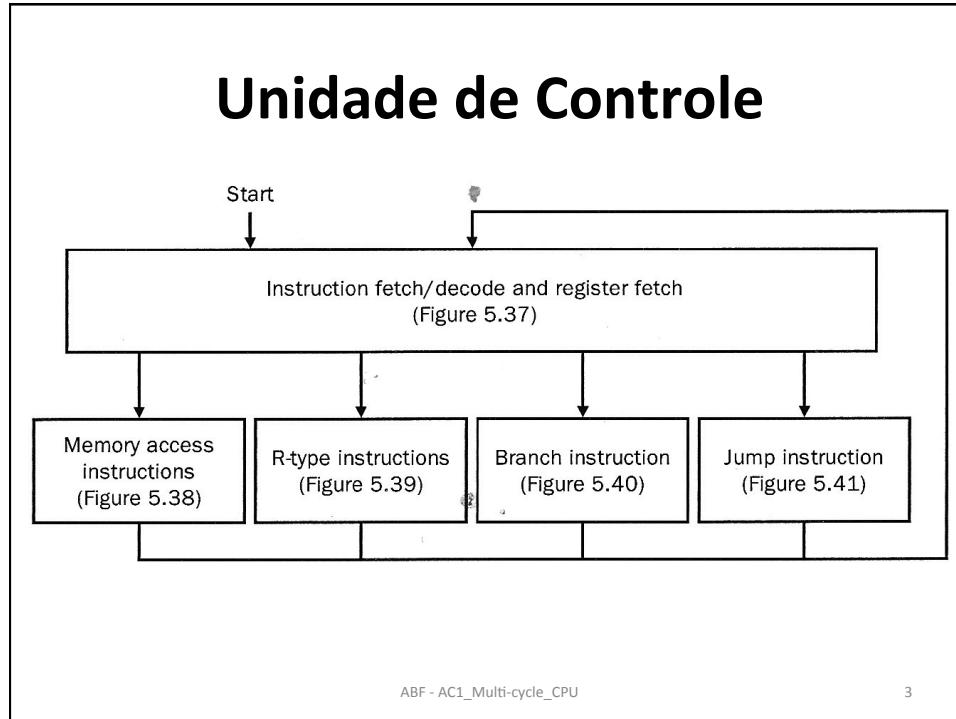


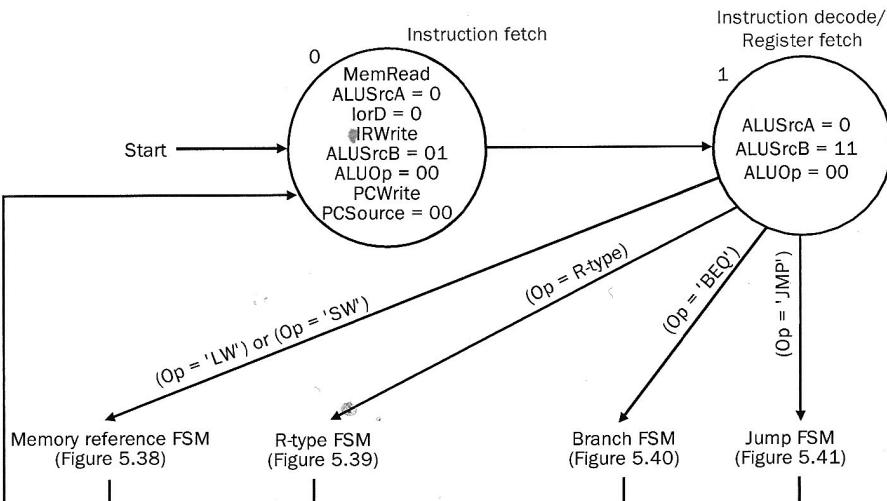
2. Multi Cycle: Control

Unidade de Controle

- Single-Cycle: circuito combinatório
- Multi-Cycle: Máquina de Estados (FSM)
 - **Ciclo corresponde a tantos Estados quantas as diferenças das operações a executar para cada categoria de instruções**
 - Em cada estado a unidade de controle gera os sinais que controlam as operações do datapath a executar nesse estado



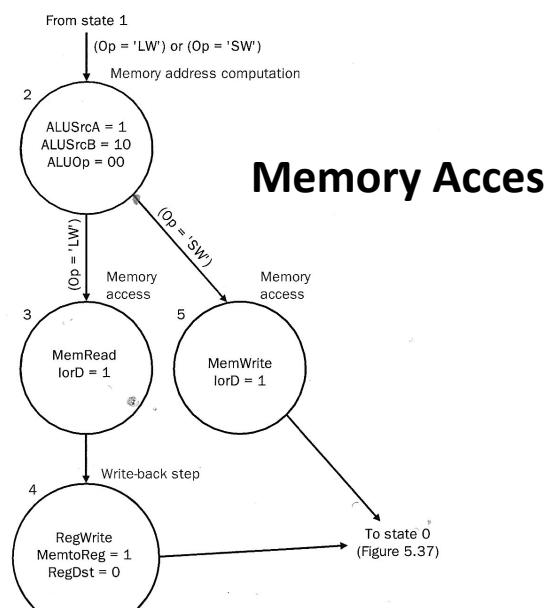
Estados *Fetch (0)* e *Decode/Reg.Read (1)*



ABF - AC1_Multi-cycle_CPU

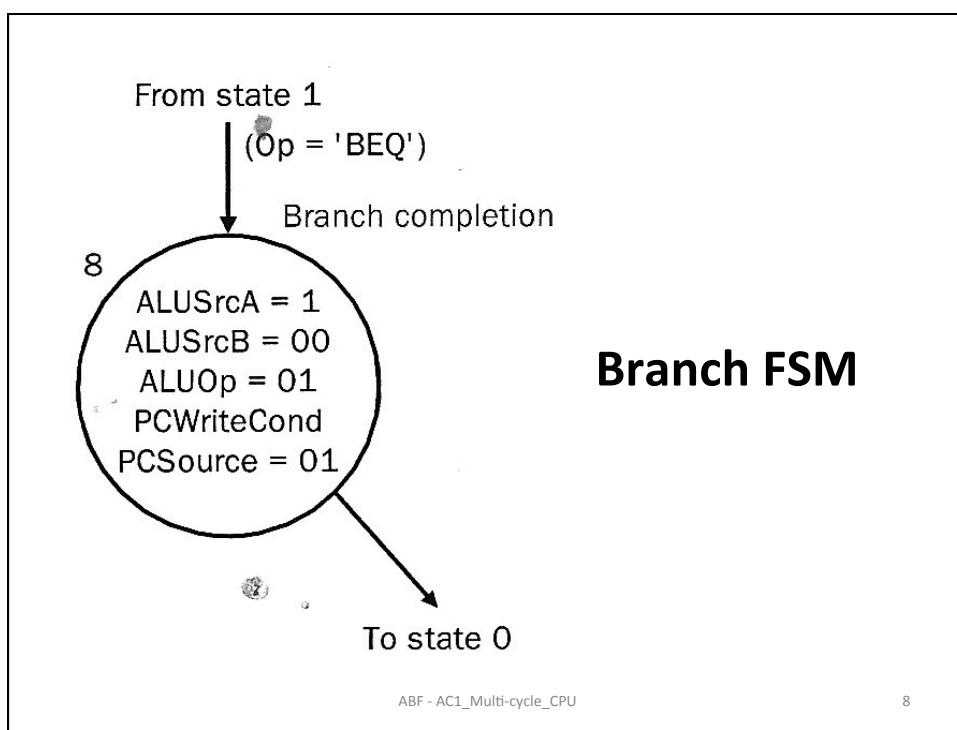
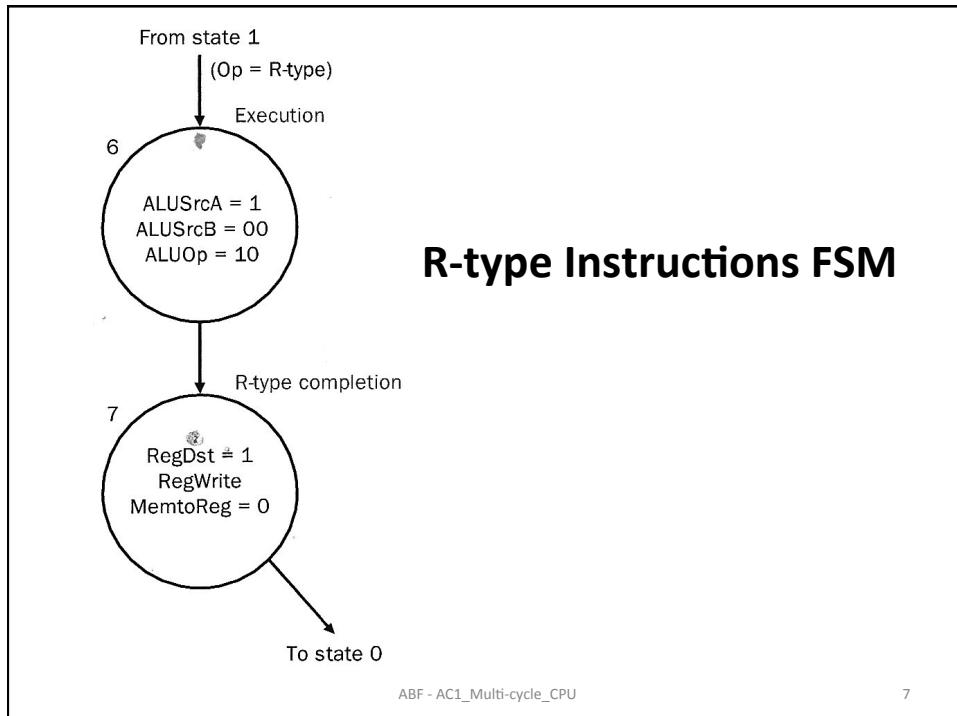
5

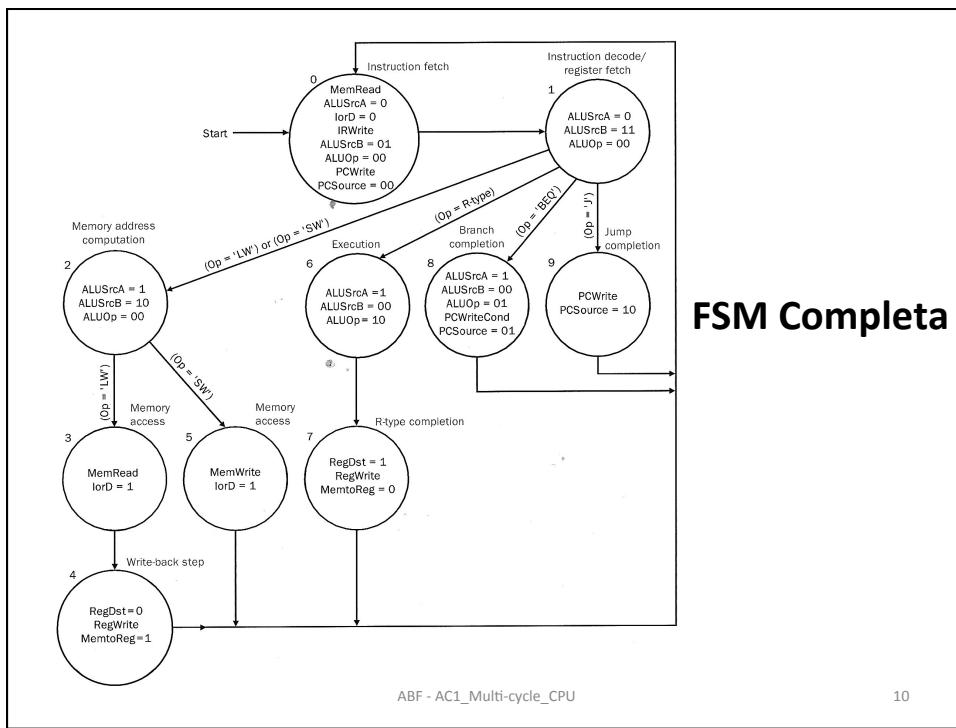
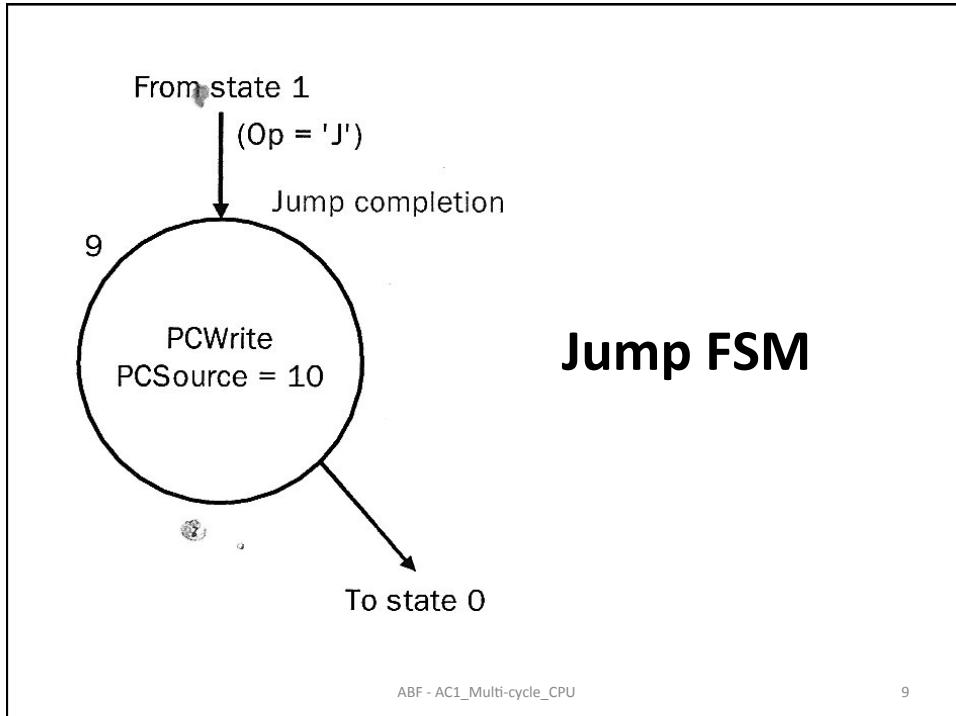
Memory Access Instructions FSM

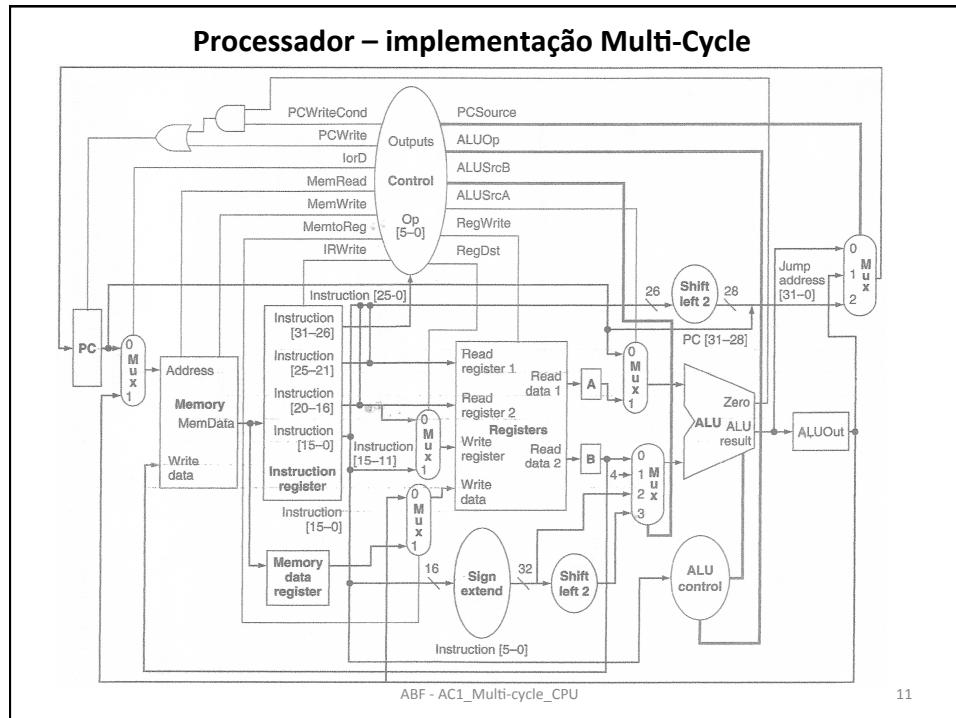


ABF - AC1_Multi-cycle_CPU

6







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3. Síntese da Unidade de Controle (FSM)

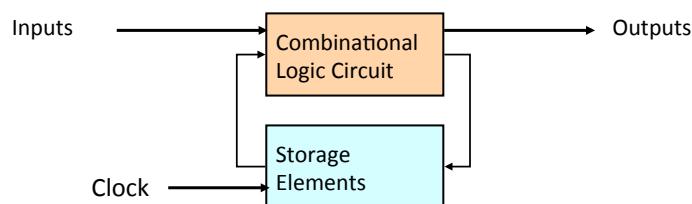
Modelo de uma FSM Síncrona

Círcuito Combinatório

Determina a saída e o estado seguinte

Elementos de Memória

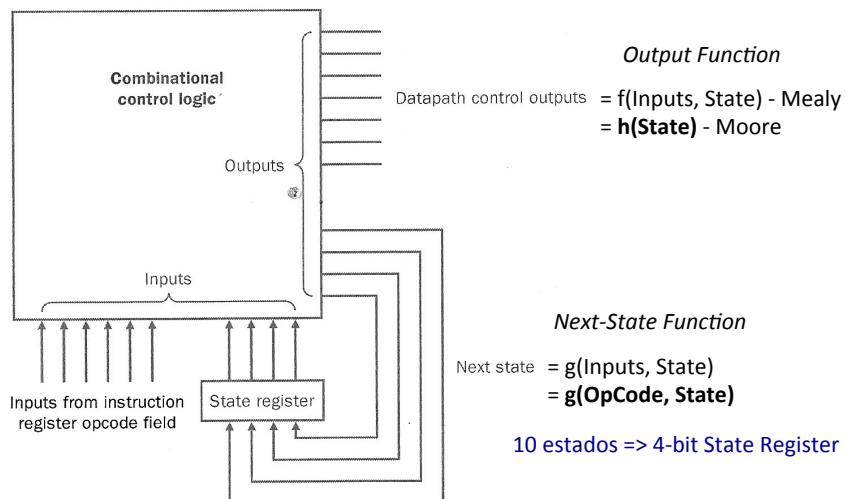
Representam o estado



ABF - IAC_Digital Logic

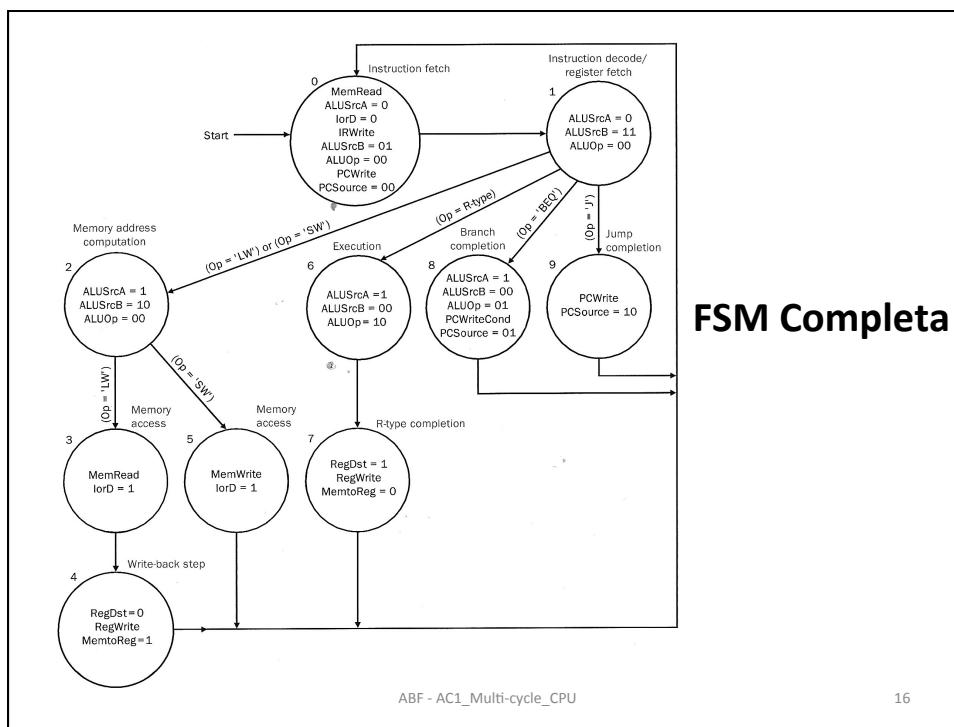
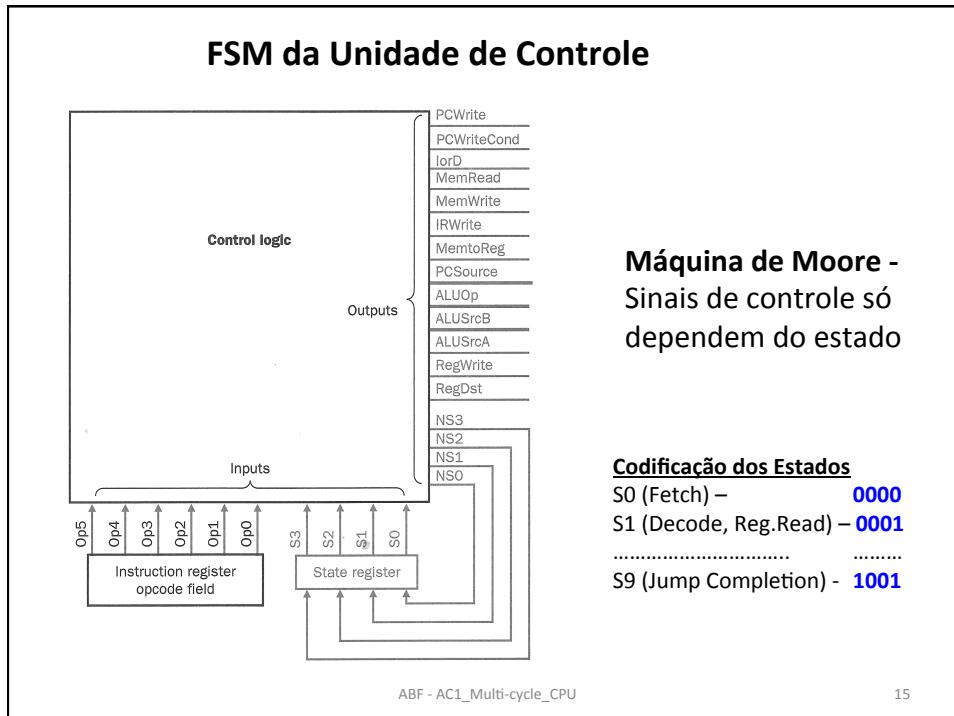
13

FSM –esquema geral



ABF - AC1_Multi-cycle_CPU

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Output	Current states	Op
PCWrite	state0 + state9	
PCWriteCond	state8	
IorD	state3 + state5	
MemRead	state0 + state3	
MemWrite	state5	
IRWrite	state0	
MemtoReg	state4	
PCSource1	state9	
PCSource0	state8	
ALUOp1	state6	
ALUOp0	state8	
ALUSrcB1	state1 + state2	
ALUSrcB0	state0 + state1	
ALUSrcA	state2 + state6 + state8	
RegWrite	state4 + state7	
RegDst	state7	
NextState0	state4 + state5 + state7 + state8 + state9	
NextState1	state0	
NextState2	state1	(Op = 'lw') + (Op = 'sw')
NextState3	state2	(Op = 'lw')
NextState4	state3	
NextState5	state2	(Op = 'sw')
NextState6	state1	(Op = 'R-type')
NextState7	state6	
NextState8	state1	(Op = 'beq')
NextState9	state1	(Op = 'jmp')

ABF - AC1_Multi-cycle_CPU

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Unidade de Control – Output Function

Outputs	Input values (S[3-0])									
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
PCWrite	1	0	0	0	0	0	0	0	0	1
PCWriteCond	0	0	0	0	0	0	0	0	1	0
IorD	0	0	0	1	0	1	0	0	0	0
MemRead	1	0	0	1	0	0	0	0	0	0
MemWrite	0	0	0	0	0	1	0	0	0	0
IRWrite	1	0	0	0	0	0	0	0	0	0
MemtoReg	0	0	0	0	1	0	0	0	0	0
PCSource1	0	0	0	0	0	0	0	0	0	1
PCSource0	0	0	0	0	0	0	0	0	1	0
ALUOp1	0	0	0	0	0	0	1	0	0	0
ALUOp0	0	0	0	0	0	0	0	0	1	0
ALUSrcB1	0	1	1	0	0	0	0	0	0	0
ALUSrcB0	1	1	0	0	0	0	0	0	0	0
ALUSrcA	0	0	1	0	0	0	1	0	1	0
RegWrite	0	0	0	0	1	0	0	1	0	0
RegDst	0	0	0	0	0	0	0	1	0	0

ABF - AC1_Multi-cycle_CPU

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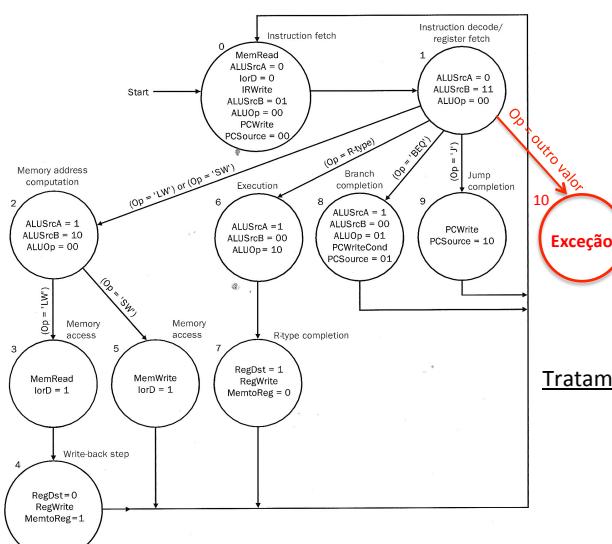
Unidade de Control – Next State Function

Op[5-0]						
Estado atual	Tipo R 000000	Jmp 00010	Beq 000100	Lw 100011	Sw 101011	Outro valor
0000	0001	0001	0001	0001	0001	0001
0001	0110	1001	1000	0010	0010	Inst.illegal
0010				0011	0101	Inst.illegal
0011				0100		Inst.illegal
0100				0000		Inst.illegal
0101					0000	Inst.illegal
0110	0111					Inst.illegal
0111	0000					Inst.illegal
1000			0000			Inst.illegal
1001		0000				Inst.illegal

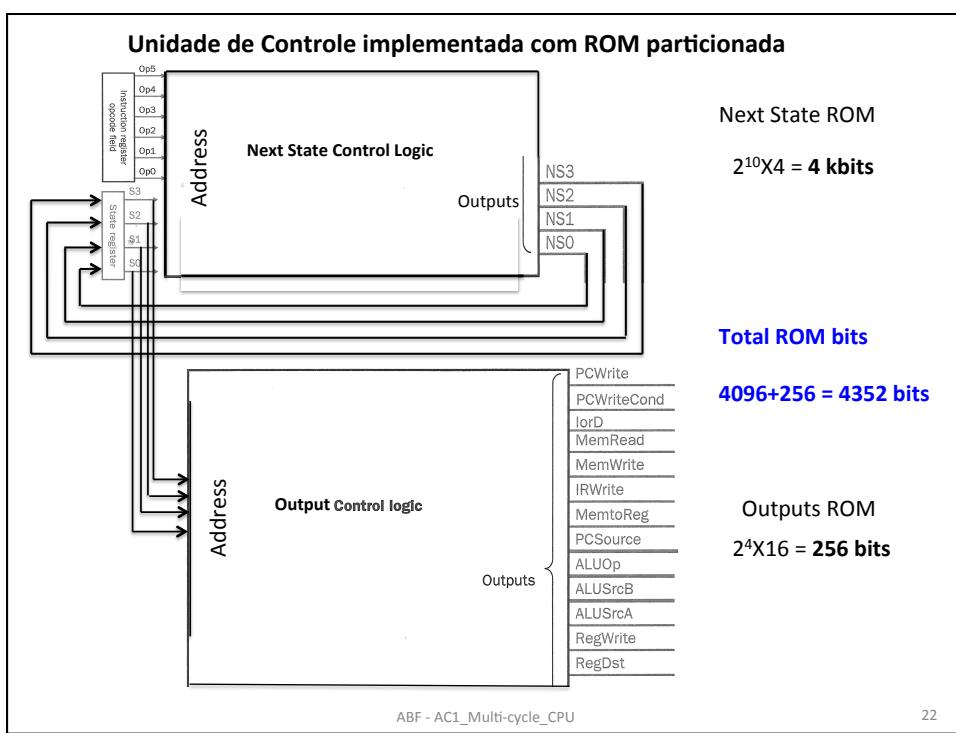
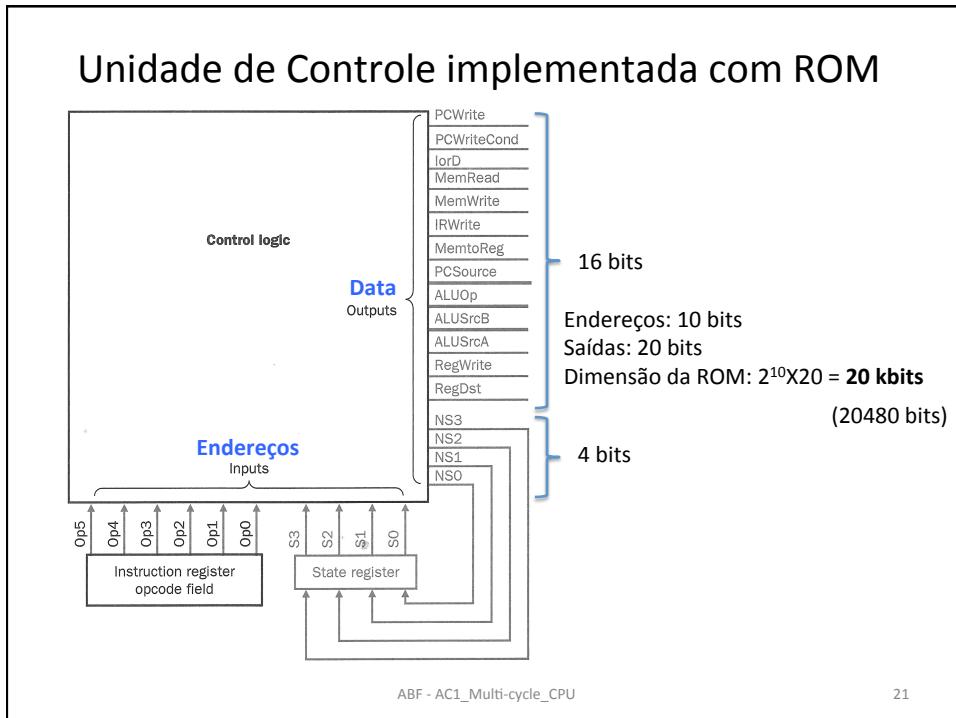
Células vazias correspondem a combinações (Estado, OpCode) impossíveis

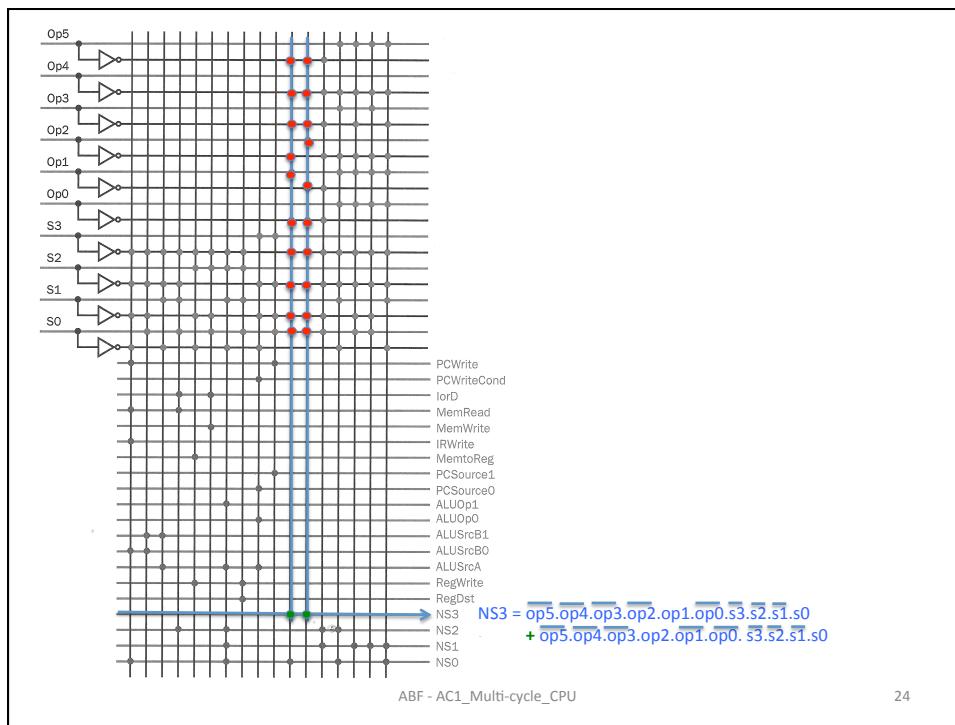
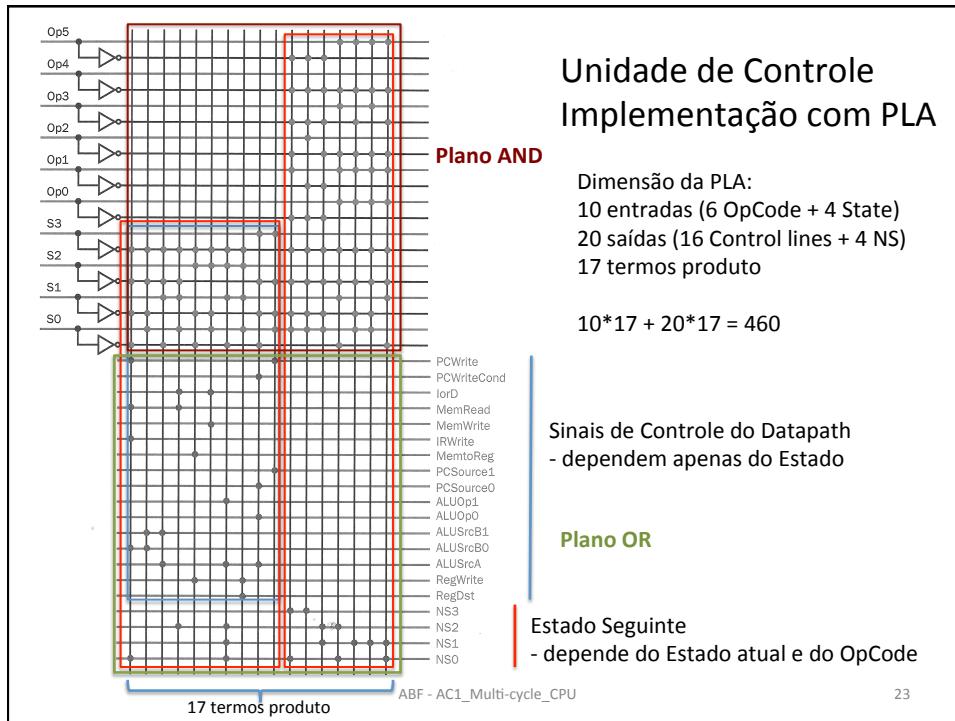
- podem ser consideradas “don’t cares”
- “Instrução ilegal” –

Exceção “Instrução ilegal”



Tratamento de Exceções em AC 2





Microprogramação

- Implementação alternativa: **unidade de controle microprogramada**
- Ideia-base: numa implementação multi-ciclo em cada ciclo de execução de uma instrução o datapath executa um conjunto de operações determinado pelos valores dos sinais de controle nesse ciclo – o conjunto dos valores dos sinais de controle nesse ciclo é uma **(micro)instrução** que o datapath executa
- A execução de uma instrução corresponde à execução de uma sequência de microinstruções (uma por cada ciclo de relógio), i.e. à execução de um **(micro)programa**