

MOS transistors (II)

- Poll for previous lecture speed
- Quiz on previous lecture material
- Blackboard preview for this week's material
- Review **Subthreshold (weak inversion)**
- Look at real subthreshold data
- **Superthreshold (above threshold, strong inversion)**
operation in triode and saturation region, overdrive voltage, velocity saturation
- The specific current I_s (the current at threshold)
- **Drain conductance (the Early effect)**
- 2nd-order drain effects: ***drain induced barrier lowering (DIBL), impact ionization***
- The intrinsic voltage gain of a transistor

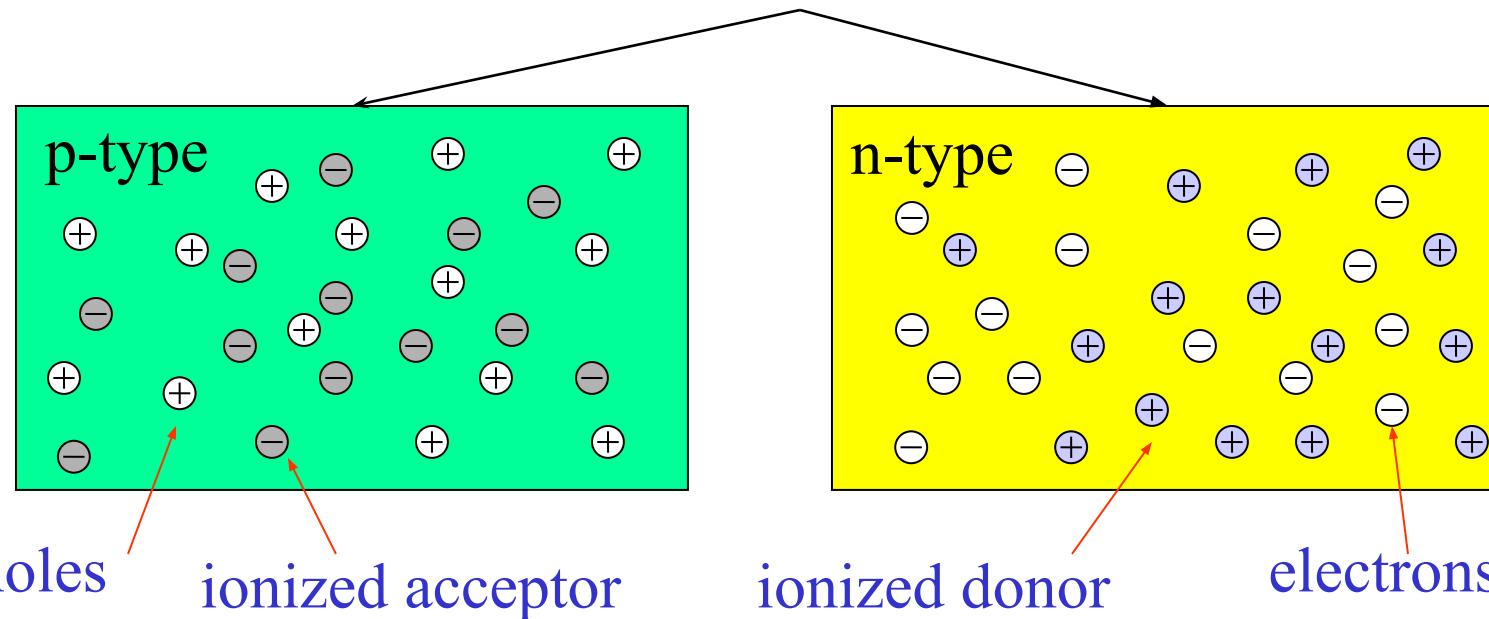
Blackboard preview about superthreshold operation

Reminder about OLAT forum for questions about lecture and exercises

Review on Semiconductors

Intrinsic silicon is undoped

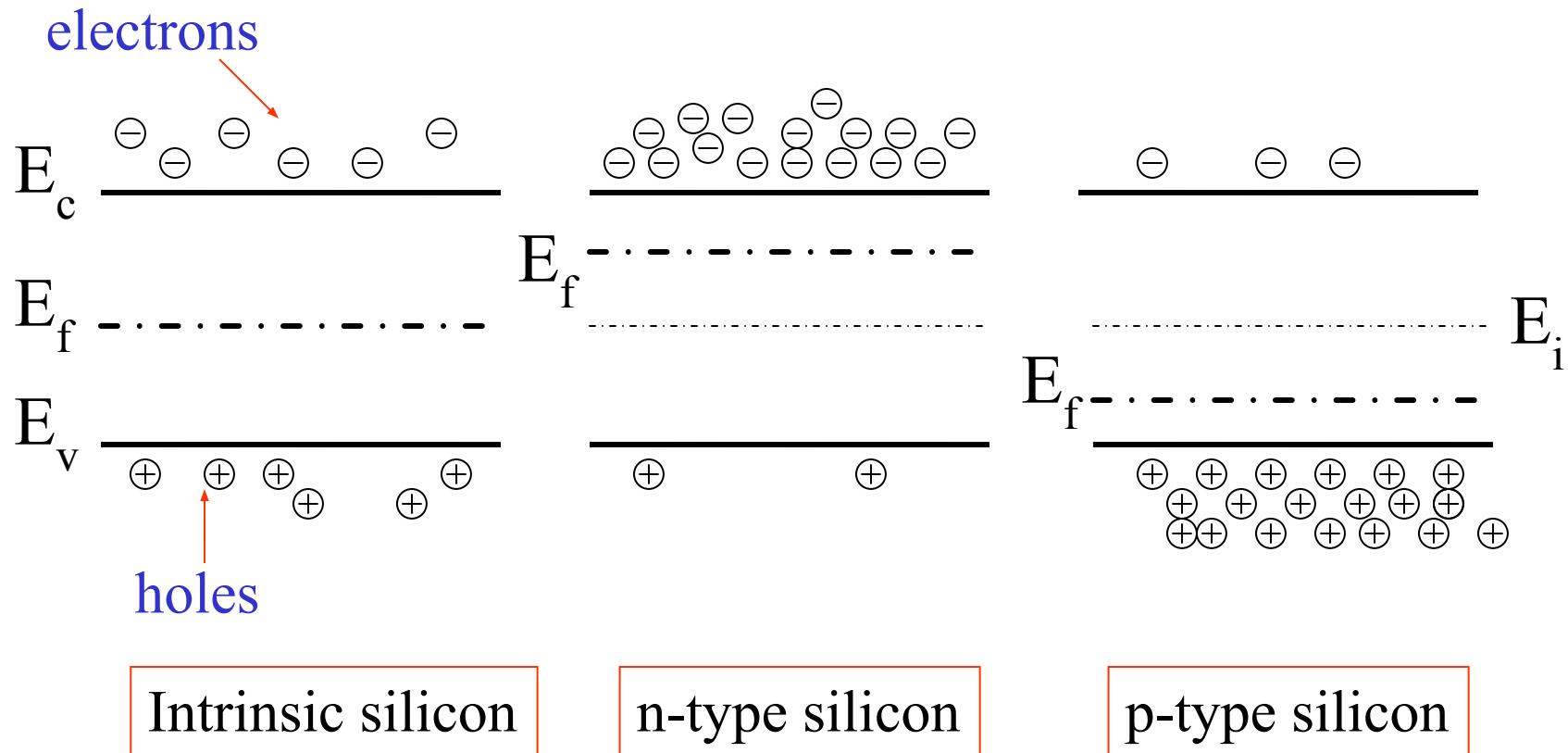
Extrinsic silicon is doped



Majority carriers are holes
Minority carriers are electrons

Majority carriers are electrons
Minority carriers are holes

Review on Energy Band Diagrams



Intrinsic silicon

n-type silicon

p-type silicon

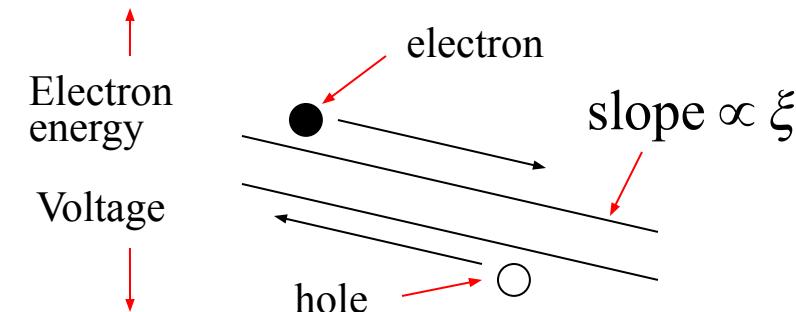
$$np = n_i^2 \quad n = n_i \exp\left(\frac{E_f - E_i}{kT}\right) = N_D \quad p = n_i \exp\left(\frac{E_i - E_f}{kT}\right) = N_A$$

Mechanisms of Carrier Transport

Drift: Movement of charge carriers due to an external field

$$\text{Current} \rightarrow I = qN\mu\xi$$

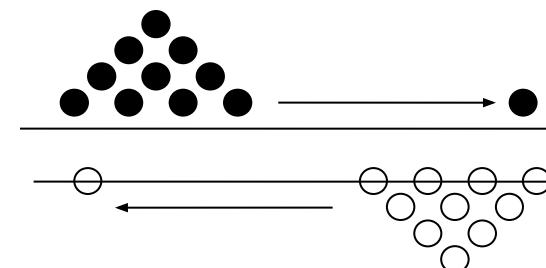
Carrier density Carrier mobility Electric field



Diffusion: Movement of carriers due to a concentration gradient

$$\text{Current} \rightarrow I = -qD \frac{\partial N}{\partial x}$$

Diffusion constant Concentration gradient



Einstein relation:

$$D = \frac{kT}{q} \mu$$

Electrostatics in 1-D

Relationship between electric-field and charge density (Gauss' Law)

$$\frac{\partial \xi}{\partial x} = \frac{\rho}{\epsilon}$$

Charge
density

Permittivity

Relationship between electrical potential voltage and electric field

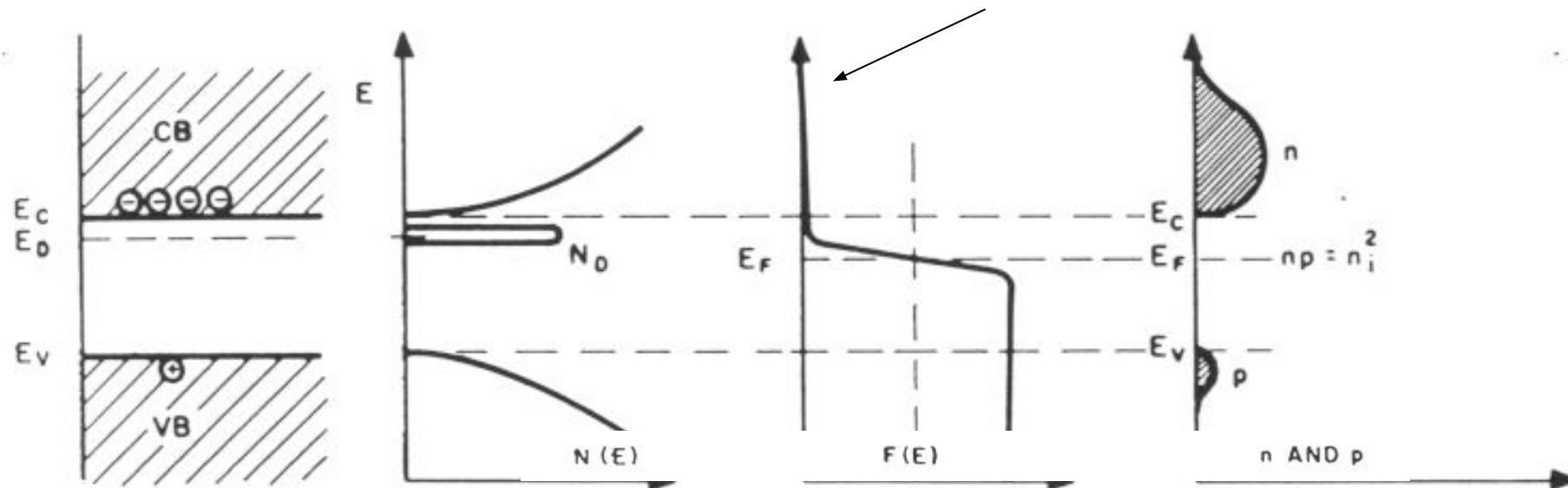
$$\frac{\partial V}{\partial x} = -\xi$$

Electric
field

An n-type semiconductor

Boltzmann distribution

$$F(E) \approx e^{-(E-E_f)/kT}$$



Energy
band
diagram

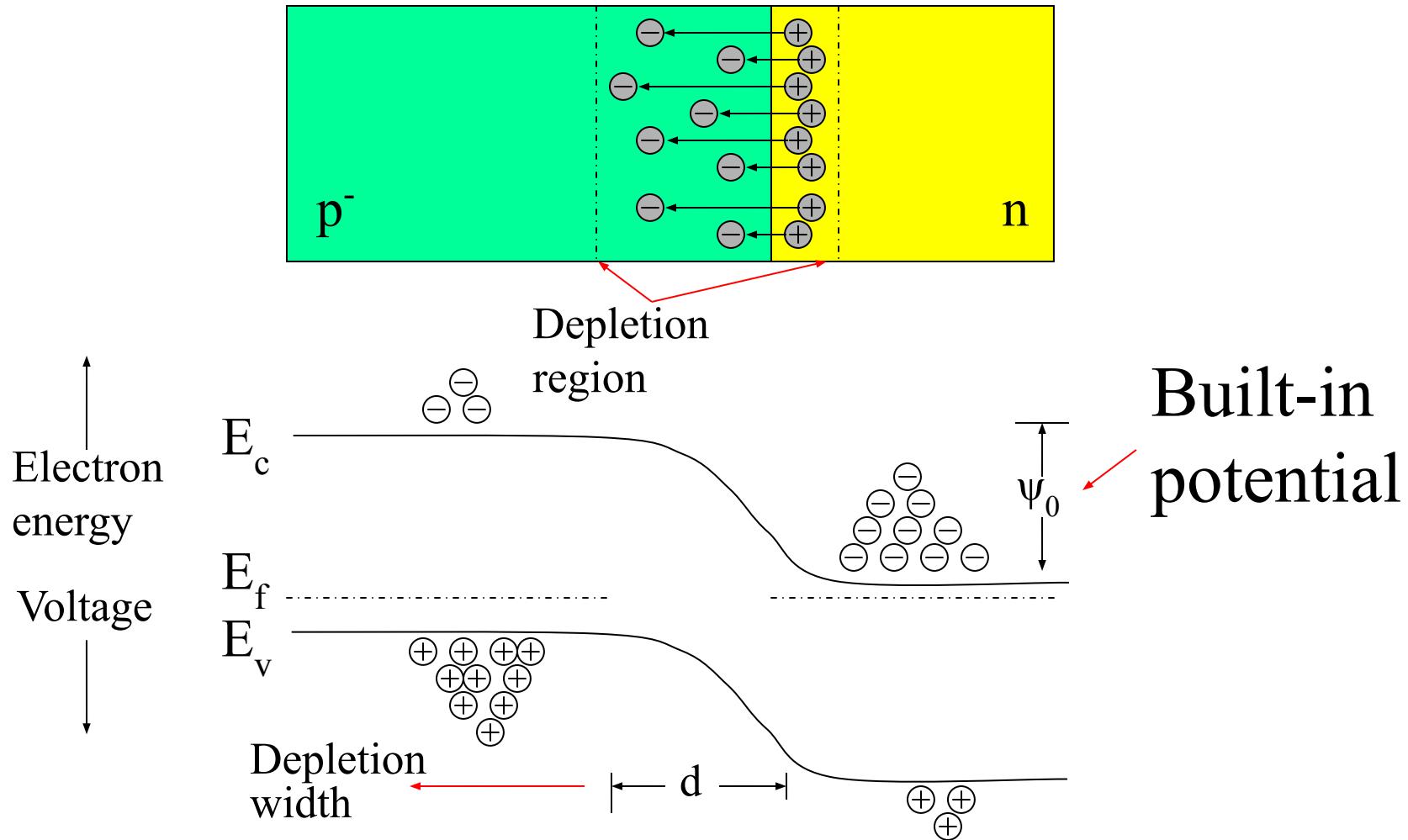
Density of
states

Fermi-Dirac
distribution

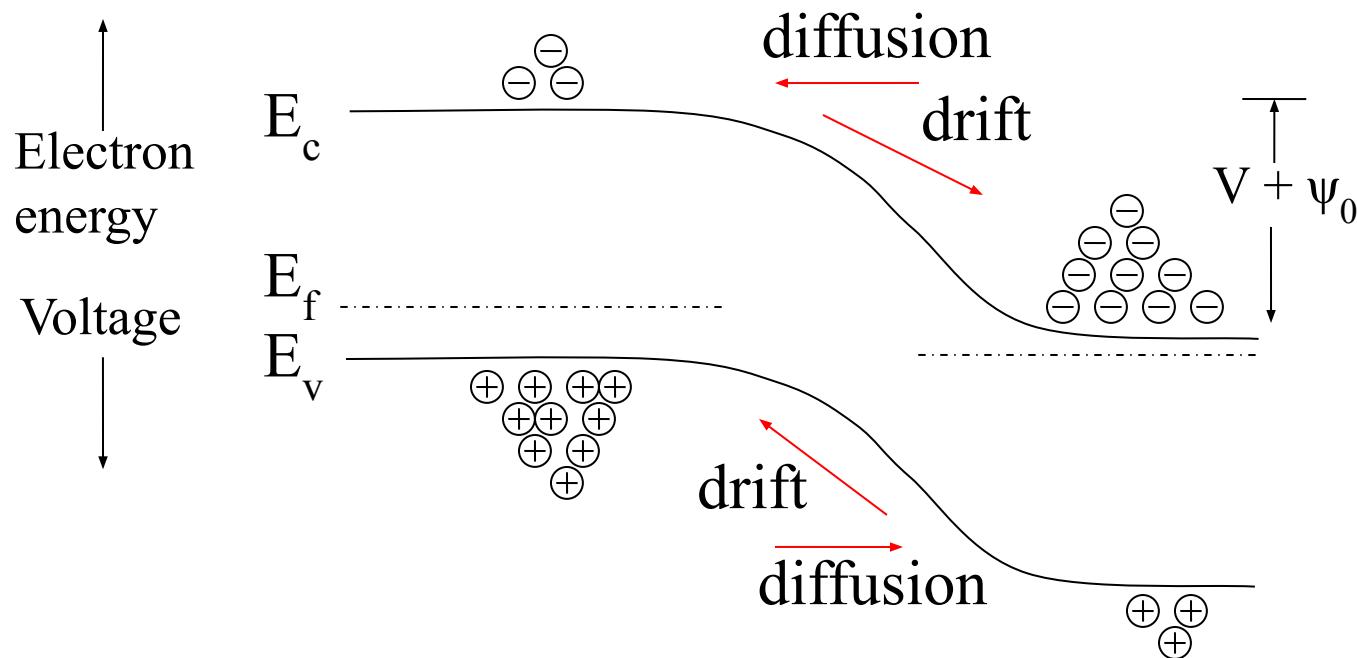
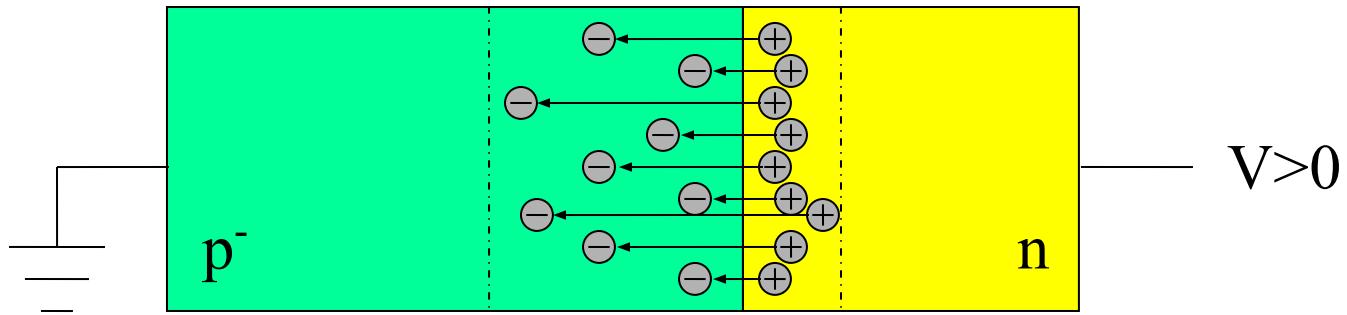
$$F(E) = \left(1 + e^{(E-E_f)/kT}\right)^{-1}$$

Carrier
concentration

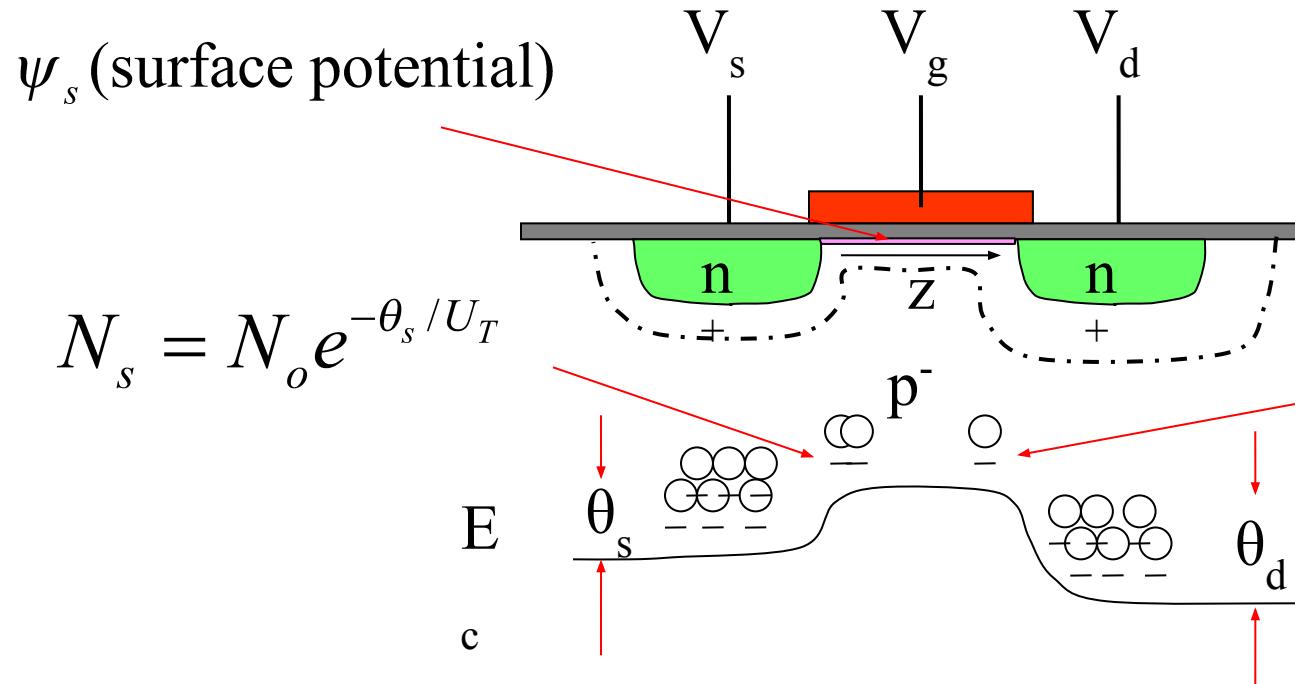
Equilibrium in a p-n Junction



Reverse-biased p-n Junction



Subthreshold nFET: Current is diffusion current



$$\begin{aligned}\theta_s &= \theta_0 - q(\psi_s - V_s) \\ \theta_d &= \theta_0 - q(\psi_s - V_d)\end{aligned}$$

$$\frac{dN}{dz} = \frac{N_s - N_d}{L}$$

$$N_d = N_o e^{-\theta_d / U_T}$$

N =carrier density per unit volume

W =channel width

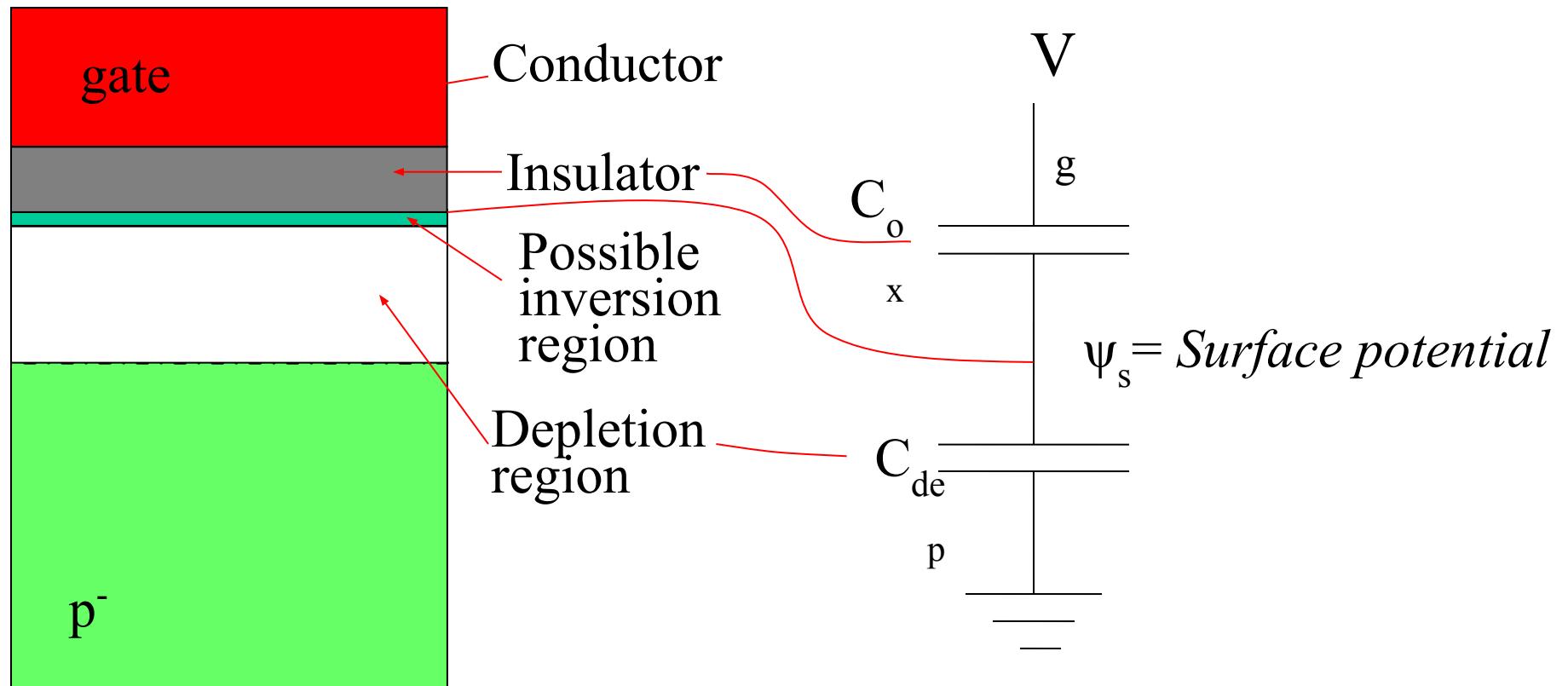
L =channel length

D =diffusion constant

θ_0 =built-in voltage

$$I = -q \frac{W}{L} D_n (N_s - N_d) = I_0 e^{\psi_s / U_T} (e^{-V_d / U_T} - e^{-V_s / U_T})$$

Influence of gate on surface potential



$$\frac{\partial \psi_s}{\partial V_g} = \frac{C_{ox}}{C_{ox} + C_{dep}} \equiv \kappa(\text{kappa})$$

Subthreshold nFET

Subthreshold nFET Equation

$$I_{ds} = I_0 e^{\frac{\kappa V_g}{U_T}} \left(e^{-\frac{V_s}{U_T}} - e^{-\frac{V_d}{U_T}} \right)$$

kT/q

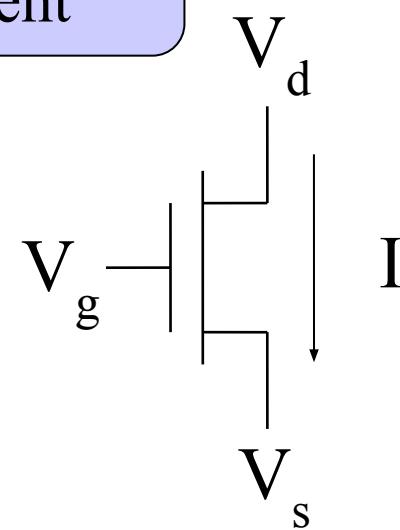
Concentration at source
Forward current

Concentration at drain
Reverse current

Saturation current

Barrier lowering

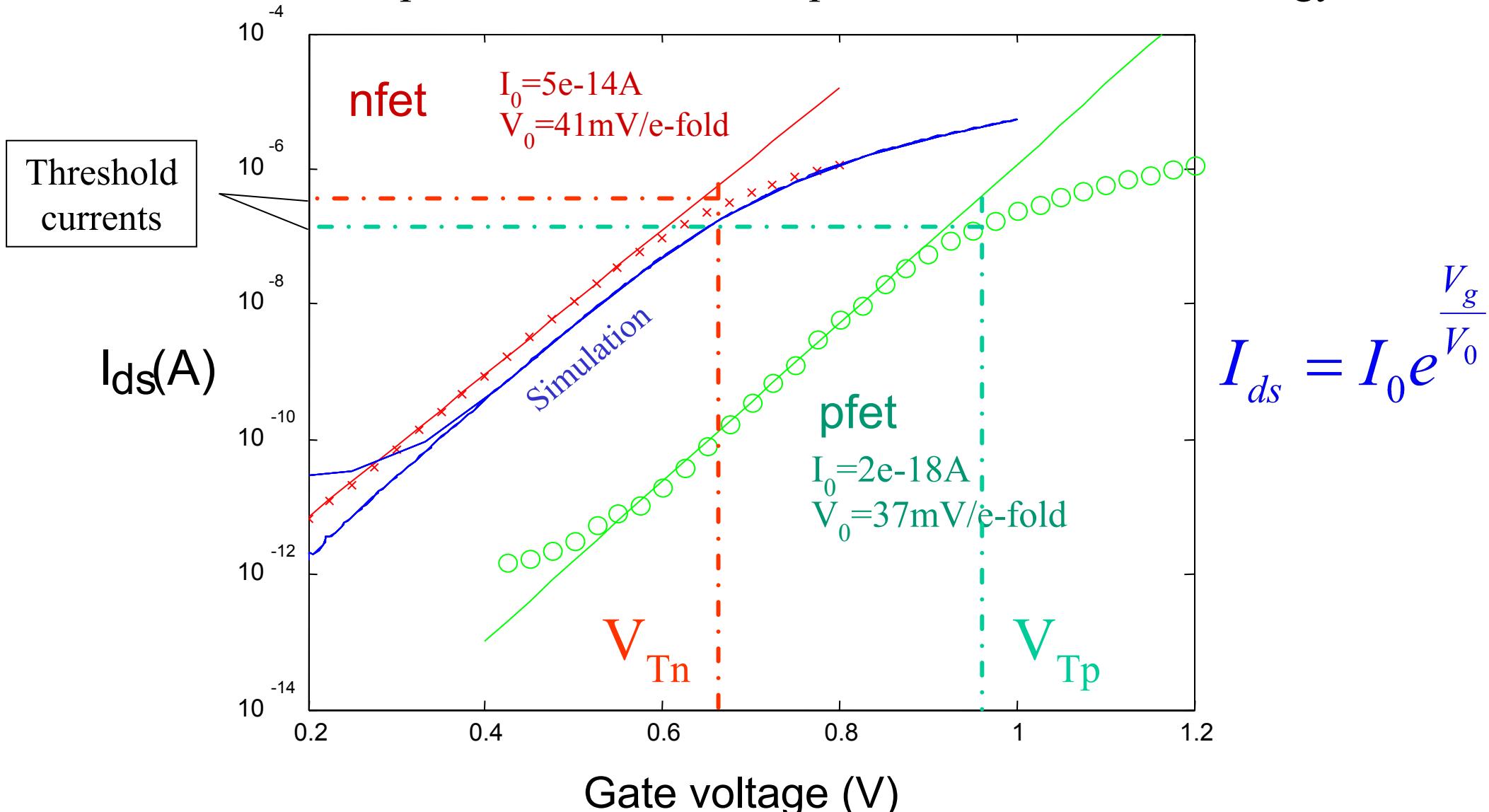
$$I_{dsat} = I_0 e^{\frac{\kappa V_g - V_s}{U_T}}$$



Example Lab Report

Lab 2 results: subthreshold transconductance

32x32 μm n & p FETs on old classchip in AMIS 1.6 μm technology

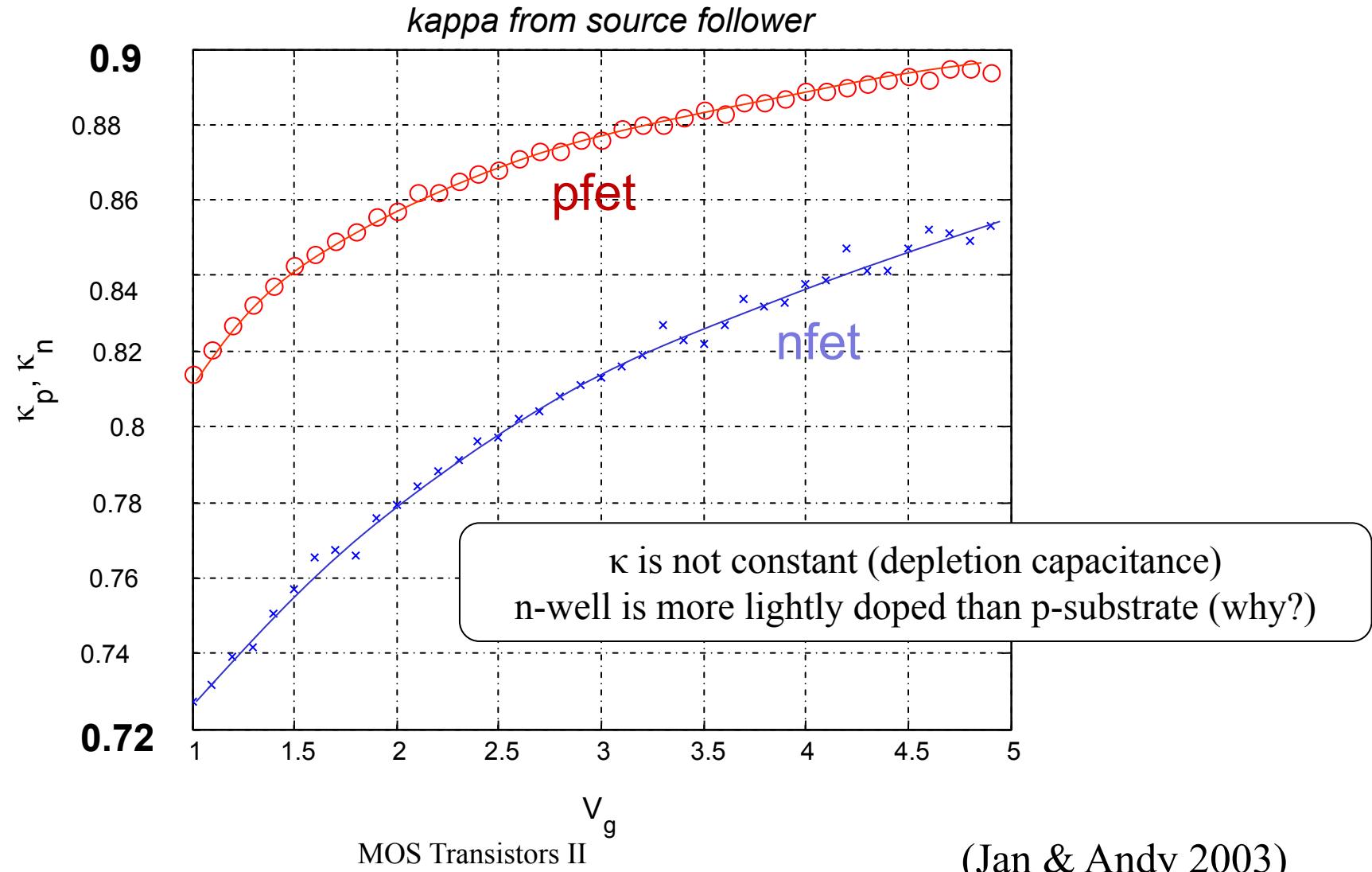


Lab 2 results

back gate coefficient (kappa) from source follower

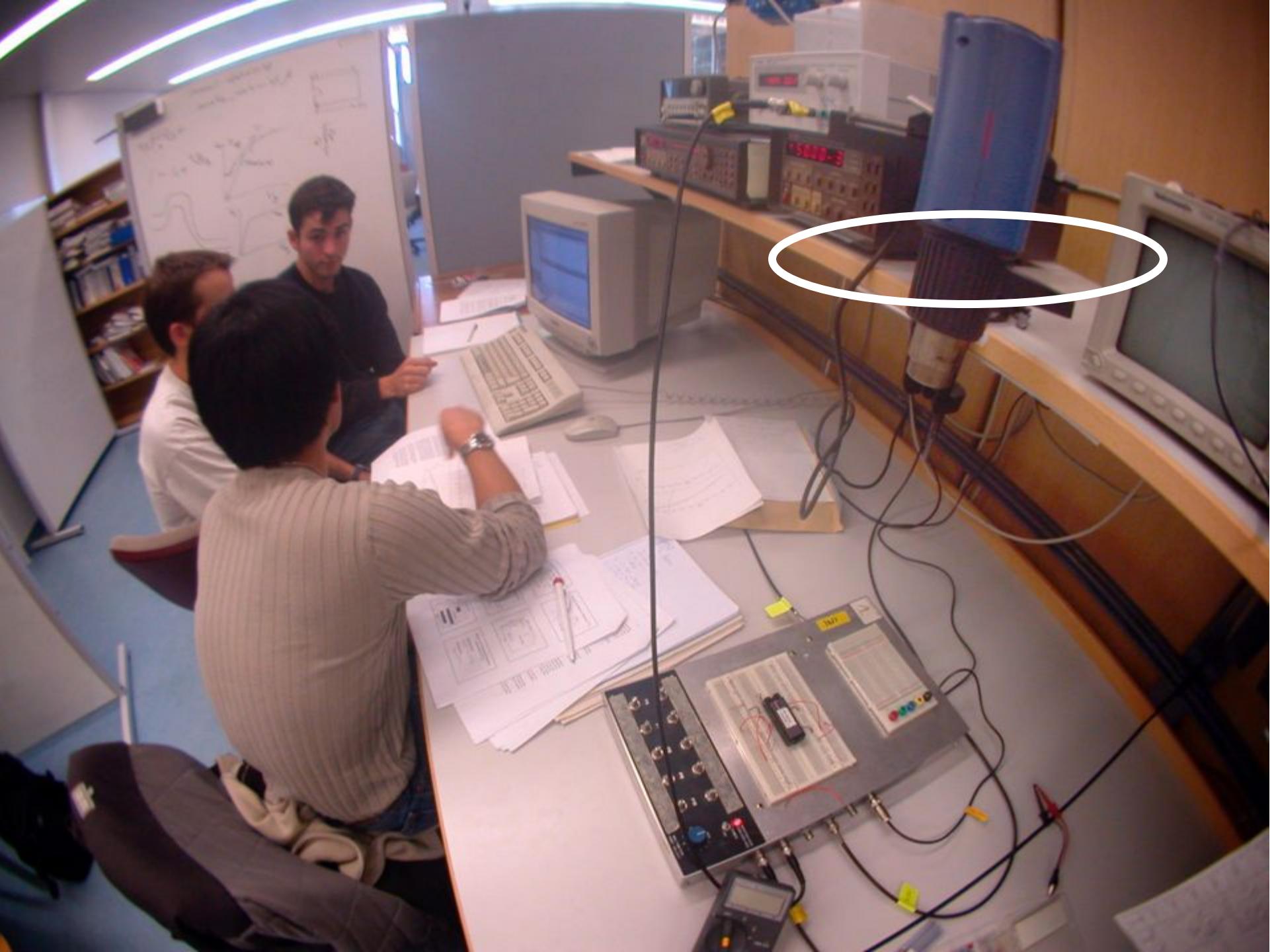
$$\kappa V_g - V_s = \text{constant}$$

$$\kappa = \frac{dV_s}{dV_g}$$



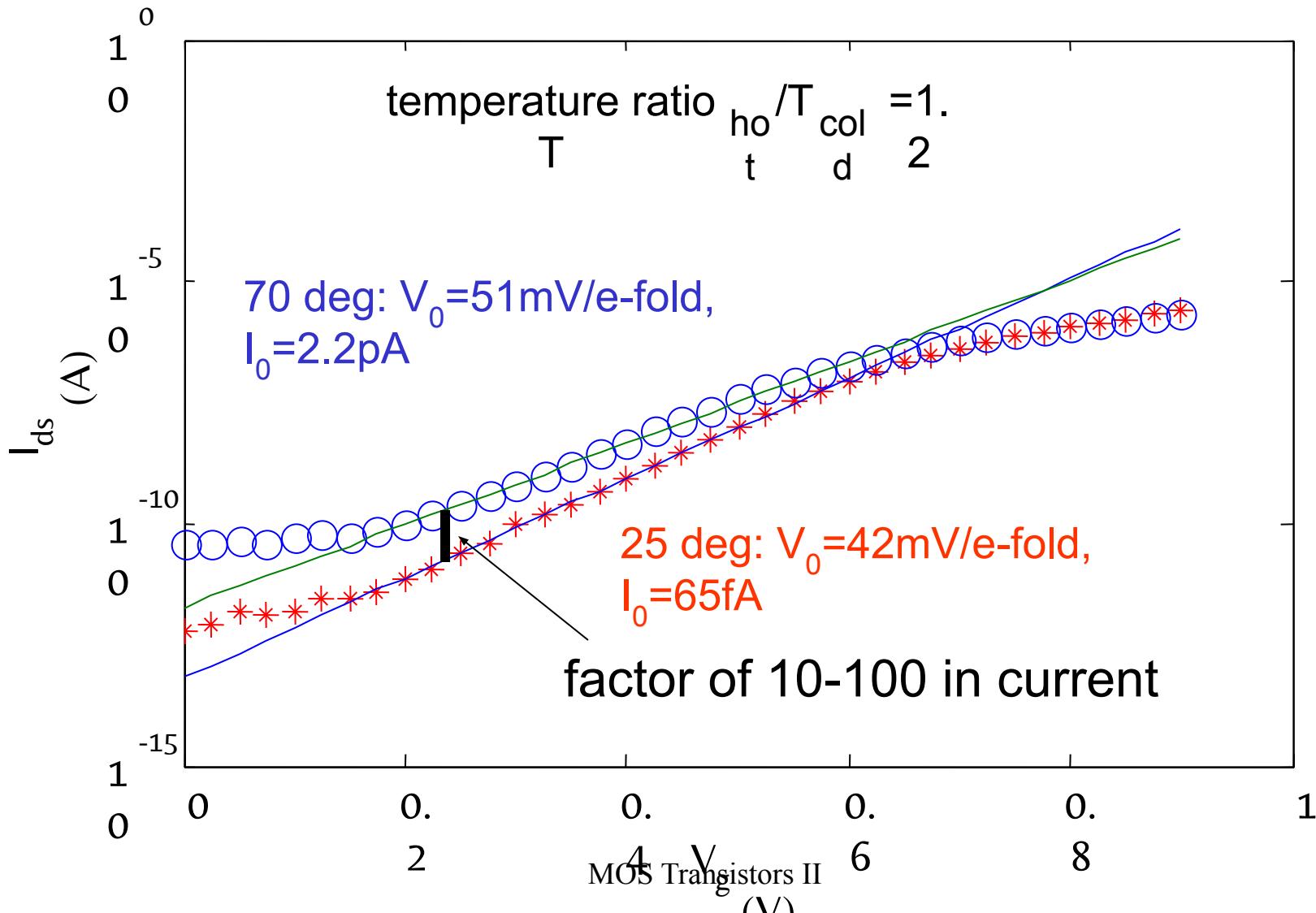
How does temperature affect current?

$$I = I_0 e^{\kappa V_g q / kT}$$



Effect of temperature on subthreshold characteristics

Data from Peter, Bryn & Zhen



Mismatch

Dominant cause of FET mismatch is random dopant fluctuation

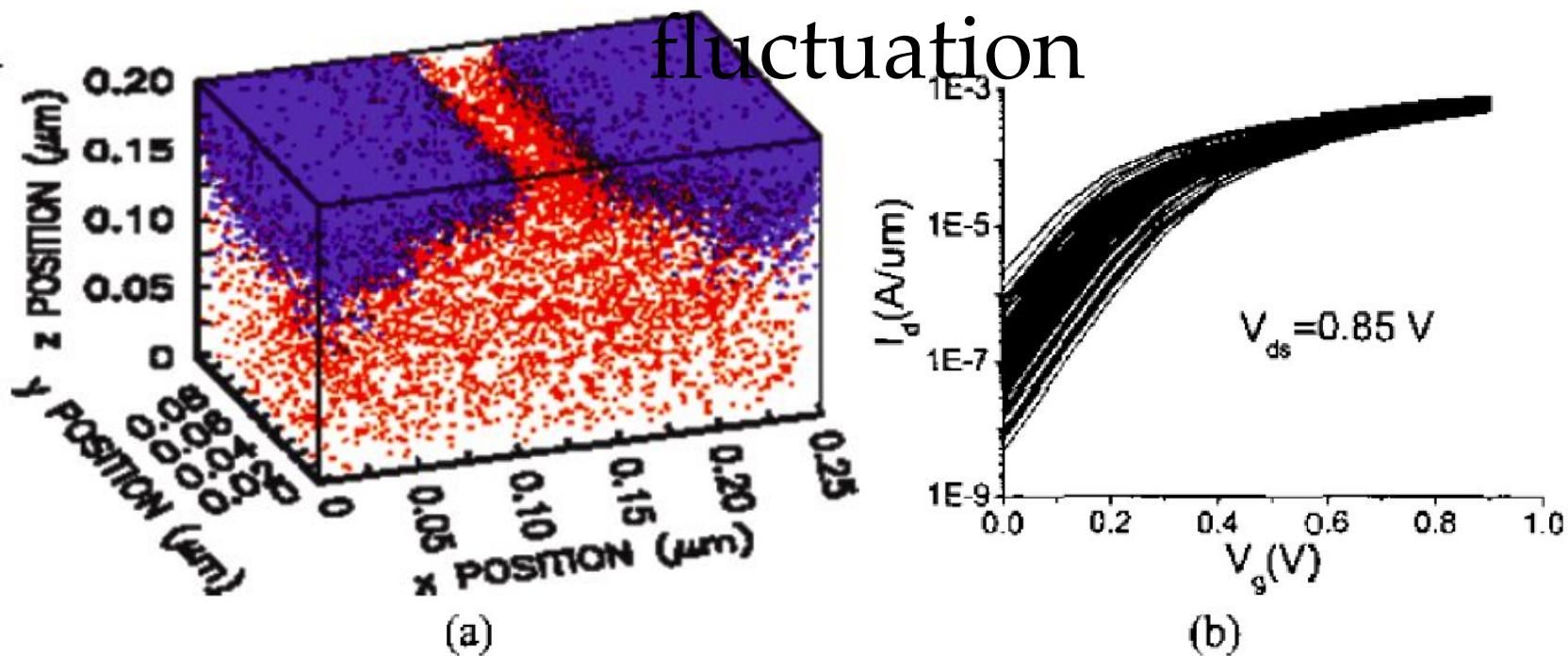


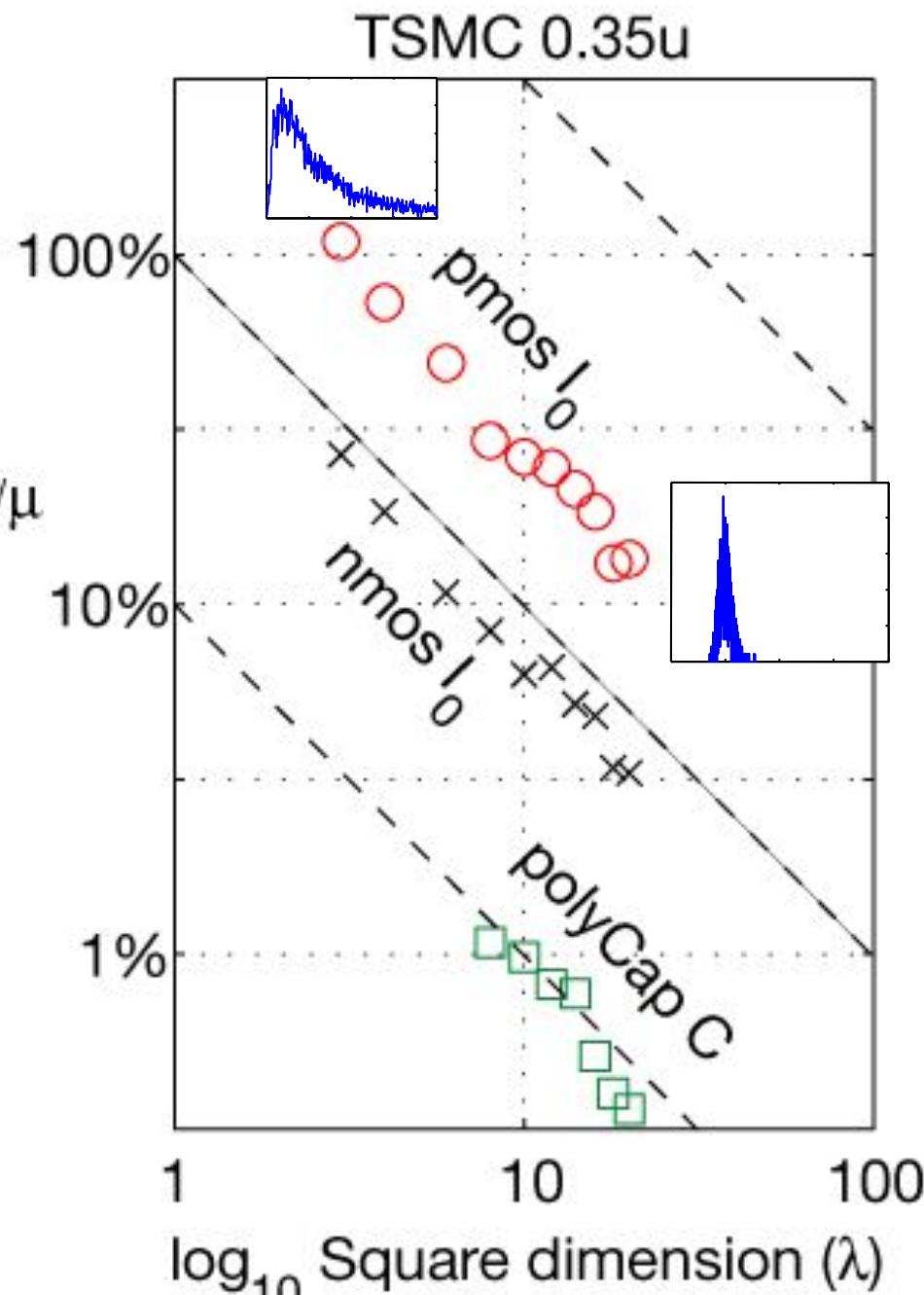
Fig. 1 (a) Potential distribution in a 35 nm MOSFET in which the detailed positions of dopants are considered. (b) Gate Characteristics from 200 macroscopically identical 35 nm MOSFETs, obtained by 'atomistic' device simulation.

Transistors are mismatched!

$$I = I_0 e^{\kappa V_g q / kT}$$

$\log \sigma/\mu$

- Built-in barrier heights have normal distribution
- Mismatch decreases as $1/\sqrt{W*L}$



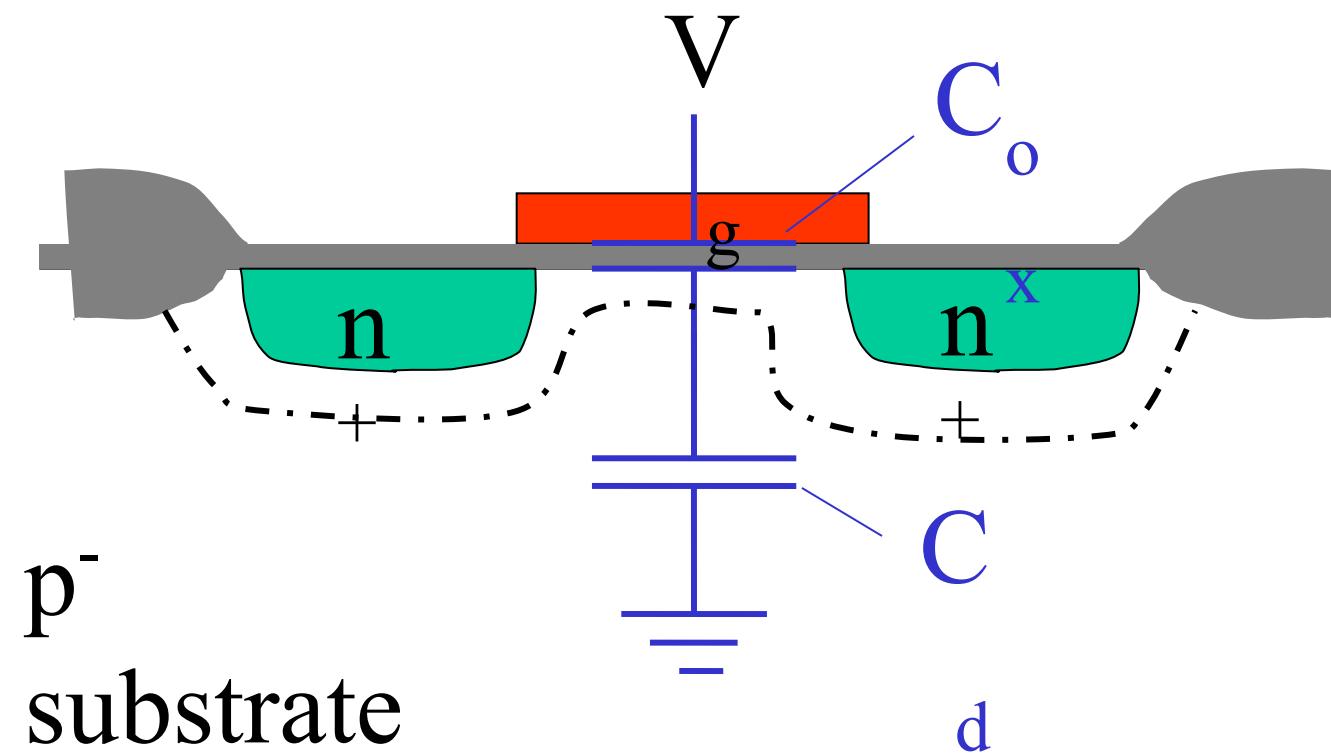
Brad Minch, 1999

Regimes of operation for nFET (dependent on V_{gs})

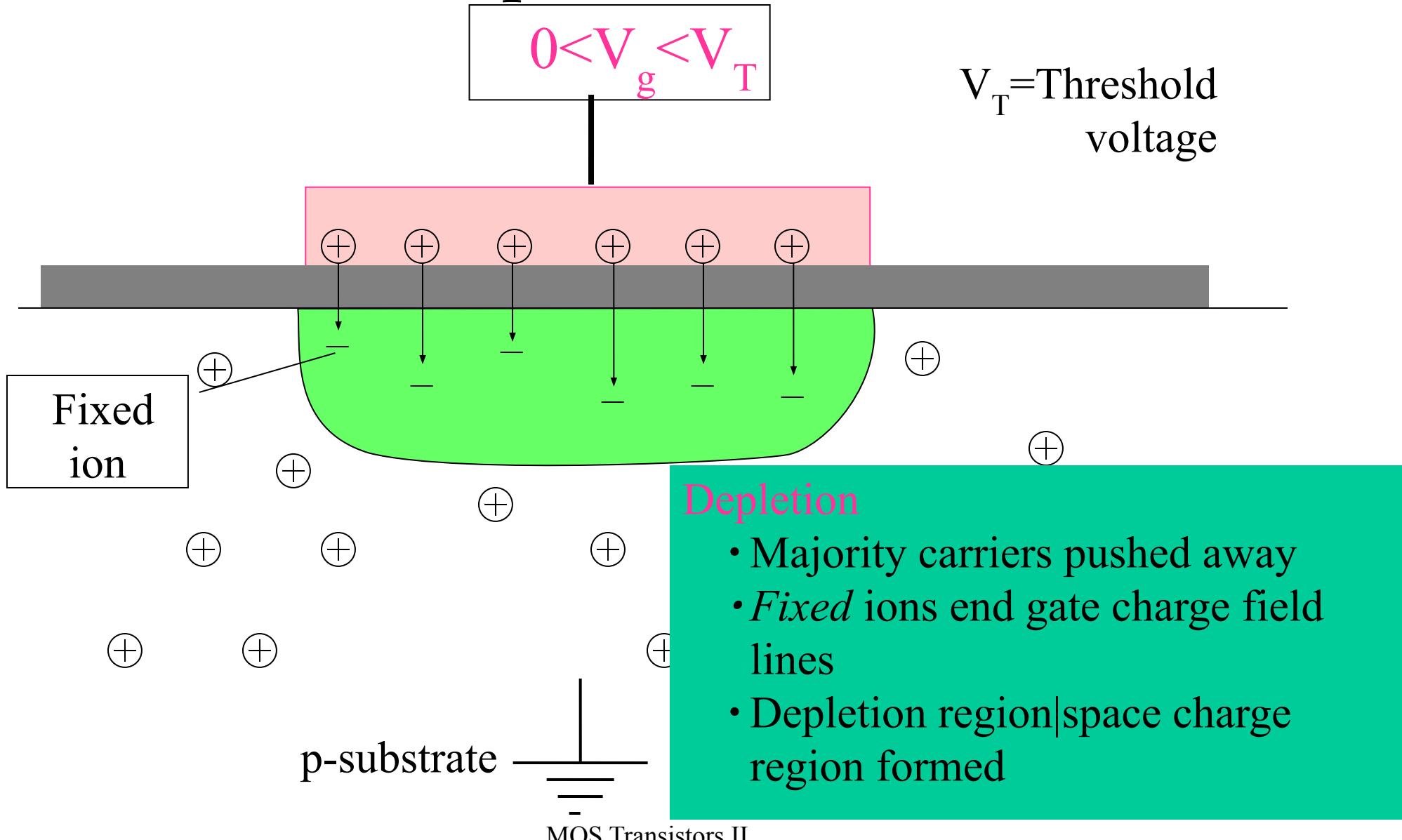
- Cutoff
- Subthreshold (Weak Inversion) Regime
Current flows through diffusion

- Above threshold (Strong Inversion) Regime
Current flows through drift

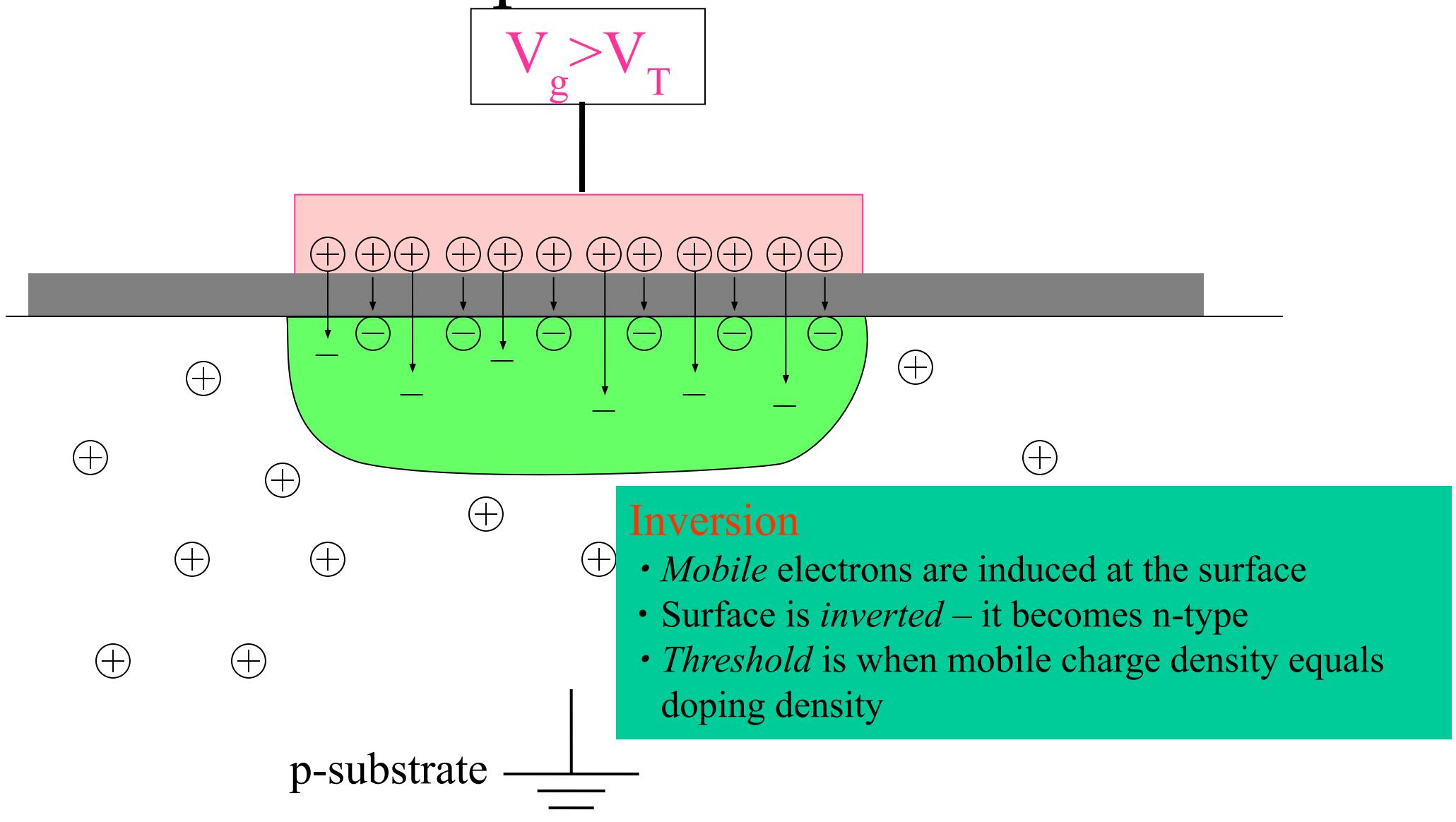
To understand strong inversion operation, we must understand how mobile charge density depends on gate to source voltage



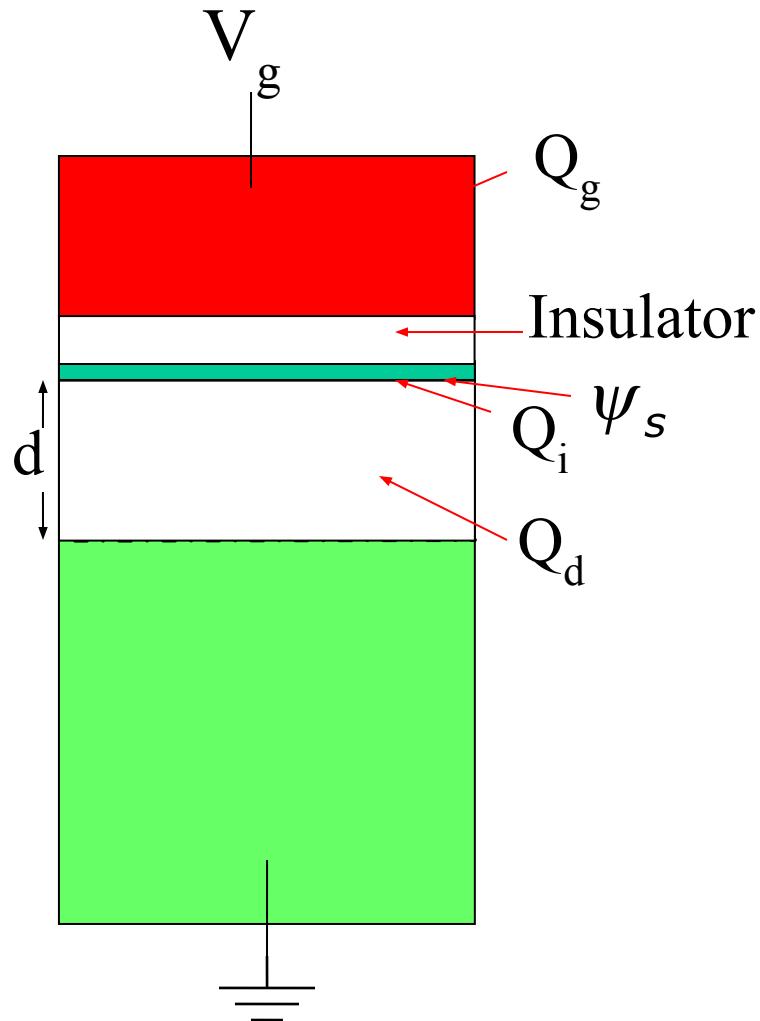
MOS capacitor structure



MOS capacitor structure



MOS Structure in Inversion

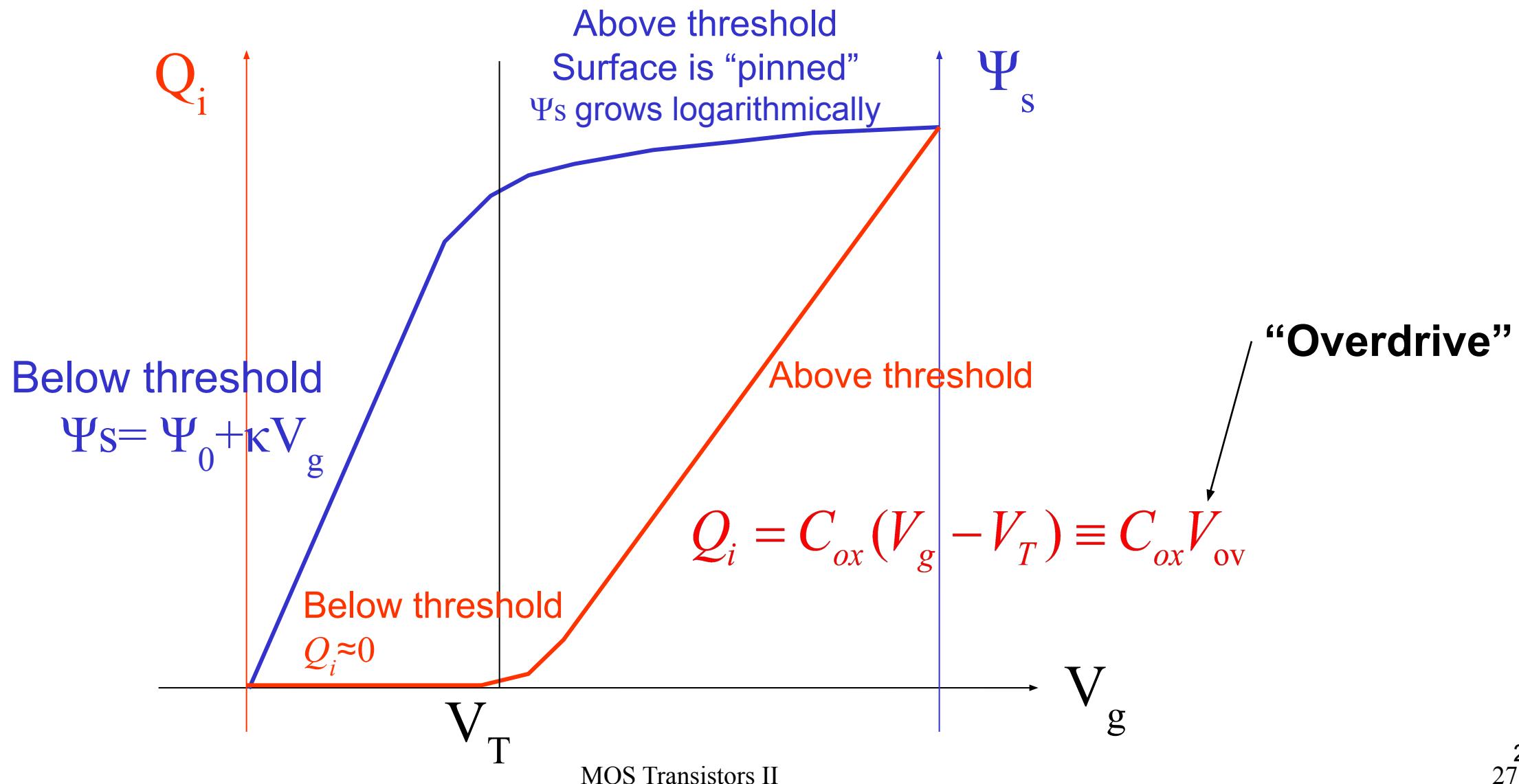


In **subthreshold**, changes in Q_g (due to a change in V_g) are balanced by the change in the **depletion charge**, Q_d .

In **superthreshold**, changes in Q_g are balanced by changes in the **inversion charge**, Q_i .

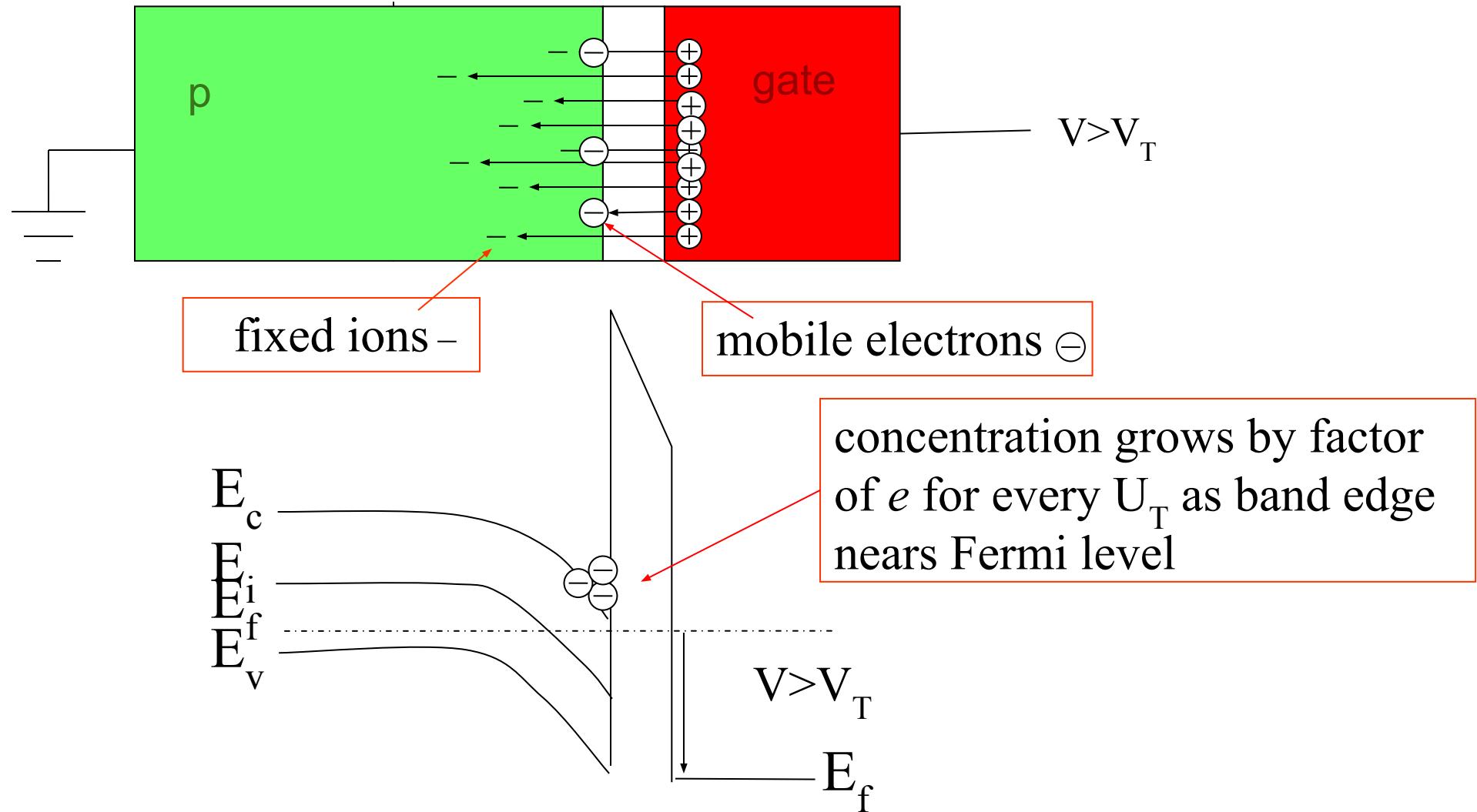
$$Q_g = Q_d + Q_i$$

nFet curve: Ψ_s and Q_i vs. V_{gs}

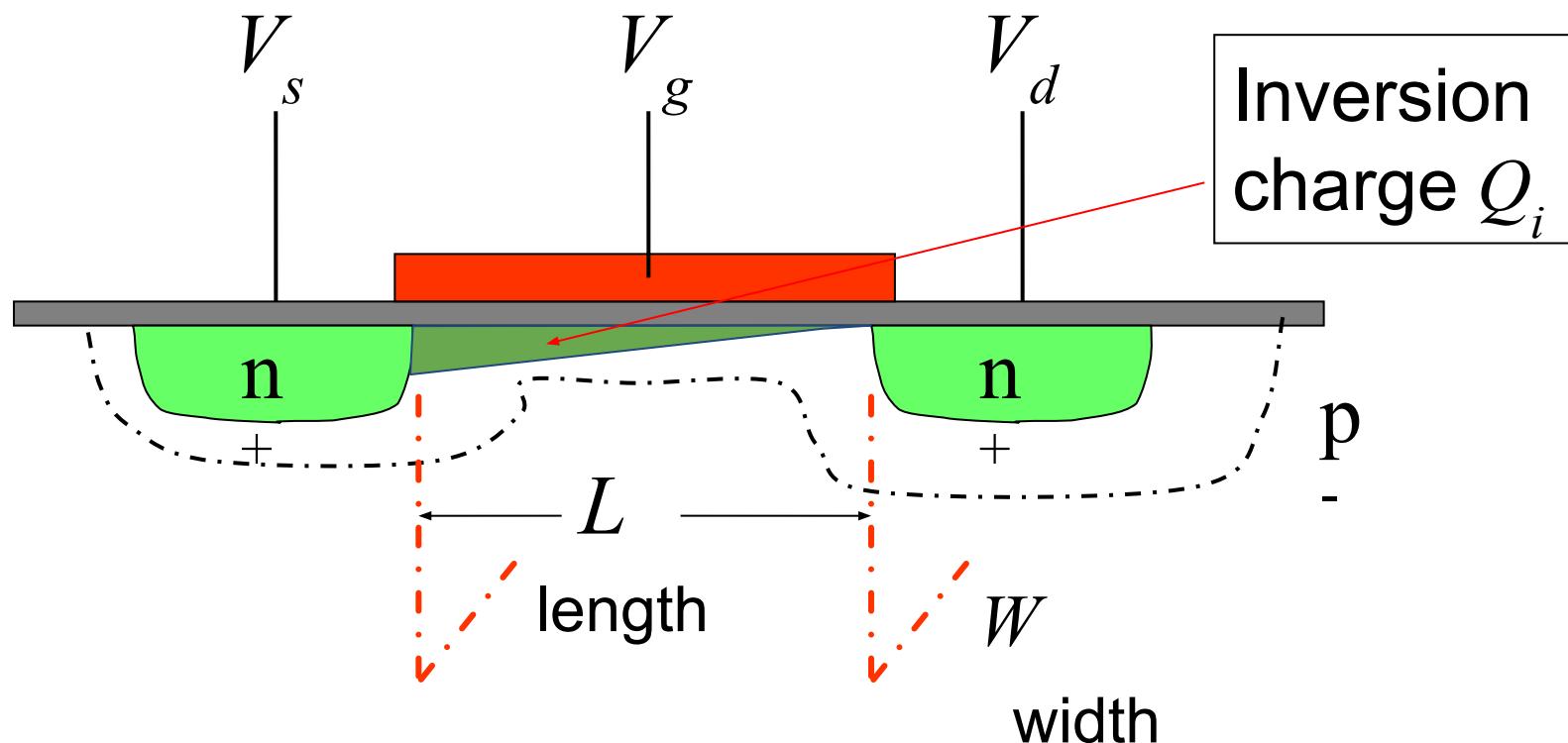


Why is there an abrupt threshold?

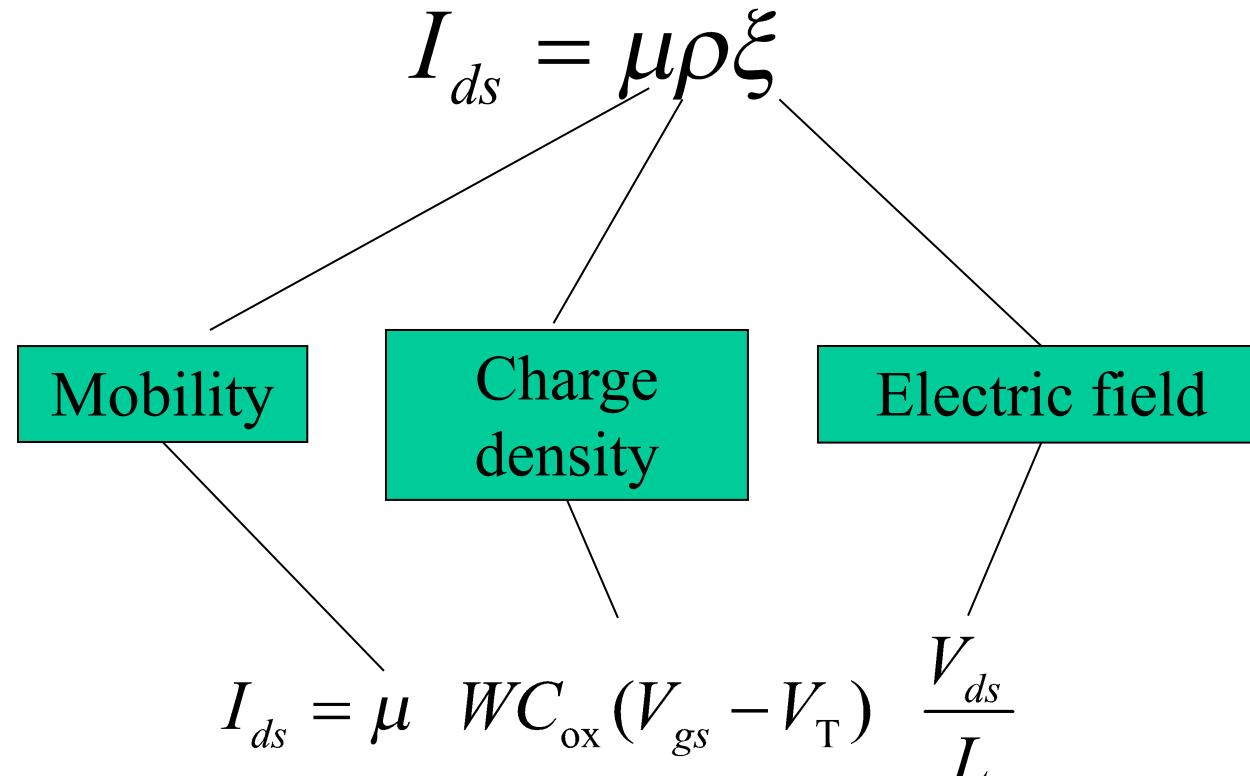
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Calculating above-threshold current

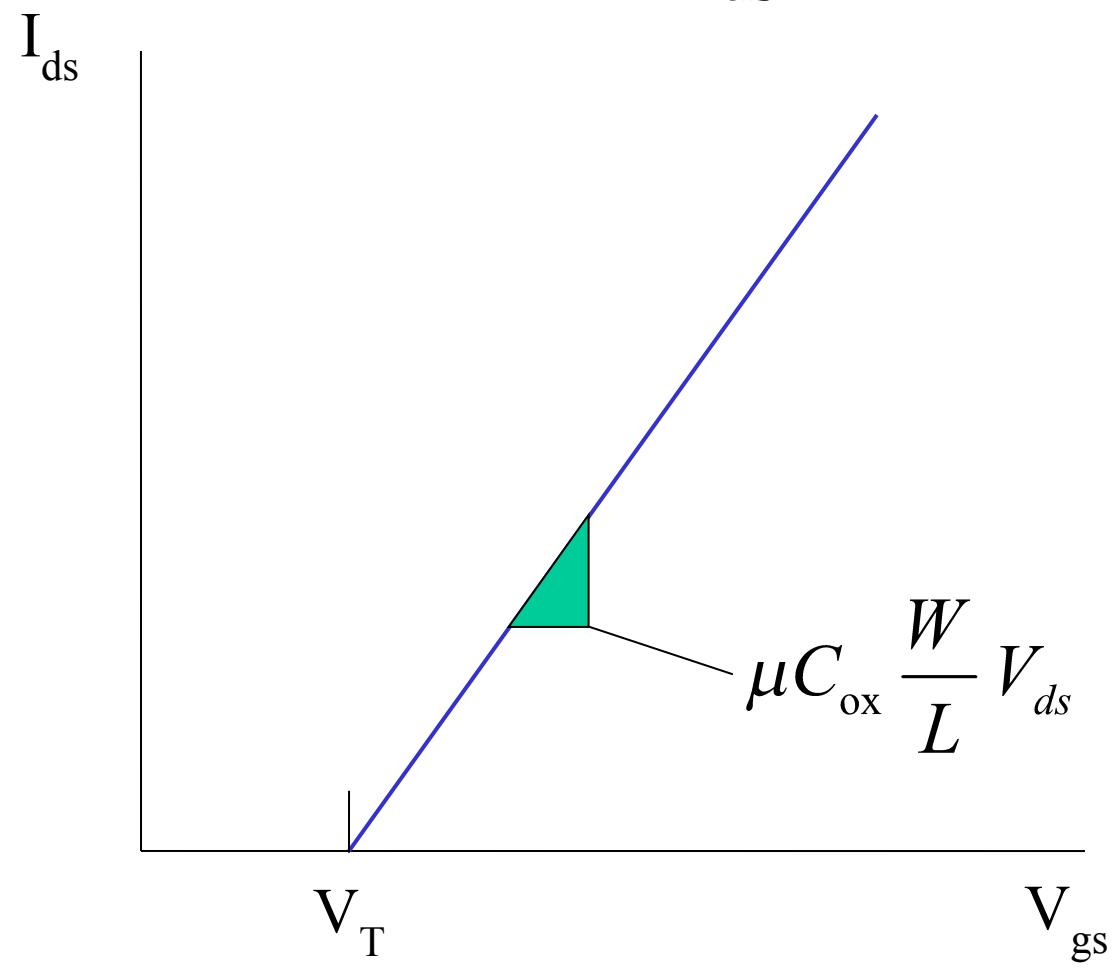


Above-threshold small V_{ds} current



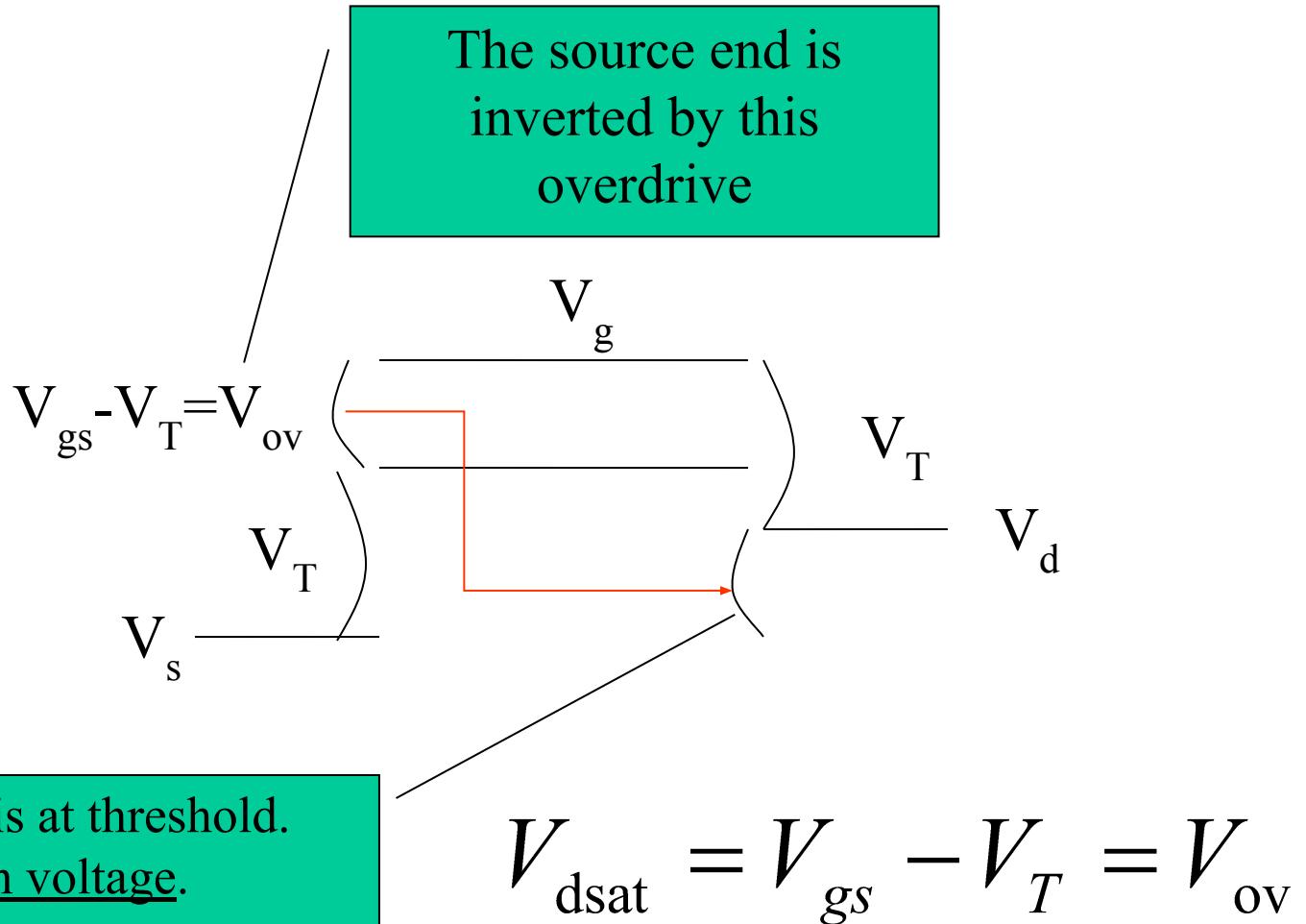
$$I_{ds} = \mu C_{\text{ox}} \frac{W}{L} (V_{gs} - V_{\text{T}}) V_{ds} = \mu C_{\text{ox}} \frac{W}{L} V_{\text{ov}} V_{ds}$$

Above threshold, strong inversion
Linear/Triode/Ohmic characteristic
(small V_{ds})



Saturation in strong inversion happens when the drain goes into subthreshold

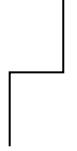
- The drain current saturates when the concentration at the drain end goes to zero.
- Saturation occurs whenever the drain end of channel is at or below threshold.



Above-threshold saturation current

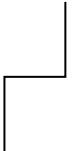
Triode region

$$I_{ds} = \mu C_{\text{ox}} \frac{W}{L} (V_{gs} - V_T) V_{ds}$$



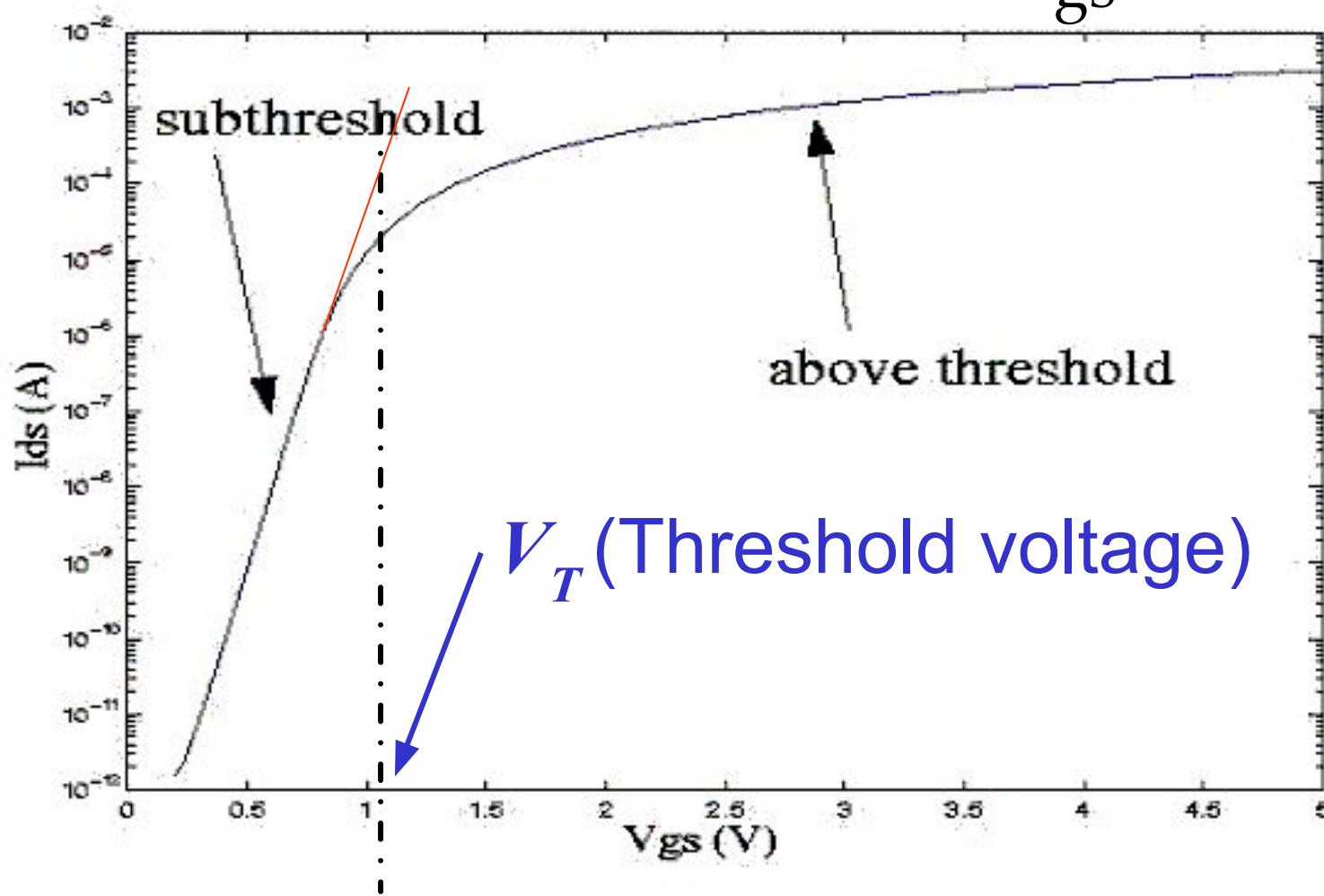
Replace V_{ds} with saturation
 $V_{ds} = (V_{gs} - V_T)$

$$\text{Saturation current } I_{ds,sat} = \frac{\mu C_{\text{ox}}}{2} \frac{W}{L} (V_{gs} - V_T)^2 = \frac{\mu C_{\text{ox}}}{2} \frac{W}{L} V_{ov}^2$$



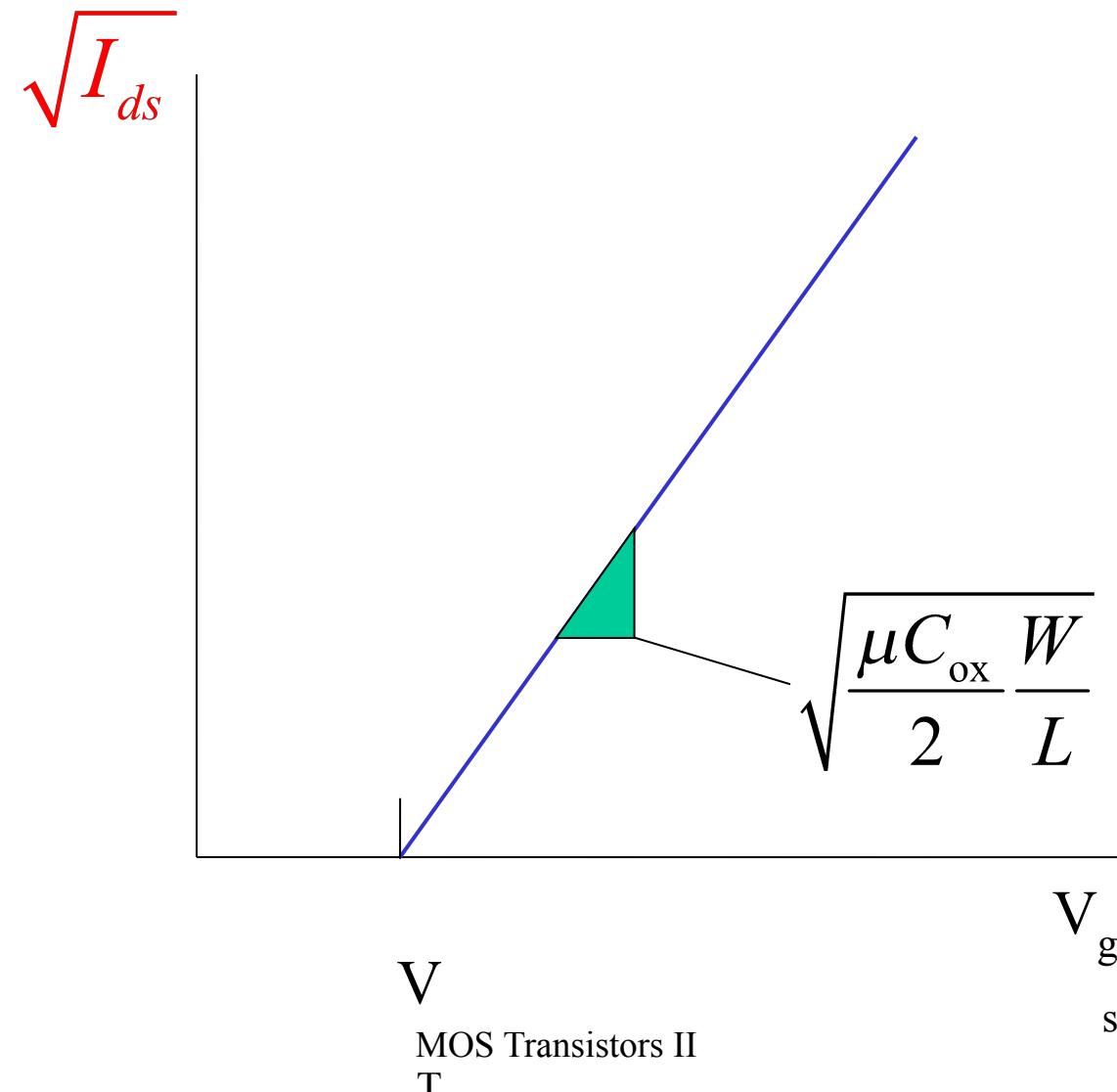
Account for downward curvature

nFet curve: I vs V_{gs}



Threshold voltage is the voltage where the measured I_{ds} is half of the I_{ds} computed from the extrapolated exponential.

Above-threshold saturation current



Regimes of Above Threshold Operation (dependence on V_{ds})

Triode/Linear/Ohmic Region

$$I = \mu C_{ox} \frac{W}{L} (V_g - V_T)(V_d - V_s)$$

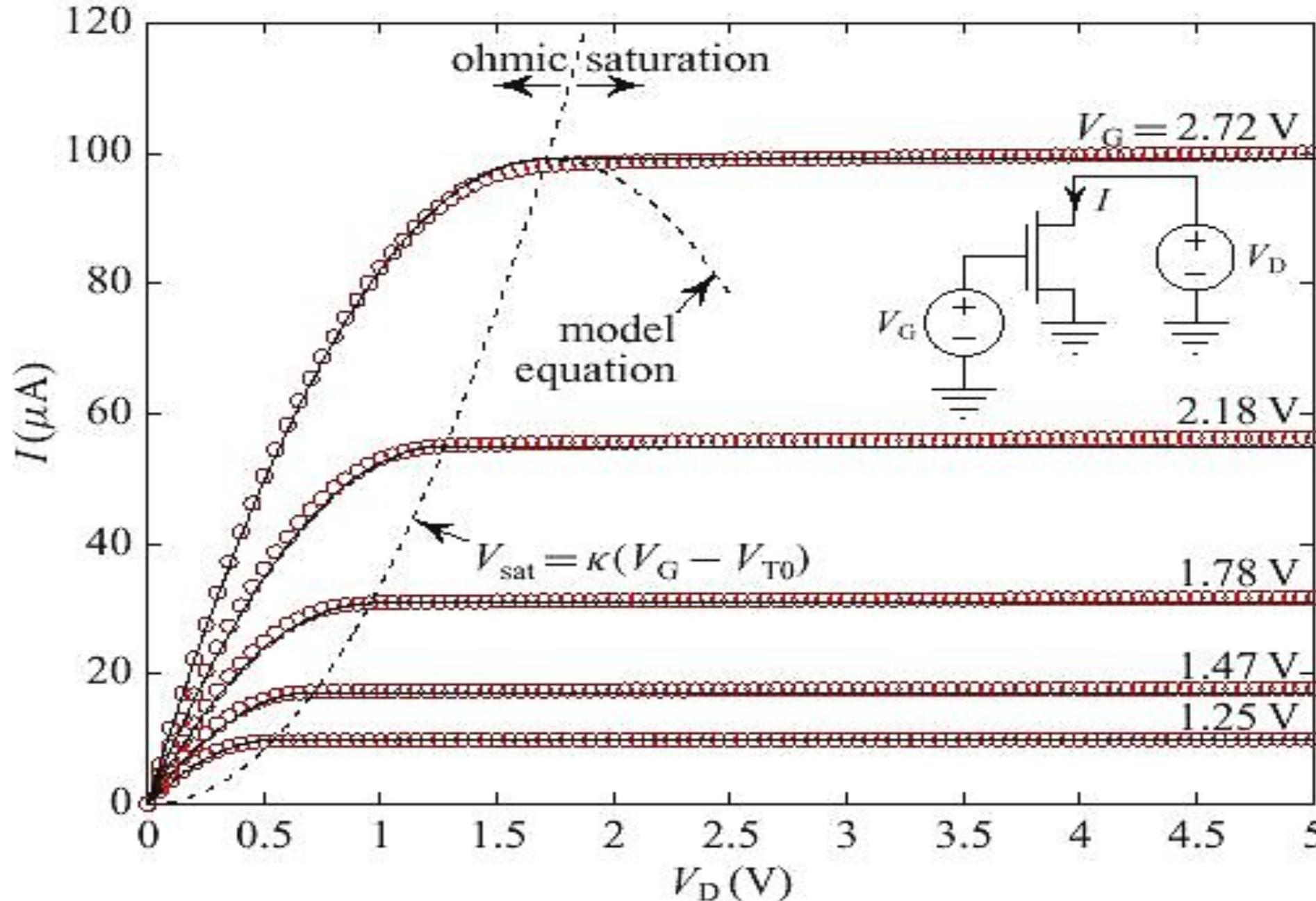
$$I = \beta (V_g - V_T) V_{ds}$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

Saturation Region

$$I = \frac{\beta}{2} [(V_g - V_T)^2]$$

Above Threshold nFET curve: I vs V_{ds}



Threshold Voltage depends on V_s

1. V_T depends on V_s because carriers come from the source.
2. As V_s increases, V_T increases more, because of the capacitive divider from gate to channel to substrate.

V_T = effective threshold voltage

$$V_T = V_{T0} + \frac{V_s}{\kappa}$$

$$Q_i = -C_{ox} (V_g - V_T)$$

e.g.

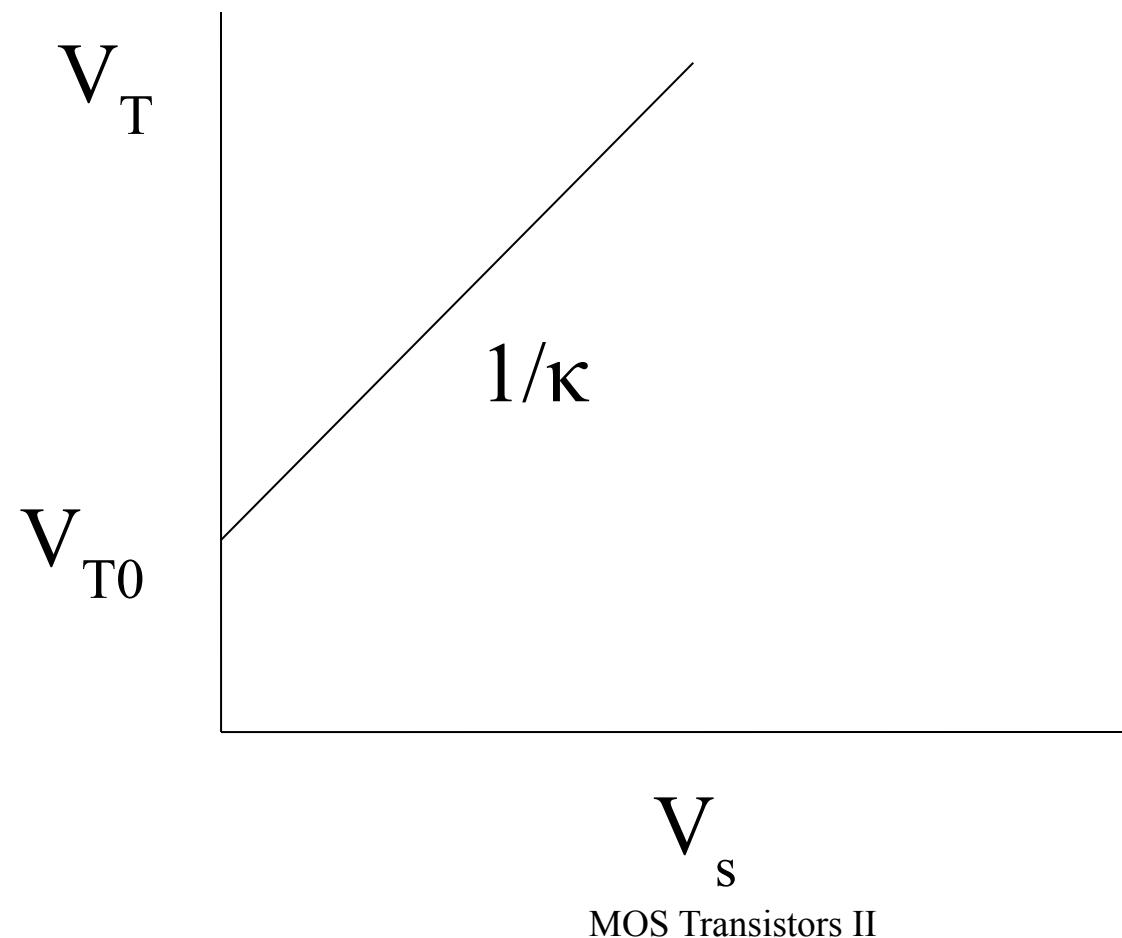
$$V_{T0} = 1V,$$

$$\kappa = 0.8, V_s = 1$$

$$V_T = 1 + 1/0.8 = 2.25V$$

$$= -C_{ox} \left(V_g - V_{T0} - \frac{V_s}{\kappa} \right)$$

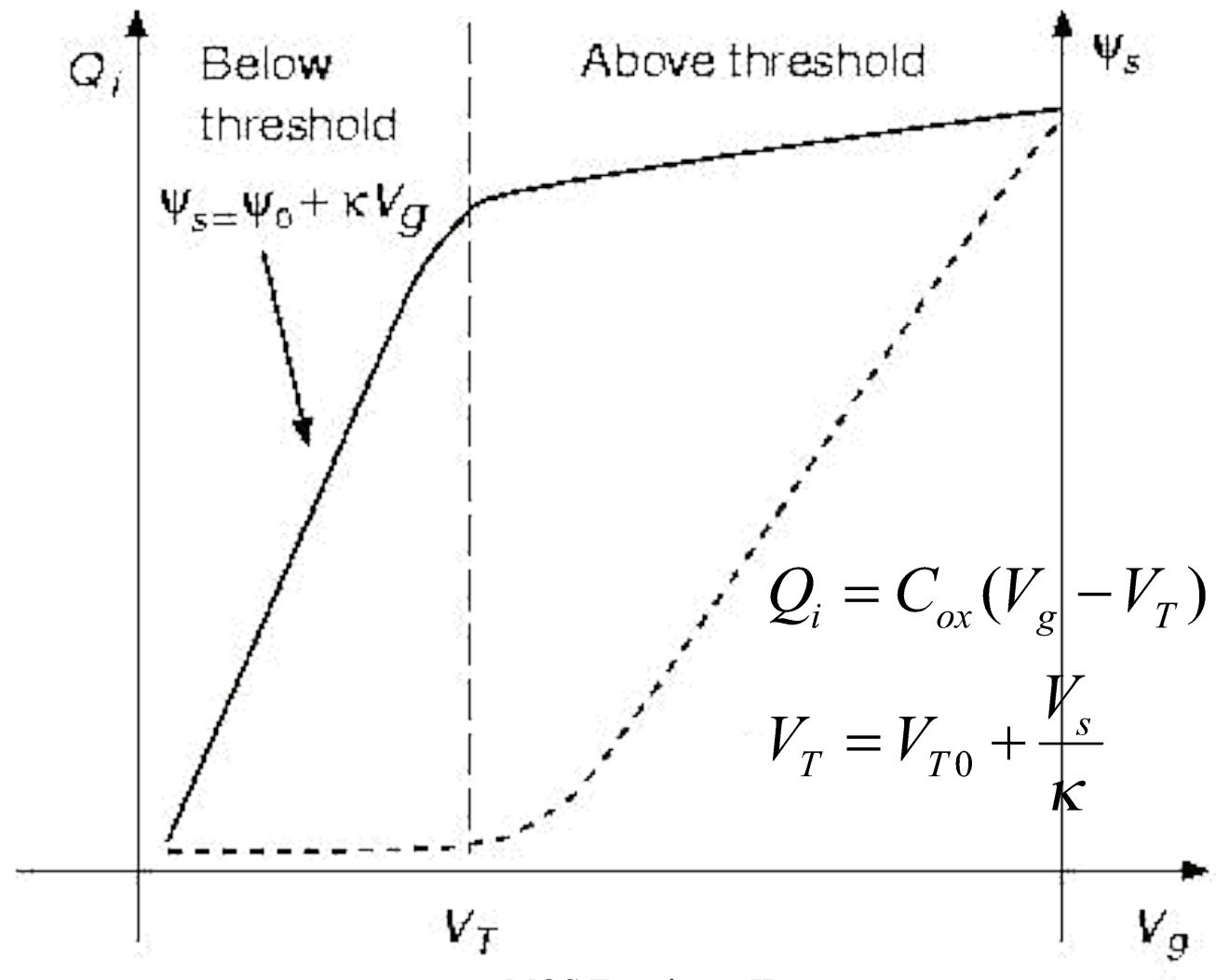
V_T as function of V_s



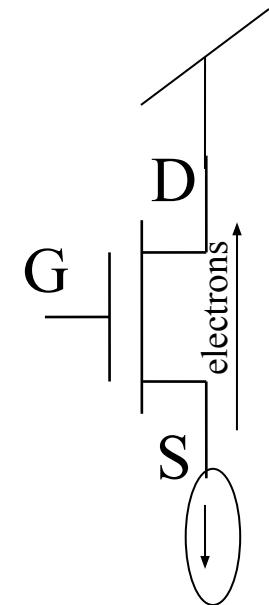
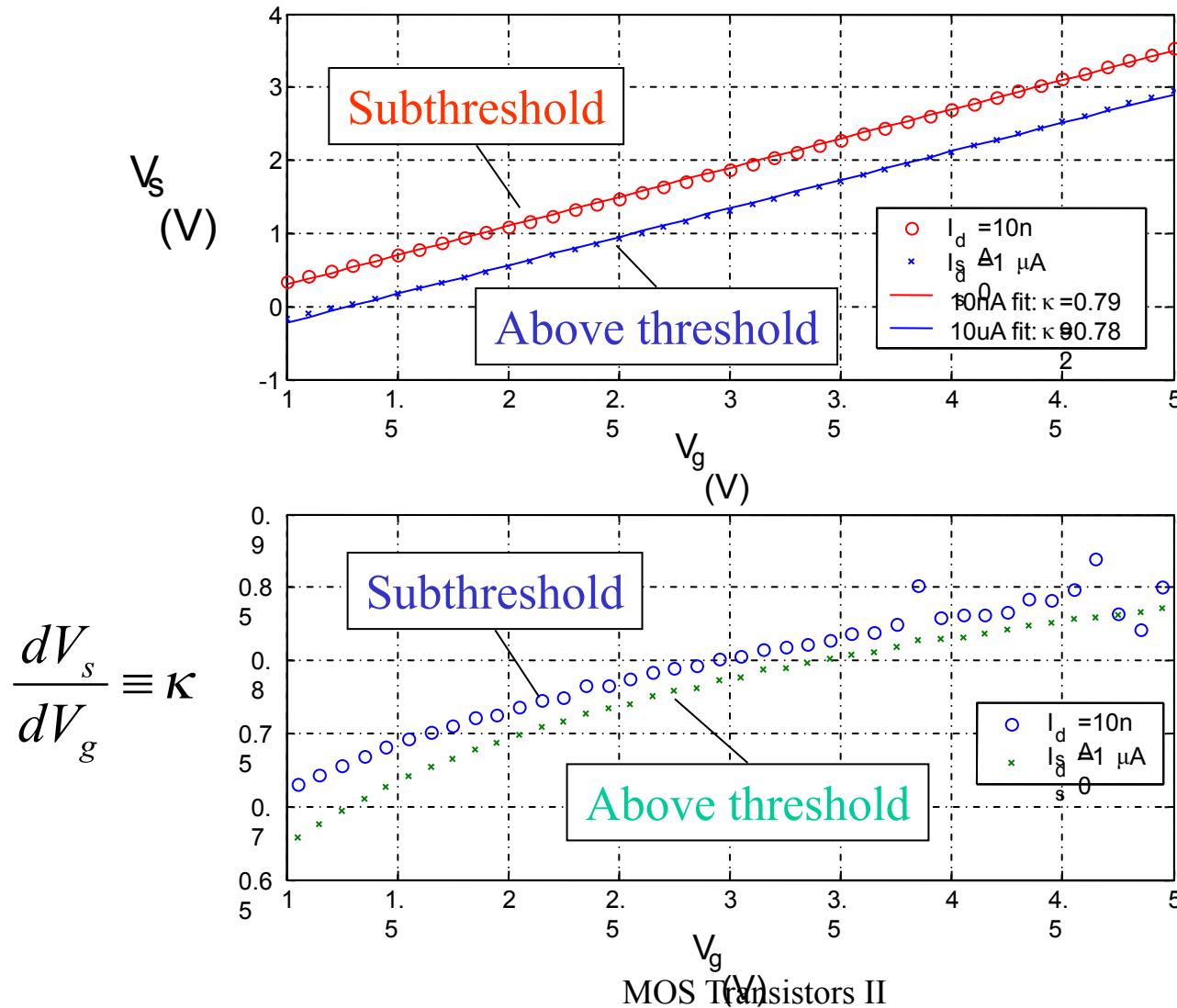
The meaning of κ in weak and strong inversion

- In weak inversion (subthreshold)
 κ is the efficiency of the gate in controlling the surface potential
- In strong inversion (above threshold)
 $1/\kappa$ is the efficiency of the source in raising the threshold voltage

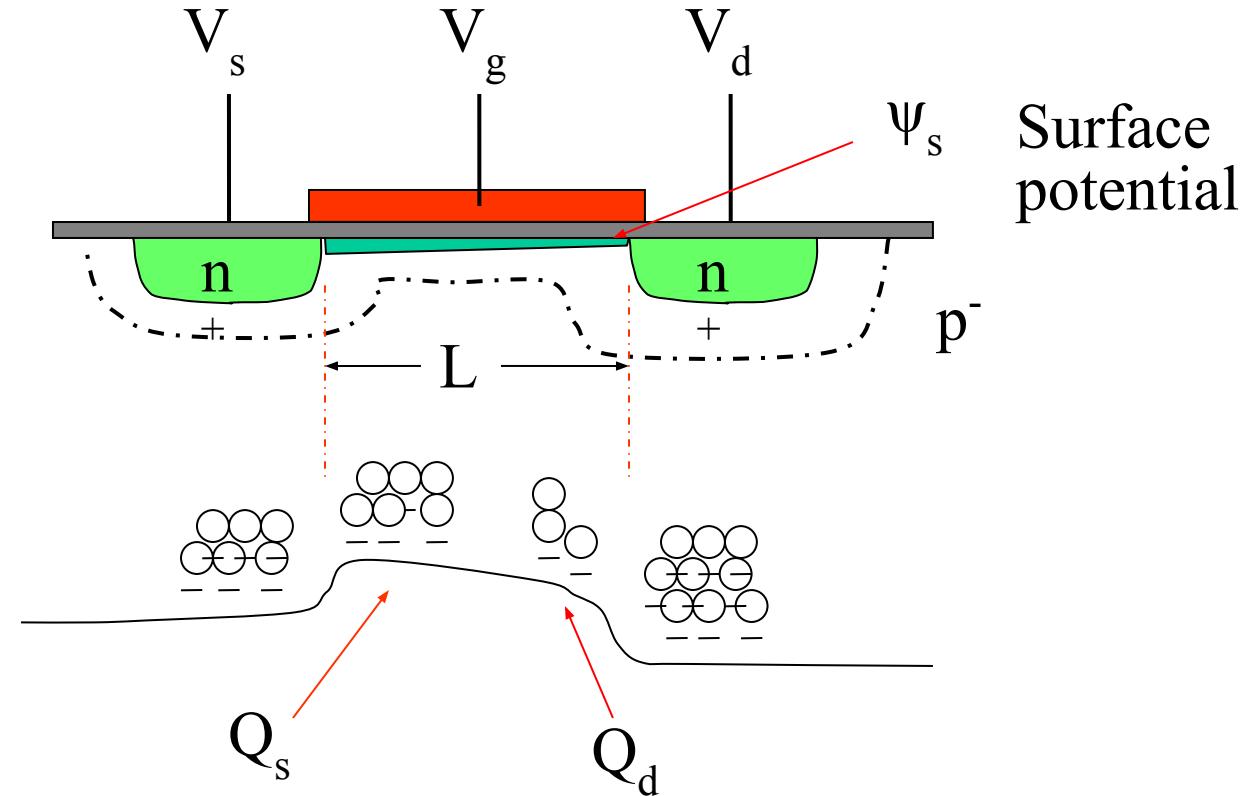
nFet curve: Q_i vs V_{gs}



κ in weak and strong inversion



Computing above threshold current more exactly #1/3



Computing above threshold current more exactly #2/3

Start with Drift Current: $I = \mu_n Q_i W \xi$

Next write equations for electric field along channel ξ

Channel Capacitance: $C = \frac{dQ_i}{d\psi_s} = C_{ox} + C_d$ (1)

Field in the channel: $\xi = -\frac{d\psi_s}{dz}$ (2) From (1) and (2)
 $\xi = -\frac{1}{C} \frac{dQ_i}{dz}$ (3)

Drift Current: $I = \mu_n Q_i W \xi$

Substitute (3): $I = \mu_n Q_i W \frac{1}{C} \frac{dQ_i}{dz} = \frac{1}{2} \frac{\mu_n}{C} \frac{d}{dz} Q_i^2$ (4)

Integrate (4): $IL = W \frac{\mu_n}{2C} (Q_s^2 - Q_d^2)$ (5)

Computing above threshold current more exactly #3/3

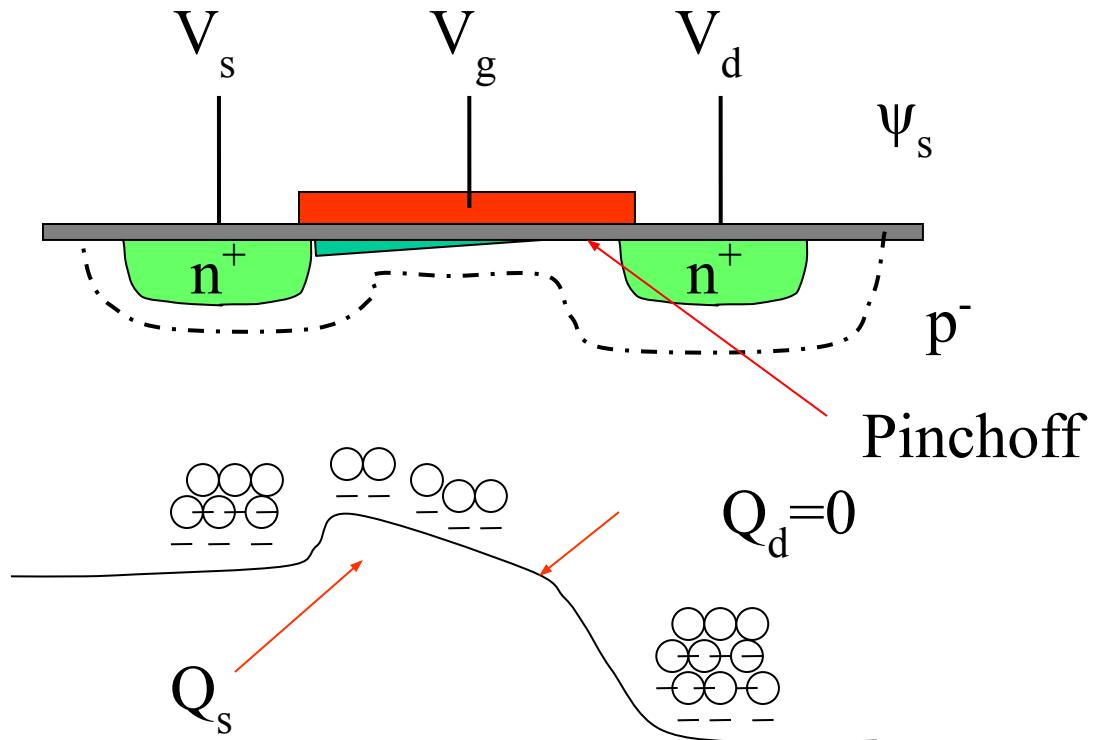
$$I = \frac{W}{L} \frac{\mu_n}{2C} \left(Q_s^2 - Q_d^2 \right)$$

$$Q_s = C_{ox} \left(V_g - V_{T0} - \frac{V_s}{\kappa} \right) \quad Q_d = C_{ox} \left(V_g - V_{T0} - \frac{V_d}{\kappa} \right) \quad \kappa = \frac{C_{ox}}{C_{ox} + C_{dep}}$$

$$I = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \kappa \left[\left((V_g - V_{T0}) - \frac{V_s}{\kappa} \right)^2 - \left((V_g - V_{T0}) - \frac{V_d}{\kappa} \right)^2 \right]$$

$$I = \frac{\mu_n}{2} C_{ox} \frac{W}{L} \frac{1}{\kappa} \left[\left(\kappa(V_g - V_{T0}) - V_s \right)^2 - \left(\kappa(V_g - V_{T0}) - V_d \right)^2 \right]$$

Above Threshold nFET in Saturation #4/3



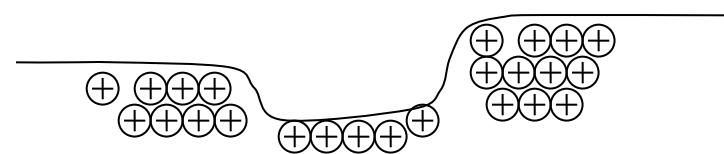
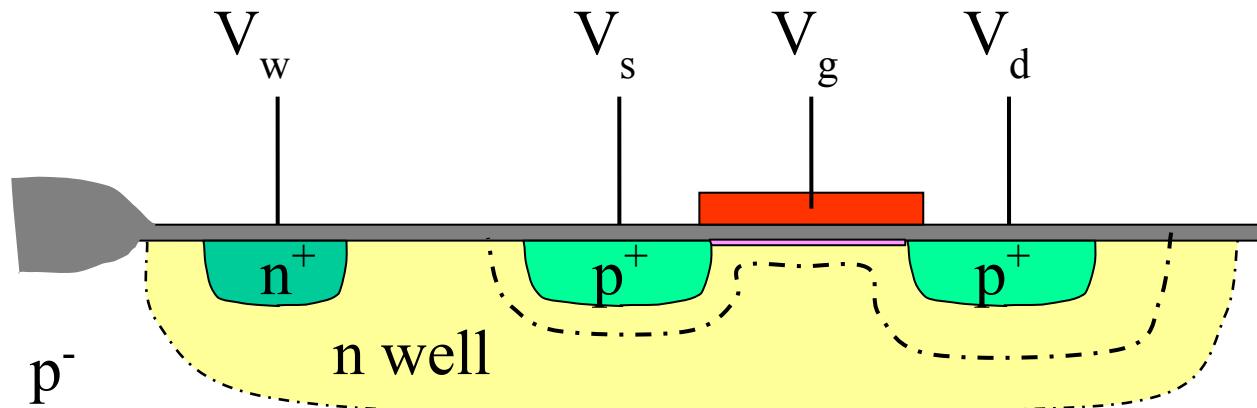
Set $Q_d = 0 \Rightarrow$

$$I = I_f = \frac{\beta}{2\kappa} \left[(\kappa(V_g - V_{T0}) - V_s)^2 \right]$$

$$= \frac{\beta}{2} \left[(V_g - V_T)^2 \right]$$

Above Threshold pFET

well (back gate) source gate drain



Everything works the same except all voltage polarities are flipped and n-well voltage is the reference; it is usually V_{dd}

5 minute break

Reminder to stop and restart zoom recording

The specific current I_s

- The **specific current** is defined as

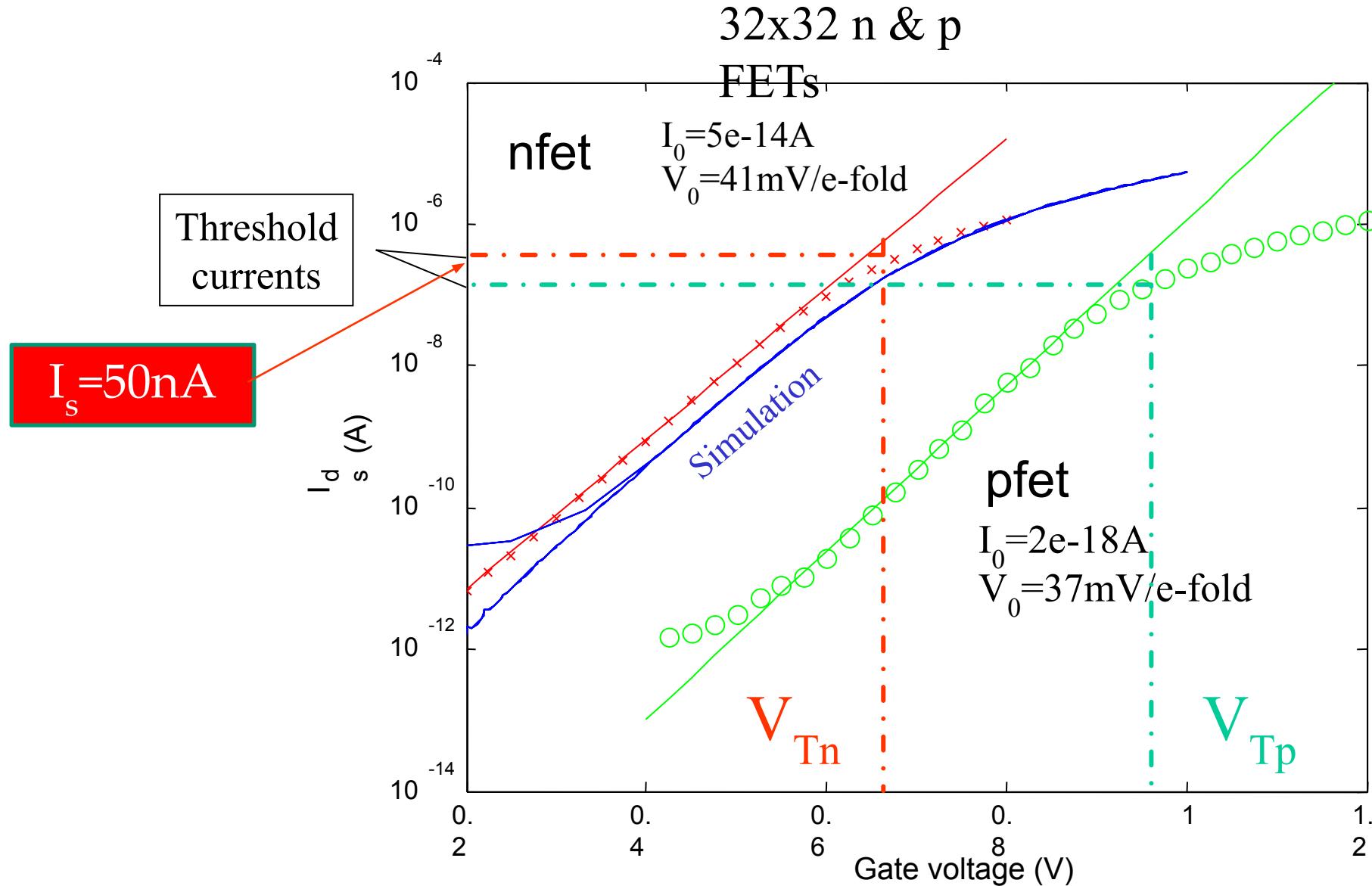
$$I_s = 2\mu C_{ox} \frac{W}{L} U_T^2 = 2\beta U_T^2$$

- It is approximately the current at a gate overdrive of $V_{ov} = V_g - V_T = U_T$
- This current is a working definition of the border between weak and strong inversion (the middle of moderate inversion).
- Knowing β and V_T , you can estimate I_s —very useful for a designer to know where the transistor will be working, given a current
- Example (compare with slide 13):

If $\mu_n = 400 \text{ cm}^2/\text{Vs}$, $C_{ox} = 1 \text{ fF}/\mu\text{m}^2$, $\frac{W}{L} = 1$

$$I_s = 2 \times \frac{400 \text{ cm}^2}{\text{Vs}} \times \left(\frac{1 \text{ m}}{100 \text{ cm}} \right)^2 \times \frac{1e-15 \text{ F}}{(1e-6 \text{ m})^2} \times (25e-3 \text{ V})^2 = 50 \text{ nA}$$

Slide 13 again: subthreshold transconductance



$$I_{ds} = I_0 e^{\frac{V_g}{V_0}}$$

Mobility is a function of electric field

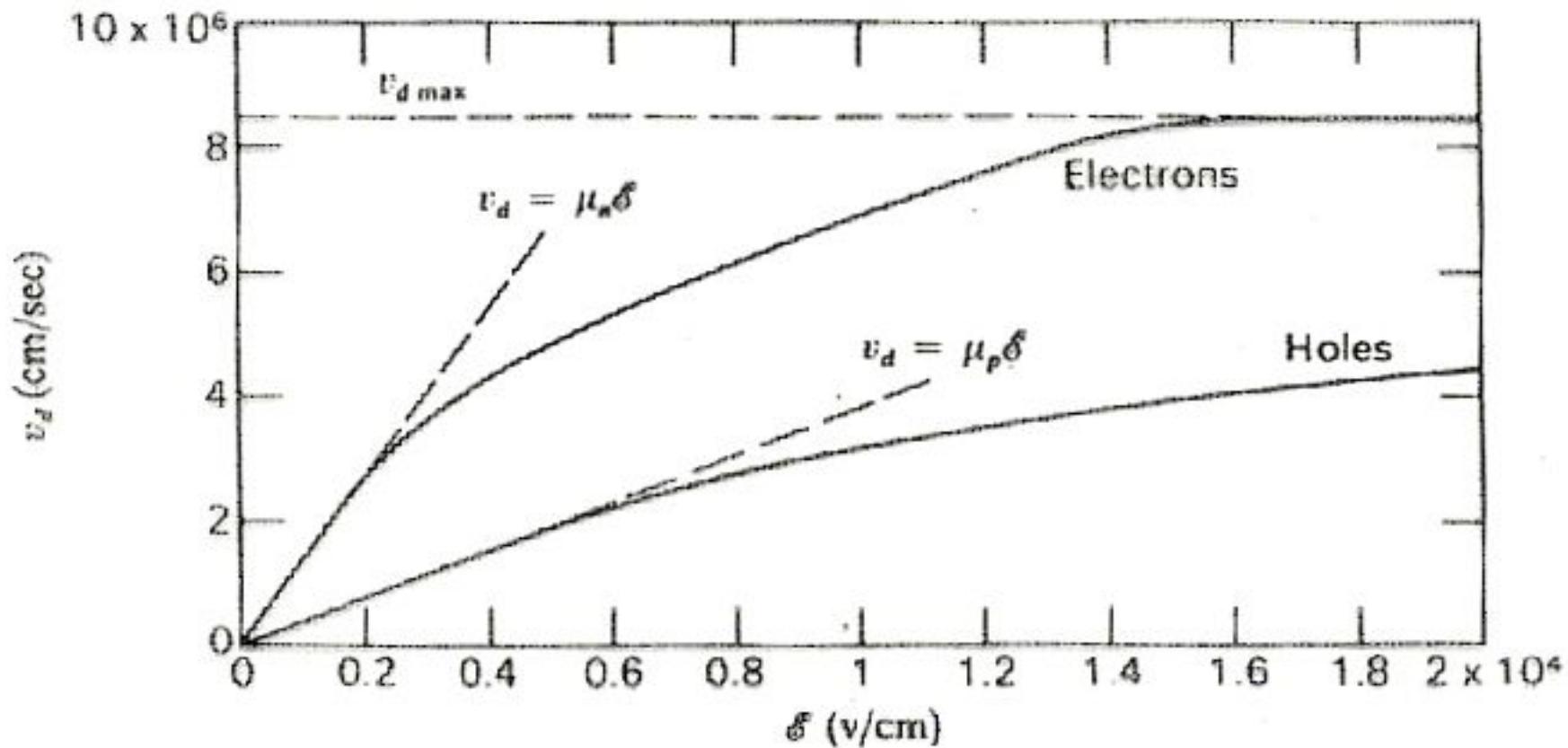


Fig. 4.10 Effect of electric field on the magnitude of the drift velocity of carriers in silicon.³

Reminder from first lecture:
Mobility is a function of electric field

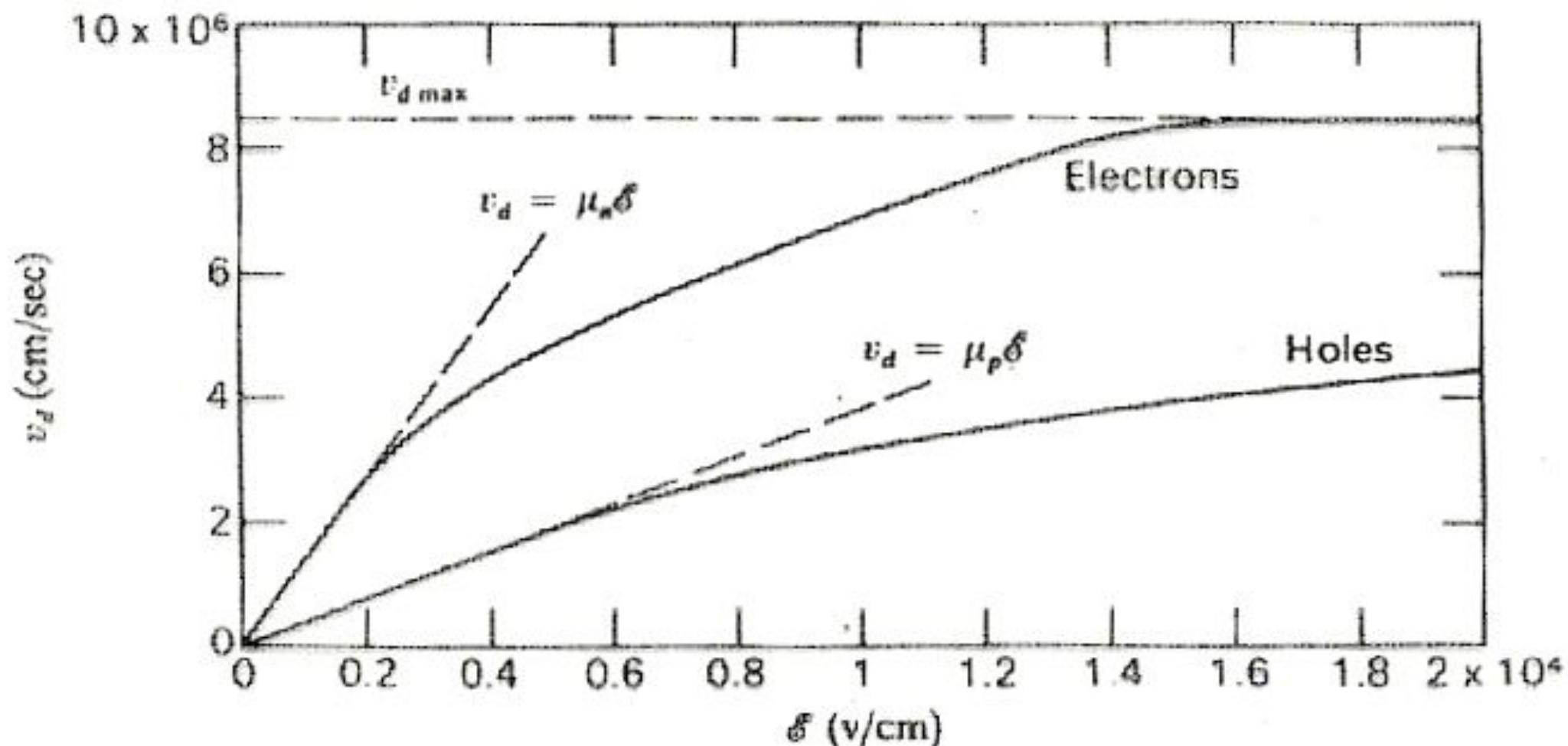
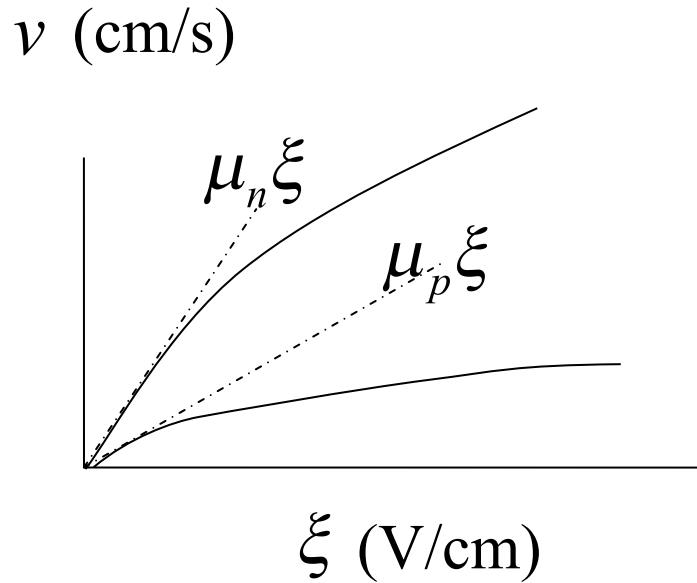


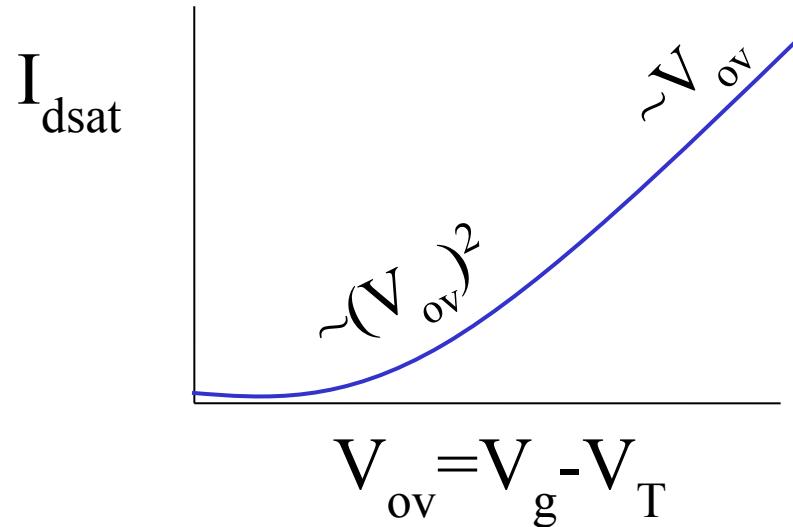
Fig. 4.10 Effect of electric field on the magnitude of the drift velocity of carriers in silicon.³

I_{dsat} is *linear* in gate overdrive when
velocity saturation limits it

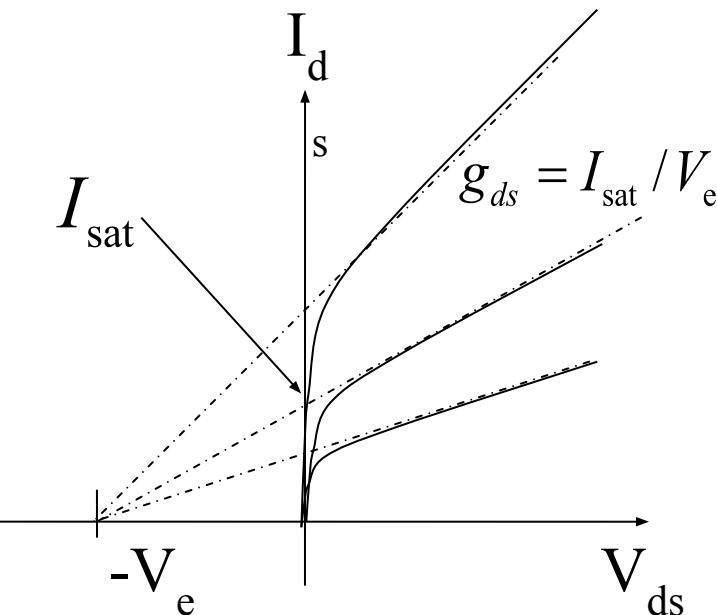


When channel is short and field is high along channel then carriers saturate at thermal velocity

Saturation current is then linear in overdrive



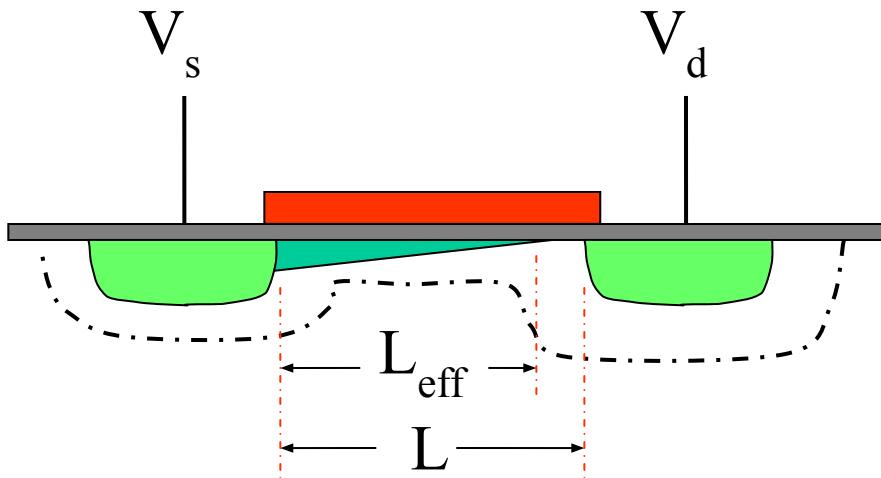
Drain conductance: the Early effect (named after Jim Early from bipolar transistor era)



(Early voltage)

- I_{ds} appears to have a finite conductance
- This conductance is proportional to the saturation current
- It comes from channel length modulation induced by drain voltage changes

Early Effect channel length modulation calculation



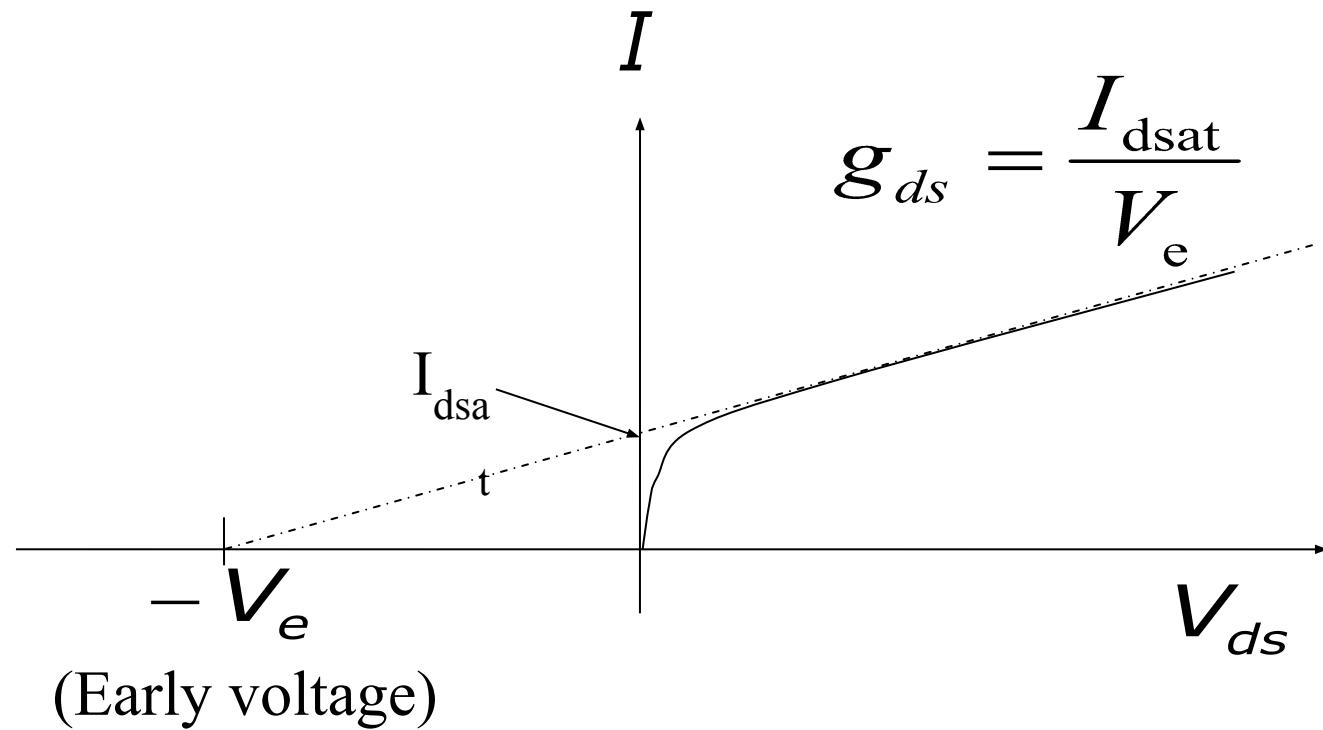
$$g_d = \frac{\partial I}{\partial V_{ds}} = \frac{\partial I}{\partial L_{eff}} \frac{\partial L_{eff}}{\partial V_{ds}}$$
$$I \propto \frac{1}{L} \quad \text{so} \quad \frac{\partial I}{\partial L_{eff}} = \frac{-I}{L_{eff}}$$

$$g_d = \frac{-I}{L_{eff}} \frac{\partial L_{eff}}{\partial V_{ds}} = \frac{I}{V_e} \quad \text{where} \quad -\frac{1}{V_e} = \frac{1}{L_{eff}} \frac{\partial L_{eff}}{\partial V_{ds}}$$

Note how V_e goes like L , because the length modulation effect decreases as the transistor channel becomes longer

$$I = I_{sat} + g_d V_d = I_{sat} \left(1 + \frac{V_d}{V_e} \right)$$

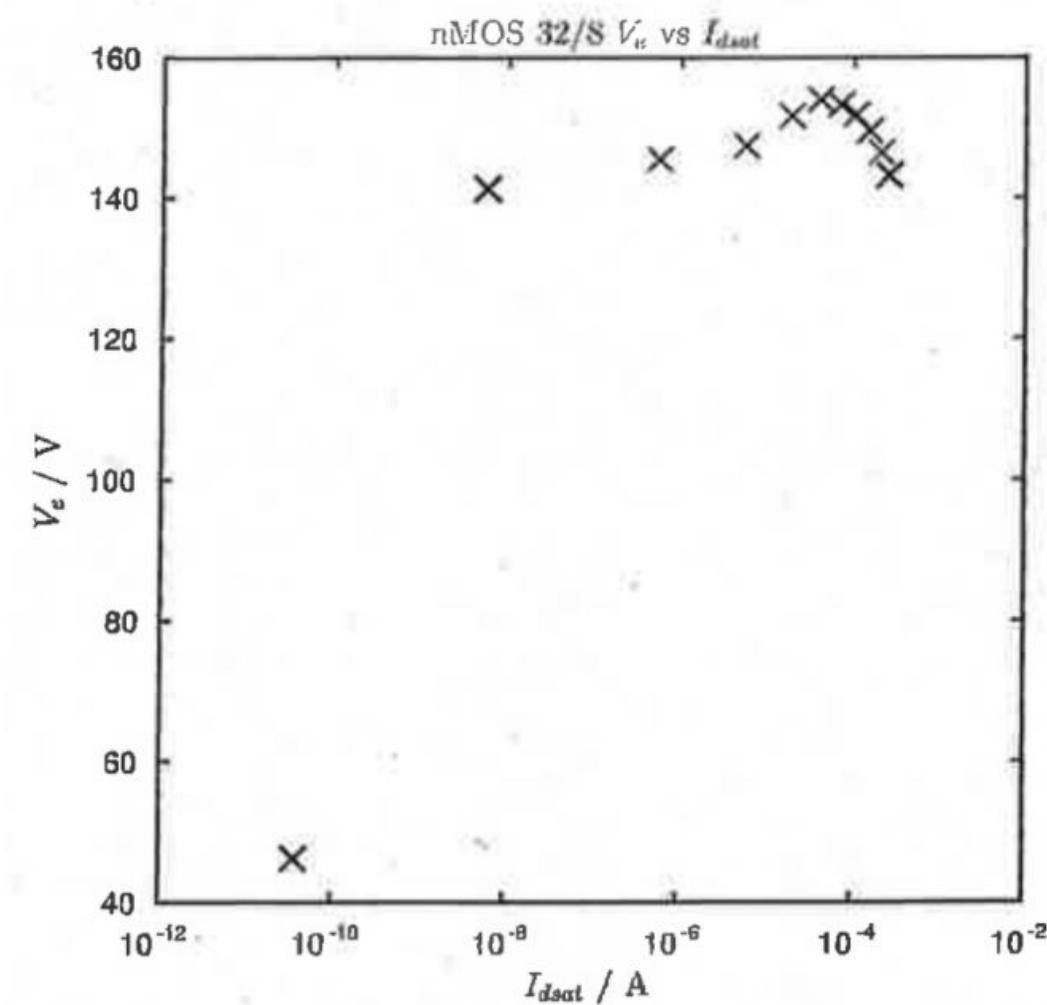
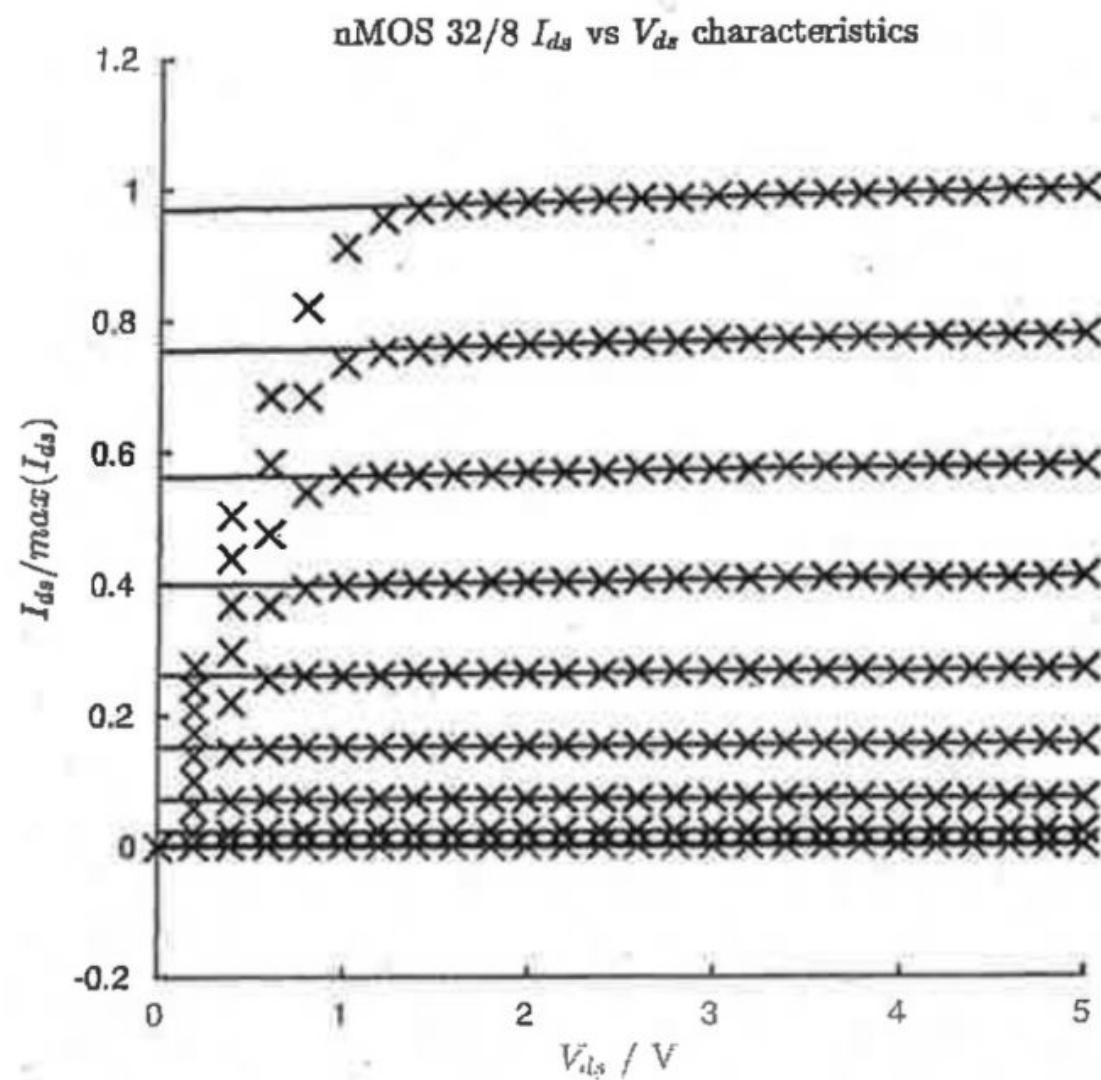
Early Voltage



V_e is not really constant with V_d or I_d . It is just the 1st order approximation to reality

Early effect measurements

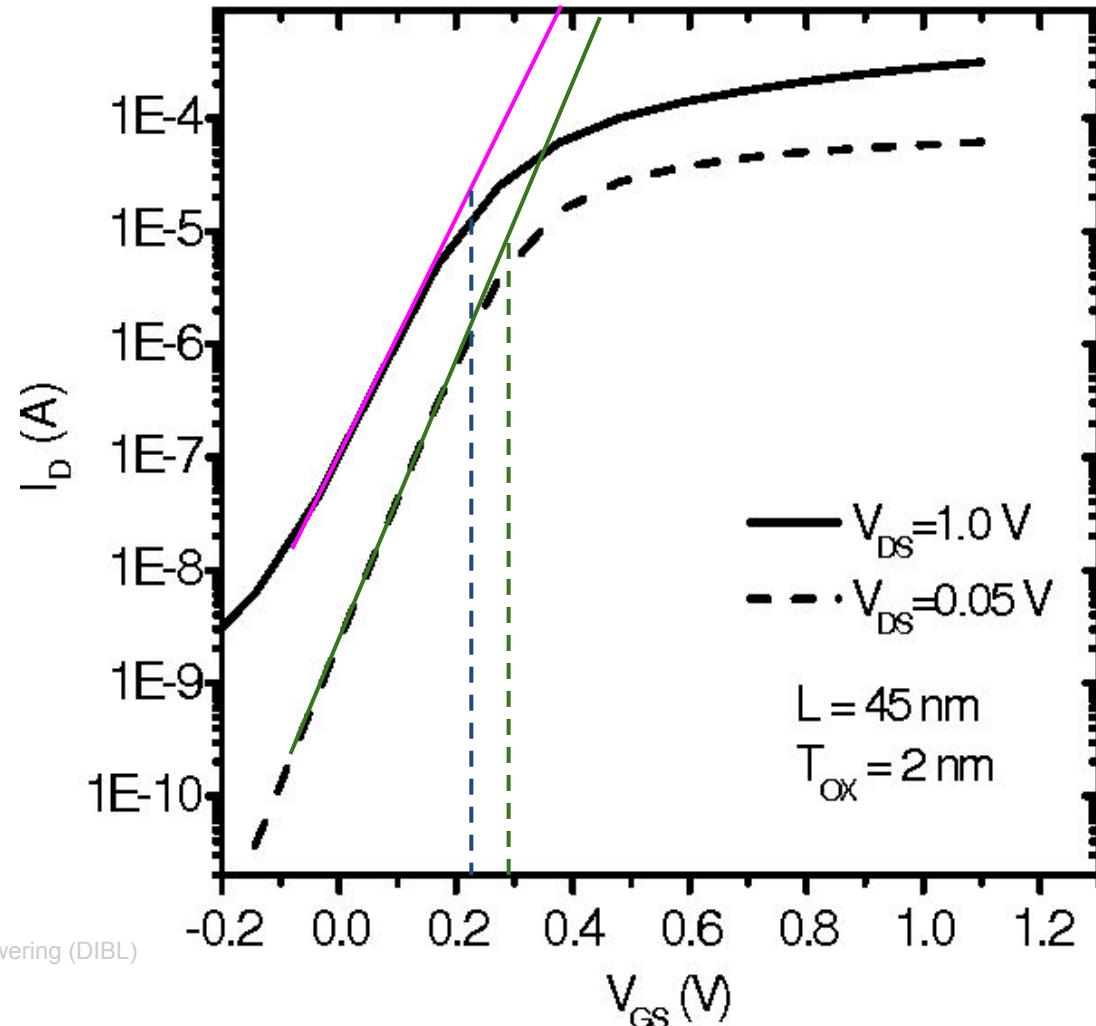
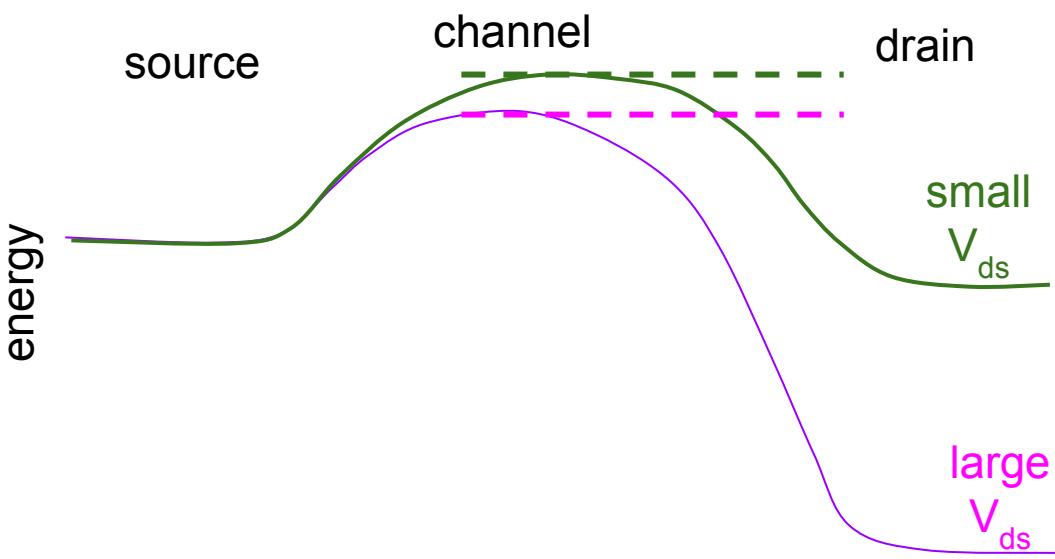
from 2015 measurement of 1.5um classchip



2nd Order Drain effects: DIBL

- DIBL=Drain Induced Barrier Lowering

- Increased drain voltage lowers the energy barrier by reaching through the channel all the way to the source.
- Especially occurs in short transistors.
- Large drain voltage decreases V_T by hundred mV or so.

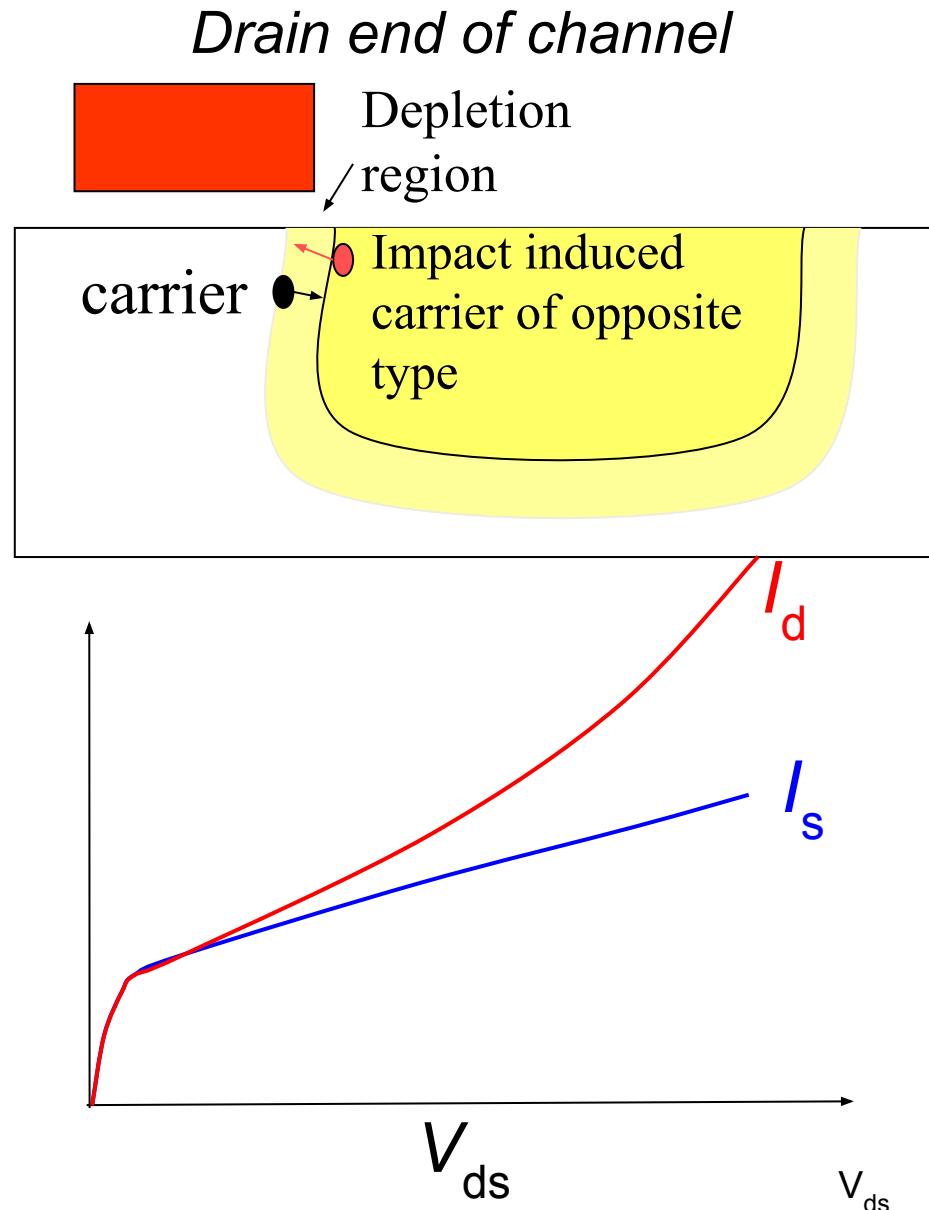


Karim, M., S. Venugopalan, Y. Chauhan, D. Lu, A. Niknejad, and C. Hu. 2011. "Drain Induced Barrier Lowering (DIBL) Effect on the Intrinsic Capacitances of Nano-Scale MOSFETs."

<https://www.semanticscholar.org/paper/25e505ec53e87299cccd96e87c31e9837ec4df3fa>

2nd Order Drain effects: Impact Ionization

- Impact Ionization
 - Only occurs if drain voltage is high enough to give electrons ionization energy.
 - Drain current is larger than source current.
 - Electrons gain enough energy to create new hole/electron pairs; the holes are pulled by E field to substrate.
- Both DIBL and Impact Ionization look approx. exponential in the drain voltage



Subthreshold nFET Conductances

Subthreshold nFET in saturation

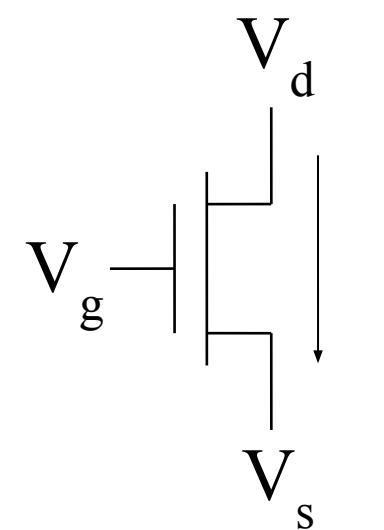
$$I = I_0 e^{\frac{\kappa V_g - V_s}{U_T}}$$

Subthreshold Gate Transconductance

$$g_m = \frac{\partial I}{\partial V_g} = \frac{\kappa I}{U_T}$$

Subthreshold Source Conductance

$$g_s = \frac{\partial I}{\partial V_s} = \frac{-I}{U_T}$$



Drain Conductance

$$g_{ds} = \frac{I_{dsat}}{V_e}$$

Above-threshold nFET Conductances

Saturation Region

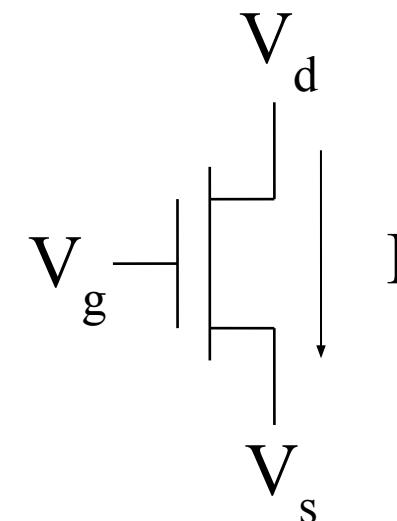
$$I_{dsat} = \frac{\beta}{2} \left[(V_g - V_T)^2 \right] = \frac{\beta}{2} V_{ov}^2 \quad \beta = \mu C_{ox} \frac{W}{L}$$

Above-threshold Gate

Transconductance

$$g_m = \frac{\partial I}{\partial V_g} = \beta(V_g - V_T) = \beta V_{ov} = \sqrt{\frac{2I}{\beta}}$$

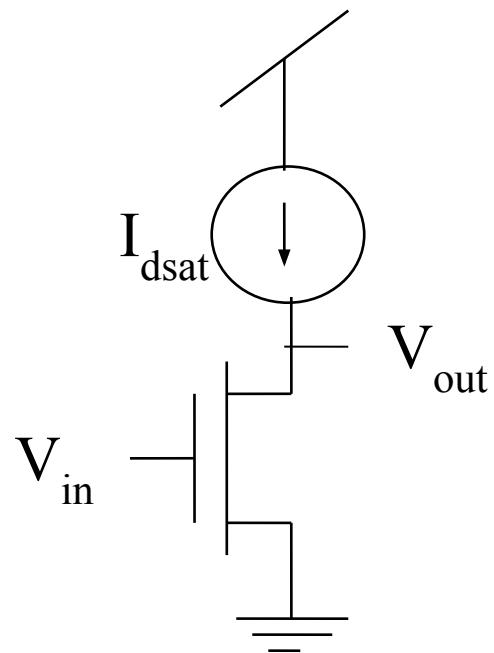
Gate overdrive



Drain Conductance

$$g_{ds} = \frac{I_{dsat}}{V_e}$$

Quiz: What is the intrinsic voltage gain of a transistor?

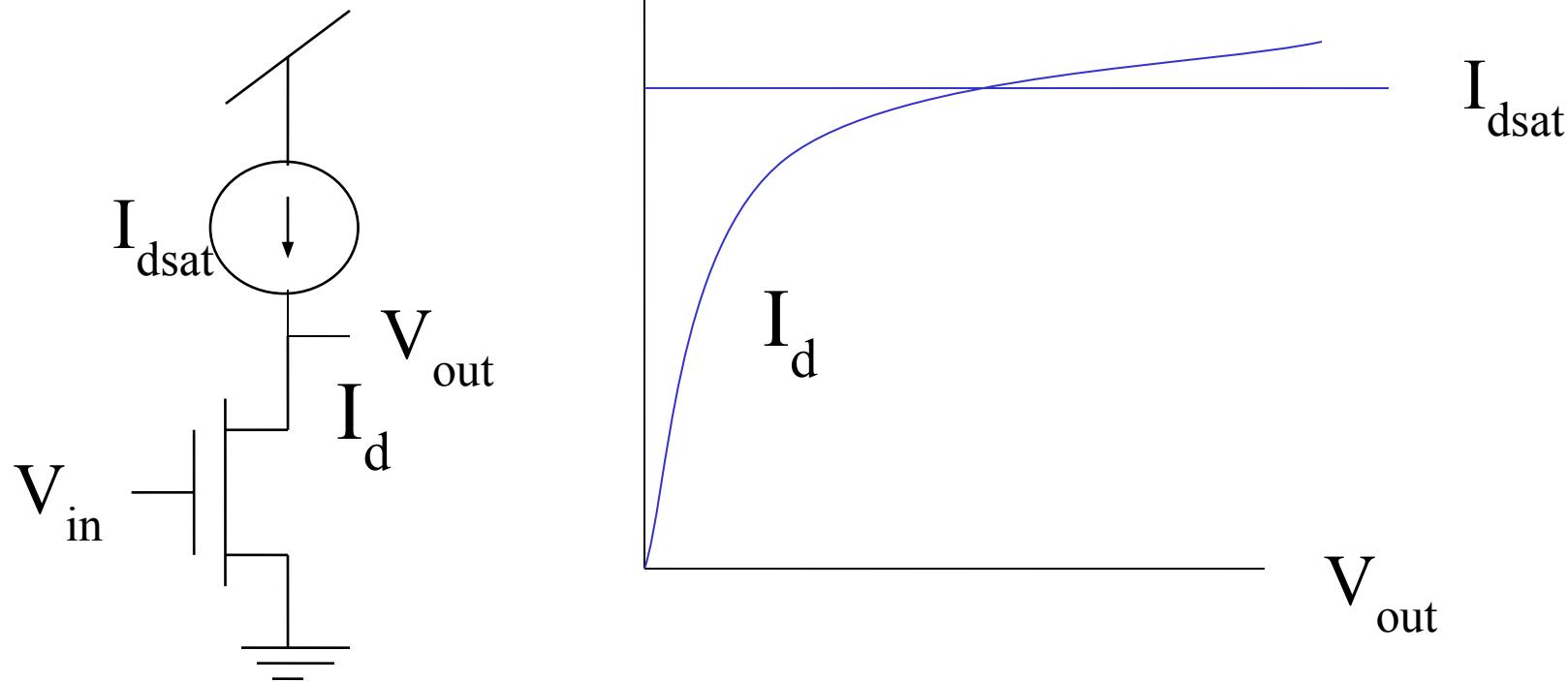


A perfect current source of value I_{dsat} is the load on the drain.

What is the voltage gain

$$A = -dV_{out}/dV_{in}?$$

Intrinsic voltage gain of a transistor



Hints: *Transconductance*: Use equivalent voltage dependent current source. *Drain conductance*: use parallel conductance

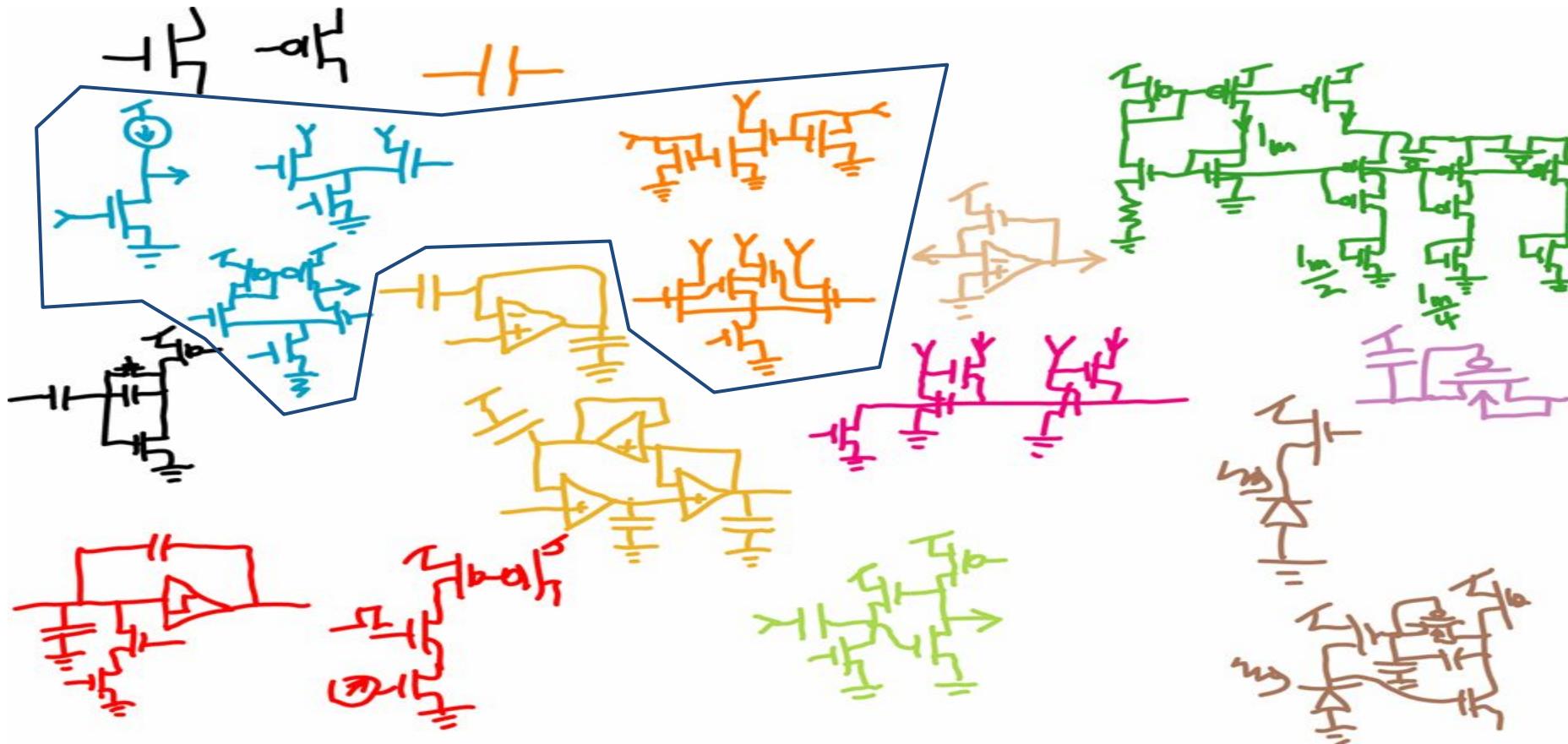
Actual transistor models for numerical simulation have *many* more parameters

SPICE BSIM 3v3 parameters

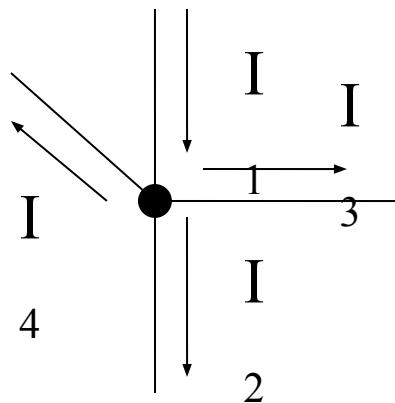
```
1 * DATE: Sep 18/03
2 * LOT: T37E          WAF: 0097
3 * Temperature_parameters=Default
4 .MODEL rmos1 NMOS (
5 +VERSION = 3.1           TNOM   = 27           LEVEL   = 49
6 +XJ      = 1E-7          NCH    = 2.2E17        TOX     = 7.7E-9
7 +K1      = 0.5833102     K2     = 5.647696E-3  VTH0    = 0.4880389
8 +K3B     = -10           W0     = 7.338516E-6  K3      = 5.9079814
9 +DVTOW   = 0             DVT1W   = 0            NLX     = 2.84499E-7
10 +DVTO   = 2.1441956    DVT1   = 0.7522377   DVT2    = -0.3
11 +U0     = 376.7345667   UA     = -5.34179E-10  UB     = 1.996229E-18
12 +UC     = 3.317139E-11  VSAT   = 1.651673E5   A0      = 1.0614003
13 +AGS    = 0.1210821    BO     = 7.31447E-7   B1      = 5E-6
14 +KETA   = 2.815182E-3  A1     = 0            A2      = 0.4307747
15 +RDSW   = 1.128276E3   PRWG   = -0.0772184  PRWB   = -0.109444
16 +WR     = 1             WINT   = 1.508923E-7  LINT   = 0
17 +XL     = -5E-8         XW     = 1.5E-7        DWG    = -2.852237E-9
18 +DWB    = 1.865087E-9  VOFF   = -0.0855312  NFACTOR = 1.6879905
19 +CIT    = 0             CDSC   = 2.4E-4       CDSCD   = 0
20 +CDSCB  = 0             ETAO   = 0.7          ETAB    = 0.0325933
21 +DSUB   = 0.7929405    PCLM   = 1.9809329   PDIBLC1 = 2.864232E-3
22 +PDIBLC2 = 2.23503E-6  PDIBLCB = -1E-3      DROUT   = 0
23 +PSCBE1  = 7.792935E8  PSCBE2 = 1E-3        PVAG    = 0.5319574
24 +DELTA   = 0.01         RSH    = 79           MOBMOD  = 1
25 +PRT    = 0             UTE    = -1.5         KT1     = -0.11
26 +KT1L   = 0             KT2    = 0.022        UAI     = 4.31E-9
27 +UB1    = -7.61E-18     UC1    = -5.6E-11     AT      = 3.3E4
28 +WL     = 0             WLN    = 1            UW     = 0
29 +WWN    = 1             WWL    = 0            LL      = 0
30 +LLN    = 1             LW     = 0            LWN    = 1
31 +LWL    = 0             CAPMOD = 2           XPART   = 0.5
32 +CGDO   = 2.68E-10      CGSO   = 2.68E-10    CGBO    = 1E-12
33 +CJ     = 9.289554E-4   PB     = 0.8          MJ      = 0.3513355
34 +CJSW   = 3.454219E-10  PBSW   = 0.8          MJSW    = 0.1369253
35 +CJSWG  = 1.82E-10      PBSWG = 0.8          MJSWG   = 0.1369253
36 +CF     = 0             PVTTH0 = -0.0275935  PRDSW   = -109.7848325
37 +PK2    = 2.740574E-3   WKETA = -1.803631E-3  LKETA   = 4.876318E-3
38 *
```

THE END

Next week: Some static circuits.



Kirchhoff's Current Law (KCL)

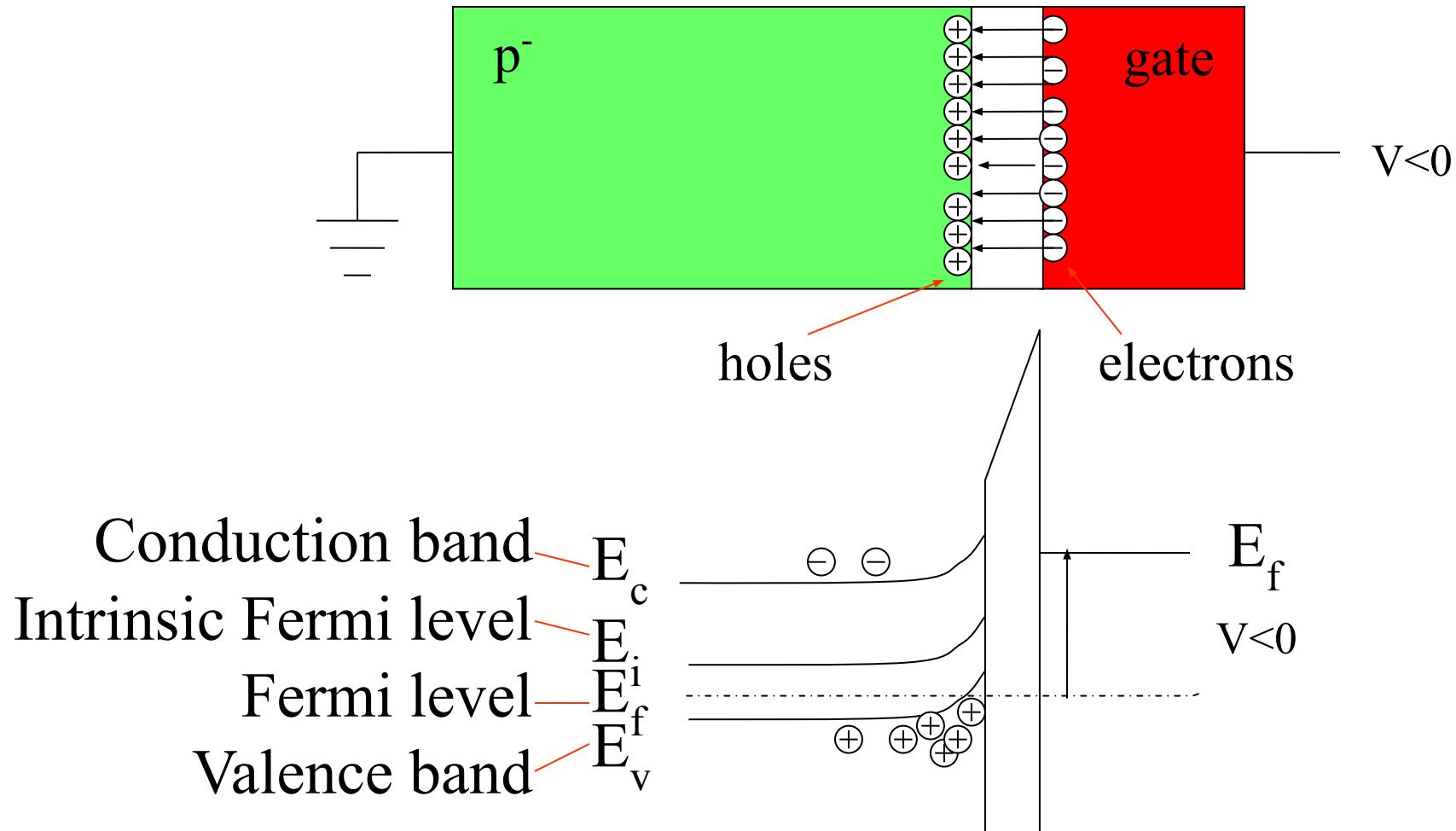


Sum of currents entering = sum of currents leaving node

Net current at a node=0

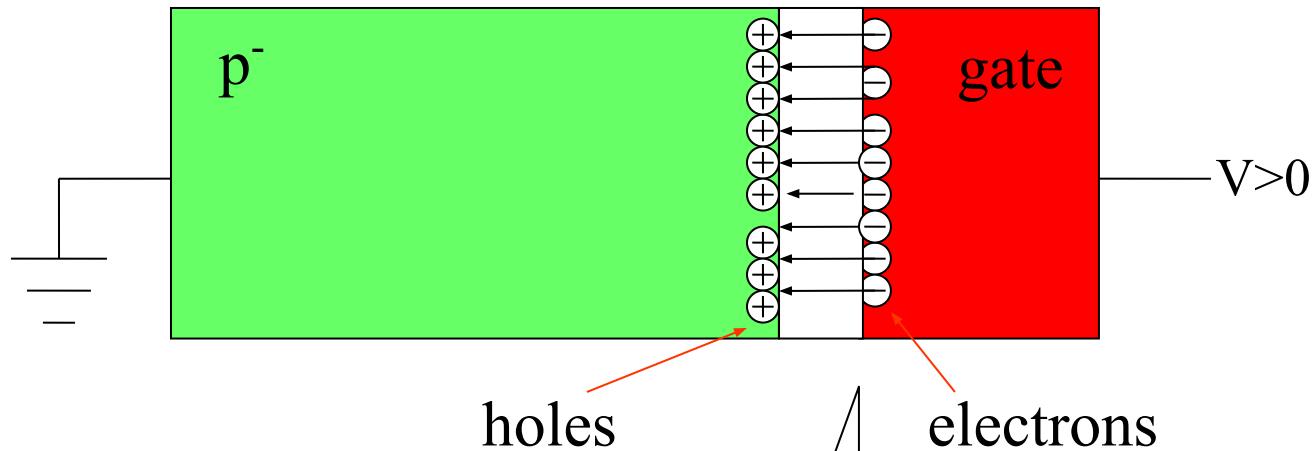
$$I_1 = I_2 + I_3 + I_4$$

Electrostatics of the MOS Structure



Accumulation
MOS Transistors II

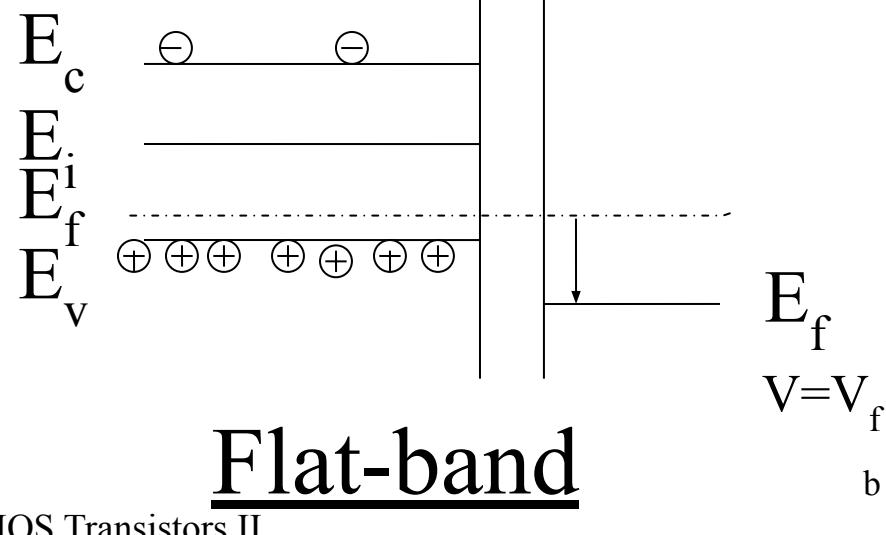
Electrostatics of the MOS Structure



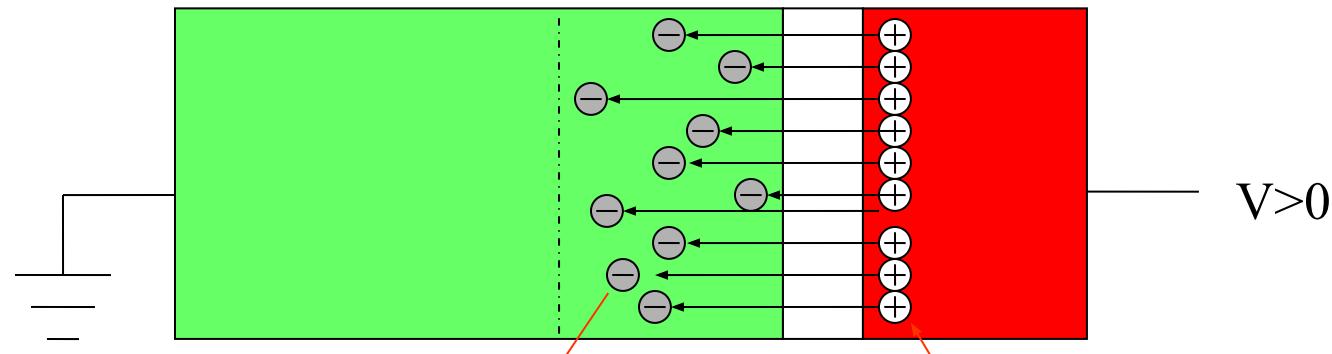
V_g (flat-band voltage)

= gate voltage when

$$\psi_s = 0$$

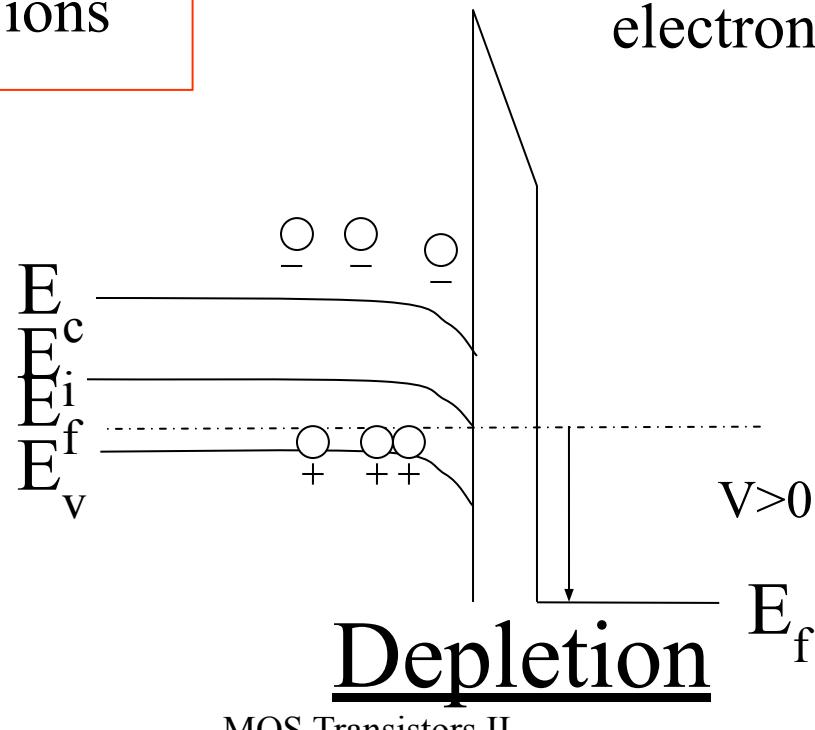


Electrostatics of the MOS Structure (II)

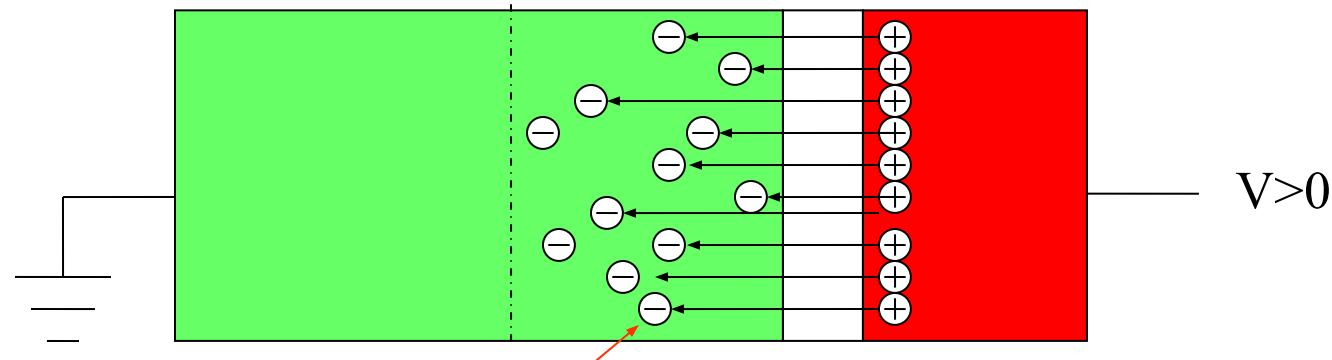


Fixed ions

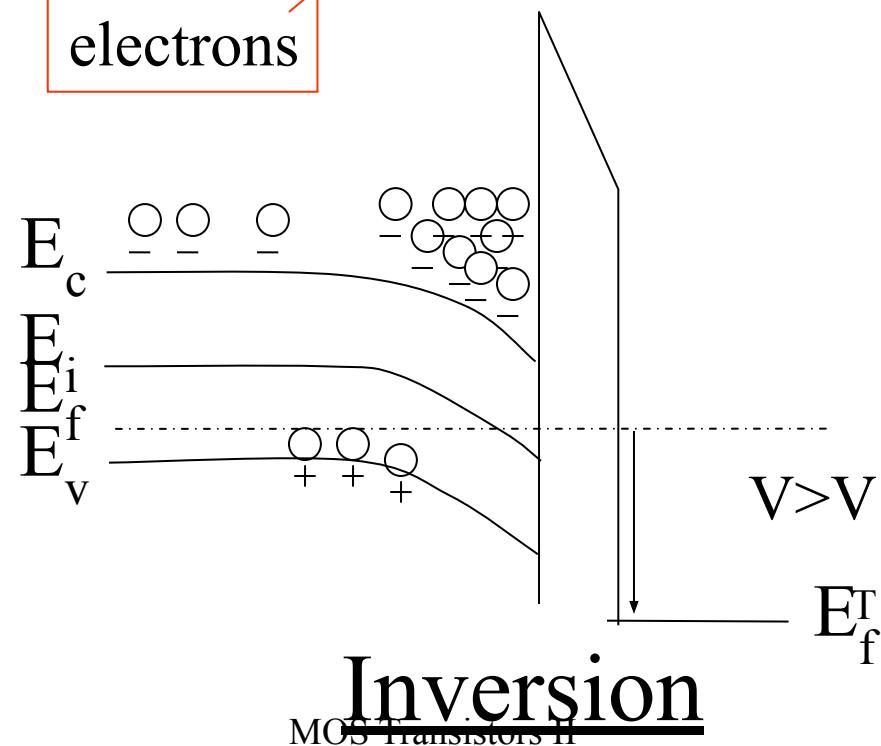
electrons



Electrostatics of MOS structure (III)

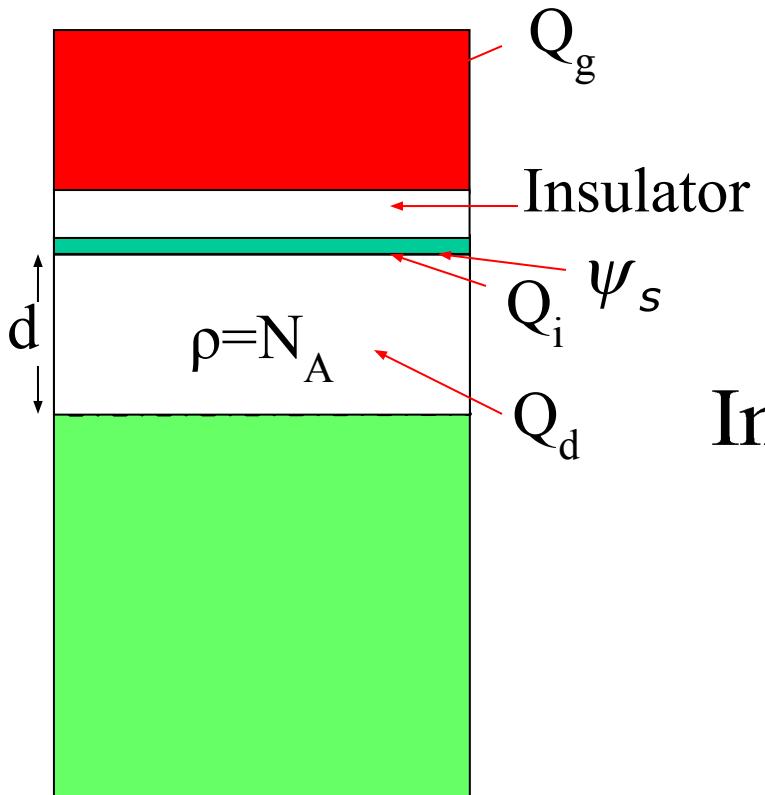


electrons



Inversion
MOS Transistor II

MOS Structure in Inversion



Poisson's equation

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho}{\epsilon_s} = \frac{qN_A}{\epsilon_s} \quad (1)$$

Integrate (1) $\Rightarrow \psi_s = -\frac{\rho d^2}{2\epsilon_s}$

$$\Rightarrow d = \sqrt{\frac{2\epsilon_s \psi_s}{qN_A}}$$

$$Q_g = Q_d + Q_i$$

$$Q_d = -qN_A d = -\sqrt{2\epsilon_s \psi_s qN_A}$$

Threshold Voltage of nFET

$$V_{T0} = V_{fb} + 2\psi_B - \frac{Q_d}{C_{ox}} \quad (1) \quad V_{T0} = \text{threshold voltage when } V_s = 0$$

V_{fb} = flat-band voltage

$2\psi_B$ = surface potential of channel when free electron concentration in channel=acceptor ion concentration

Q_d = depletion space charge at threshold

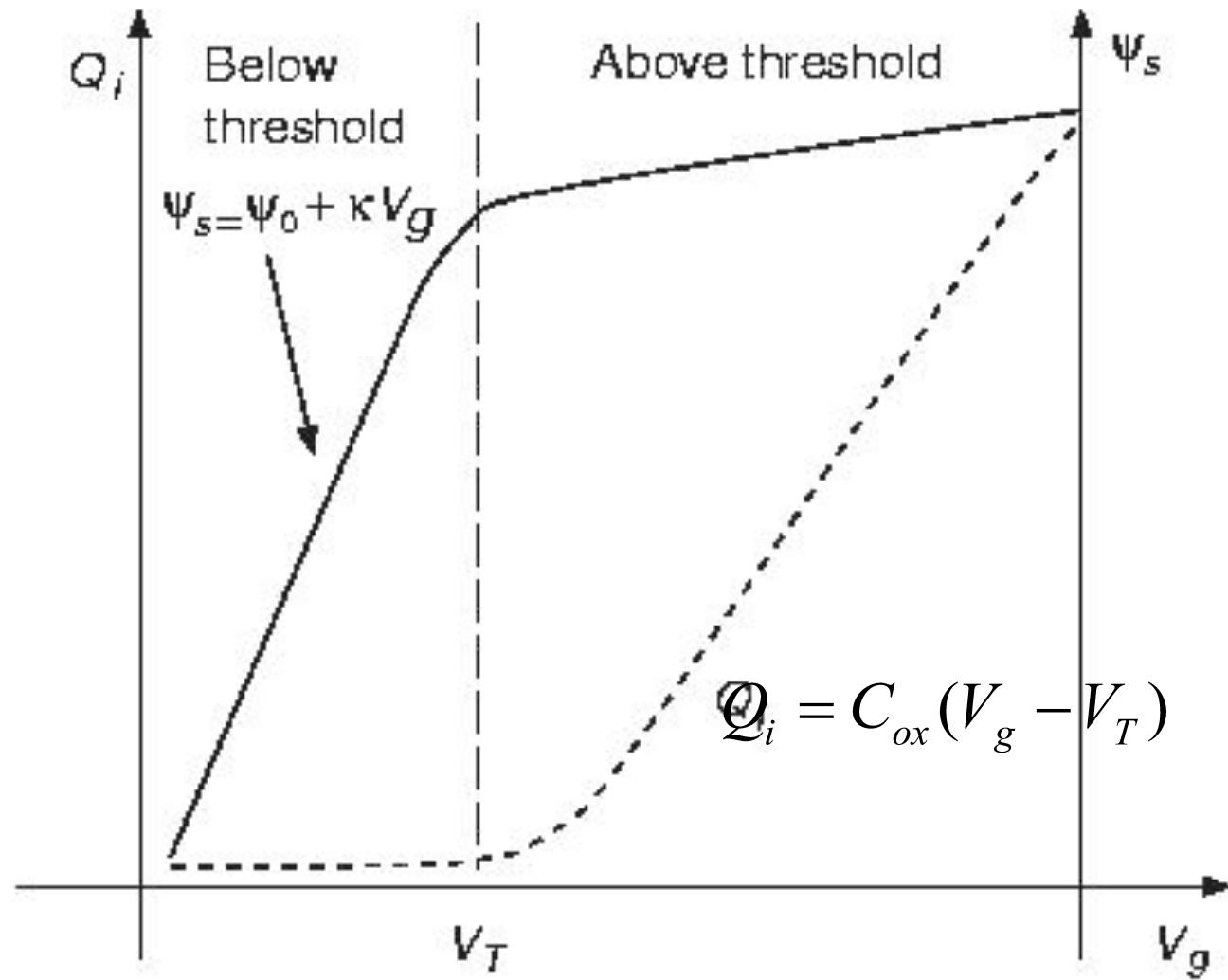
C_{ox} = gate oxide capacitance

Substitute $Q_d = -2\sqrt{\epsilon_s q N_A \psi_B}$ in (1)

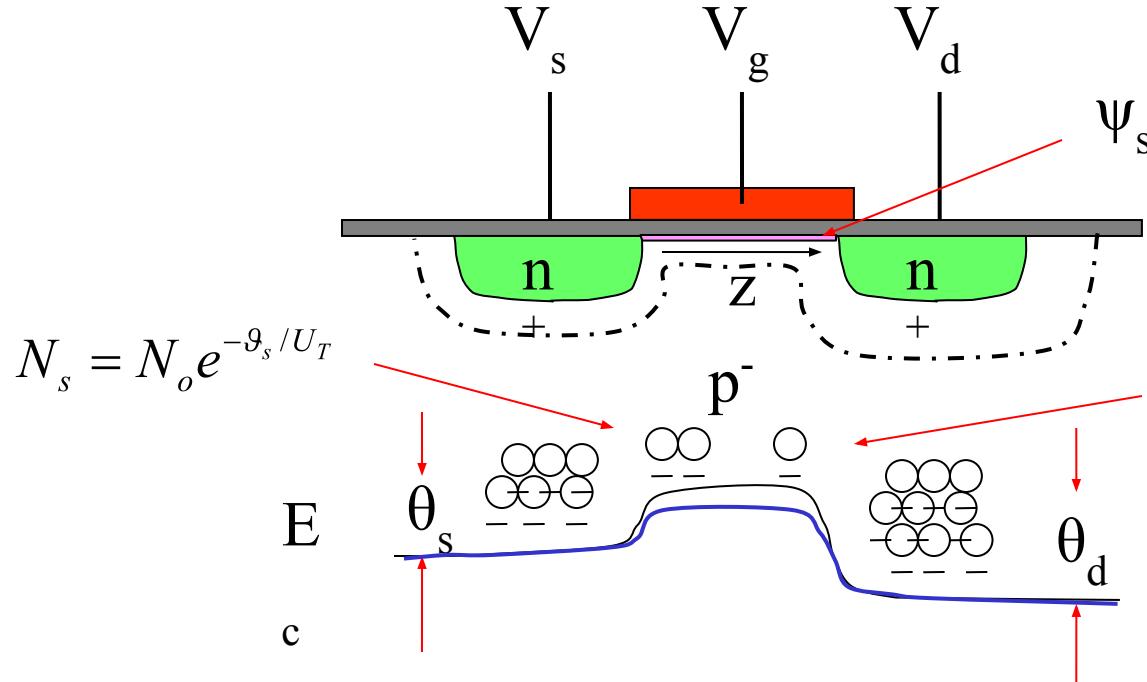
$$V_{T0} = V_{fb} + 2\psi_B + \gamma \sqrt{2\psi_B}$$

$$\gamma = \frac{\sqrt{2\epsilon_s q N_A}}{C_{ox}} = \text{body factor coefficient}$$

nFet curve: Q_i vs V_{gs}



Subthreshold nFET



Surface potential

$$N_d = N_o e^{-\theta_d / U_T}$$

N =carrier density per unit volume

W =channel width

L =channel length

t =channel depth

D =diffusion constant

θ_0 =built-in voltage