Lab 10

November 23, 2018

Silicon Synaptic Circuits

This week, we will see how synaptic circuits generate currents when stimulated by voltage pulses. Specifically we will measure the response of the synapse to a single pulse, and to a sequence of spikes.

The objectives of this lab are to:

- Analyze log-domain synapse circuits.
- Measure the response properties of the diff-pair integrator synapse.

10.1 Prelab

10.1.1 A log-domain pulse integrator

1. Write the equations characterizing I_τ, I_w, I_c, and I_{syn} in Fig. 10.1, assuming all corresponding pFETs are in saturation and operate in weak-inversion.
2. Derive the circuit's response to a step input (*i.e.* $I_w > 0$).
3. Derive the corresponding equation when the input pulse is switched off (*i.e.* $I_w = 0$).

Suppose we stimulate the circuit with a regular spike train of frequency f.

1. What happens to V_{syn} in steady-state?
2. How is the response to a single spike related to the steady-state response (in terms of I_w and I_τ)?

10.2 This Week's Test Circuits

This week we will be using the Classchip 2005-rev1 chip. The pinout of the chip is shown in Fig. 10.2.

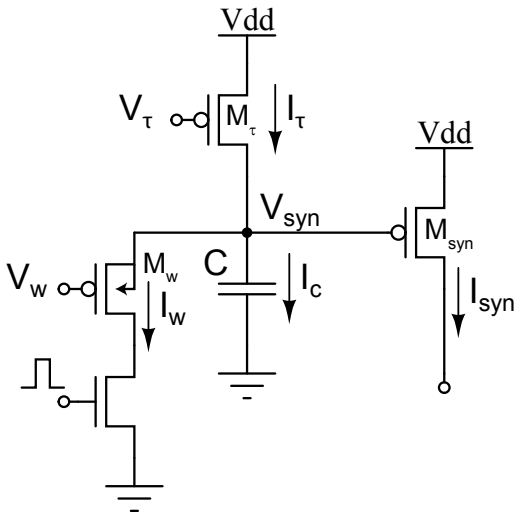

Figure 10.1: Schematic of a log-domain pulse integrator.

Don't forget to current-limit the power supply. Set FollBias (pin 5) to $\approx 0.7V$, connect pin 15 to *Gnd* and pins 25, 35 to V_{dd}. It is a good idea also to bias appropriately the N-FETs and P-FETs on the chip (*i.e.* connect pins 1, 2, 3, 4, 6, 7, 8 to V_{dd} and pins 9, 10, 11, 12, 13, 14 to *Gnd*).

10.3 Experiments

Experiment 1: Measuring the DPI's step response

You will need to use the function generator, the Keithley 230, and the oscilloscope to carry out this experiment.

Connect the synapse digital input (pin 37) to the function generator output. On the function generator change the frequency and duty cycle to generate a step that lasts a few milliseconds. Set the function generator to "burst" mode to generate a single step. Make sure that the DC offset is at 1.25V and an amplitude at 2.5 V. You can trigger the pulse manually by pressing "single". **Always make sure that the input goes between 0V and 5V.**

Use the potbox to set the *weight* (pin 27) and *tau* (pin 29) biases so that the transistors run in subthreshold. Tie the "enable" bias (pin 39) to 0V. Set the DPI *synthr* (pin 28) to a deep subthreshold bias (*e.g.* close to V_{dd}).

On the oscilloscope, trigger on the function generator output and measure the synapse V_{syn} node (pin 38) and the neuron's V_{mem} (pin 36). In order to measure V_{syn}, set the offset on the oscilloscope to around 5V so that you can use a scale of 100mV. (*Make sure that V_{syn} response is reasonable by first moving the biases around*).

Experiment with different values of *synthr* and *tau* to find the right range of parameters.

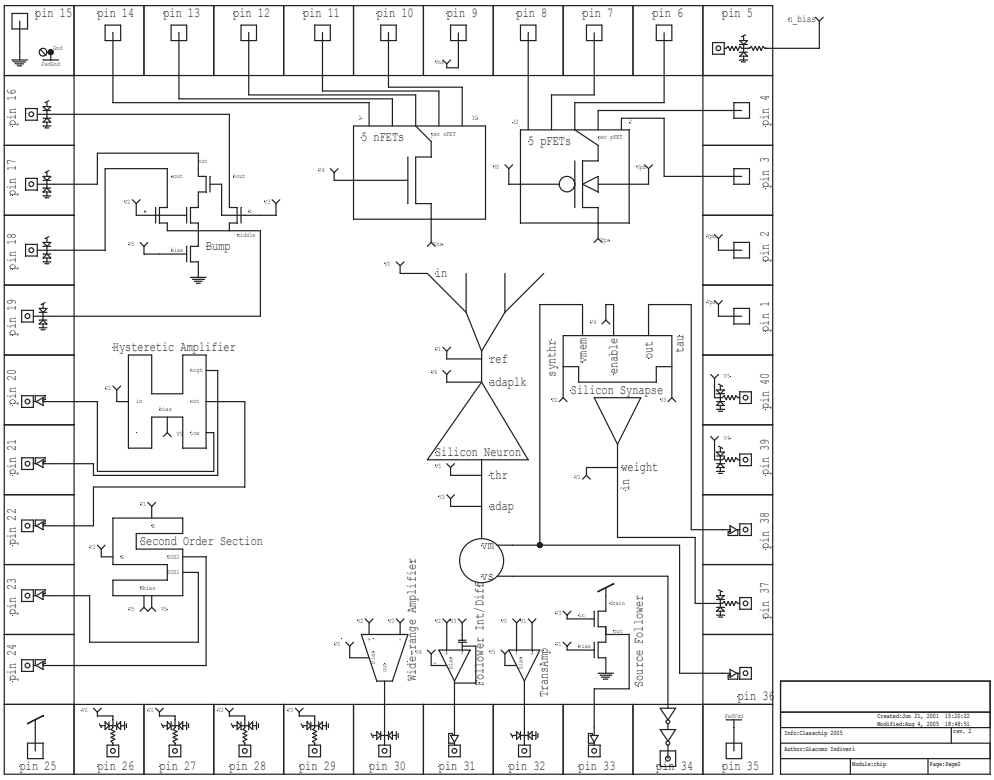

Figure 10.2: Pinout of the Classchip 2005-rev1.

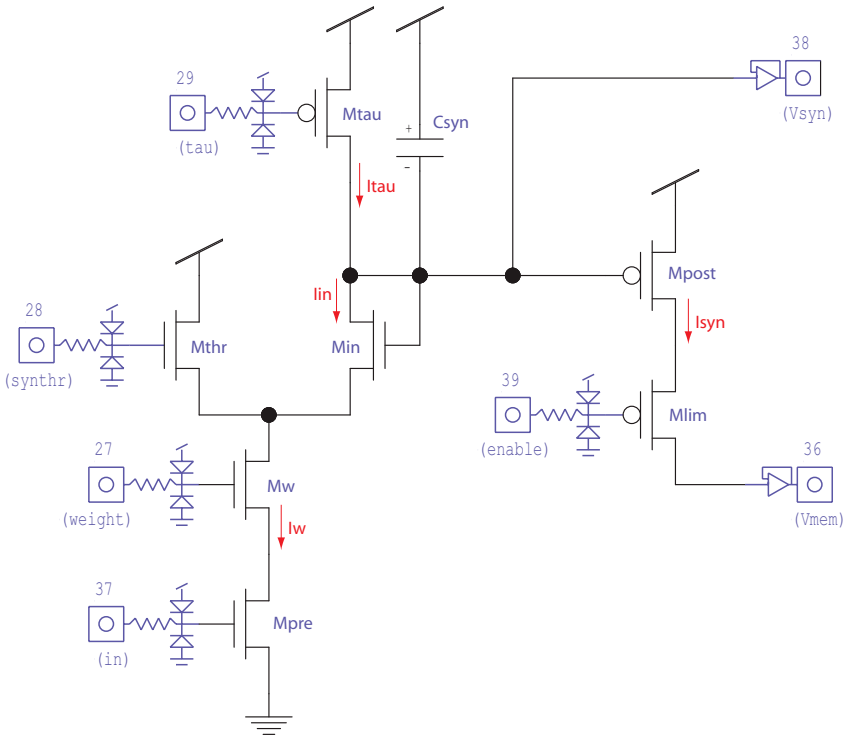

Figure 10.3: Schematic and pinout of the diff-pair integrator synapse.

Set the synapse's time constant to three reasonable values and plot V_{mem}, V_{syn}, and $exp(-V_{syn})$ in response to the step onset, for the different time-constant settings. On a separate graph, plot the same traces in response to the end of the step.

Experiment 2: Adjusting the DPI's response properties

In this experiment we will adjust the *synthr* value to compensate for variations in other parameters of the circuit.

Set the bias parameters of the synapse to reasonable values. Measure the response of the synapse to a single short pulse (you might need to adjust the frequency and duty cycle settings of the function generator).

Compute the EPSC by taking the derivative of V_{mem} and measure the EPSC peak.

Change the synapse's time constant and repeat the same experiment. Adjust *synthr* to obtain an equivalent EPSC peak with this different time-constant.

Hand in a graph with the two EPSC plots superimposed, specifying the values found for the time-constant and *synthr*.

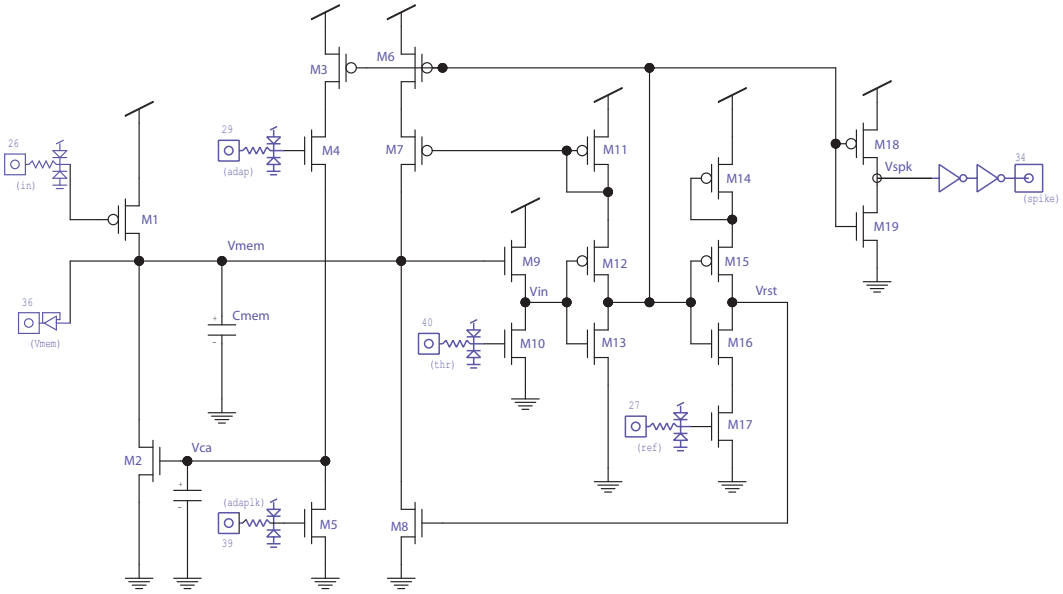

Figure 10.4: Schematic and pinout of the I&F neuron.

10.4 Postlab

Construct a circuit that updates its synaptic weight based on the STDP learning rule.

10.5 What we expect you to remember

The schematic for a synapse circuit. How the synaptic current changes as a function of the synaptic weight, the time constant, and the presynaptic frequency.

10.6 Next Week

Silicon neurons.