Lab 3

October 7, 2018

Transistors II – Transistor superthreshold saturation current and drain characteristics

The objective of this lab is to understand *super-threshold* (also called *above-threshold* or *strong inversion*) transistor operation and to understand transistor drain conductance characteristics, particularly *channel length modulation*. The specific experimental objectives of this lab are as follows:

1. To characterize drain current of a transistor as a function of gate voltage in superthreshold operation in the ohmic (triode) and saturation regions.
2. To characterize the drain saturation properties in sub- and super-threshold.
3. To characterize drain conductance (the Early effect) and how it scales with transistor length and saturation drain current.

An intuitive and quantitative understanding of all these effects, along with the subthreshold behavior from the first week, is useful for the design of effective circuits, especially analog design of high performance amplifiers.

This lab has a substantial pre-lab exercise that must be completed before coming to the lab session.

3.1 Terminology

- above-threshold = super-threshold = strong inversion
- sub-threshold = below-threshold = weak inversion
- triode region = ohmic region = linear drain conductance behavior with small drain-source voltage
- saturation = large V_{ds}
- overdrive = $V_{\mathrm{g}} - V_{\mathrm{T}}$
- $U_{\mathrm{T}} = kT/q$ = thermal voltage = 25mV at room temperature
- V_{T} = threshold voltage = 0.4V to 0.8V depending on process

3.2 Useful Quantities

The following is a list of the physical parameters and constants we will be referring to in this lab, along with their values when appropriate. The units that are most natural for these quantities are also included; these units are not self–consistent, so make sure you convert the units when appropriate.

ε_0	Permittivity of vacuum = 8.86e-12 F/m
ε_{Si}	Permittivity of Si = $11.7\varepsilon_0$
ε_{ox}	Relative permittivity of SiO_2 = $3.9\varepsilon_0$
μ_n	electron surface mobility, cm^2/V–sec
μ_p	hole surface mobility, cm^2/V–sec
C_{ox}	gate capacitance across the oxide per unit area, $fF/\mu m^2$
C_{dep}	capacitance of depletion region per unit area, $fF/\mu m^2$
t_{ox}	gate oxide thickness = 300Åfor the class chip in 1.6um techology.
V_T	threshold voltage, V (V_{T0} is V_T when V_s = 0).
W	electrical width of transistor channel, μm
L	electrical length of transistor channel, μm
β	$\equiv \mu C_{ox} W/L$, $\mu A/V^2$
V_E	Early voltage, characterizes drain conductance.

3.3 Prelab

Assume that all questions apply to the native device in a p-substrate, n–well process, i.e. an n–fet, unless stated otherwise.

1. Write the most general expression for I_{ds} above threshold in terms of V_g, V_s, V_d (all voltages are referenced to the bulk), and the parameters and constants given above. Leave out the drain conductance Early effect in this equation. Assume $\kappa = 1$ and that $V_{Tn} > 0$ and $V_{Tp} < 0$. What are the differences between this equation and that for the p–fet device?

2. Sketch graphs of the drain current vs. the drain voltage V_d for several gate voltages V_g above threshold, with $V_s = 0$. Indicate the ohmic and saturation regions and the behavior of the saturation voltage V_{dsat} as the gate overdrive voltage increases. How do these characteristics differ from the subthreshold ones?

3. Derive an expression for the current in the ohmic region, in terms of V_g and $V_{ds} \equiv V_d - V_s$, from the general I_{ds} equation. You may assume that $V_s = 0$. Sketch a graph of I_{ds} vs. V_g, showing V_{T0} and an expression for the slope.

4. State the drain voltage condition for above-threshold saturation and derive an expression for the saturation current, I_{dsat}, from the general I_{ds} equation. Sketch a graph of $\sqrt{I}_{dsat}$ vs. V_g with $V_s = 0$, showing V_{T0} and an expression for the slope.

5. Calculate C_{ox} for the classchip from the values given above. What is C_{ox} per square micron in fF?

6. Write the expression for the drain current in saturation including the Early effect, using I_{dsat} to represent the saturation current in the absence of the Early effect. Use V_E to represent the Early voltage.

7. Sketch the setups you will use.

3.4 Experiments

First, we want to remind you to be careful of static protection. Review the section in the Lab 2 handout which deals with this topic. Also, make sure the current limit on your power supply is set low (turned down to limit current to maximum 100mA or less) so if you hook the circuit up wrong, you won't blow up your chip by fusing a bonding wire or bonding pad.

You will use the same chip as in lab 2 (run number T71H-AF). The schematic of the test transistors is once more attached at the end of this lab as Fig. 3.2.

In the following two experiments, you will use the size W/L=32/32 n- and p-fet devices. (W and L mean width and length of the transistor channel in microns.) If this device is not functional, use the next shorter device. The only difference in the measurements is the drain-source voltage: in the first experiment you will use a small V_{ds}, in the second, a large V_{ds}. You can take all the data for experiments 1 and 2 in one quick session. *Draw a quick sketch of your setup before wiring up the chip, showing the Keithley instruments and the specific chip pin numbers.* Remember to use the + lead of the Keithley 236 (the K236 Hi input) to measure current – do not try to measure current into the - lead of the K236. Remember that the Lo input for the K236 is on the BNC, not the triax.

3.4.1 Experiment 1: Drain current in the ohmic region

In this experiment you will characterize the *linear* dependence of the current on the gate voltage in the strong-inversion ohmic region. For both native and well devices, measure I_{ds} as a function of V_g with $V_d = 50\text{mV}$ and $V_s = 0$.

Right after you measure I_{ds} for small V_{ds}, take the same data for $V_{ds} = V_{dd}$. You will use this data for the next experiment.

Sweep V_g from 0 to Vdd in steps of 100mV or less. From this curve, determine V_{T0} and β for both devices by fitting your data to the expression derived in the prelab. Include a single plot showing both native and well curves in your report. What is the ratio between β for the 2 devices? Does it make sense? Is the relationship between I_{ds} and $V_{gs} - V_T$ really linear? What is the likely cause of any discrepancy?

Extra credit

If things are going well, you may try the following analysis to determine the effective surface mobility, using the data you just collected. You may find it interesting to compare this mobility with the published bulk mobilities.

From the data you took above obtain a plot of μ_n and μ_p vs. V_g. Use the values for V_{T0} you obtained in the first part of this experiment. Display curves for both native and well devices on the same graph. Why does the mobility peak and then decay instead of remaining constant? What is the ratio between the peak mobilities for electrons and holes? How different are these values from the bulk mobilities for electrons and holes? (for electrons, $\mu_n = 1350\text{cm}^2/Vs$, for holes, $\mu_p = 480\text{cm}^2/Vs$

3.4.2 Experiment 2: Drain current in the saturation region

In this experiment you will characterize the *quadratic* dependence of the current on the gate voltage in the saturation region. Repeat Experiment 1, but this time use $V_{ds} = V_{dd}$. (If you planned ahead, you already have this data). Plot $\sqrt{I_{ds}}$ with appropriate fits and determine values for V_{T0} and β for both transistors. Again, include a single plot showing both native and well curves in your report.

Are the measurements of V_{T0} and β from the saturation measurement consistent with the values obtained in the ohmic region? Which is a better approximation, the linear one or the quadratic?

3.4.3 Experiment 3: Drain characteristics, the Early effect and drain conductance

In this experiment, with two possible choices, you will either characterize the drain conductances of 5 transistors of different lengths operating at the same gate source voltage, or you will characterize the drain conductance of a single transistor operating at several different current levels.

Your TA will tell you which of these measurements your group should do.

Drain characteristics of transistors vs. channel length

This experiment studies how Early voltage scales with transistor length.

At a single subthreshold gate voltage, for the 5 native transistors of different lengths, measure I_{ds} vs V_{ds}.

Do the drain currents scale with 1/length as you expect?

Extract the Early voltages for each device over the same drain voltage range (see Sec. 3.4.4) and plot the Early voltage versus drawn channel length. Remember that the transistor length is given in lambda, where lambda=0.8um.

Answer the following questions based on your measurements, and expectations from theory:

1. How linear is the relationship between transistor channel length and Early voltage?
2. What is the slope in volts/micron (V/um)?
3. Would you expect the drain resistance to be higher for native or well transistors?
4. Comment on your results: What do they imply about minimum channel length?
5. Does the scalar metric of V/um for Early effect provide a usable characterization of Early effect?

For extra credit, you can measure the well transistors too.

Drain characteristics of a single transistor at different saturation currents

This experiment studies how Early voltage scales with transistor current; in particular, how valid are the simple assumptions about channel length modulation?

Use the 32/8 native transistor that shares the gate with the other native transistors. Measure I_{ds} as a function of V_{ds} for at least 10 values of V_g, spanning sub- and above-threshold operation. For each value of V_g, sweep V_{ds} from 0 to Vdd in steps of 200mV or less. Include a single plot showing all this data on a semilogy plot.

You can take all the data in one continuous grab if you use a vector for the constant gate voltage source value. Use a vector like [.7:.2:3] (for example). Your drain current data can then be exported as an n by m matrix where n is the number of drain voltages, and m is the number of different gate voltages.

Can you see how the saturation voltage is constant for weak inversion operation, and how it increases with the gate overdrive $V_g - V_T$ in strong inversion?

Fit a line to the ”flat” part of each curve (see Sec. 3.4.4). Select a range of drain voltages to fit the line and use the same range for each curve, because the Early effect is actually curved in reality, and what you are actually seeing is the start of Drain Induced Barrier Lowering (DIBL) or impact ionization.

Compute the Early voltage for each drain curve and include another plot of Early voltage versus drain current, plotting the drain current on a log scale. Comment on your results: How constant is the Eearly voltage with drain current? Speculate on the reasons for your observations.

3.4.4 Extracting Early voltage and saturation current in Matlab

You can fit fit the drain currents by using a matlab script similar to the following (the script `extractVEarly.m` is available from OLAT):

```
figure(11); clf
vearlygate=[]; % the computed early voltages
idsatgate=[]; % the computed Idsat's
% data in vd, id, id(:,i) is i'th sweep
for i=1:size(id,2);
    ids=id(:,i);
    ind=find(vds>1.5 &vds<4); % find drain voltages in range
    vdstofit=vd(ind);
    idstofit=ids(ind);
    idstofit=idstofit'; % row vector
    p=polyfit(vdstofit,idstofit,1); % fit line to this range
    vearlygate(i)=p(2)/p(1);% compute early voltage
    idsatgate(i)=p(2);  % and Idsat
    idsnorm=ids/max(id(:));% normalize Id by max current
    plot(vd,idsnorm,'bo',...
       vds,polyval(p,vds')/max(ids(:)),'b-');
    xlabel 'V_{ds}'
    ylabel 'I_{ds}/max(I_{ds})'

end
title 'pFET 32/8 drain characteristics'

% plot V_E vs Idsat
figure(12); clf;

semilogx(idsatgate,vearlygate,'ro');
xlabel 'I_{dsat} (A)'
ylabel 'V_E'
title 'pFET 32/8 V_{Early} vs. I_{dsat}'
set(gca,'ylim',[0,inf]);
```

3.5 Postlab

1. Give an intuitive explanation to why the relationship between the above–threshold current and the gate voltage is linear in the ohmic region but quadratic in the saturation region. Explain the physics, not just the equations.

2. In the subthreshold region: (a) Is the current linearly proportional to the gate voltage in the ohmic region like it is above threshold? Why? (b) Does the drain–source

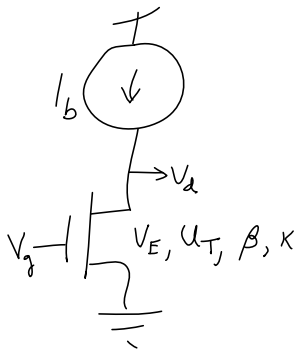

Figure 3.1: Intrinsic voltage gain of a transistor.

voltage at which the current saturates depend on the gate voltage? Why? Explain the physics and not just the equations.

3. This question probes the basic mechanism of voltage amplifier design using MOS transistors. Imagine we want to use a single transistor together with a perfect current source to make an inverting amplifier with voltage gain, as in Fig. 3.1. We are interested in calculating the *intrinsic small-signal voltage gain* of this transistor. We use an nfet, ground the source and connect the drain to a current source coming from the positive supply. We apply a gate voltage, and measure the drain voltage. Suppose the drain is hooked up to a perfect current source of infinite impedance that sources a known current I_b. Calculate the voltage gain A from gate to drain (that is, $A = \partial V_d / \partial V_g$) in weak and strong inversion operation in terms of the bias current I_b and the usual transistor parameters κ, β, $U_T = kT/q$, and V_E. Assume that the gate voltage has been biased (in reality by some feedback circuit) so that the drain voltage is in the saturation part of the I_{ds} vs. V_{ds} curve, so that I_{dsat} is slightly smaller than I_b

3.6 Congratulations

If you did everything in this lab, you have done a lot. This is probably the most difficult but also one of the most important labs. because practical and intuitive knowledge of transistor characteristics if crucial in understanding and synthesizing new circuits.

3.7 What we expect

How transistors work above threshold. What is the linear or triode region and what is the saturation region? How does the linear region depend on gate and threshold voltage? What is the "overdrive"? What is the specific current? How the Early effect comes about. Typical values for Early voltage. How to sketch graphs of transistor current vs. gate voltage and drain-source voltage. How above-threshold transistors go into saturation and why the saturation voltage is equal to the gate overdrive. Can you write the above-threshold current equations? How does above-threshold current depend on W/L, C_{ox}, and mobility μ?

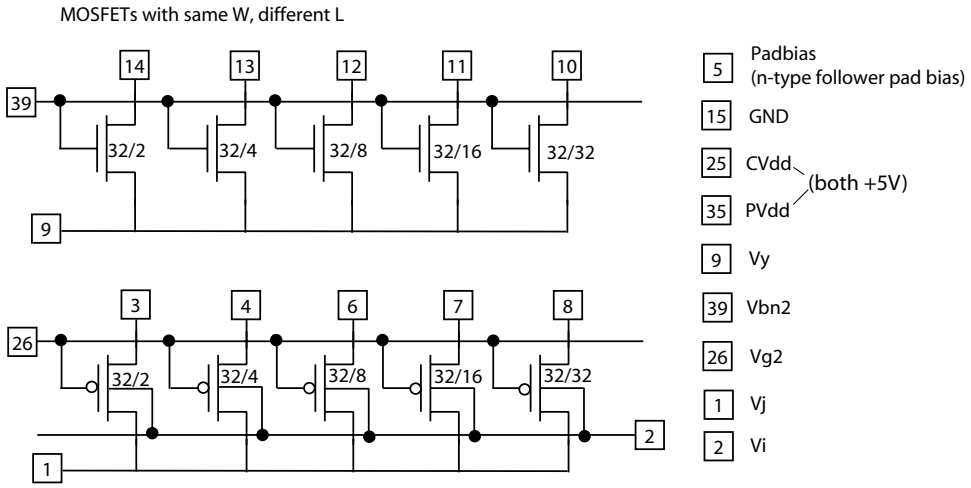

Figure 3.2: Schematic of individual MOSFETS on classchip2005a with pinout.

How do transconductance and drain resistance combine to generate voltage gain? And what is the intrinsic voltage gain of a transistor?

What effect does velocity saturation have on transistor operation, specifically, how does it change the relation between saturation current and gate voltage? What is DIBL (drain induced barrier lowering) and II (impact ionization)?

What is the dominant source of mismatch? How does transistor mismatch scale with transistor size? What are typical values of transistor threshold voltage mismatch?

3.8 Next Week

Continuation of static circuits: Diode-connected transistors, current mirrors, differential pairs, bump circuits, and transconductance amplifier.