

Silicon Synapses

NE-I Class

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Outline

1 Synapses

- Real synapses
- Software models
- Synapses in VLSI

2 Pulse Integrators

- Non-linear integrators
- A log-domain (pulse) integrator
- The diff-pair integrator

3 Computing with synapses

- Short-term depression
- Spike-driven Learning

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What is a synapse?

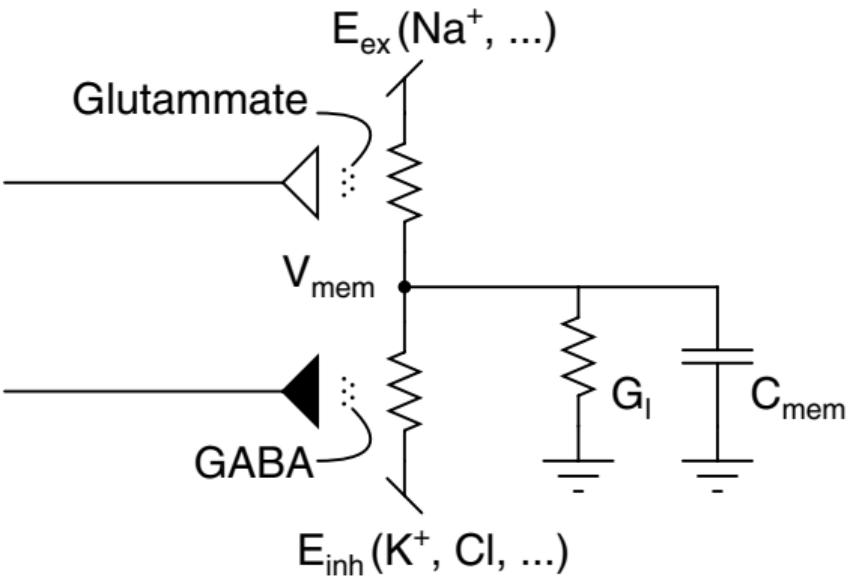


In 1897 Charles Sherrington introduced the term **synapse** to describe the specialized structure at the zone of contact between neurons as the point in which one neuron *communicates* with another.

2005 winner of the Science and Engineering Visualization Challenge.
<http://www.sciencemag.org/sciext/vis2005/show/slidel.dtl>

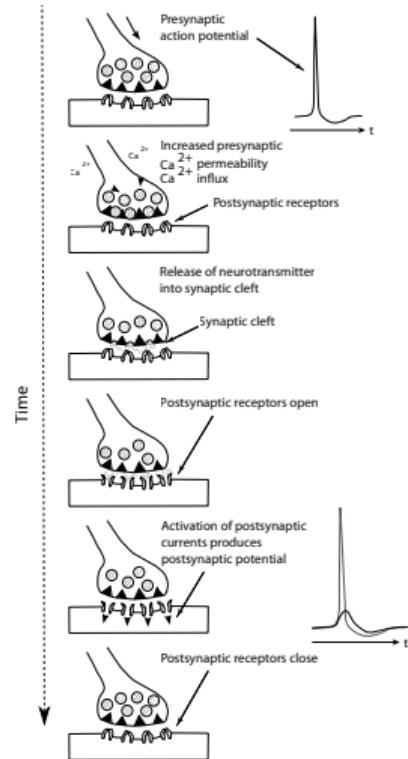
by G. Johnson, *Medical Media*, Boulder, CO.

Synapses in the nervous system



- Electrical | Chemical
- Excitatory | Inhibitory
- Depressing | Facilitating
- AMPA | NMDA
- ...

Synaptic transmission



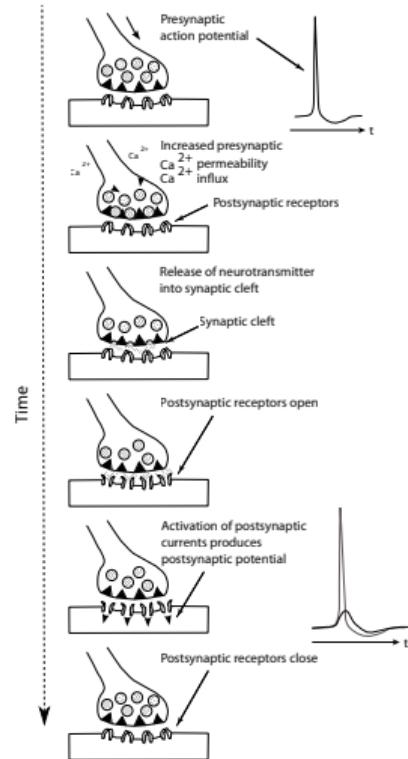
In chemical synapses the presynaptic and postsynaptic membranes are separated by extracellular space.

The arrival of a presynaptic action potential triggers the release of neurotransmitter in the extracellular space.

The neurotransmitters react with the postsynaptic receptors and depolarize the cell.

Chemical synaptic transmission is characterized by specific temporal *dynamics*.

Synaptic transmission



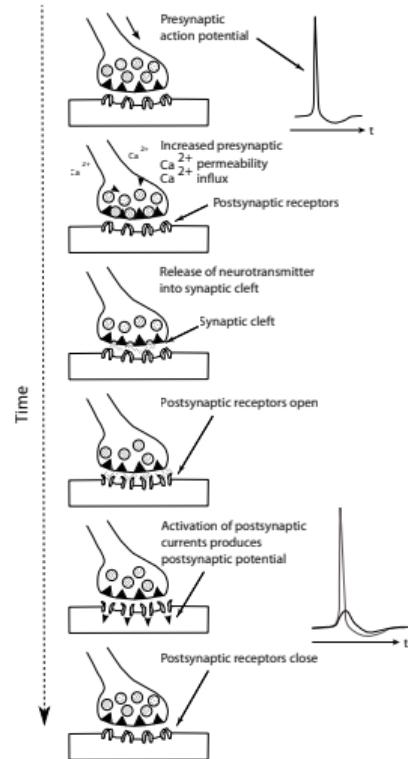
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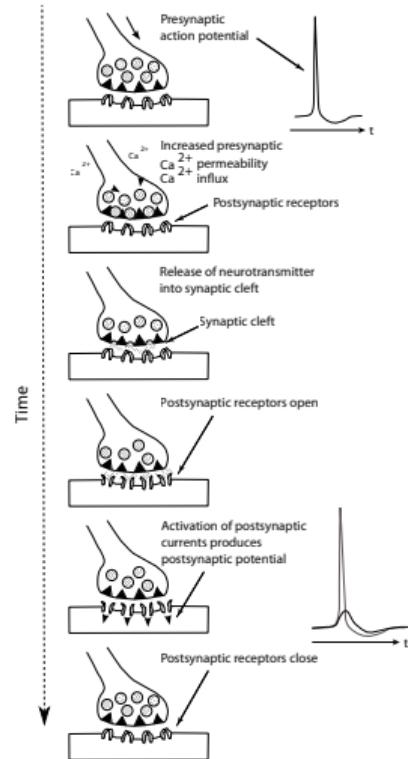
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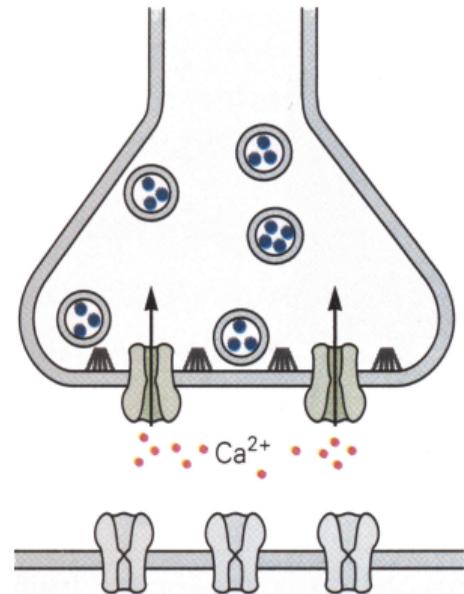
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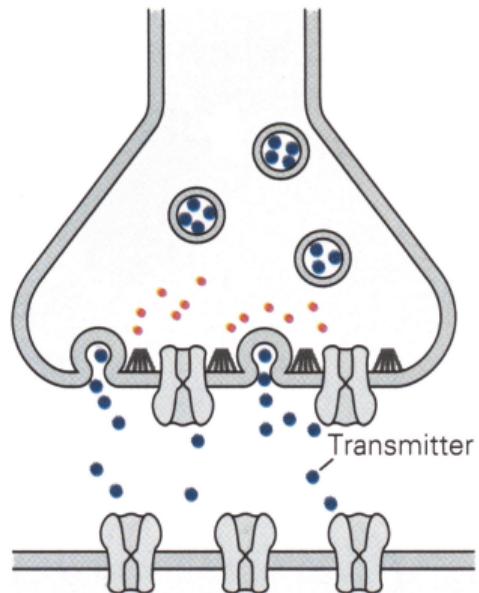
Synaptic transmission

Action potential in
nerve terminal
opens Ca^{2+} channels



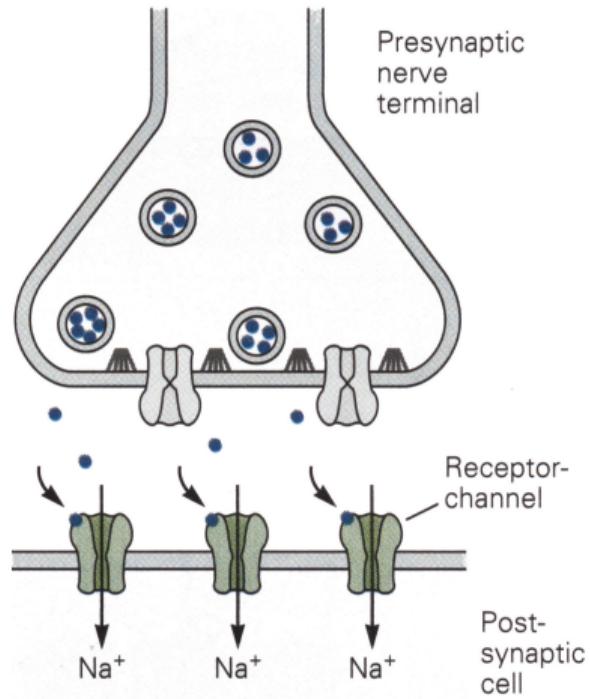
Synaptic transmission

Ca^{2+} entry causes vesicle fusion and transmitter release

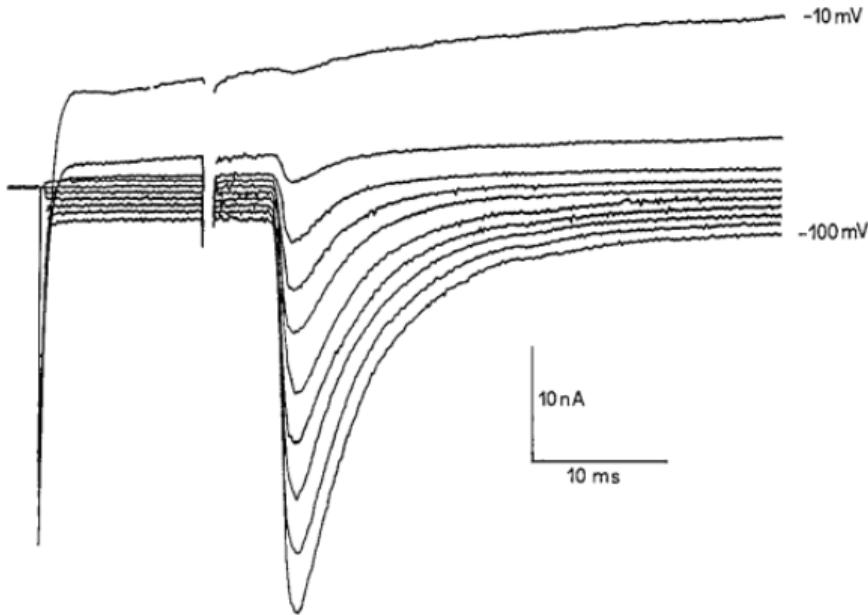


Synaptic transmission

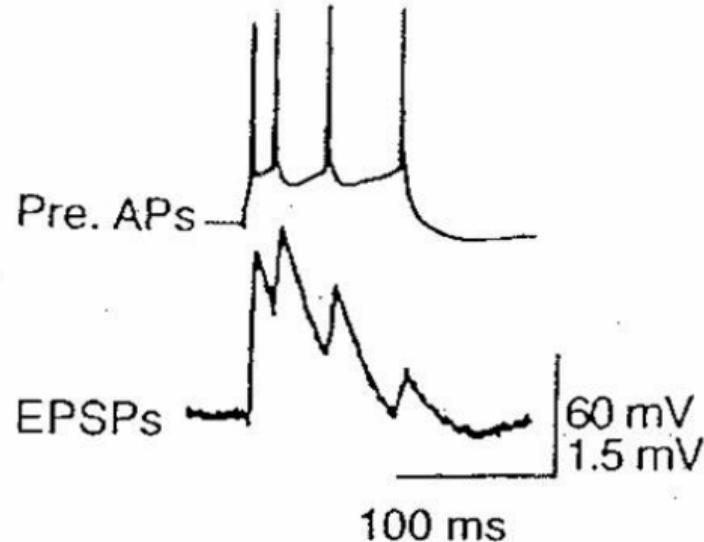
Receptor-channels open,
 Na^+ enters the postsynaptic
cell and vesicles recycle



EPSC and EPSP



Superimposed excitatory post-synaptic currents (EPSCs) recorded in a neuron at different membrane potentials (from Sacchi *et al.*, 1998).



Excitatory post-synaptic potential (EPSP) in response to multiple pre-synaptic spikes (from Nicholls *et al.* 1992).

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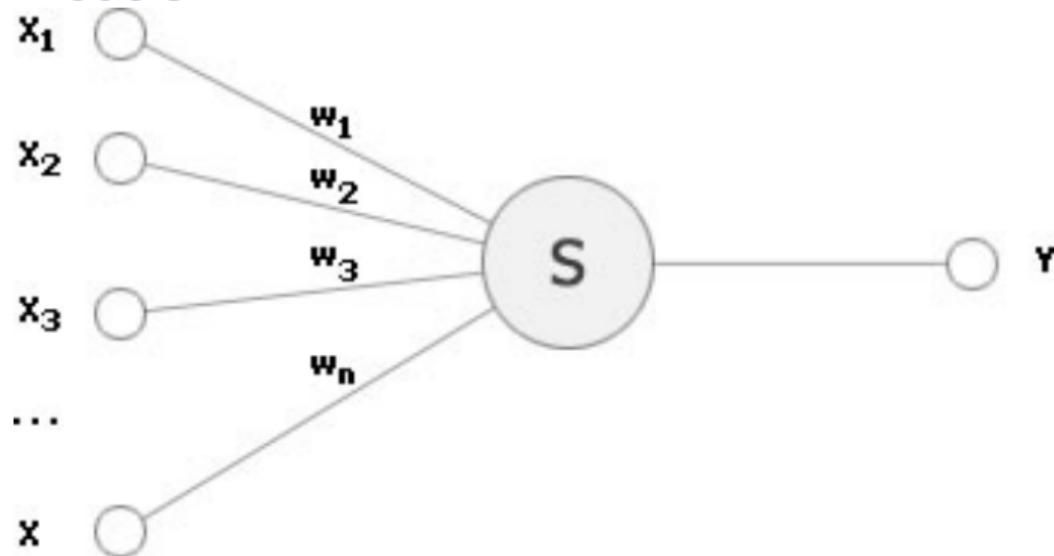
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Neural network models



In classical neural network theory

- signals are (typically) continuous values that represent the neuron's mean firing rate,
- neurons implement a saturating non-linearity transfer function (S) on the input's *weighted sum*,
- the **synapse** implements a multiplication between the neuron's input signal (X_i) and its corresponding synaptic weight (w_i).

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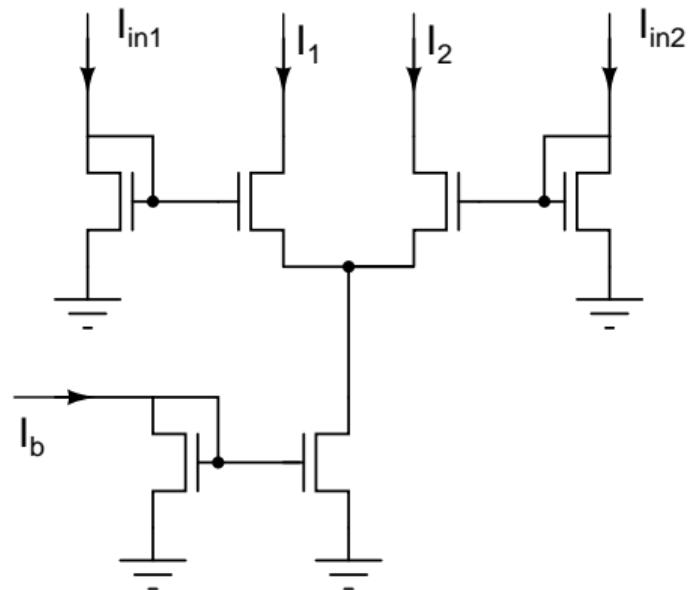
VLSI synapses in classical neural networks

The role of the VLSI synapse in implementations of “classical” neural network models is that of a *multiplier*.

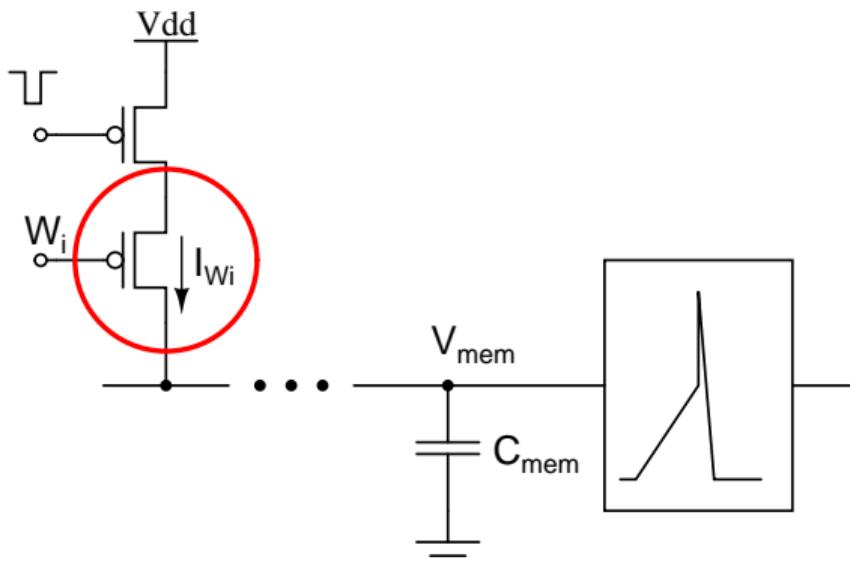
VLSI synapses in classical neural networks

The role of the VLSI synapse in implementations of “classical” neural network models is that of a *multiplier*.

Multiplying synaptic circuits have been implemented using a wide range of analog circuits, ranging from the single MOS-FETs to the Gilbert multiplier.



VLSI synapses in pulse-based neural networks



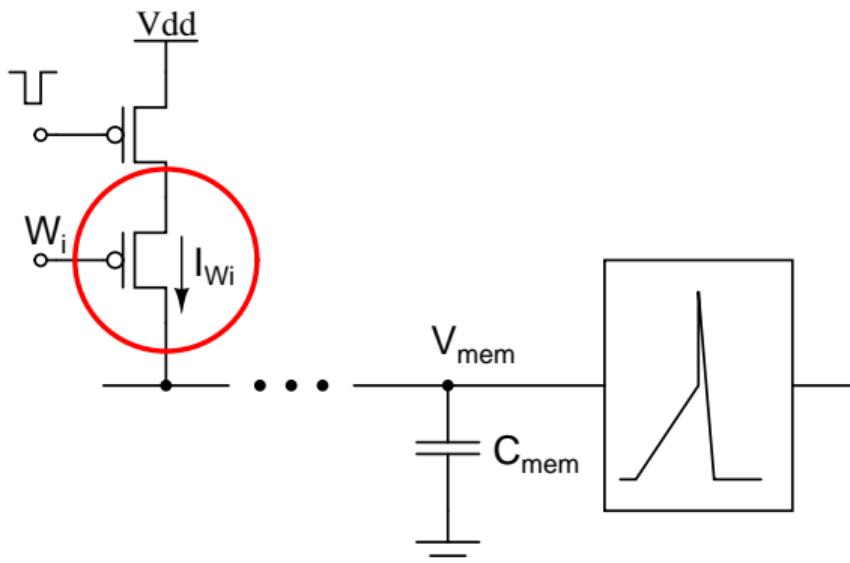
$$\Delta V_i = \frac{I_{Wi}}{C_{mem}} \Delta t$$

In pulse-based neural networks the *weighted* contribution of a synapse can be implemented using a single transistor.

In this case p-FETs implement excitatory synapse, and n-FETs implement inhibitory synapses.

The synaptic weight can be set by changing the W_i bias voltage or the Δt duration.

VLSI synapses in pulse-based neural networks



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What about temporal dynamics?

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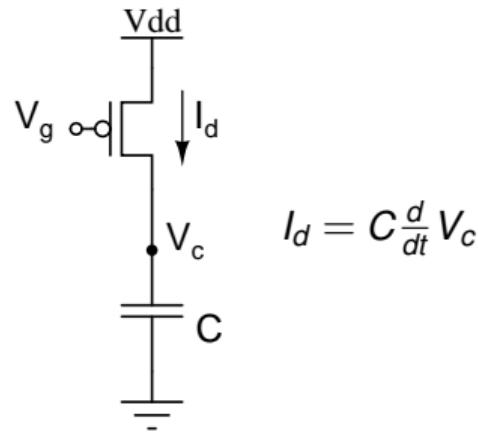
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Linear pulse charge/ exponential discharge

A *linear* integrator is a linear low-pass filter. Its impulse response should be a *decaying exponential*.

Linear pulse charge/ exponential discharge

A *linear* integrator is a linear low-pass filter. Its impulse response should be a *decaying exponential*. With VLSI and subthreshold MOSFETS its fairly easy to implement exponential voltage to current conversion, and linear voltage increase or decrease over time.

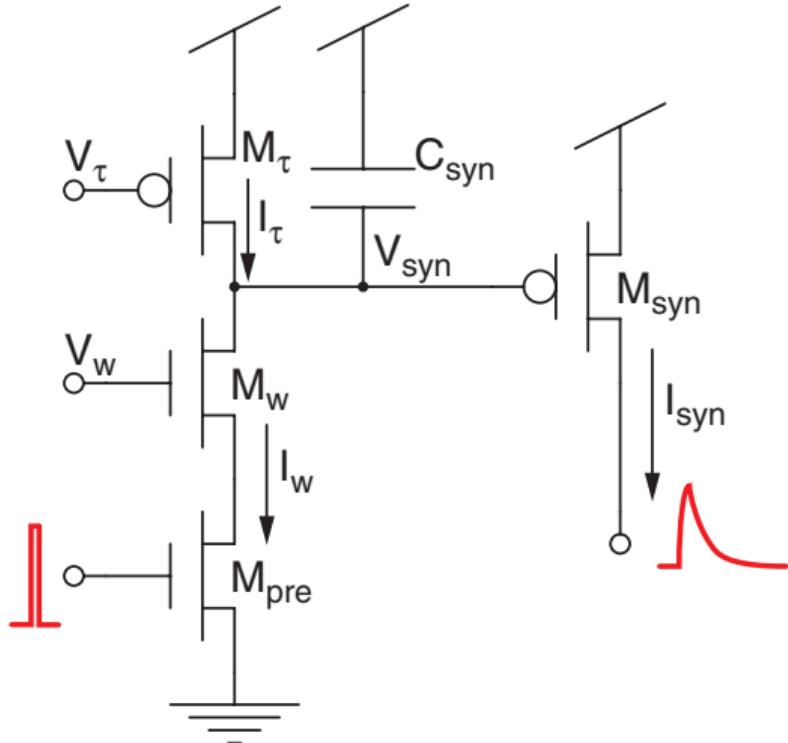


Circuit diagram of an exponential discharge. A capacitor C is connected between the output node $V_g(t)$ and ground. The node $V_g(t)$ is also connected to the gate of a MOSFET. The drain of the MOSFET is connected to V_{dd} , and the source is connected to ground. The drain current is labeled $I_d(t)$.

$$I_d(t) = I_0 e^{\frac{\kappa}{U_T} (V_{dd} - V_g(t))}$$

Exponentially decaying integrator circuit

used as a synapse



$$I_w = I_0 e^{\frac{\kappa V_w}{U_T}}$$

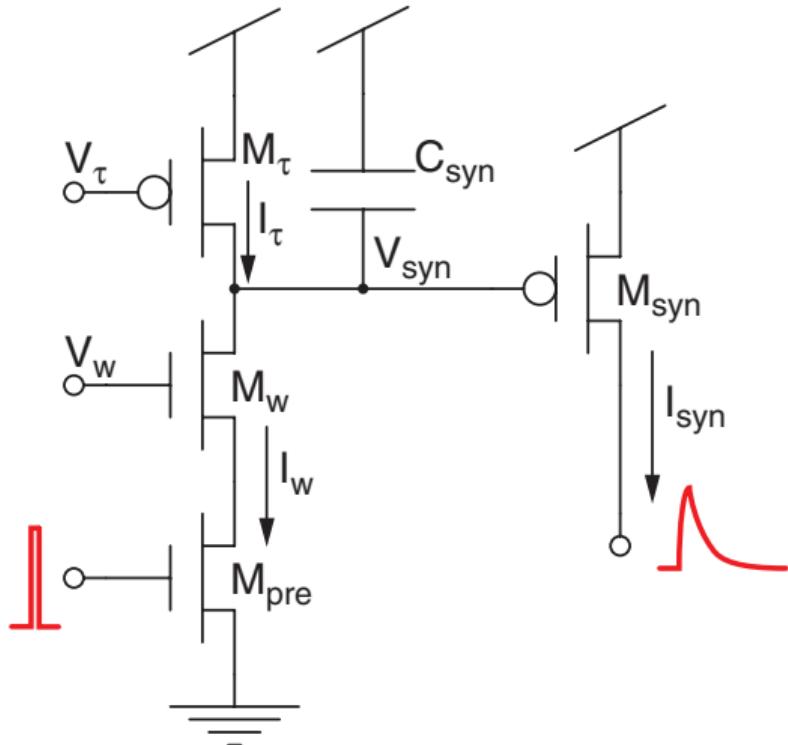
$$I_\tau = I_0 e^{\frac{\kappa(V_{dd} - V_\tau)}{U_T}}$$

$$I_c = C \frac{d}{dt} (V_{dd} - V_{syn})$$

$$I_{syn} = I_0 e^{\frac{\kappa(V_{dd} - V_{syn})}{U_T}}$$

Exponentially decaying integrator circuit

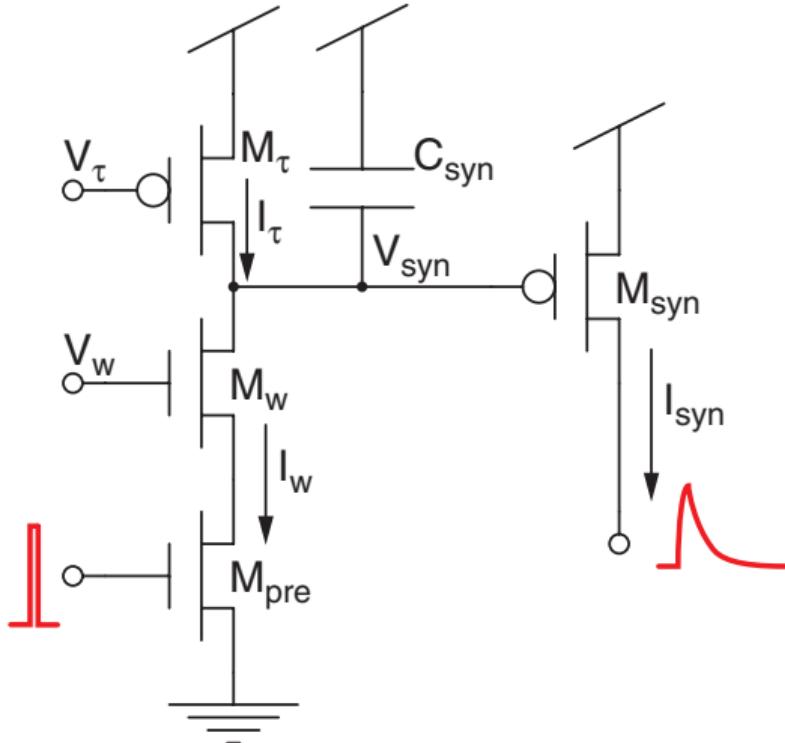
Analytical solution



$$I_{syn}(t) = \begin{cases} I_{syn}^- e^{+\frac{(t-t_i^-)}{\tau_c}} & \text{(charge phase)} \\ I_{syn}^+ e^{-\frac{(t-t_i^+)}{\tau_d}} & \text{(discharge phase)} \end{cases}$$

Exponentially decaying integrator circuit

Analytical solution

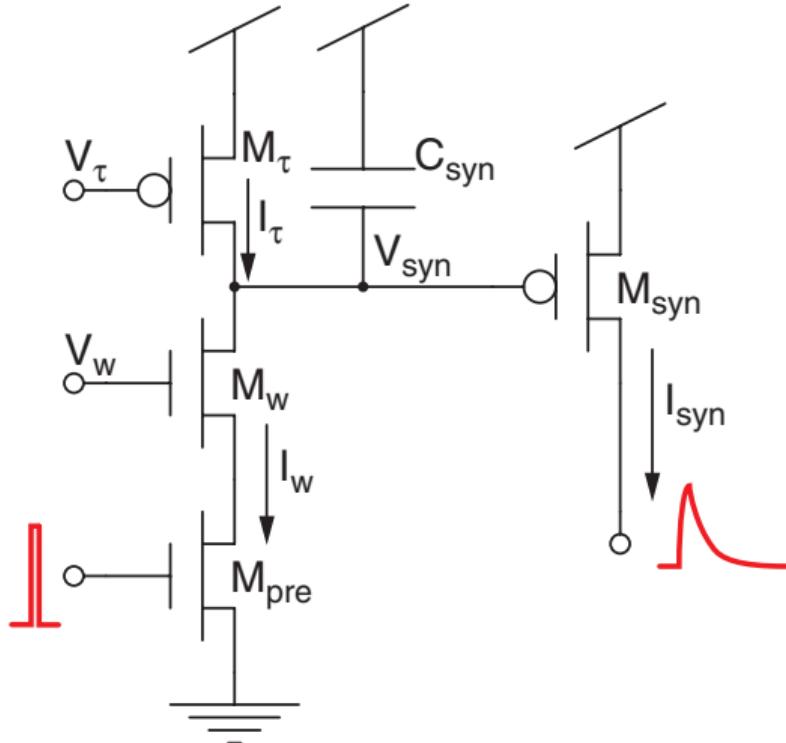


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$$I_{syn}(t_{i+1}^-) = I_{syn}(t_i^-) e^{\Delta t \left(\frac{1}{\tau_c} + \frac{1}{\tau_d} \right)} e^{-\frac{(t_{i+1}^- - t_i^-)}{\tau_d}}$$

Exponentially decaying integrator circuit

Analytical solution

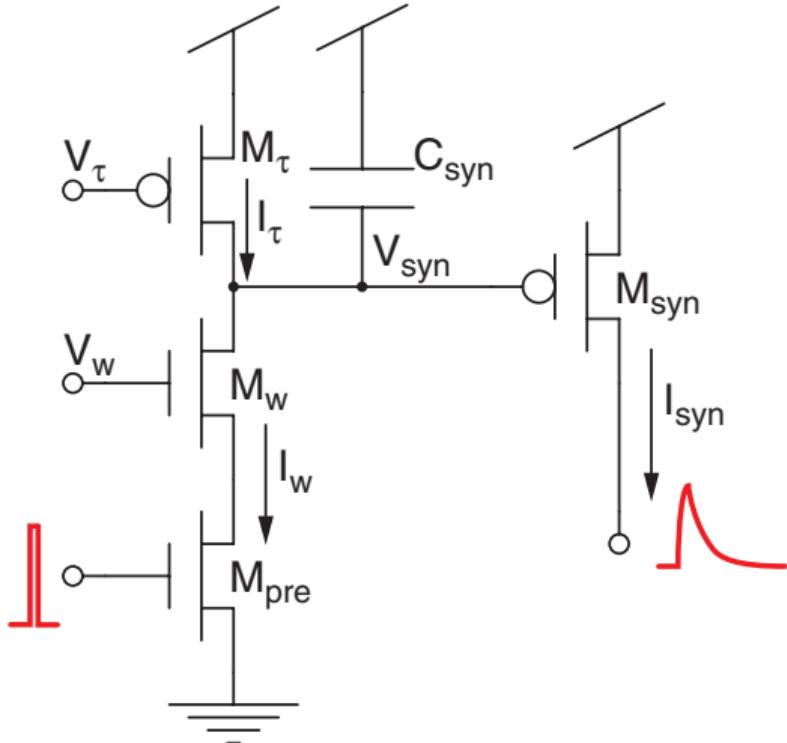


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$$I_{syn}(t) = I_0 e^{n \Delta t \left(\frac{1}{\tau_c} + \frac{1}{\tau_d} \right)} e^{-\frac{t}{\tau_d}},$$

Exponentially decaying integrator circuit

Analytical solution



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$$I_{syn}(t) = I_0 e^{-\frac{\tau_c - f \Delta t (\tau_c + \tau_d)}{\tau_c \tau_d} t},$$

$$\text{with } f = \left(\frac{n}{t}\right), \quad f < \left(\frac{\tau_c}{\tau_c + \tau_d}\right) \frac{1}{\Delta t}$$

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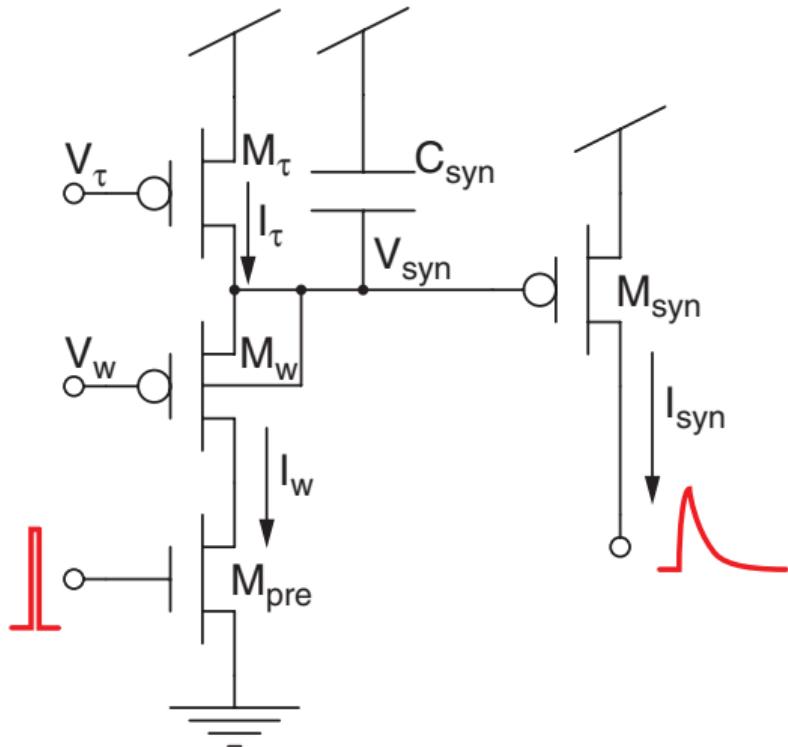
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Log-domain pulse integrator

Circuit equations



$$I_w = I_0 e^{\frac{\kappa}{U_T} (V_{\text{syn}} - V_w)}$$

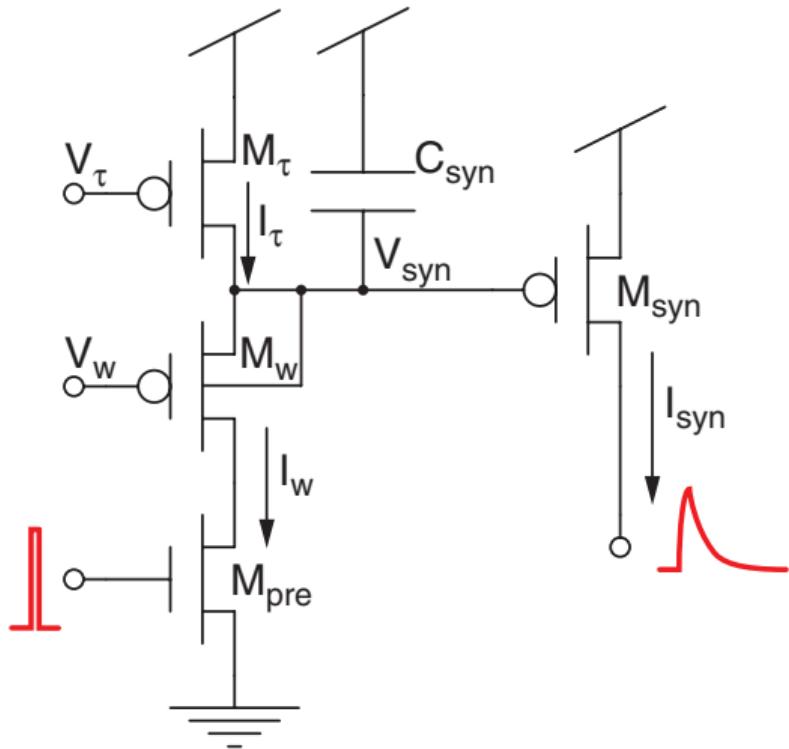
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Log-domain pulse integrator

Analytical solution



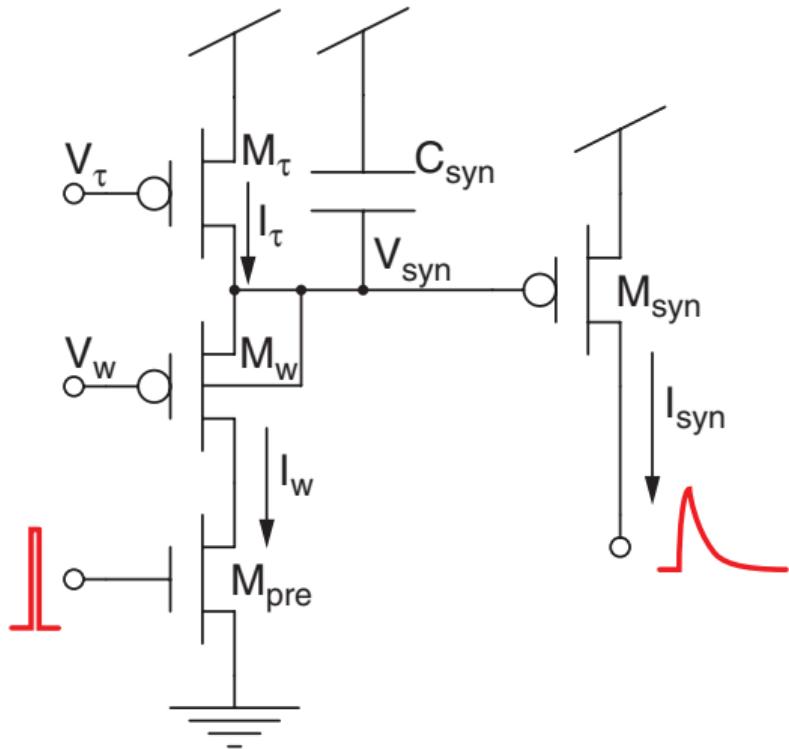
$$\frac{d}{dt} I_{syn} = -I_{syn} \frac{\kappa}{U_T} \frac{d}{dt} V_{syn}$$
$$\tau \frac{d}{dt} I_{syn} = -I_{syn} + I_{syn} \frac{I_w}{I_{\tau}}, \quad \tau = \frac{C_{syn} U_T}{\kappa I_{\tau}}$$

$$I_w = I_0 e^{-\frac{\kappa(V_w - V_{syn})}{U_T}}$$
$$= I_0 e^{-\frac{\kappa(V_w - V_{dd})}{U_T}} e^{\frac{\kappa(V_{syn} - V_{dd})}{U_T}}$$
$$= I_{w0} \frac{I_0}{I_{syn}}$$

$$\frac{d}{dt} I_{syn} + I_{syn} = \frac{I_0 I_{w0}}{I_{\tau}}$$

Log-domain pulse integrator

Analytical solution



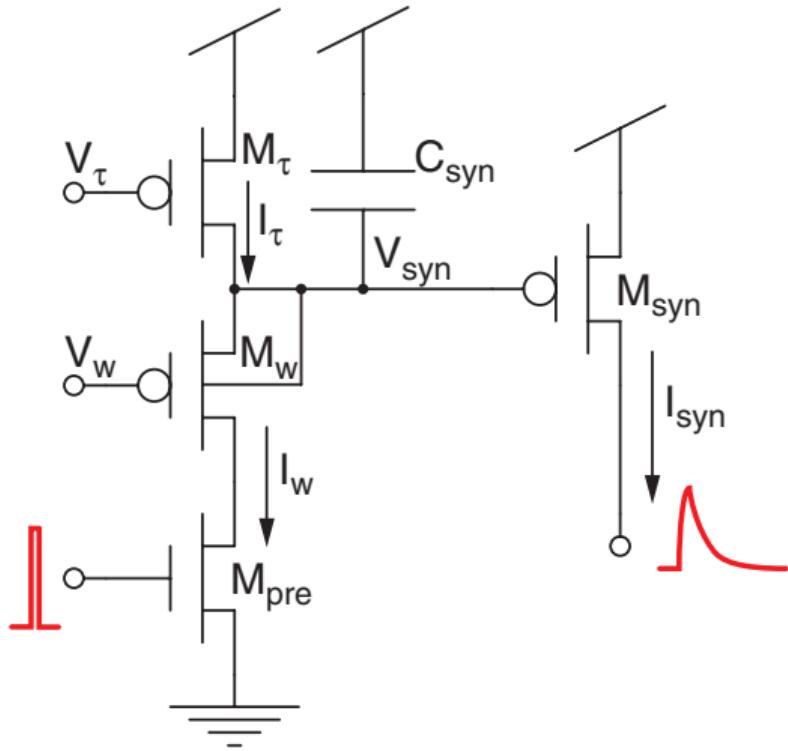
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Log-domain pulse integrator

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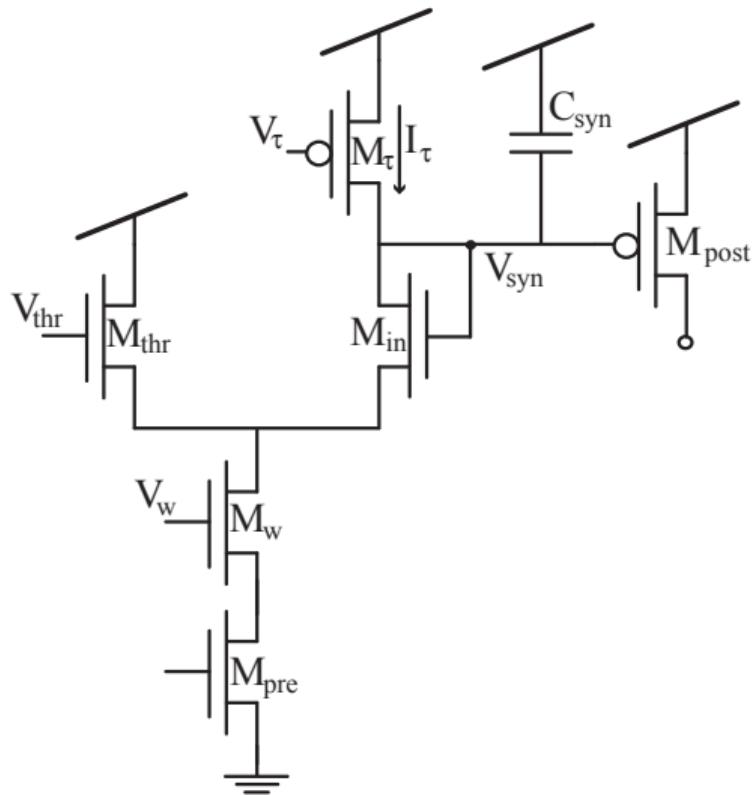
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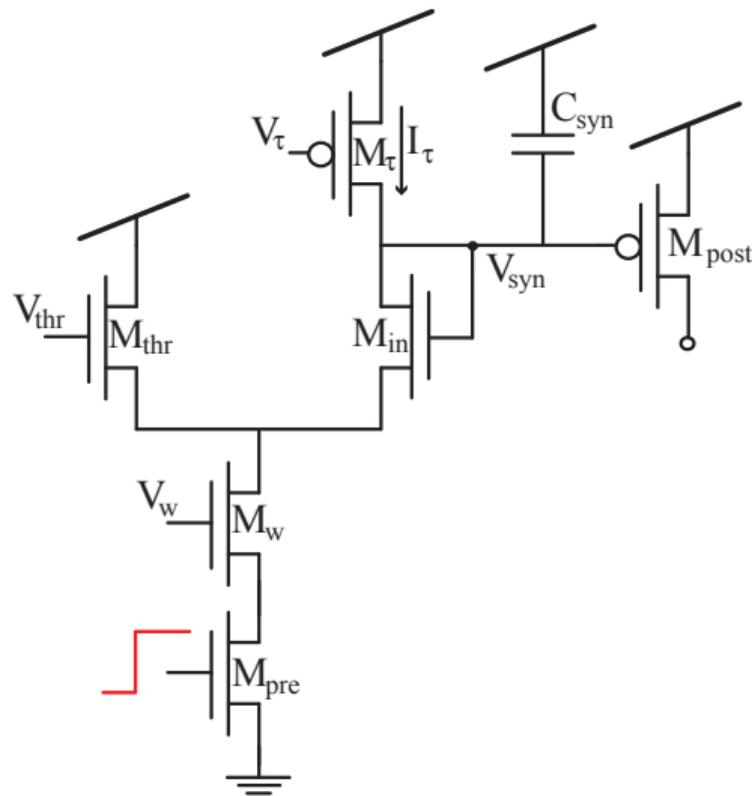
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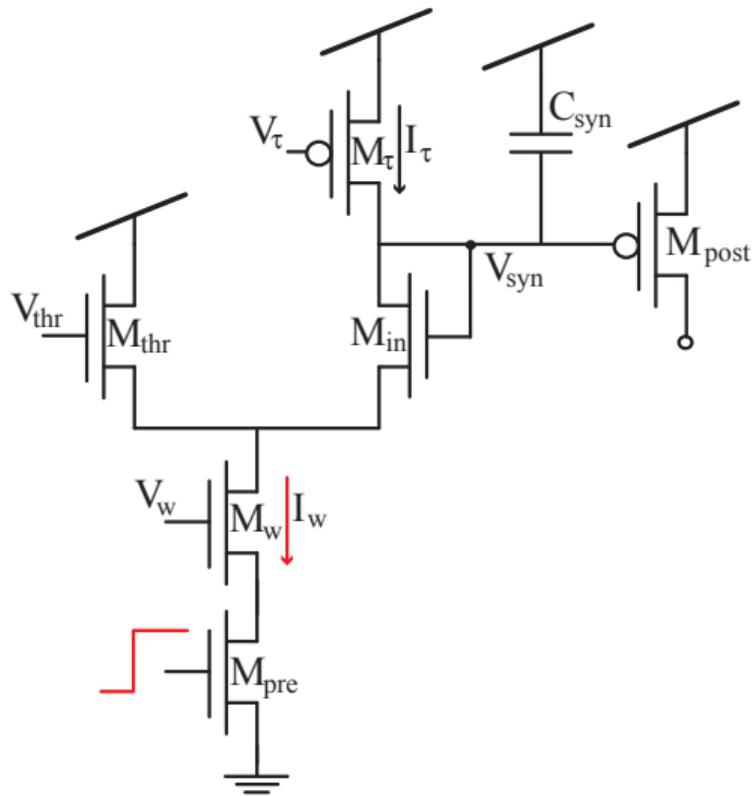
The Diff-Pair integrator (DPI) circuit



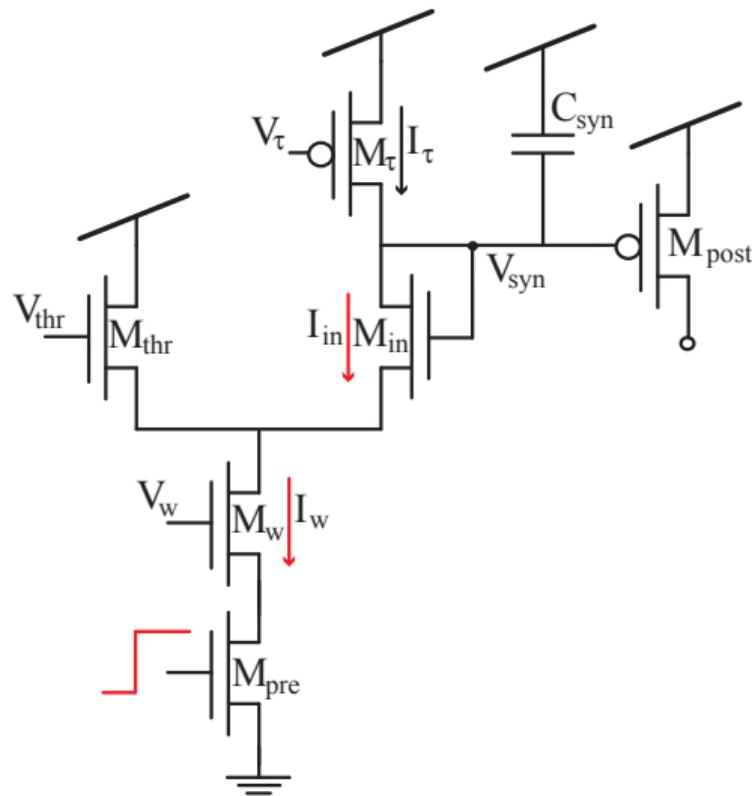
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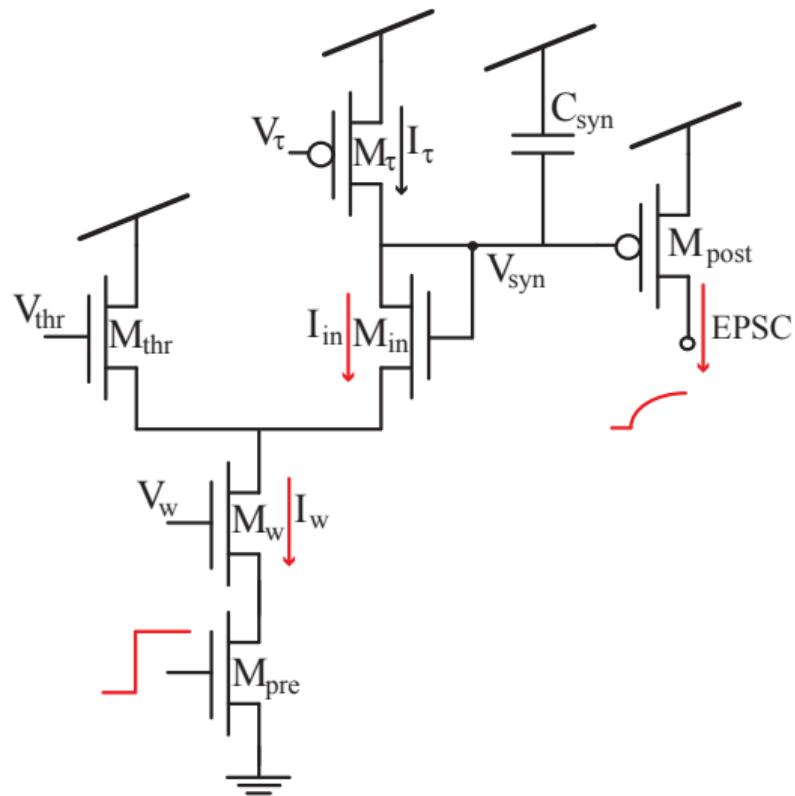
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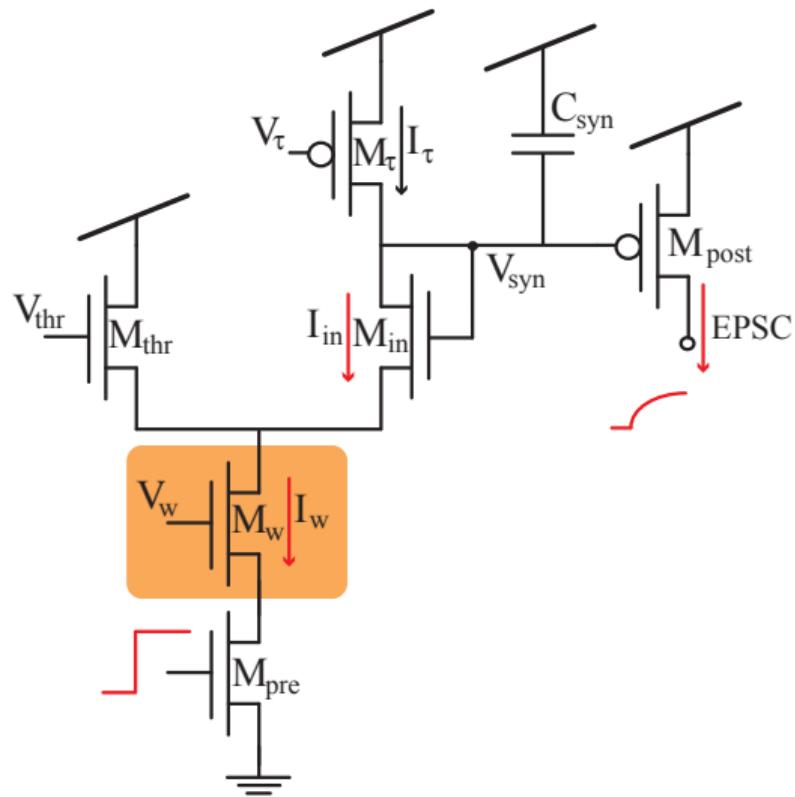
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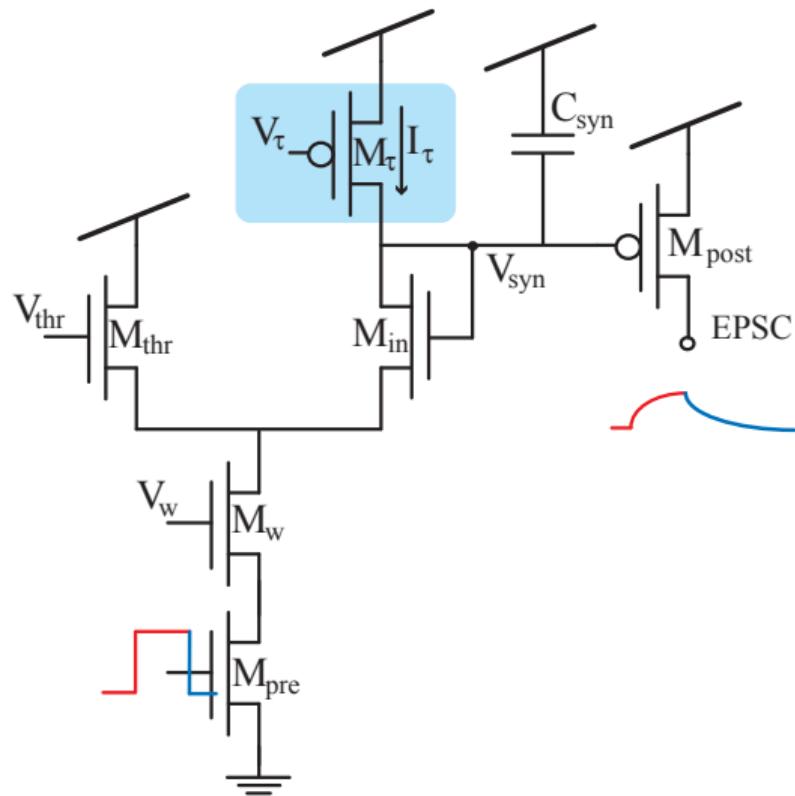
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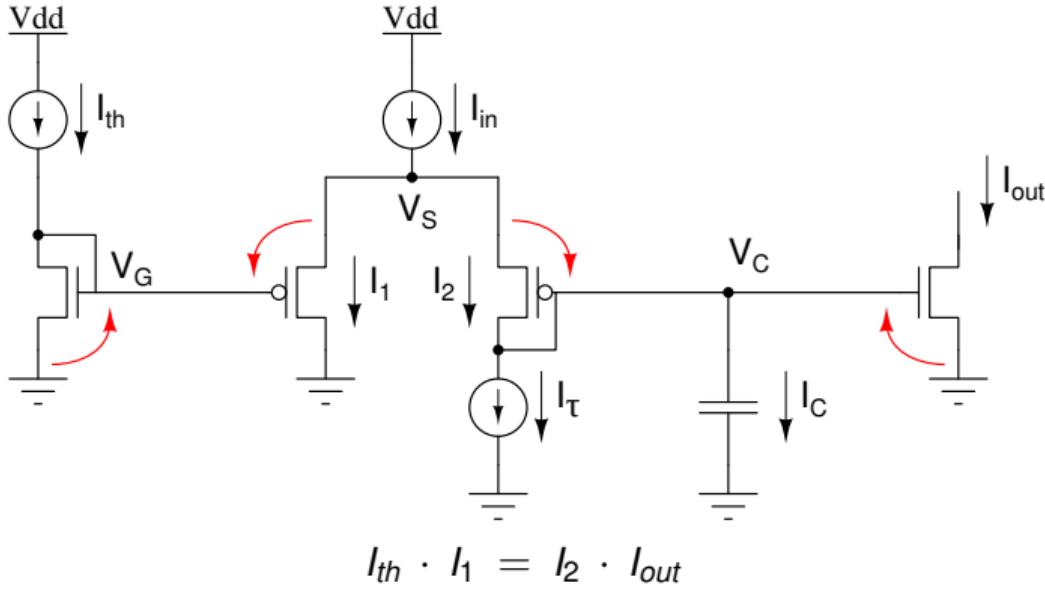
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The Diff-Pair integrator (DPI) circuit



The DPI integrator



$$\tau \left(1 + \frac{I_{th}}{I_{out}} \right) \frac{d}{dt} I_{out} + I_{out} = \frac{I_{th} I_{in}}{I_\tau} - I_{th}$$

$$I_{out} = I_0 e^{\frac{\kappa V_C}{U_T}}$$

$$I_1 + I_2 = I_{in}$$

$$I_2 = I_\tau + I_C$$

$$I_C = C \frac{d}{dt} V_C$$

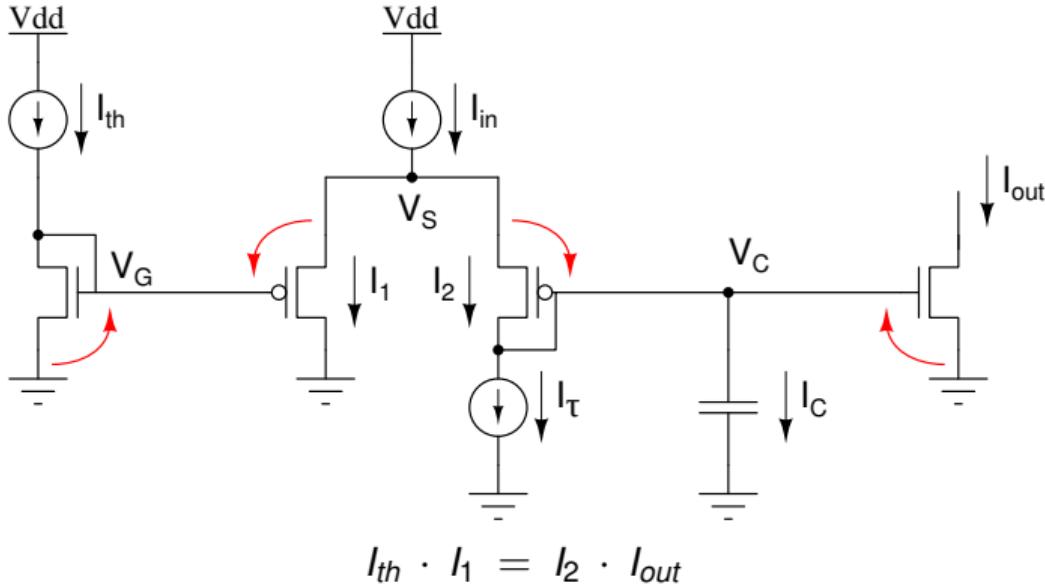
$$I_C = C \frac{U_T}{\kappa I_{out}} \frac{d}{dt} I_{out}$$

$$\tau = \frac{C U_T}{\kappa I_\tau}$$

if $I_{in} \gg I_\tau$

$$\tau \frac{d}{dt} I_{out} + I_{out} = \frac{I_{th}}{I_\tau} I_{in}$$

The DPI integrator



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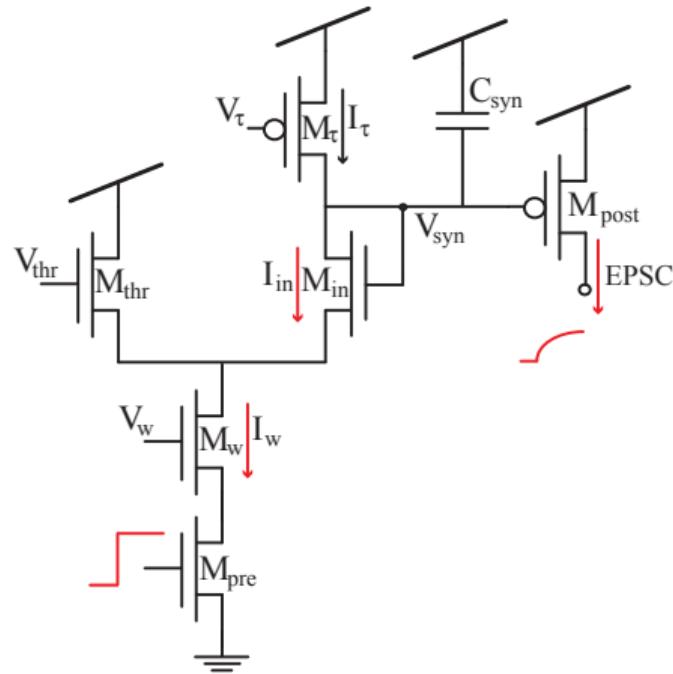
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$$\tau \frac{d}{dt} I_{out} + I_{out} = \frac{I_{th}}{I_\tau} I_{in}$$

The DPI synapse



$$I_w = I_0 e^{\frac{\kappa V_w}{U_T}}$$

$$I_\tau = I_0 e^{\frac{\kappa(V_{dd} - V_t)}{U_T}}$$

$$I_c = C \frac{d}{dt} (V_{dd} - V_{syn})$$

$$I_{in} = I_w \frac{e^{\frac{\kappa V_{syn}}{U_T}}}{e^{\frac{\kappa V_{syn}}{U_T}} + e^{\frac{\kappa V_{thr}}{U_T}}}$$

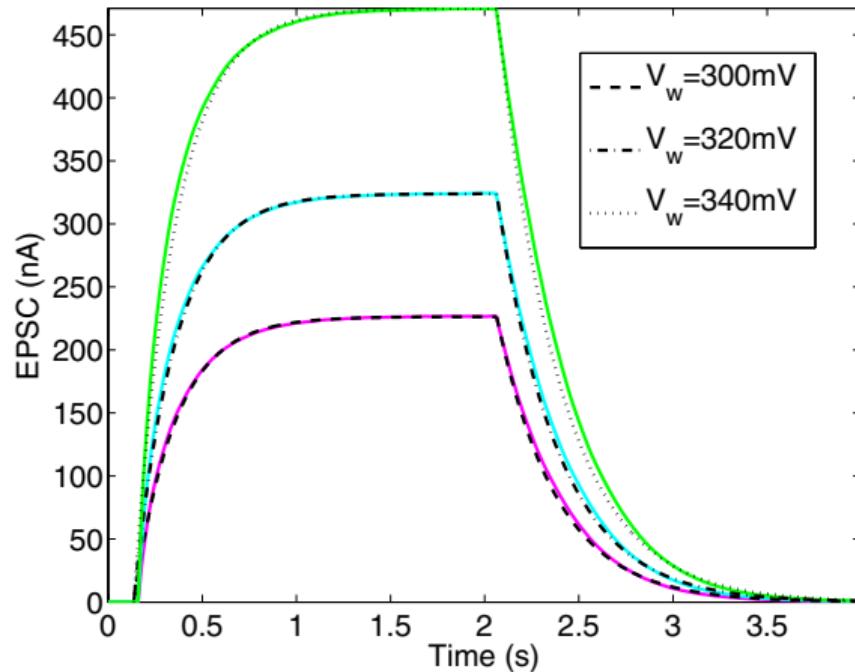
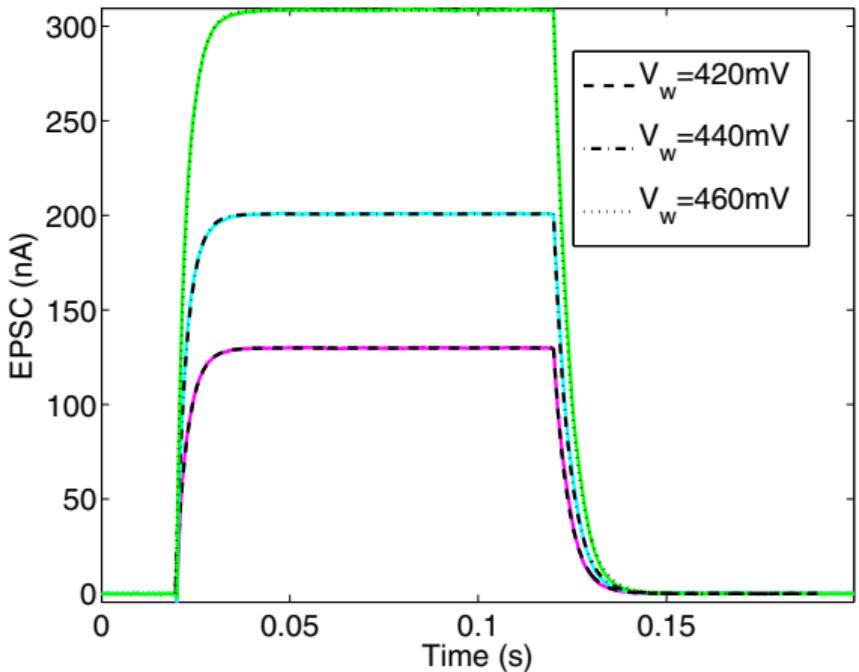
$$I_{syn} = I_0 e^{\frac{\kappa(V_{dd} - V_{syn})}{U_T}}$$

$$\frac{d}{dt} I_{syn} = -\frac{\kappa}{U_T} I_{syn} \frac{d}{dt} V_{syn}$$

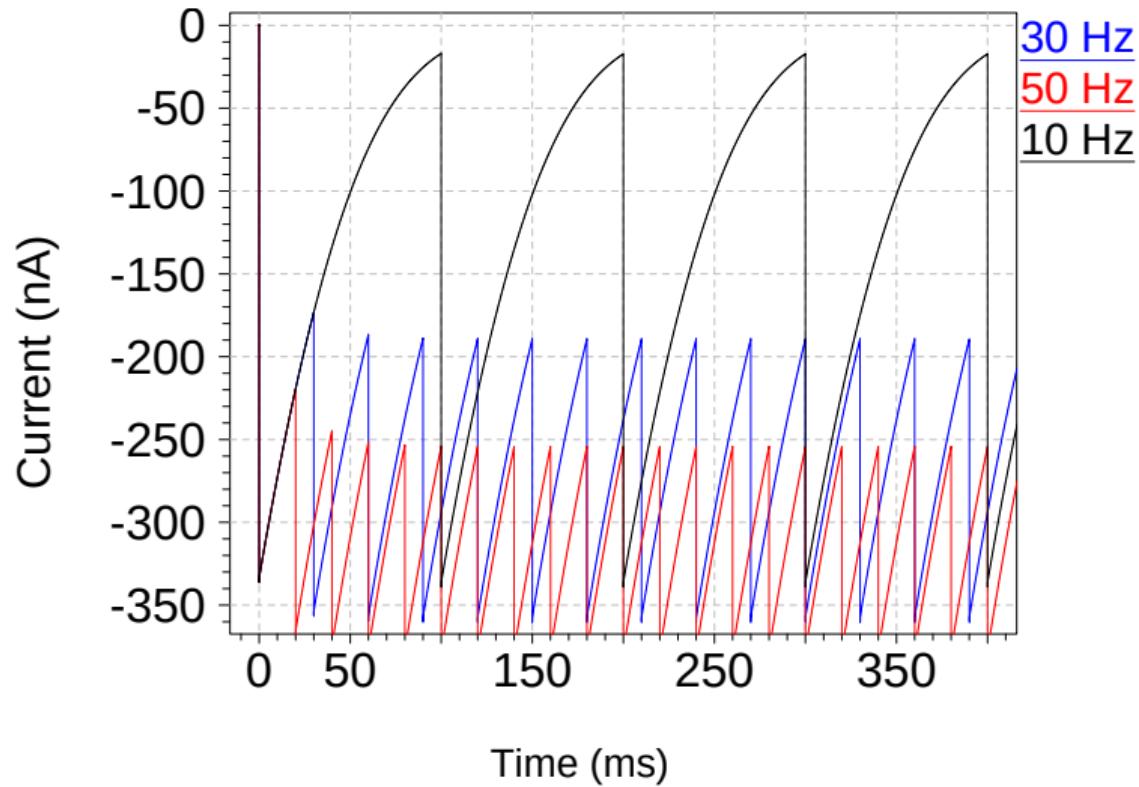
if $I_w \gg I_\tau$ then

$$\tau \frac{d}{dt} I_{syn} + I_{syn} = \frac{I_w I_{gain}}{I_\tau}$$

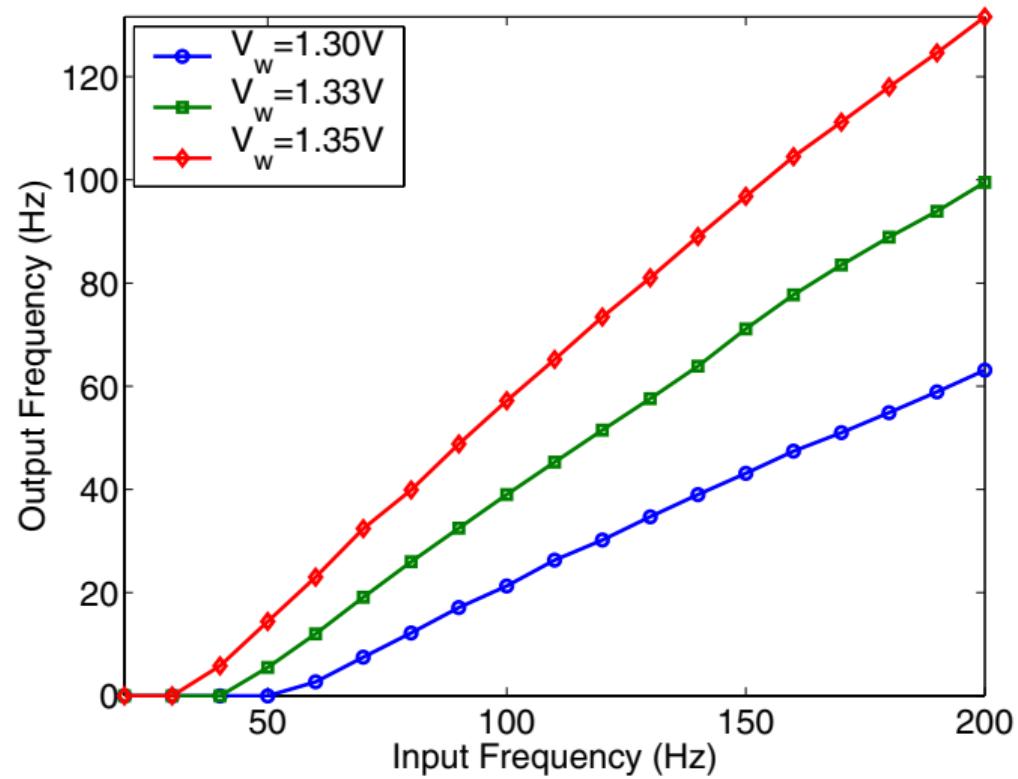
DPI measured response



DPI response to spike-trains



DPI response to spike-trains



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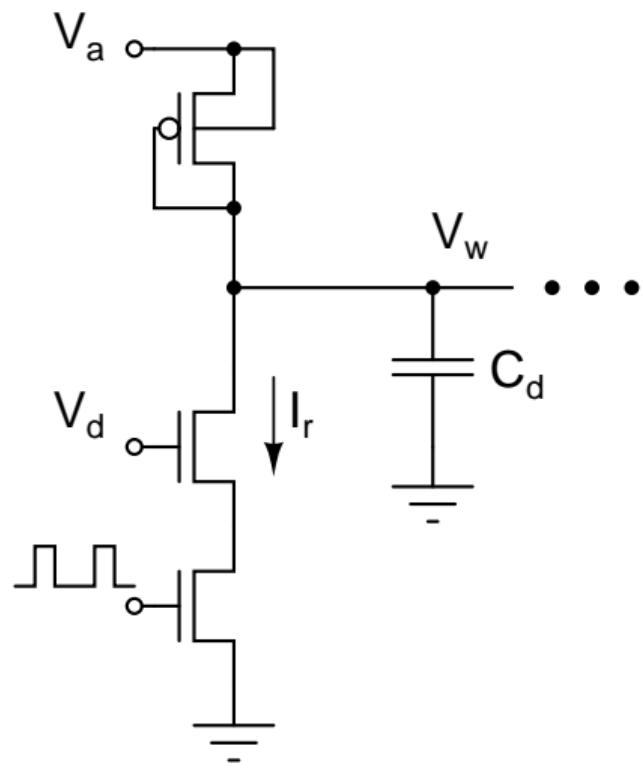
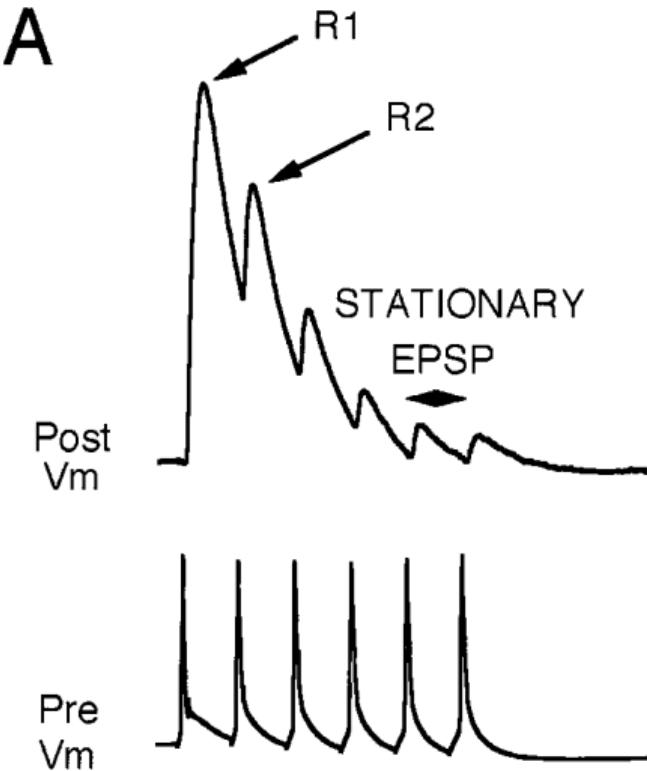
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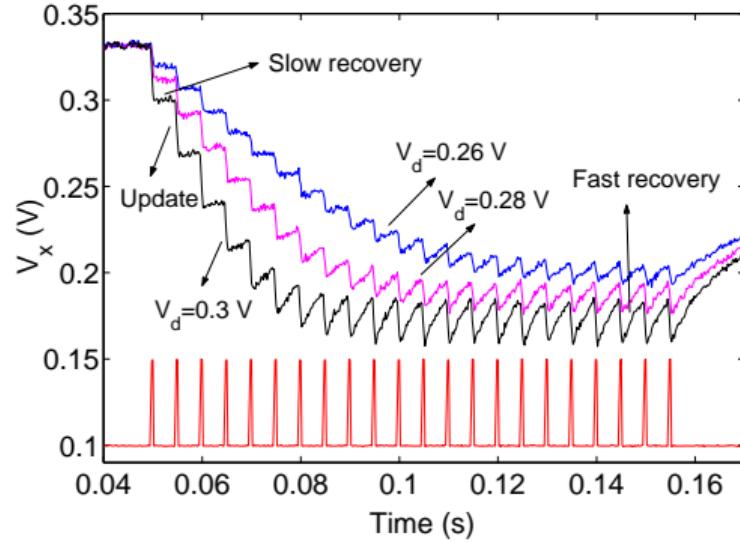
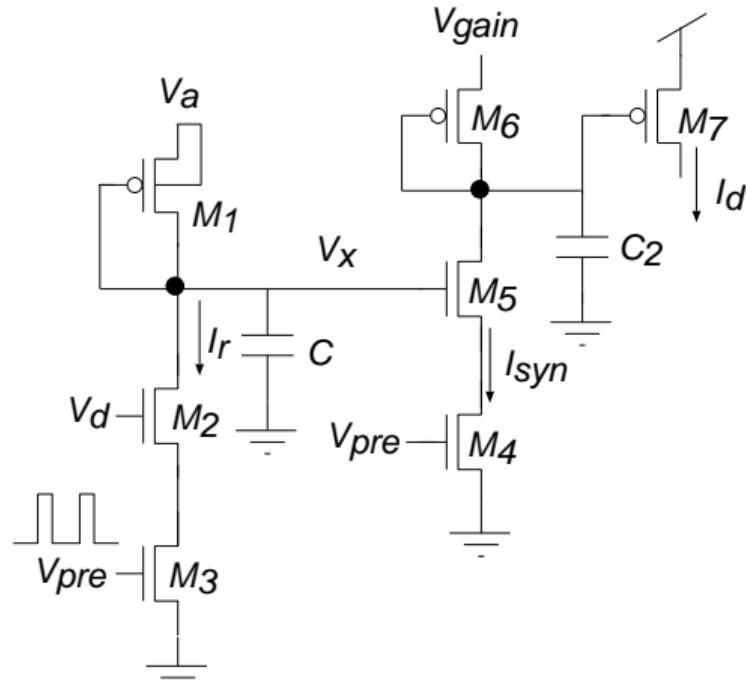
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Short-term depression



[Rasche and Hahnloser, 2001]

Short-term depression



[Boegerhausen, Suter, and Liu, 2003]

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Spike-driven learning in VLSI I



P. Häfliger, M. Mahowald, and L. Watts.

A spike based learning neuron in analog VLSI.

In M.C. Mozer, M.I. Jordan, and T. Petsche, editors, *Advances in neural information processing systems (NIPS)*, volume 9, pages 692–698. MIT Press, 1997.



E. Chicca, D. Badoni, V. Dante, M. D'Andreagiovanni, G. Salina, L. Carota, S. Fusi, and P. Del Giudice.

A VLSI recurrent network of integrate-and-fire neurons connected by plastic synapses with long term memory.

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