Lab 6

October 28, 2019

Winner–Take–All circuit

The winner–take–all (WTA) circuit models a neural network consisting of n excitatory cells and one inhibitory cell. When the excitatory cells are active, they excite the inhibitory cell which in turn inhibits all excitatory cells. The inhibitory cell's activity will increase until it silences all excitatory cells but one. If the network loop gain is high enough, this excitatory cell is able to maintain the required inhibitory cell activity by itself. Naturally, the excitatory cell that survives is the one with the largest extrinsic input.

A useful extension of the WTA network is the introduction of positive feedback and lateral coupling through both excitatory and (local) inhibitory nearest neighbor interactions. The positive feedback variant of the classical WTA network shows a hysteretic behavior in the selection/de-selection mechanism, and is therefore denoted the hysteretic winner–take–all (HWTA) network.

In this lab, we will investigate properties of both the classical WTA and HWTA circuits. Circuit schematics of a single cell in the WTA and HWTA networks are shown in Fig. 6.1. We will first characterize the response properties of the classical WTA circuit and then compare the effect of the various circuit additions to the HWTA circuit. Furthermore we will investigate the effect of the coupling diffusor circuits in the HWTA circuit. These diffusors implement both lateral excitatory and inhibitory coupling between the cells.

6.1 Reading

Study the handouts and read the papers:

Indiveri, 2001 A current-mode hysteretic winner-take-all network, with excitatory and inhibitory coupling

Douglas, Martin 2007 Recurrent neuronal circuits in the neocortex

6.2 Prelab

This prelab will help you develop intuition for the input-output current relationship of the network. We suggest you read the entire Prelab to understand the chain of reasoning before attempting to answer the questions. Assume subthreshold operation unless otherwise stated.

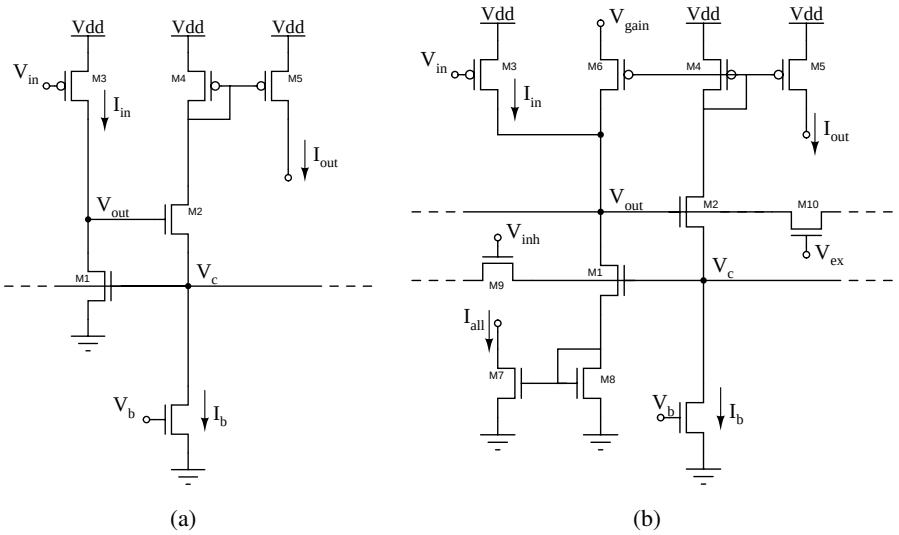

Figure 6.1: (a) Schematic of a single cell of a classical WTA network. (b) Schematic of a single cell of a HWTA network.

1. To begin, let's consider the 2-node WTA network in Fig. 6.2. Note that the WTA bias current I_b is identical for both cells (they share the same bias voltage V_b). Also note that node V_c is common to both cells. This common node is crucial, as it is through this node that the global competition takes place.

   Write down the equations for the (subthreshold) currents flowing through transistors M1 and M3, as a function of their gate, source and drain voltages, separating their *forward* and *reverse* components. Don't take into account, for the time being, the Early effect in the equations. Given that the gate voltages of M1 and M3 are the same, what happens to V_c, V_{o1} and V_{o2} if:

   - I_{i1} and I_{i2} are identical.
   - $I_{i1} \gg I_{i2}$

   In each case, determine whether M2 and M4 are conducting, and how I_{o1} and I_{o2} change as a function of the gate voltages of M2 and M4. Generalize your results to an n–input WTA circuit.

2. The analysis above applies when the input currents are sufficiently different. To understand what happens when the inputs are very similar, we have to take into account the Early effect on devices M1 and M3. Let's do a small–signal analysis. Initially, the input currents are equal, $I_{i1} = I_{i2} = I_u$, and therefore the outputs are equal, $I_{o1} = I_{o1} = 2I_b$. A small differential input ΔI_{in} is then applied, i.e. the inputs are now $I_u \pm \frac{1}{2}\Delta I_{in}$. What is the differential output, ΔV_{out}?

   Proceed as follows:

   - To help you in your reasoning, draw a transistor's subthreshold I_{ds} vs. V_{ds} curve.
   - Assume that V_c does not change.
   - Given that the drain conductance of M1 and M3 is g_{d}, figure out how much V_{o1} and V_{o2} must change to accomodate the change in current.

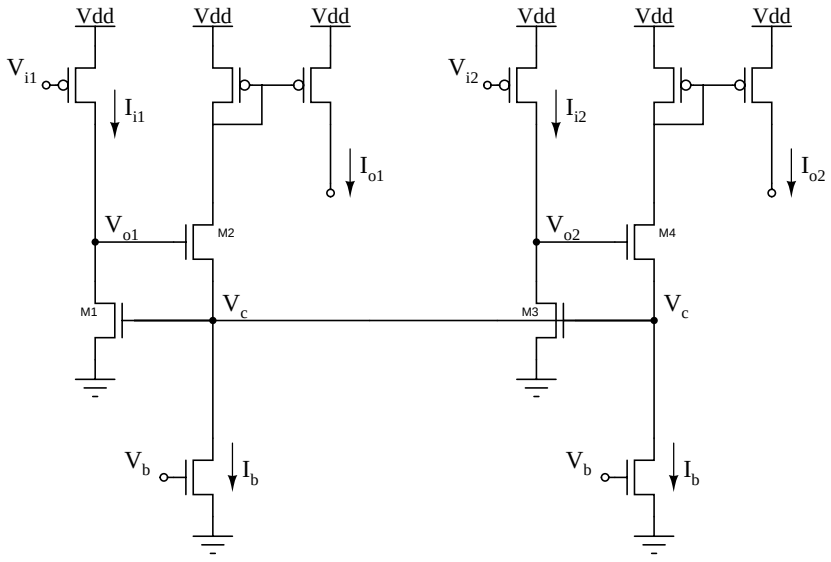

Figure 6.2: Schematic of a 2-node WTA network.

- Given these changes, use the small–signal transconductance g_{m} of M2 and M4 to figure out how much the output currents will change.
- Express the drain conductance and transconductance in terms of I_u and I_b and obtain a relationship between the normalized input and output signals, $\Delta I_{in}/I_u$ and $\Delta I_{out}/I_b$.
- Go back and justify the assumption that the V_c does not change.

How much is the gain for these normalized signals for typical parameter values? How does it change if the devices are operating above threshold?

3. Draw the setups you will use.

6.3 Experiments

The WTA circuits are on the chip **N91W-ES**. This chip is not the same as the class chip you started with. Schematic of the two types of WTA circuits are shown in Fig. 6.3.

Both types of WTA circuits contain 26 cells. The first and last input currents are set to zero, on-chip, to avoid border effects. Their other input currents are controlled by p-type transistors which have their gate voltages connected to different input pads. The pin numbers are given in the schematic. The various output currents of both types of WTA networks are scanned sequentially on to the output lines S1,R1, S2,R2 and S3,R3. The S lines hold the outputs of the selected cell chosen by a shift register consisting of SCAN cells connected in a row. The SCAN cells are clocked by the signal CK on the chip. Only one WTA cell can be selected at a time. The R lines are tied to a reference voltage so that the remaining WTA cells which are not selected will be connected to this voltage.

You will have to build a current sense amplifier with a LMC6484 opamp (check the part number on the top of the discrete chip to be sure that you have the correct one) and 10MΩ resistor to convert the current to voltage for display on the scope. The LMC6484[1] is a useful rail-to-rail input and output CMOS quad opamp chip with about 1.5 MHz unity-gain bandwidth. Make sure that the power supplies to the opamp are also connected. Your TA will draw the circuit on the board for you.

To bias the WTA chip properly, start by setting PadBias to approximately 0.8V, SPBias to 4.1V, V_{gain} and V_{inh} to 5V (use potentiometers, as we will need to change them later on), V_{ex} to ground, and V_b to 0.675V. Connect all the WTA input signals ($V_{i,n} \forall n$) to V_{dd}.

Experiment 1: Observing the behavior of the WTA

In this experiment, we will observe the winner–take–all network in action.

To start the scanner working, bias pd to 0.8V and supply a clock signal (CK) with the function generator. Make sure that the signal goes from ground to 5V (set the Ampl to 2.5V and the Offset to 1.25V on the HP 33120 function generator). A clock frequency of about 550Hz should be fine. Connect the SYNC signal from the function generator (not from the WTA chip) to CH-1 or CH-2 of the scope and trigger off that channel. *You do not have to connect the* SYNC *output of the WTA chip.* Set the time scale and the trigger position on the scope so that you only see 2 pulses of the SYNC signal, one at the very beginning of the oscilloscope's display and the other at the very end. Now you can connect the SYNC signal to the external-trigger input of the oscilloscope and trigger off that input.

Connect the reference node of the scanner (R3) and the reference node of the current-sense amp to a pot and set it to about 2.5V. Connect the voltages signals obtained from the WTA $I_{o,n}$ currents (see S3 of Fig. 6.3) to a channel of the oscilloscope and start decreasing the values of V_{i13} and V_{i14} from 5V to 4.1V with two pots. Note how the WTA cells with the largest input get all the output current. Fix V_{i13} to a constant voltage (say 4.2V) and move V_{i14} around that voltage back and forth. Repeat the same procedure keeping V_{i14} fixed and moving V_{i13}. Can you see the effect of the WTA? Turn in two plots, one showing the scanned output of the array when $V_{i13} > V_{i14}$ and the second when $V_{i13} < V_{i14}$.

Experiment 2: Two Cell Competition

In this experiment, we will measure the gain and the hysteretic characteristics of the HWTA circuit response. This is a challenging experiment because, as you showed in the Prelab, the maximum gain is very high—a five percent difference in current is enough to win. This is equivalent to a 1.5mV difference in gate voltages!

Choose the two adjacent cells 13 and 14 with which to perform this experiment and supply their input voltages V_{i13}, V_{i14} in the following way: Connect V_{i13} to a pot using a $10K$ohm resistor. Connect V_{i14} to the same pot using an other $10K$ohm resistor. Now connect the

[1] http://www.ti.com/lit/ds/symlink/lmc6484.pdf

Keithley 230 to an isolated BNC connector on the potbox (say IBNC 1) and connect the negative node of IBNC 1 to V_{i13} and the positive one to V_{i14}. You have just wired up a resistive divider which allows you to supply a differential voltage to the two inputs (via the Keithley 230) superimposed to a common DC voltage (supplied via the potentiometer). Tie all the other inputs of the WTA network to V_{dd}. Before proceeding, set the K230 to zero and choose an appropriate value with the pot for the constant input voltage (something close to 4.2V should be fine). In order to see hysteresis you should increase the WTA bias V_b to about 0.85V.

In order to access the output of cell 13 we need to manually scan from the start of the array until we reach this cell: Select the BURST mode on the HP 33120 (press SHIFT+BURST) and then press SINGLE as many times as it takes you to get the SYNC signal to switch (keep watching it on the scope). When the SYNC signal switches, you are at cell0. Now you can start counting: press SINGLE on the HP 33120 as many times as it takes you to get to the cell that you want to measure (*e.g.* apply thirteen clock cycles to reach cell 13). If you have the output of the HWTA still connected to the scope (through the current sense-amp) you can check whether you are reading the correct cell by applying a differential voltage to the inputs ($\pm$0.5V should do) and looking if the wave-form shifts on the scope.

We will need to measure the current of the cell 13 (or cell 14) with the Keithley 236. To measure the output currents, you have to disconnect S1 (in Fig. 6.3) from the sense-amp and connect it to the 236 electrometer.

We will need to capture data "by hand" in this experiment: For a given V_b setting, find the appropriate range over which to sveep the 230 differential voltage. Read the K236 output by changing (with at least 10 data points) the K230 from appropriate negative values to positive ones and then by applying the same set of K230 differential voltage values going from positive values to negative ones. Do this for two different values of V_{gain} where you see this hysteretic behavior and explain how this behavior changes with V_{gain}.

Choose a value of V_{gain} where you do not see the hysteretic effect. Now do the same experiment as above and measure the WTA gain on the new curve. Compare your measurement of WTA gain with the theory derived in the prelab? What can you say about the Early voltages of the transistors? Do your measurements seem reasonable?

6.4 What we expect

How does the WTA circuit work? Can you reason through its behavior? How does the bias current affect its performance? How can you adjust the gain of the circuit through the sizing of the transistors?

6.5 Next week

Follower integrator and differentiator.

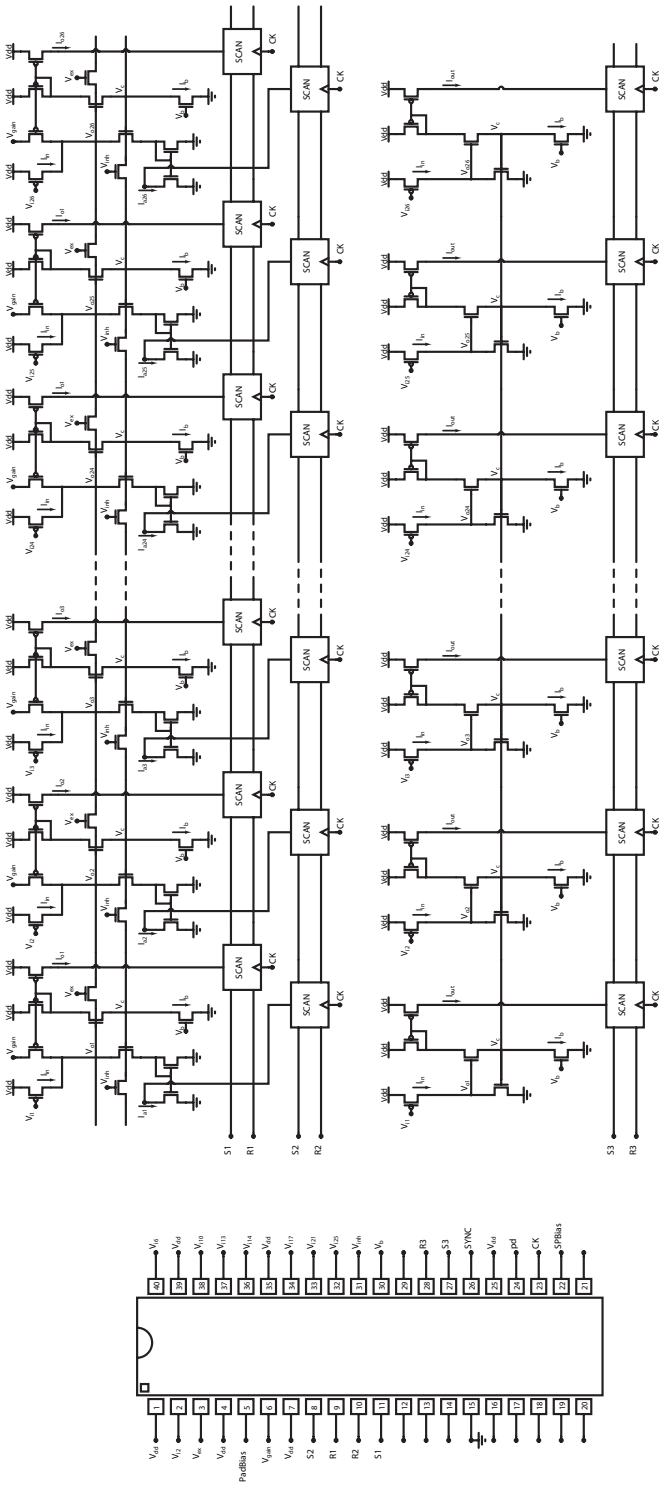

Figure 6.3: Partial Schematic of the WTA Classchip showing the relevant chip pins.