Neuromorphic Engineering I

Time and day : Lecture **Mondays, 14:00-16:00 ~~13:15 - 14:45~~, at** **https://ethz.zoom.us/j/94419667014**
Lab exercise location: Online, via Zoom sessions with your TAs, https://ethz.zoom.us/j/98109684953
Credits: **6 ECTS** credit points
Exam: Oral 20-30 minutes at INI
Labs: Reports (**max 2 persons**). You must successfully **complete at least 9 lab exercises**. These exercises should include **the first 3 labs (mandatory)** and **at least one of the last 2 labs**. If you do all lab exercises, we will drop your 3 lowest lab grades.
Grade: 70% exam + 30% lab exercises
Lectures from: Tobi Delbruck, Giacomo Indiveri, Shih-Chii Liu, Melika Paywand
Teaching assistants: Elisa Donati, Giorgia Dellaferrera, Chenxi Wu, Carsten Nielsen

Tobi Delbruck

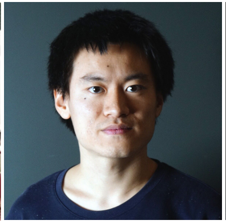
Giacomo Indiveri

Shih-Chii Liu

Elisa

Giorgia

Chenxi



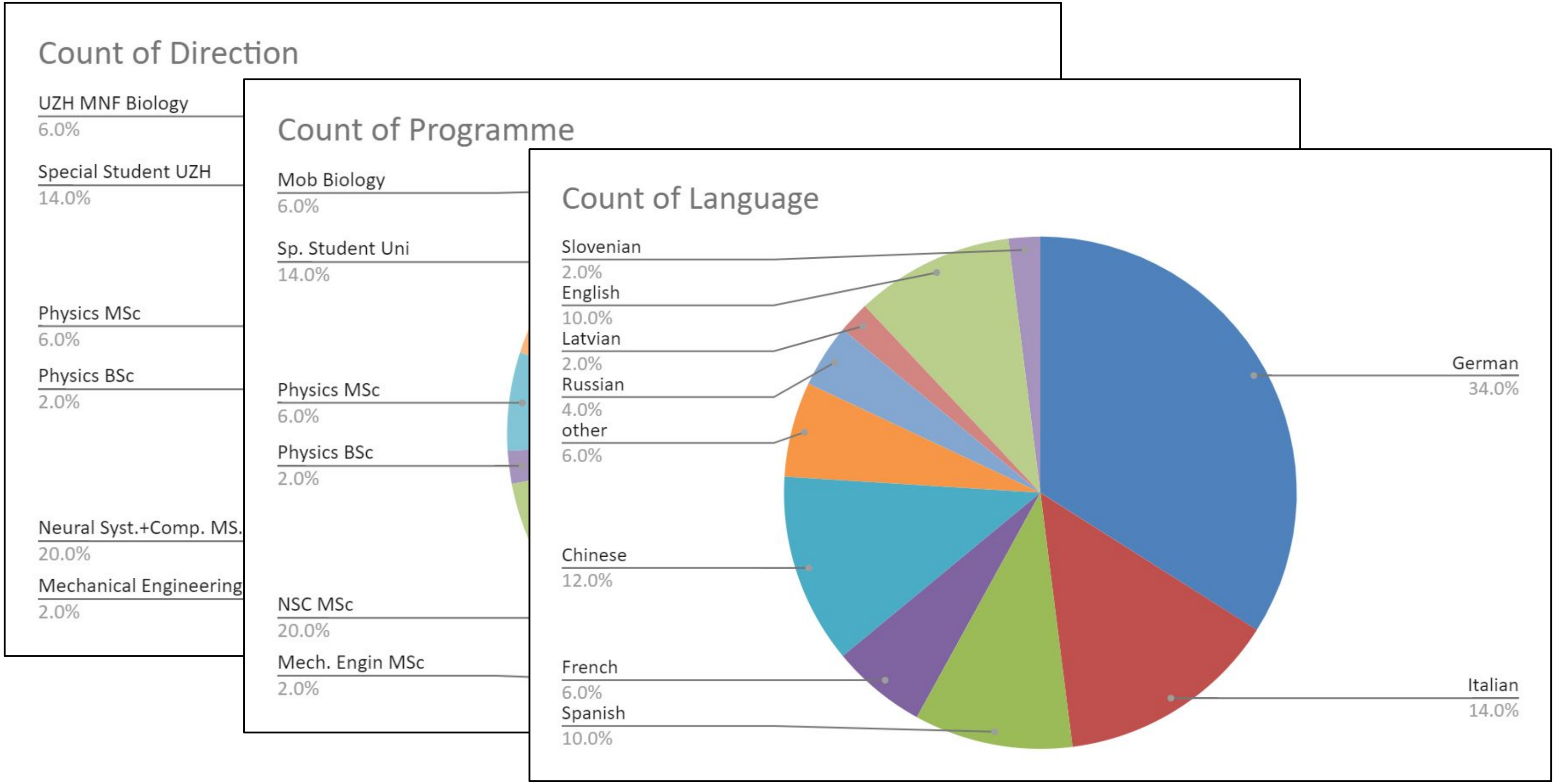
Carsten

tobi,giacomo,shih@ini.uzh.ch

To do today

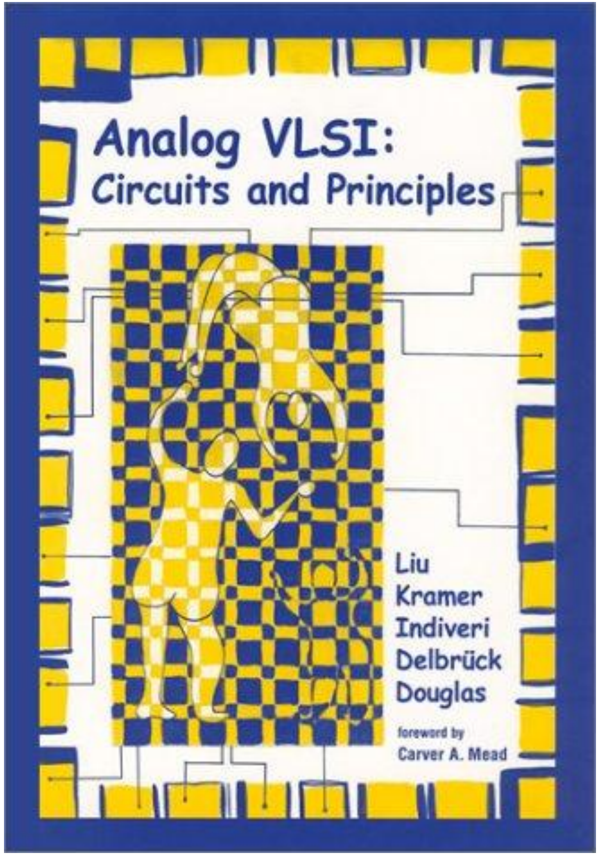
- Introduce book
- Arrange lab times (by doodle) and introduce new classchip and exercises via JupyterHub
- Introduce device physics
- Demo lab setup and class-chip use in JupyterHub

Class composition (2020) 50 registered

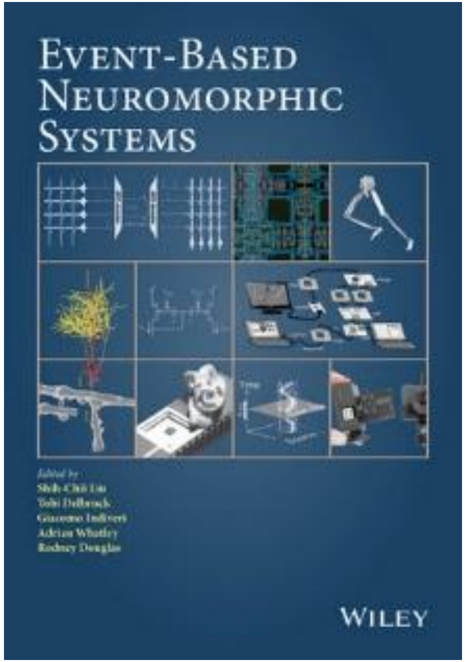


Book(s)

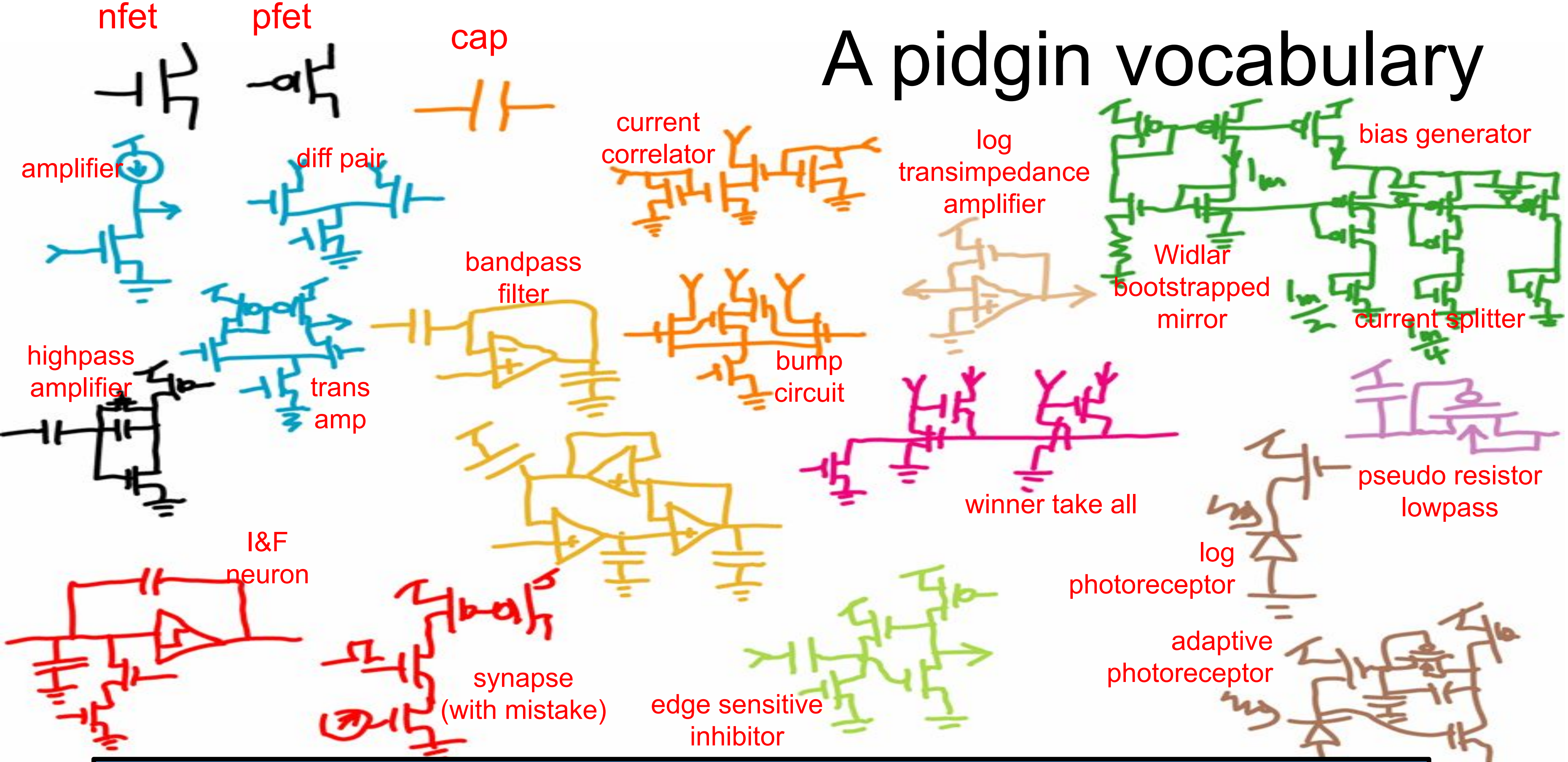
Introductory textbook (2002)
[Amazon]



System examples (2015)
[Amazon]



A pidgin vocabulary



By the end of this semester, you should recognize many of these circuits and be able to <u>reason</u> your way through the others.

Neuromorphic Electronics?

What is it all about?

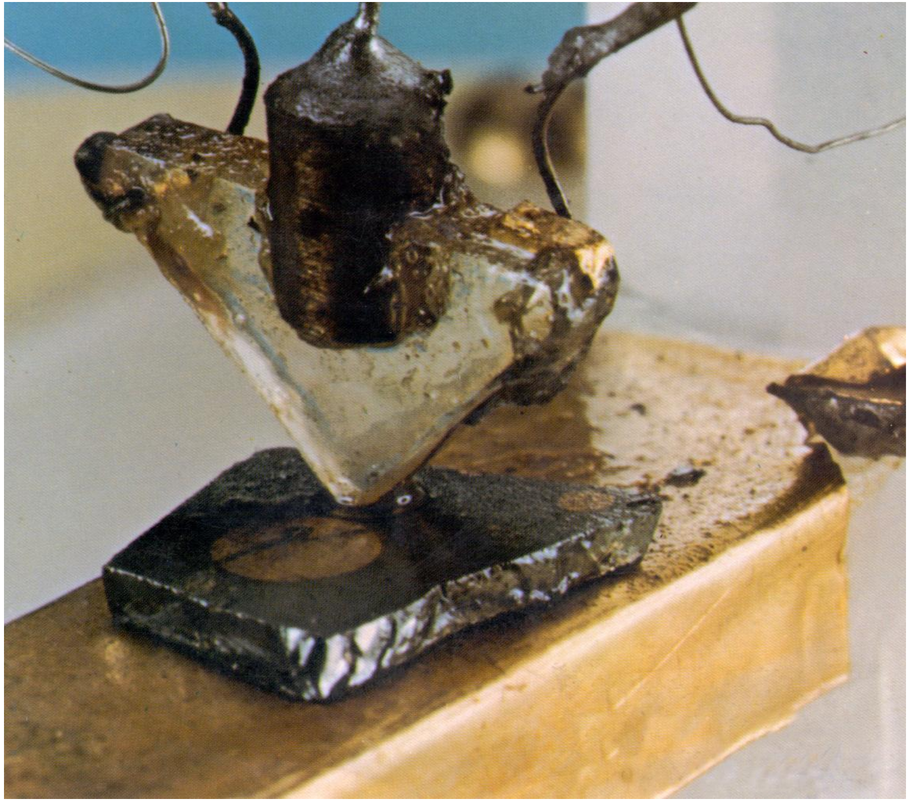
See Shih-Chii Liu talk from 2020 Telluride Neuromorphic Workshop:

[Neuromorphic electronics, A historical perspective]

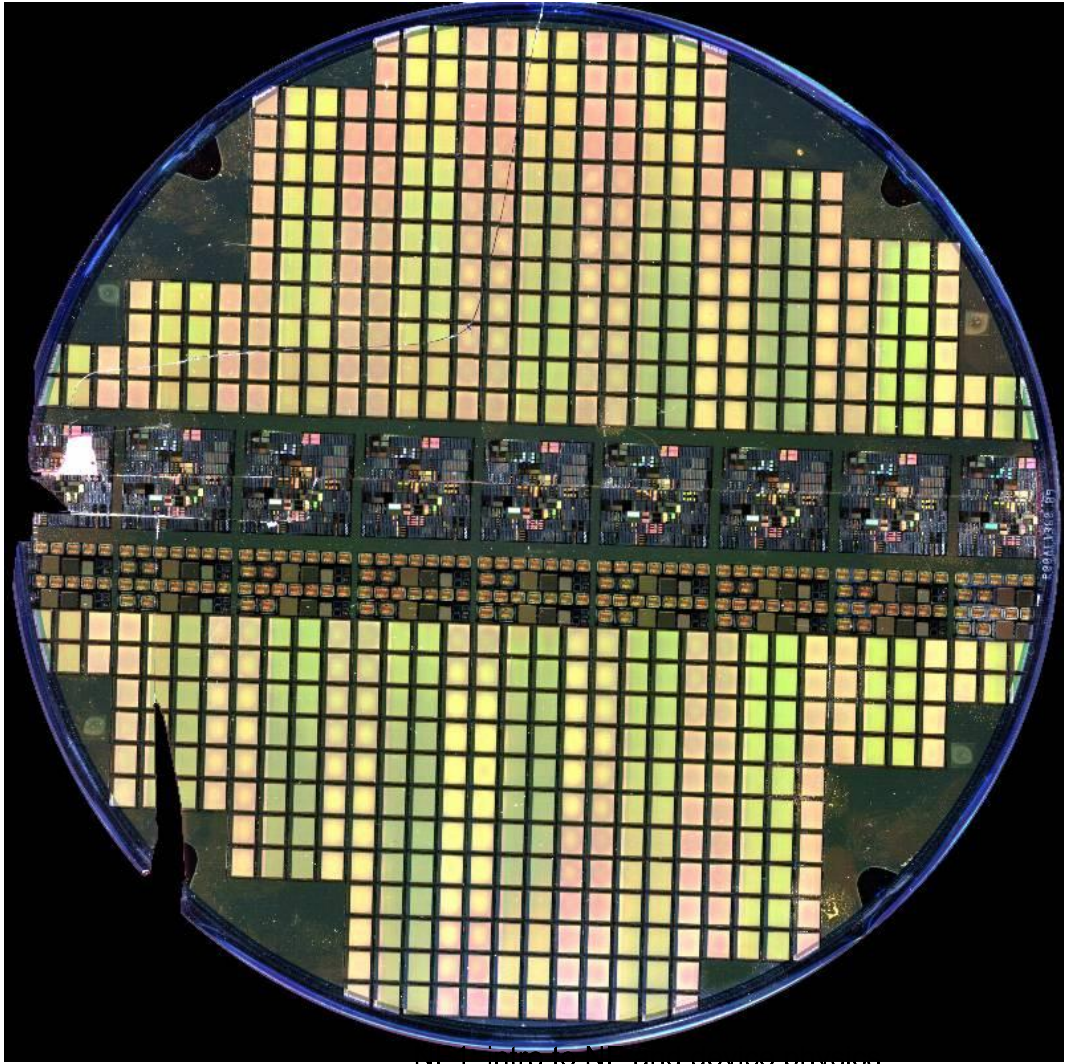
The context

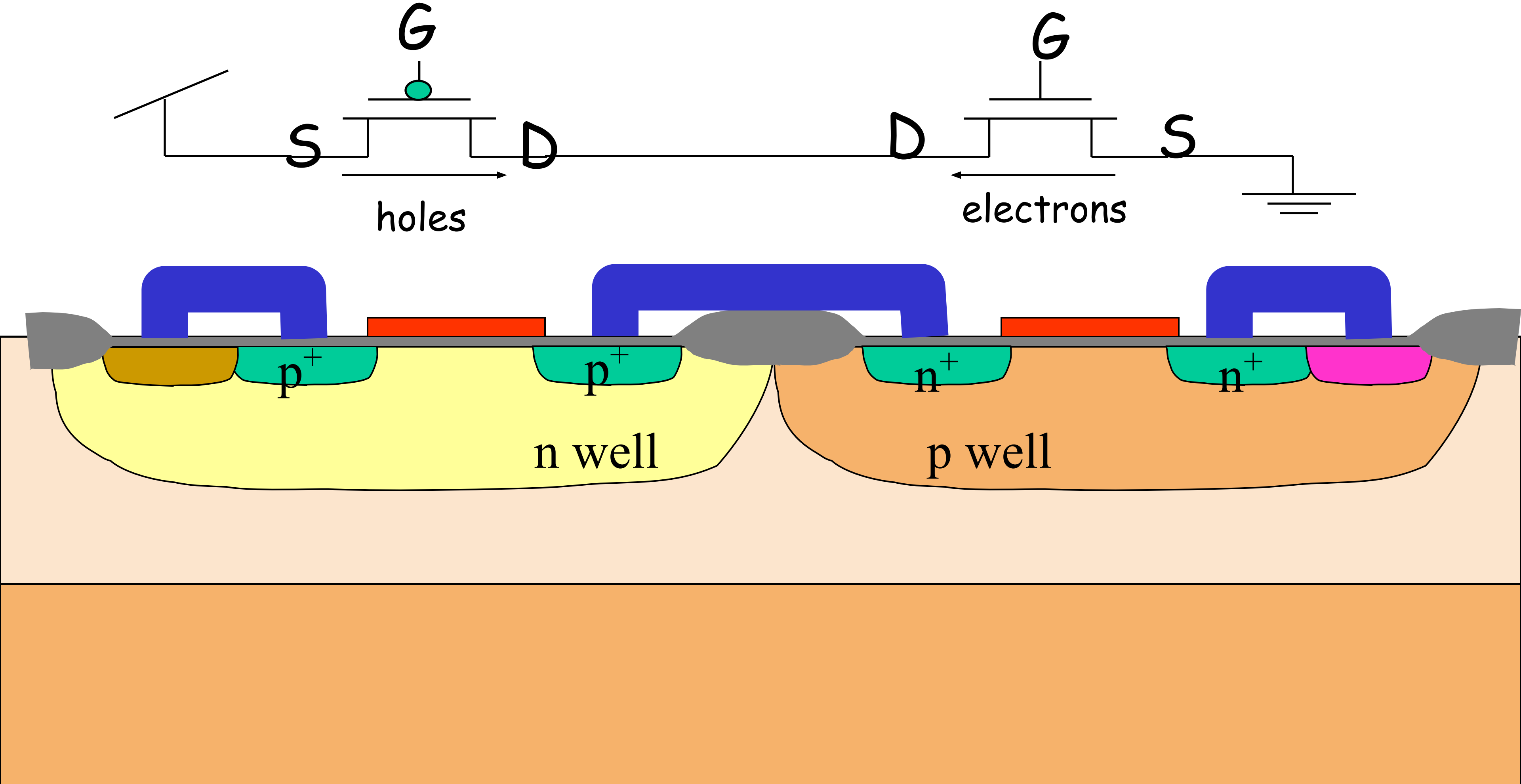
Bardeen and Brattain

1947

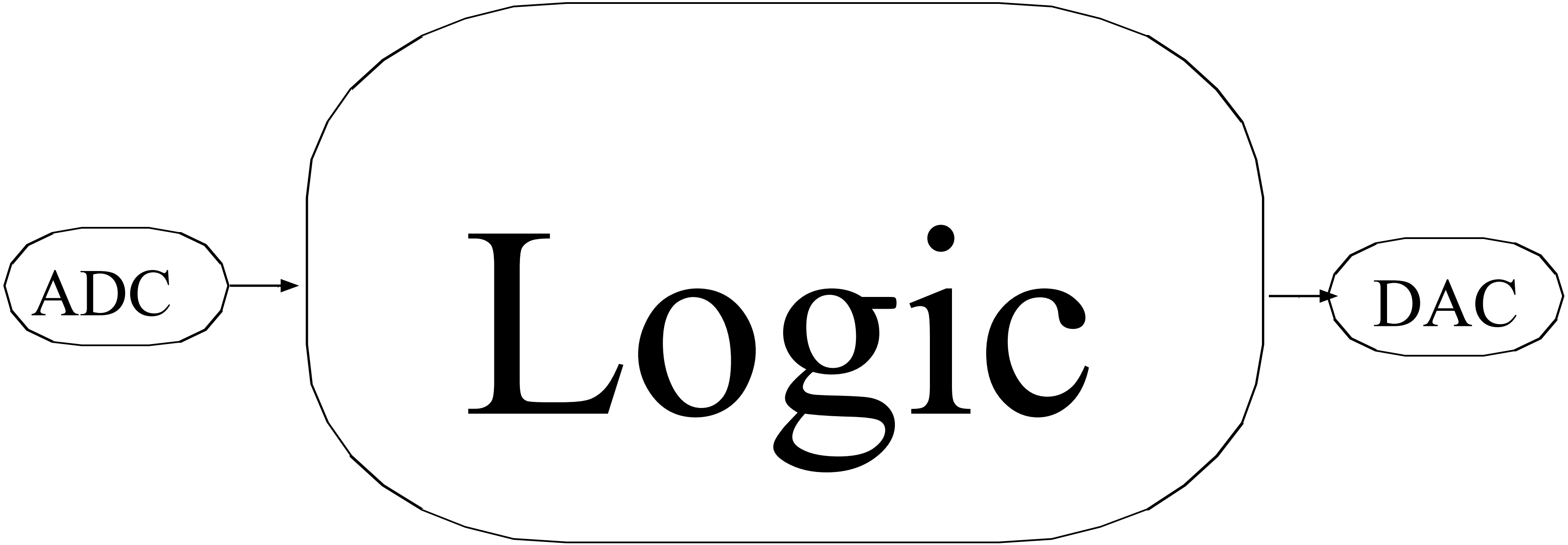


2000

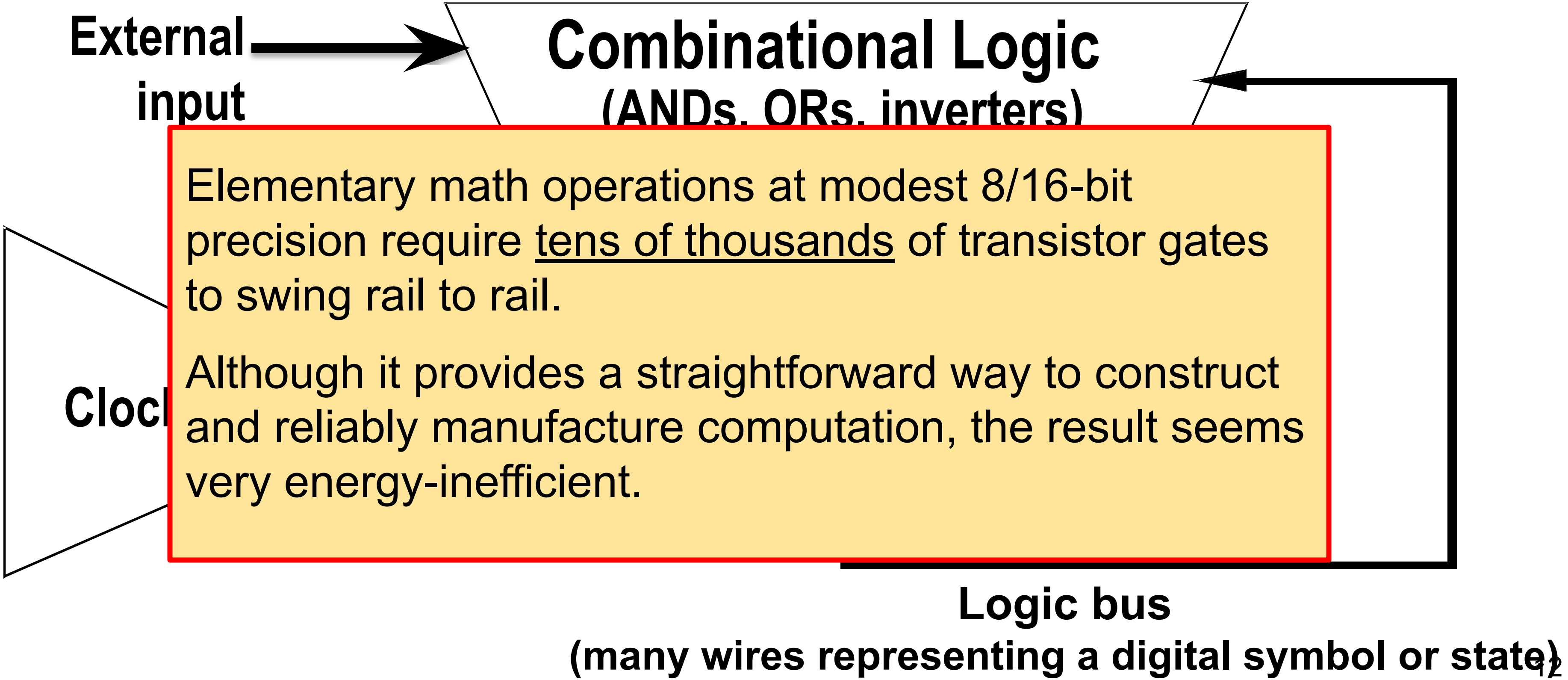



G
S
D
holes
G
D
S
electrons
p+
p+
n+
n+
n well
p well

Artificial real-world computation (or: How industry thinks of analog)



Synchronous logic is ubiquitously used to implement Finite State Machines (FSMs)



Elementary math operations at modest 8/16-bit precision require <u>tens of thousands</u> of transistor gates to swing rail to rail.

Although it provides a straightforward way to construct and reliably manufacture computation, the result seems very energy-inefficient.

The motivation from biological computation

Natural computation

even with 10kW computer power we cannot do this

Flies acrobatically
Recognizes patterns
Navigates
Forages
Communicates

10uW
10^6 neurons, 10^9 synapses
10 op/s/synapse

10^{-15} J/op
(op=synaptic activation)

Digital silicon 10^{-7} to 10^{-13} J/op (MAC)

Biology is 10^8 to 10^3 times as efficient as digital silicon

Sparsity

Estimate energy use and spike rate in the human brain

$$\underset{\text{Neurons*}}{10^{11}} \times \underset{\text{Syn/neuron}}{10^{4}} \times \underbrace{\underset{\text{V}}{10^{-1}} \times \underset{\text{A}}{10^{-9}} \times \underset{\text{sec}}{10^{-3}}}_{\text{J/syn. Act.}=10^{-13}\text{J}=\mathbf{0.1pJ}} \times \underset{\text{Avg. spike rate}}{X} = \underset{\text{W}}{10^{1}}$$

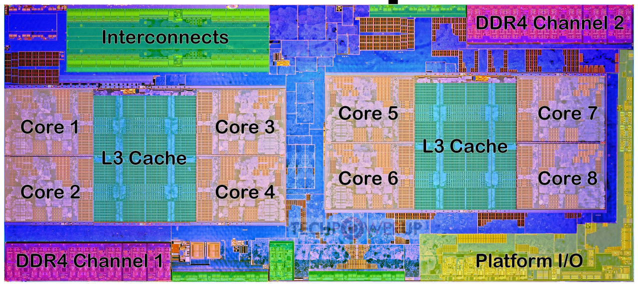
Avg. **output** spike rate = 1 Hz

10^4 fan-out means avg. synaptic **input** rate per neuron = 10 kHz

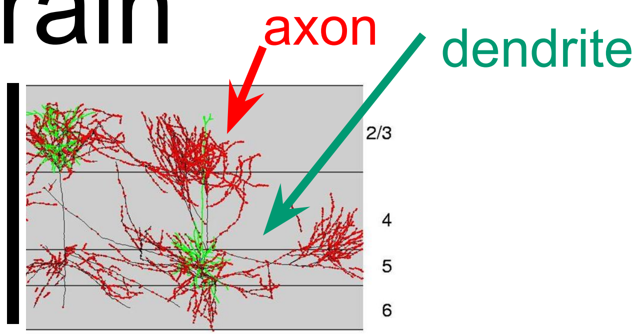
It is very different than conventional DNNs, where every neuron sends its messages to all recipients at the frame rate, e.g. 100Hz

Computer vs. Brain

AMD Ryzen
192mm^2
5B FETs
180W



Cortex
1mm^3
100k neurons
1B synapses
~1mW



Anderson et al.
2003

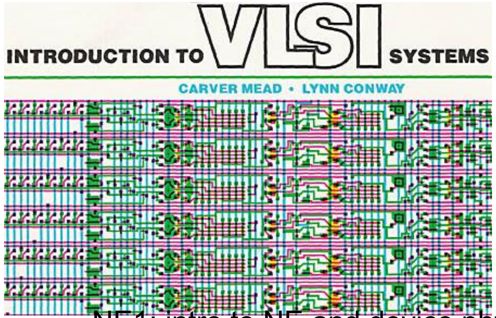
At the system level, brains are about 1 million times more power efficient than computers. Why?
Cost of elementary operation (turning on transistor or activating synapse) is about the same. It's not some magic about physics.

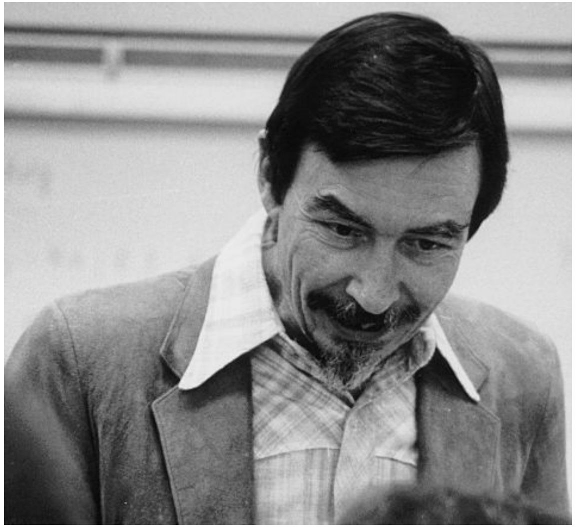
Computer	Brain
Fast global clock	Self-timed, sparse computation (avg spike rate in brain ~1Hz)
Bit-perfect deterministic logical state	Synapses are stochastic! 20% probability. Computation dances: digital→analog→digital
Memory distant in time and space to computation	Memory in synapses, at computation
Devices frozen on fabrication	Constant adaptation and self-modification

The fact that we can build devices that implement the same basic operations as those the nervous system uses leads to the inevitable conclusion that we should be able to build entire systems based on the organizing principles used by the nervous system.

Proc. IEEE, 1990

Carver Mead, Physicist by inclination
1966 Inventor of GaAs MESFET transistor
1970's: Coiner of term "Moore's Law"
1980 Co-author of main logic design textbook for 20 years
2013: ISSCC keynote talk (see more cool talks here)
"The high priest of silicon"

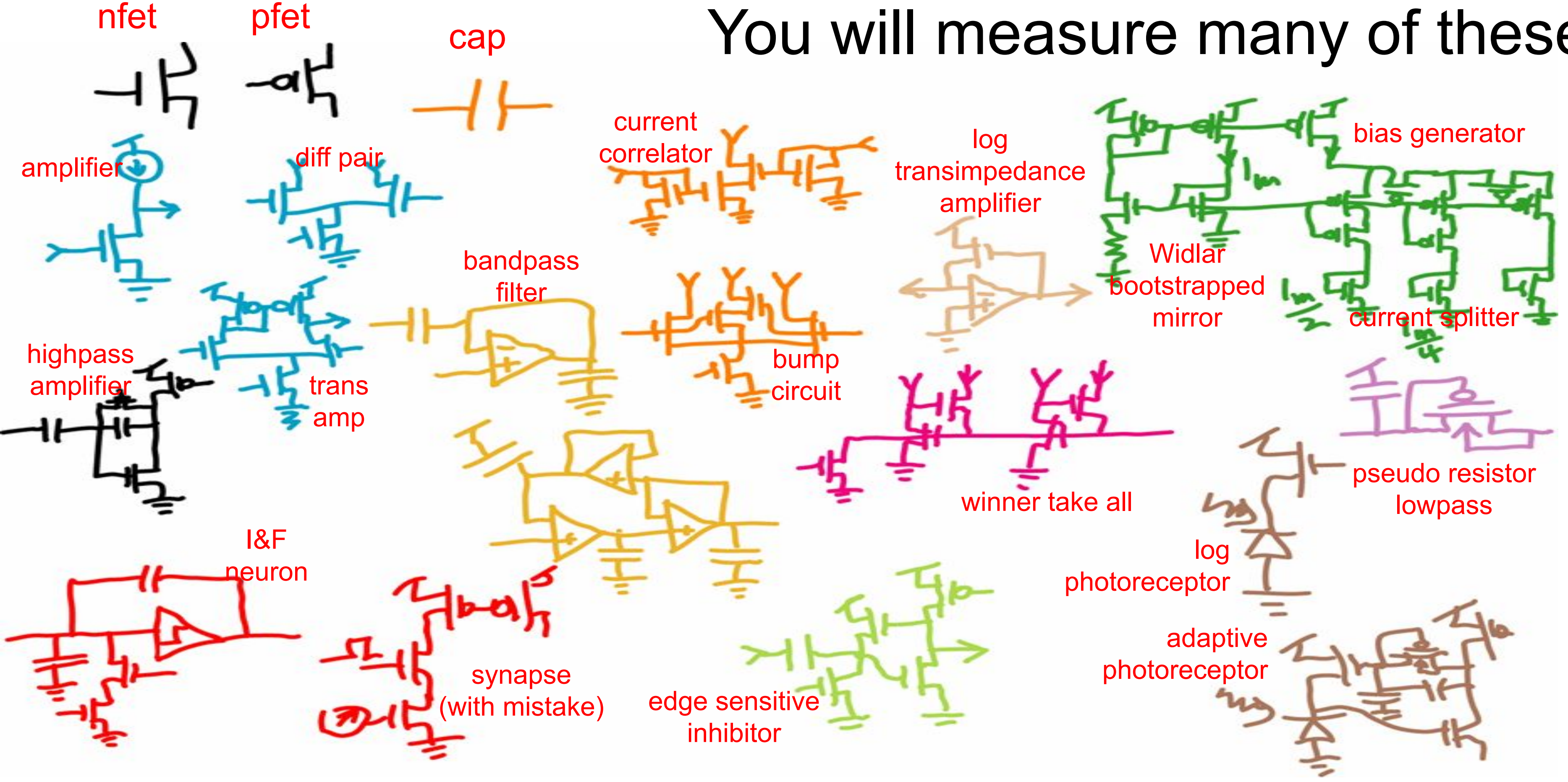




T Delbruck, CNS182 class, Caltech, ca 1989

Exercises:
First look

You will measure many of these



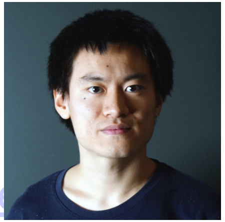
Lab exercises organization

- The labs are done in groups of 2 remotely via zoom and TLJH; the best way is for two to meet in person with your laptops, and use one for zoom and the other for TLJH.
- The first three labs last 2 hours, the rest are 4 hours (the whole morning/afternoon in which you sign up), the material for the corresponding week will be published at the end of the lecture.
- Please use the OLAT Forum to look for your lab partner.
- You should hand in the prelab, lab report and post-lab as a group on OLAT dropbox before your next lab starts.
- For questions regarding the labs, please contact chenxi@ini.uzh.ch

TLJH= The Littlest JupyterHub

Links for the lab exercises

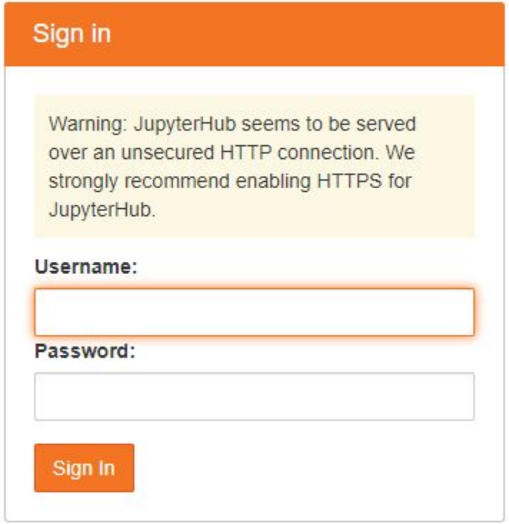
Chenxi



lab1-scheduling: Sign up at this lab exercise doodle.

Jupyter notebooks https://code.ini.uzh.ch/CoACH/CoACH-labs/tree/patch-1/jupyte

- Lab 1: Automated Data Acquisition and Analysis (Running the classchip)
- Lab 2-3: Subthreshold Behavior of Transistors, Transistor superthreshold saturation current and drain characteristics
- Lab 4-5: Static Circuits: Current Mirror, Differential Pair, Current Correlator, Bump Circuit, and Transconductance Amplifier
- Lab 6: Winner-Take-All circuit
- Lab 7: Integrator Circuits
- Lab 8: Photoreceptors I: Phototransduction
- Lab 9: Photoreceptors II: Photoreceptor Circuits
- Lab 10: Silicon Synaptic Circuits
- Lab 11: Silicon Neuron Circuits
- Lab 12: *TBA*



2020
Class chip: COaCH

AMS (Austria Microsystems)
180nm technology
t_{ox}=3.75 nm, C_{ox}=9 fF/um^2.

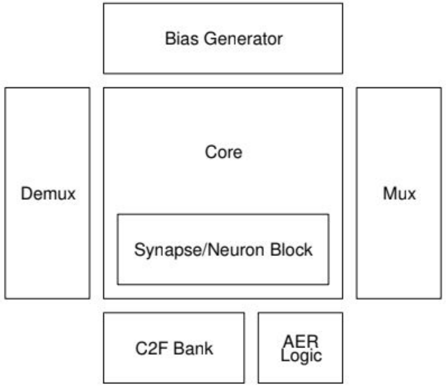
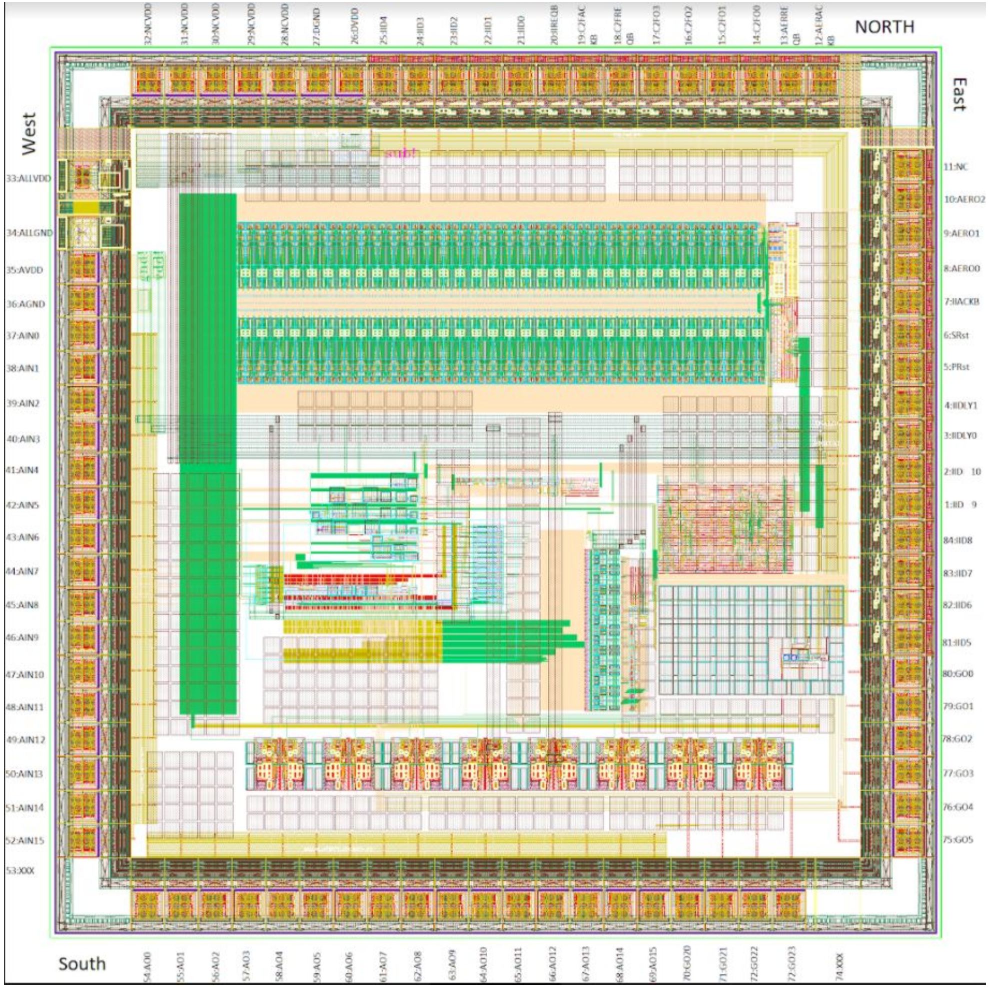
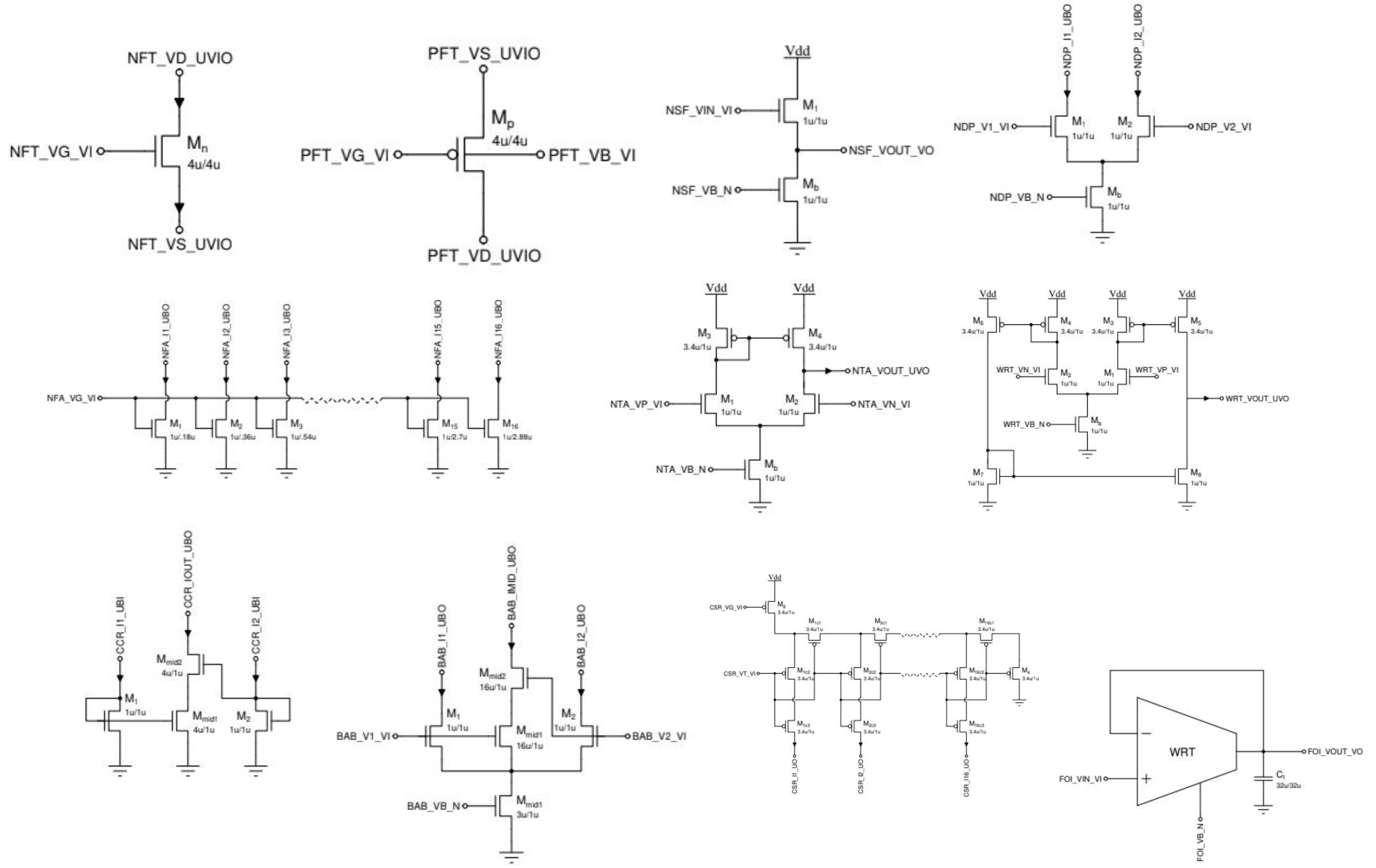


Figure 3: Overview block diagram of the chip architecture. Note that blocks are not drawn to scale - the core is in fact very small, and the bias generator larger than the other blocks combined.

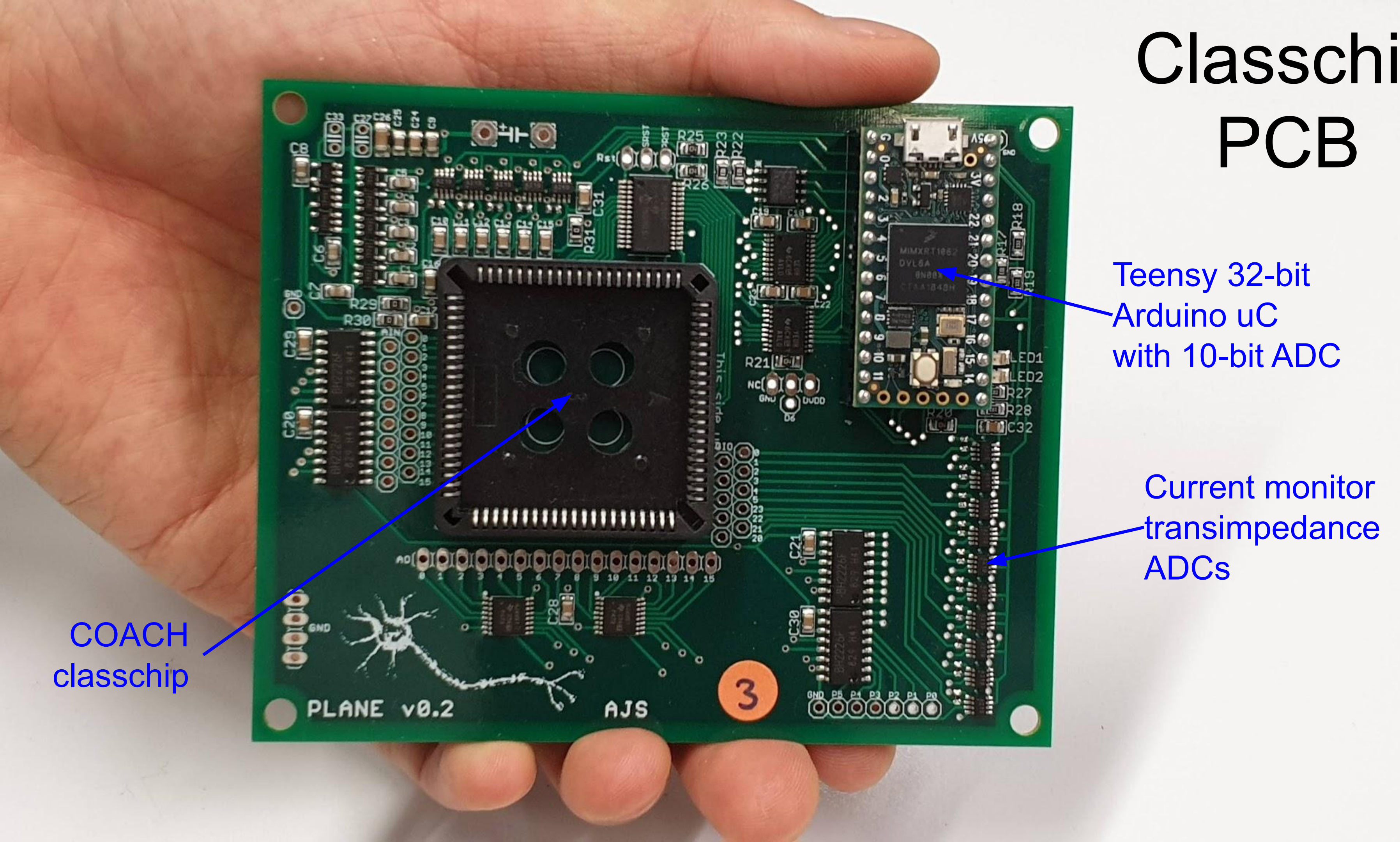


Partial contents of class chip

3 Test Circuits

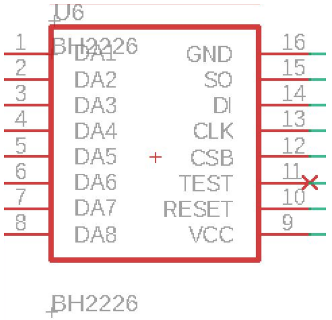


Classchip PCB

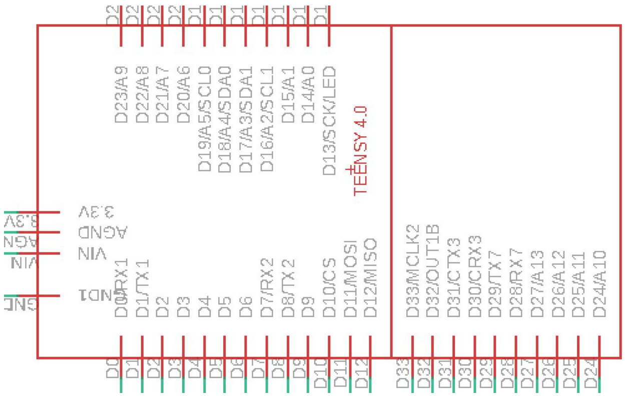


Measuring currents and voltages

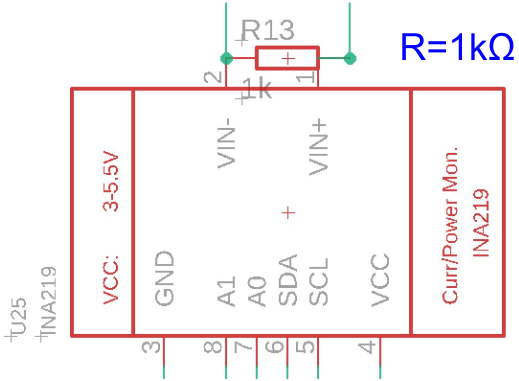
Set voltages using 8-bit 2226 DAC



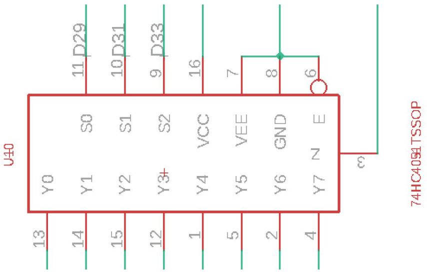
Measure voltages using Teensy 10-bit ADC: Vref=Vdd=3.3 V.

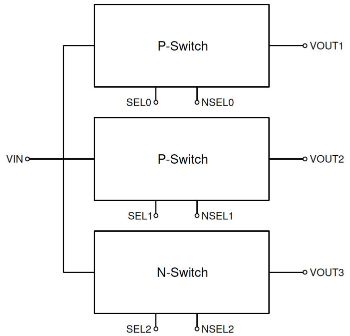


Measure large currents with the INA219 Bidirectional current meter



Select circuit pins with on-chip multiplexers



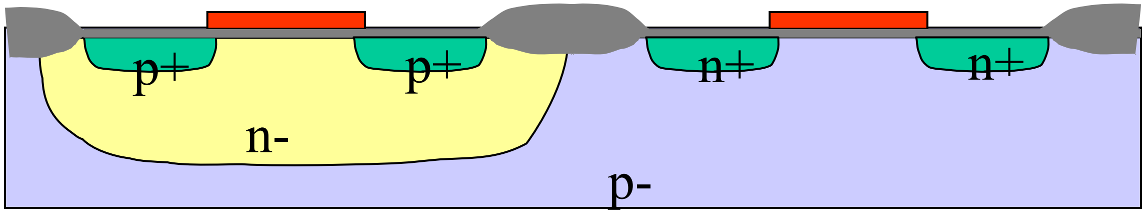


Measure small currents with the on-chip transimpedance amplifier:
you will learn in the exercise

Python notebooks show you the API

First look at semiconductors and transistors

MOS transistors – semiconductor device physics



We need to understand enough about semiconductors and junctions to understand how MOS transistors work

- Insulators, conductors, semiconductors
- Crystal structure of silicon
- Band structure (valence, conduction, and forbidden bands)
- Holes and electrons
- Mechanisms of charge transport (diffusion & drift)
- Doping with donors and acceptors
- Fermi-Dirac distribution
- Law of mass action ($np=n_i^2$)
- p-n junction
- Reverse biased junction and its capacitance

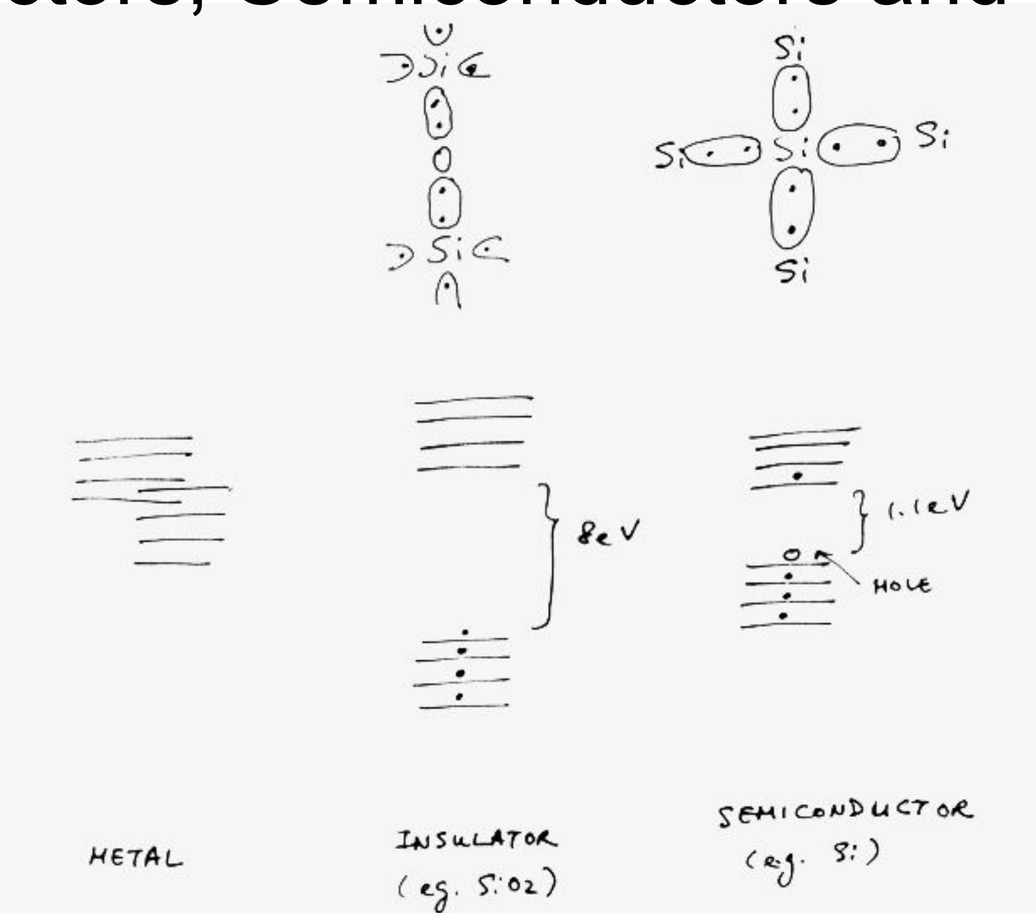
Donors and Acceptors in the periodic table

I	II	III	IV	V	VI	VII	Zero
H							He
Li	Be	B	C	N	O	F	Ne
Na	Mg	Al	Si	P	S	Cl	Ar
K	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Cd	In	Sn	Sb	Te	I	Xe

Acceptors
1 missing electron

Donors
1 extra electron

Conductors, Semiconductors and Insulators



Mead, ca 1989, from Andy Grove

Donors and Acceptors in the periodic table

I	II	III	IV	V	VI	VII	Zero
H							He
Li	Be	B	C	N	O	F	Ne
Na	Mg	Al	Si	P	S	Cl	Ar
K	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Cd	In	Sn	Sb	Te	I	Xe

Acceptors | Donors

1 missing electron | 1 extra electron

The silicon lattice with an electron donor atom

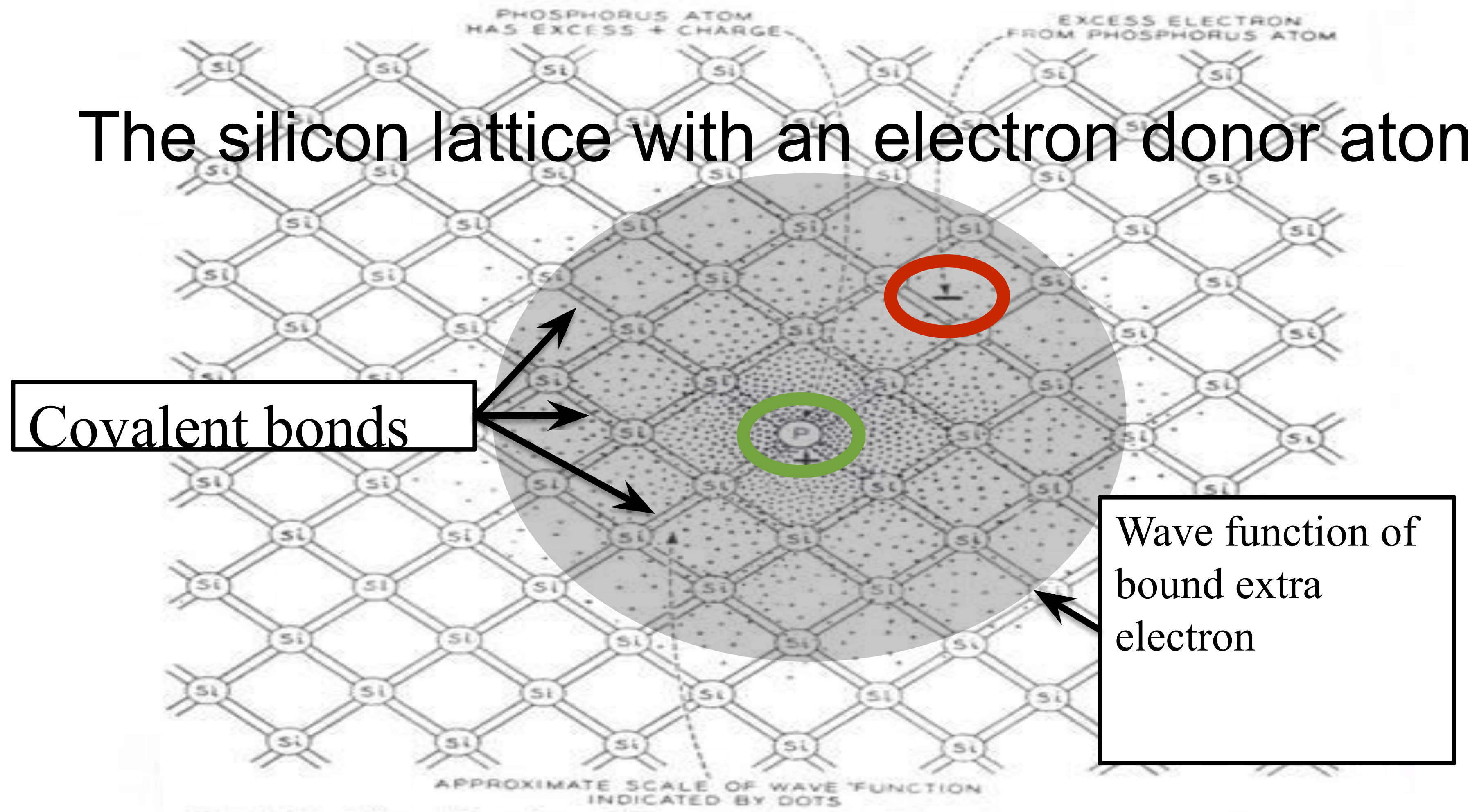
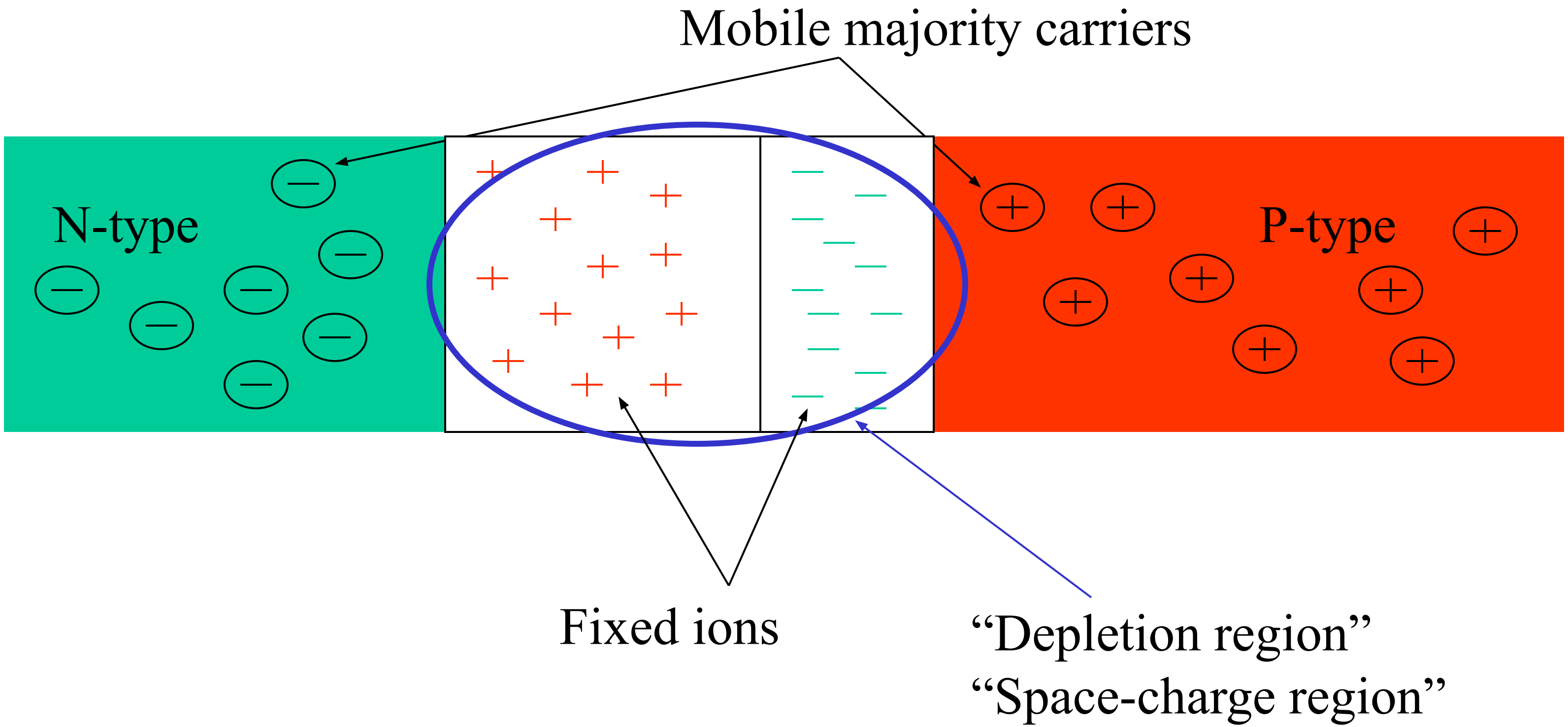
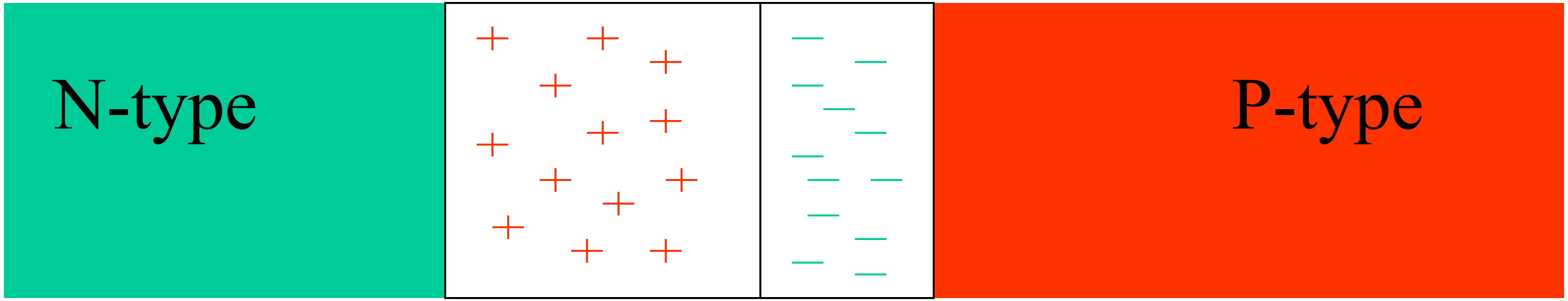


FIG. 1–14—Wave Function of Electron Bound to Phosphorous Atom in Silicon.

A P-N junction



A P-N junction



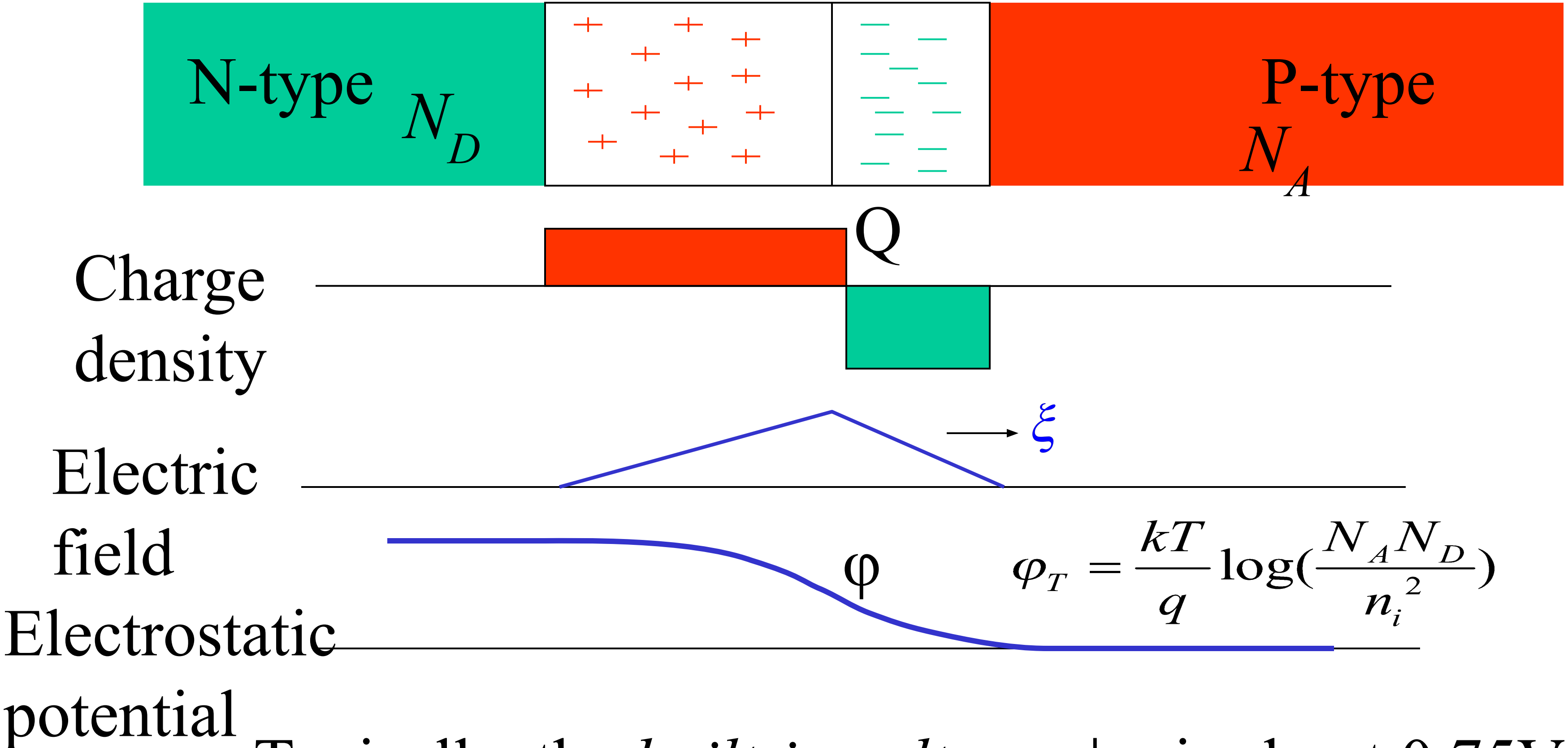
Electric field

Diffusion of holes from *p* region

Diffusion of electrons from *n* region

In equilibrium, *Drift* = *Diffusion* for electrons *and* holes

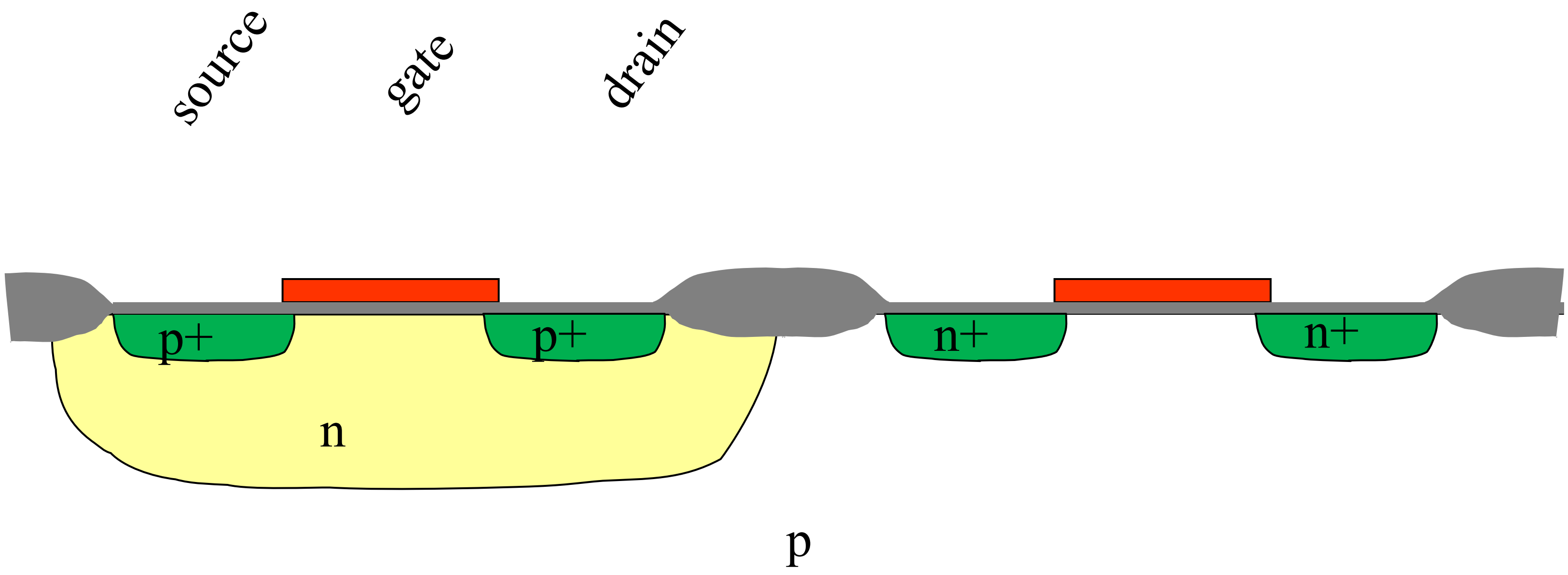
Charges, fields, and potentials in a PN junction



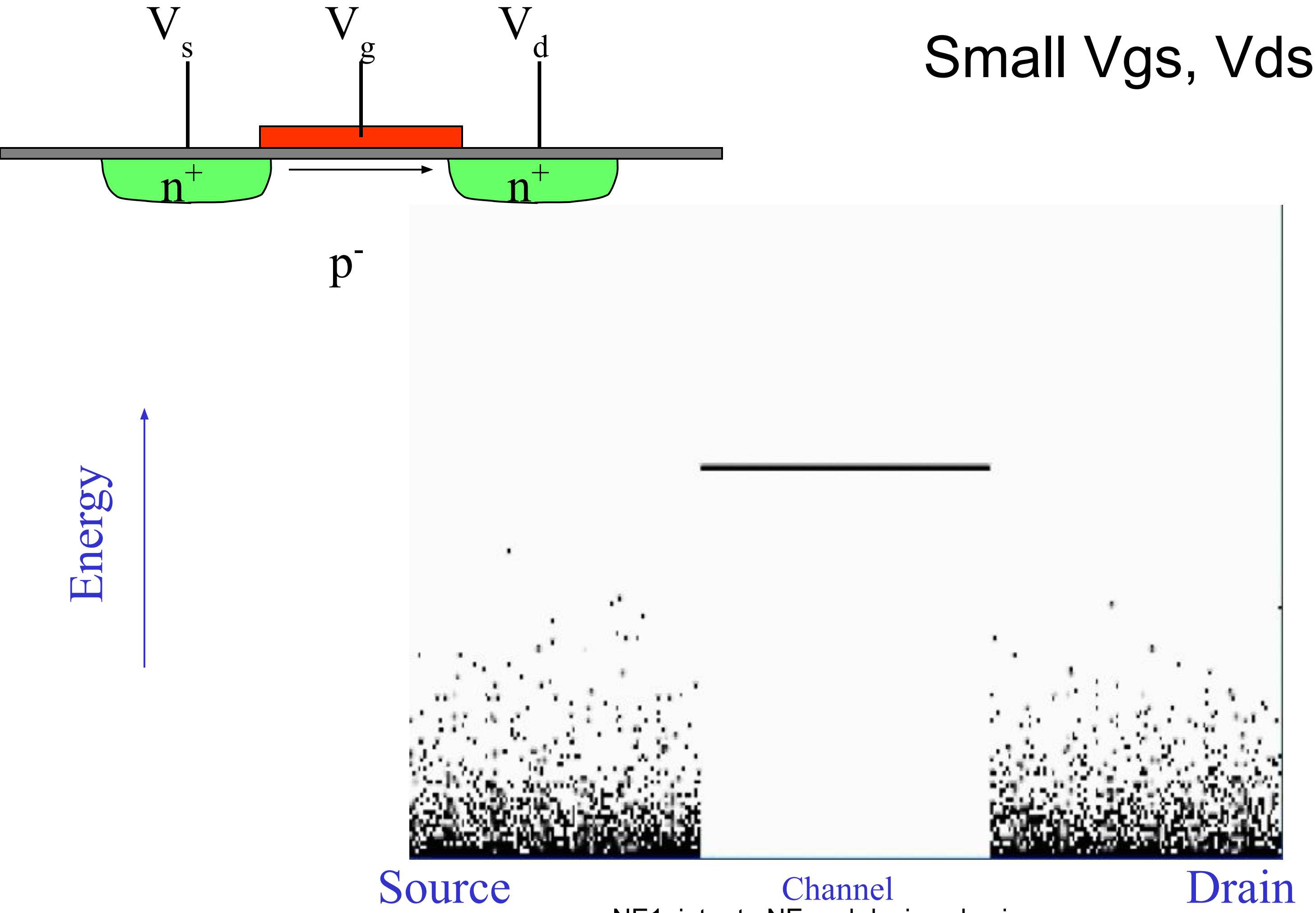
$$\varphi_T = \frac{kT}{q}\log\left(\frac{N_A N_D}{n_i^2}\right)$$

Typically, the *built-in voltage*, ϕ_T, is about 0.75V

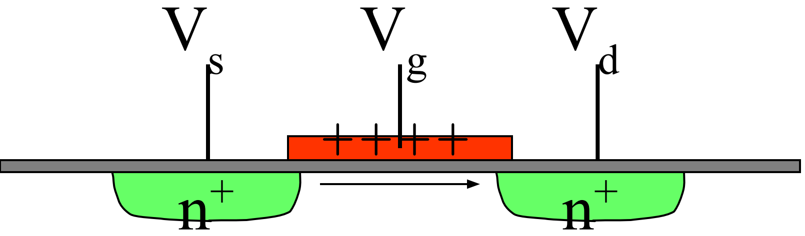
MOS transistors use insulated gates to control barrier energies at PN surface junctions at source and drain

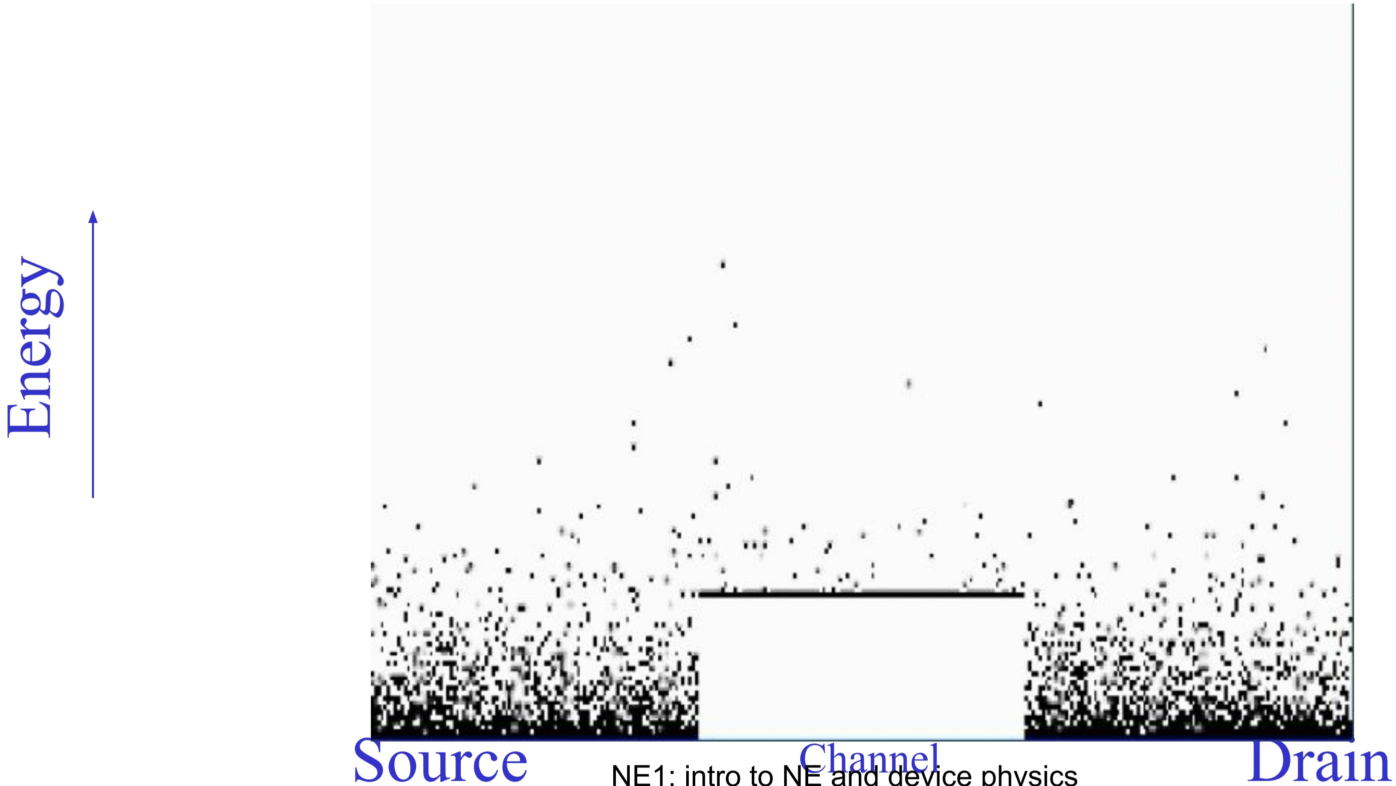


Small Vgs, Vds=0

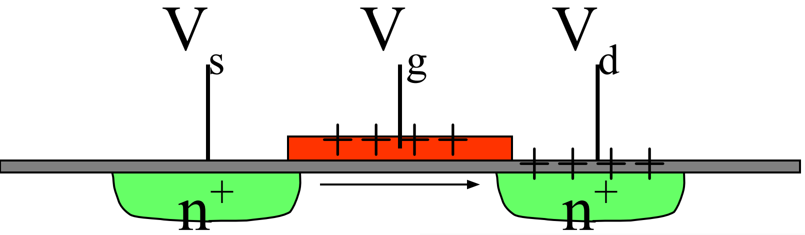


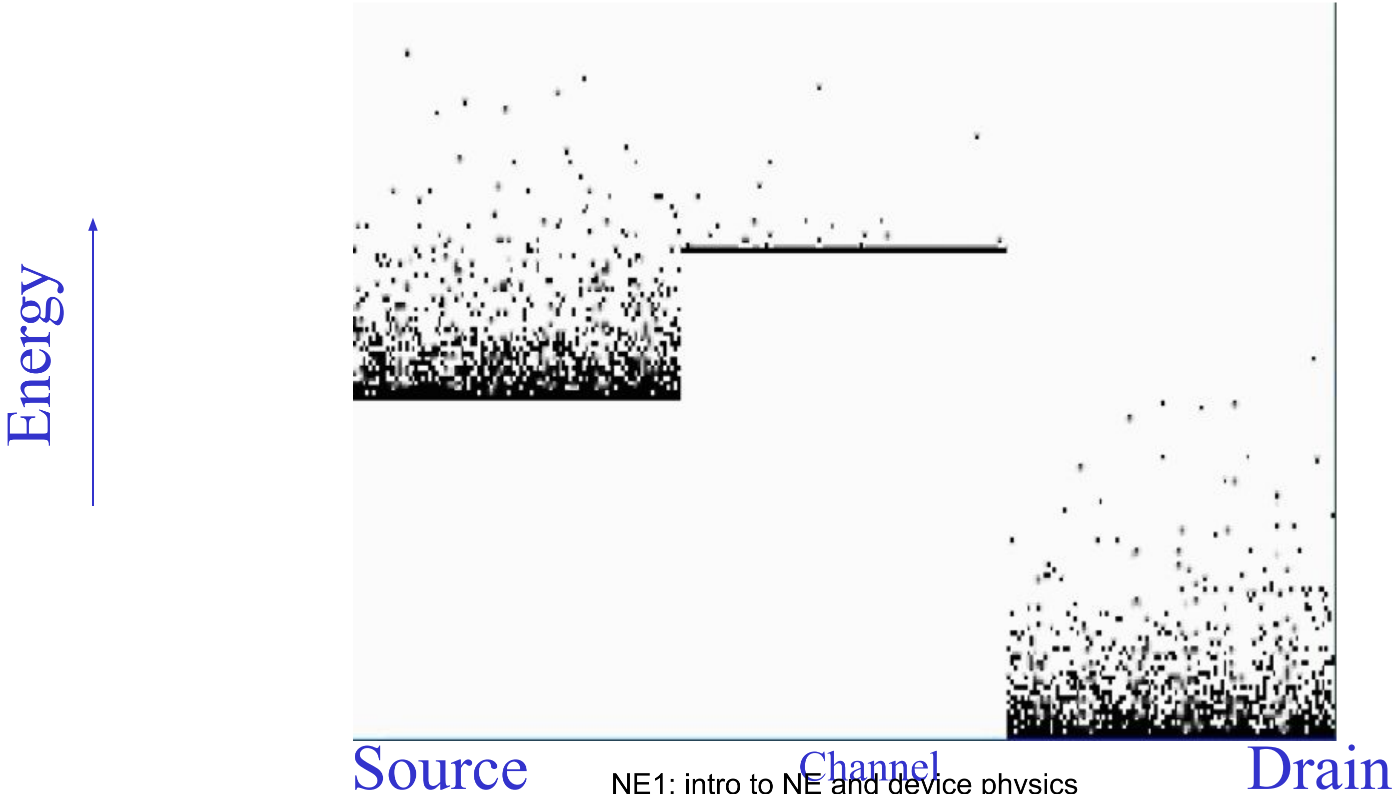
Larger Vgs, Vds=0





Larger Vgs, Large Vds





Closer look at silicon crystal structure and energy bands

The Diamond Structure of Silicon

Each atom is <u>covalently</u> bonded to 4 neighbors

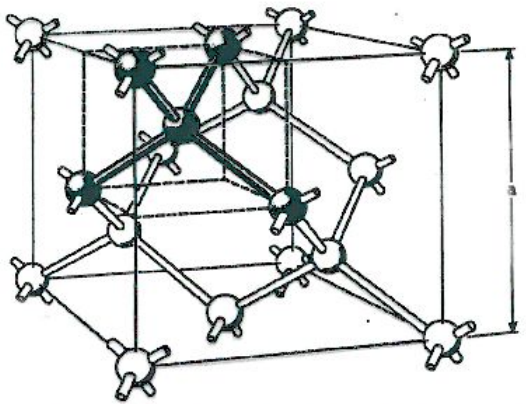


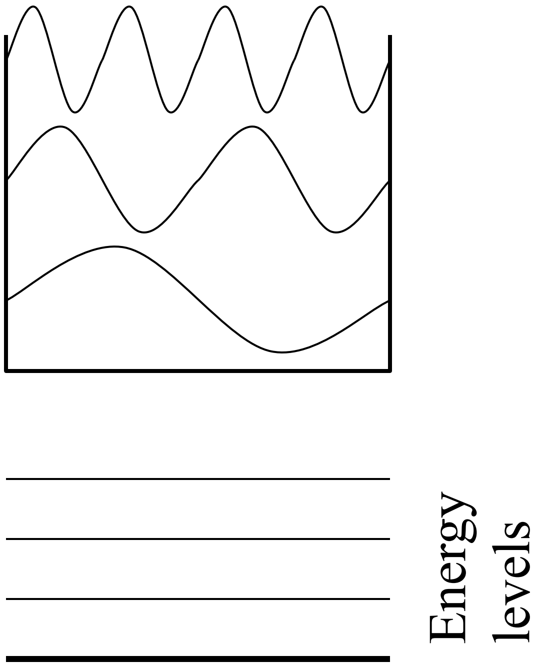
FIG. 1-3--The Diamond Structure, Showing How Each Atom Forms Four Bonds with Its Nearest Neighbors.

C Ge Si GaAs

Si dominates because it has a clean oxide interface: SiO_2

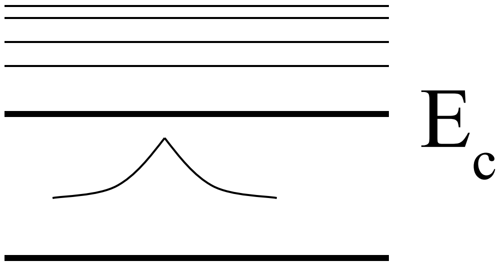
Bands arise from periodic structure of crystal

Wavefunctions of electron in a box

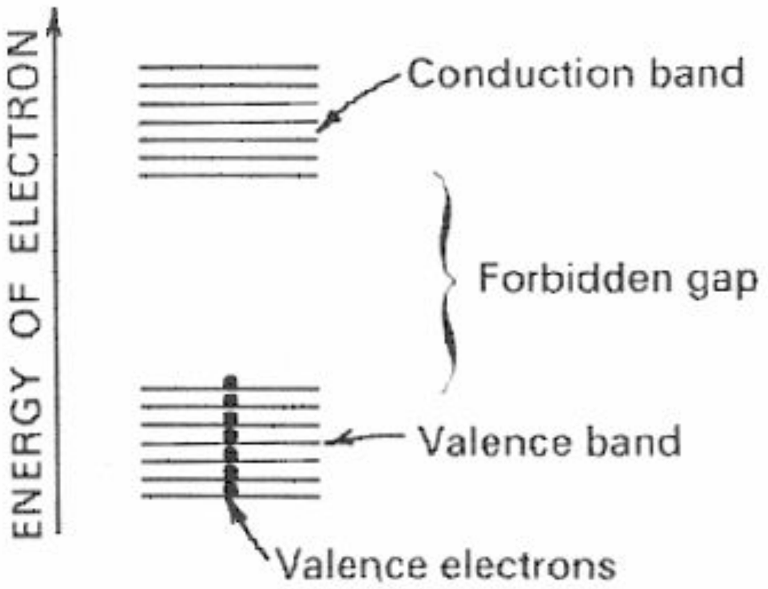


A crystal is like a periodic box

- Only wavefunctions with discrete nonzero energies act like free particles
- Wavefunctions at forbidden energies die off exponentially



Schematic energy band representation for electrons in a solid

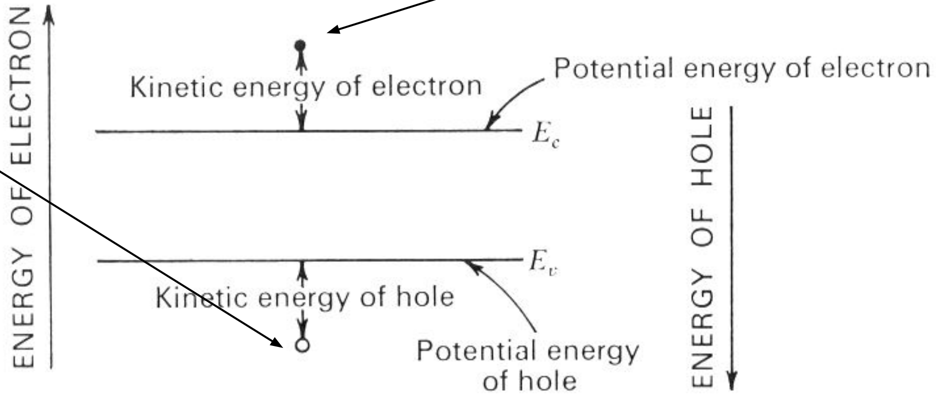


Electrons and *Holes*

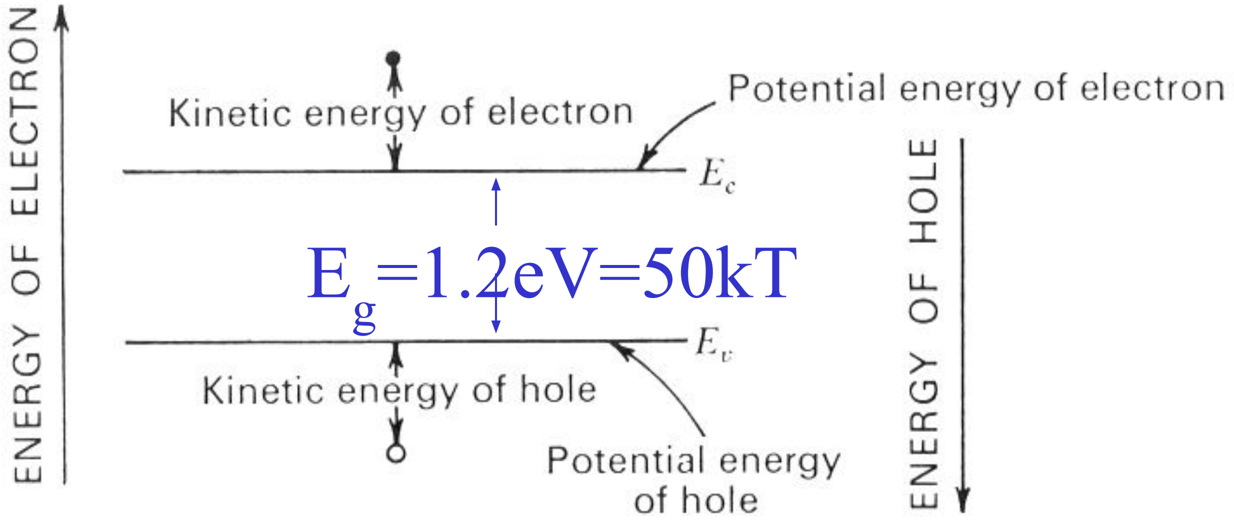
Holes are bubbles in the valence band

- The electrons move, but it is easier to talk about the vacancy (the hole) moving, just like it is easier to talk about a bubble moving than about the water around it moving
- Holes have positive charge and the *effective mass* in silicon is 2.5 times larger for a hole than for an electron

When electrons are broken loose from the lattice and enter the *conduction band*, they become *mobile*, and move almost as if in vacuum



The meaning of energy in the band diagram



The *band gap* of silicon is about 1.2eV at room temperature

The *Thermal Energy*

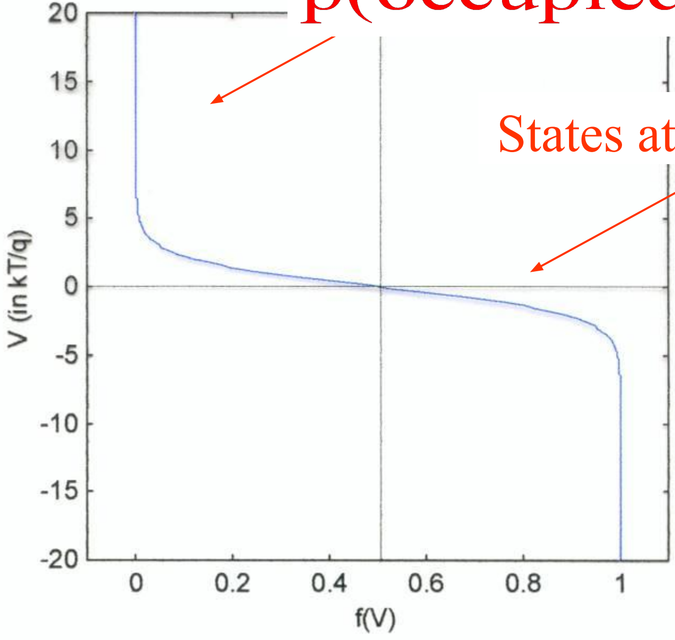
- Each *degree of freedom* of a system in thermal equilibrium has average energy ***kT/2***, where ***k*=1.38 × 10^{-23} J/K** is **Boltzmann's constant** and ***T*** is absolute temperature. I.e. at 300C, *kT*=4.1 × 10^{-21} J
- The **thermal voltage** ***kT/q*** is the voltage a single charge falls through to pick up the thermal energy *kT*
- ***q*** *i*s the ***elementary charge*** 1.6 x 10^{-19} C
- **$U_T \equiv kT/q$=25mV**=1/40V at room temperature
- ***kT/q* is the natural scale of voltage for electronic systems in thermal equilibrium**

The Fermi-Dirac distribution

States above Fermi level are **occupied** with Boltzmann distribution

$$\mathrm{p(occupied)} \approx e^{-(E-E_f)/kT}$$

Energy relative to Fermi level in kT units



States at the Fermi level are ½ occupied

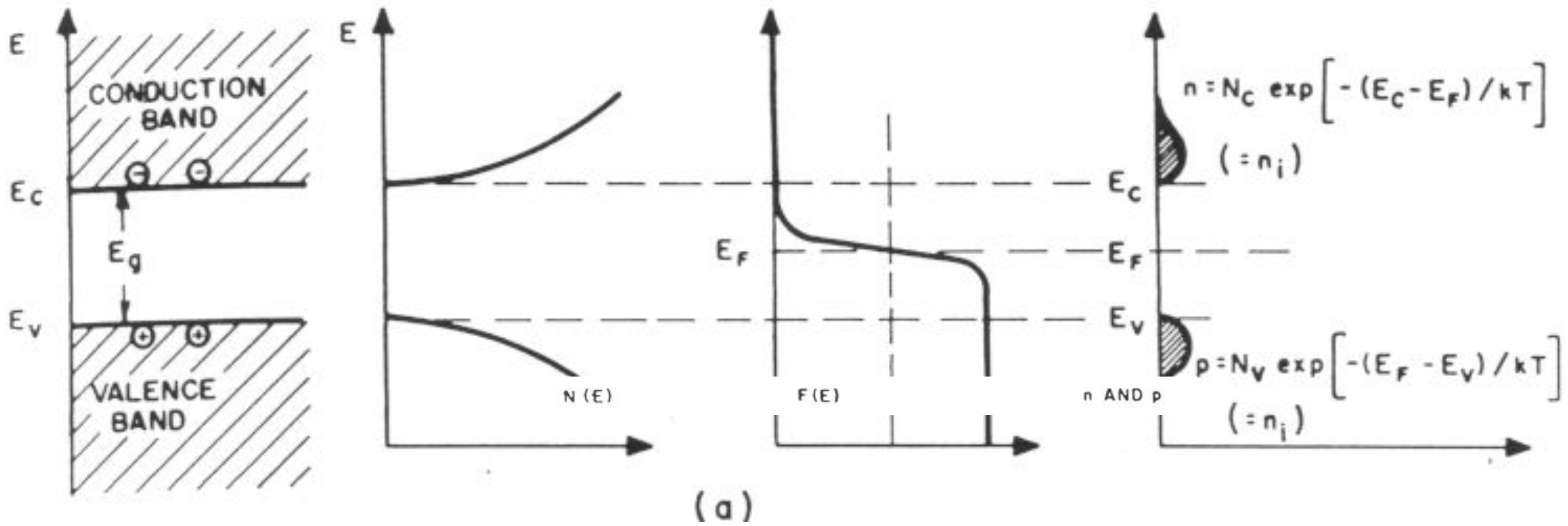
E_f

States below Fermi level are **unoccupied** with Boltzmann distribution

$$\mathrm{p(unoccupied)} \approx e^{-(E_f-E)/kT}$$

Probability of occupation of a state

An *intrinsic* (undoped) semiconductor



Band diagram | Density of states | Fermi-Dirac distribution | Carrier concentrations

Donors and Acceptors in the periodic table

I	II	III	IV	V	VI	VII	Zero
H							He
Li	Be	B	C	N	O	F	Ne
Na	Mg	Al	Si	P	S	Cl	Ar
K	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Cd	In	Sn	Sb	Te	I	Xe

Acceptors	Donors
1 missing electron	1 extra electron

Doping levels

- Concentration (density) of Si is about $10^{23}/cm^3$
- Doping can vary from about $10^{15}/cm^3$ to $10^{19}/cm^3$
- These doping levels still represent only a tiny fraction of the total atoms, from 10^{-8} to 10^{-4}

A donor atom in the silicon lattice

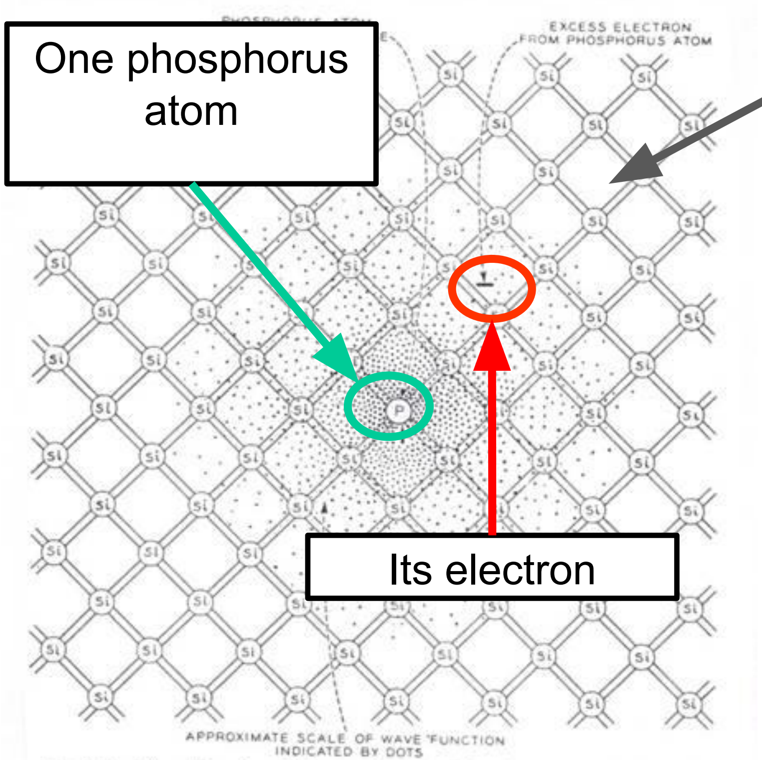


FIG. 1-14—Wave Function of Electron Bound to Phosphorous Atom in Silicon.

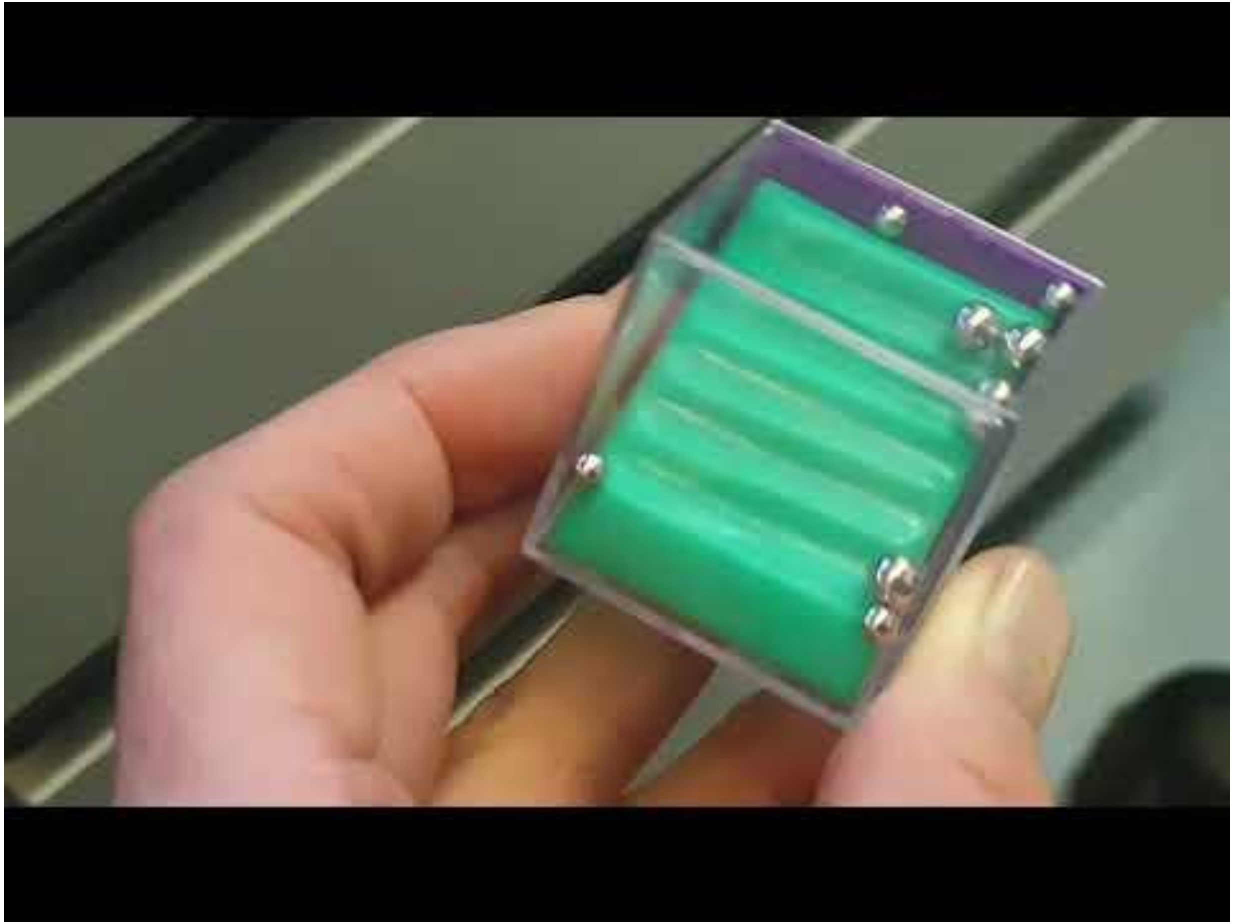
Binding energy of phosphorus donor electron is reduced from free atom binding energy (~0.5 eV) approximately by silicon *dielectric constant*

$$\varepsilon_{Si} \approx 12\varepsilon_0$$

$$E_{binding} \approx \frac{0.5eV}{12} \approx 0.05eV \approx 2kT$$

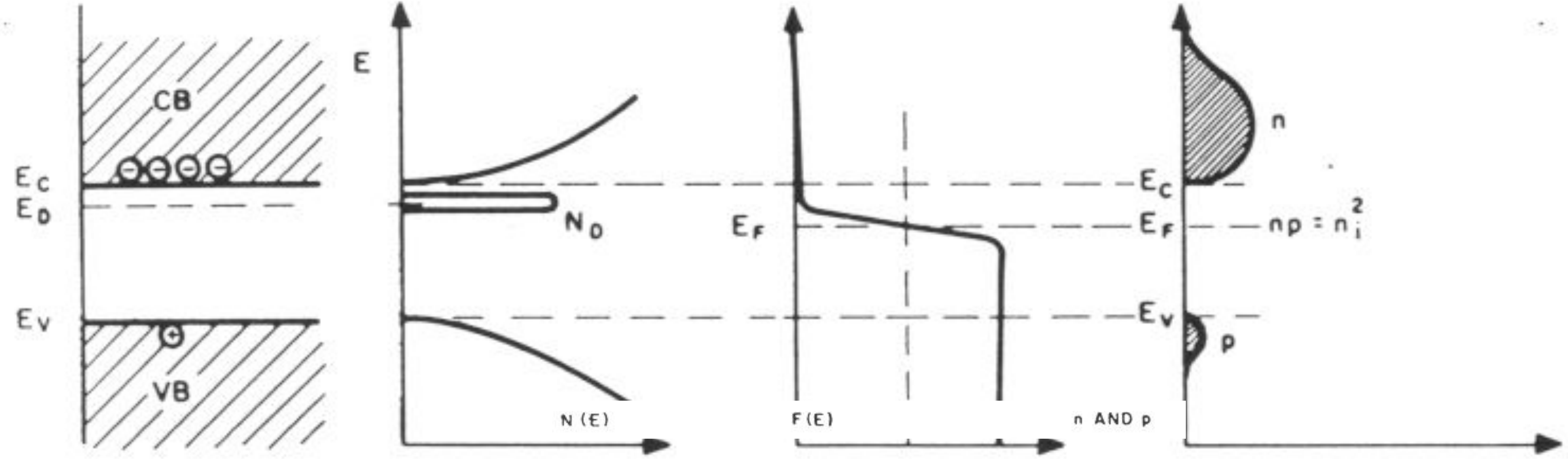
So why does it donate a free electron? It is still bound with twice the thermal energy.

Answer: There are many more ways (states) to be free than bound. Practically <u>all</u> donor electrons are *mobile electrons* at room temperature

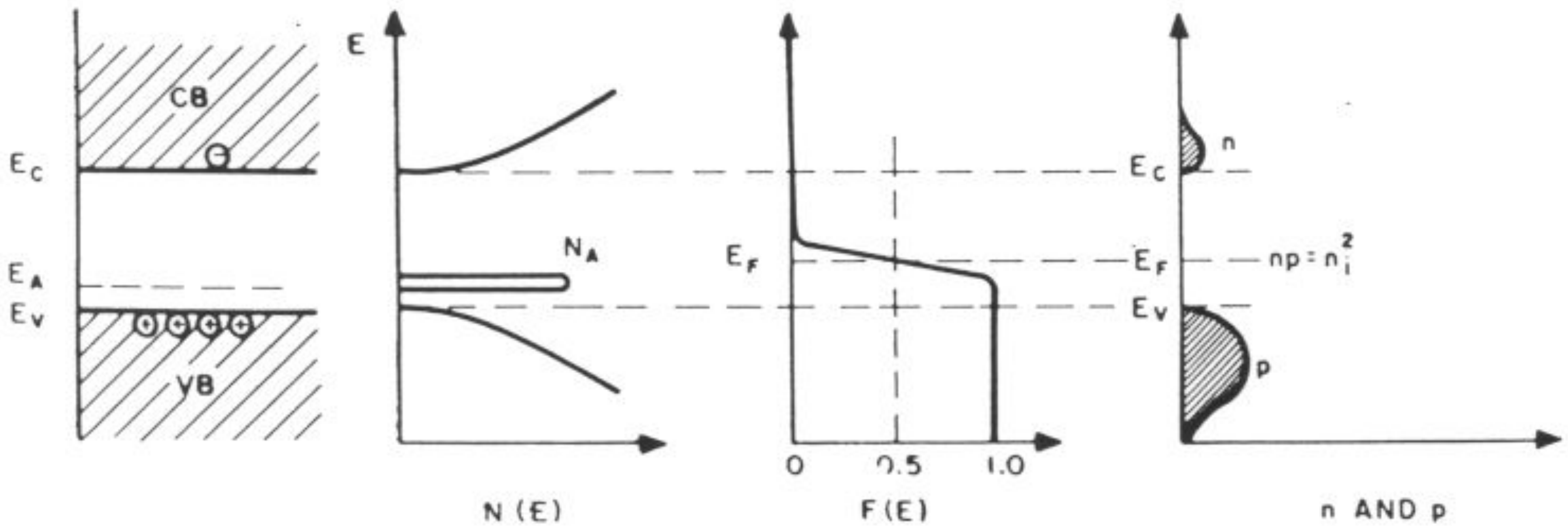


Ball “binding energy” is substantial, but there are so many other possible unbound states that it is very unlikely to be in the correct configuration

An *n-type* semiconductor



A *p-type* semiconductor



Law of mass action: $\boldsymbol{np=n_i^2}$

- In equilibrium, more holes means less electrons, and vice-versa.
- n_i is the *intrinsic carrier density*
- At room temperature n_i is $10^{10}/\text{cm}^3$, or about $1/10^{13}$ Si atoms.
- n_i increases with temperature

Electron transport

1. *Drift* and *Diffusion*
2. *Mobility*
3. The *Einstein relation*

An electric field causes carriers to drift

Velocity

$$\vec{J} = qnv = qn\mu(\vec{\xi})$$

Current Flux

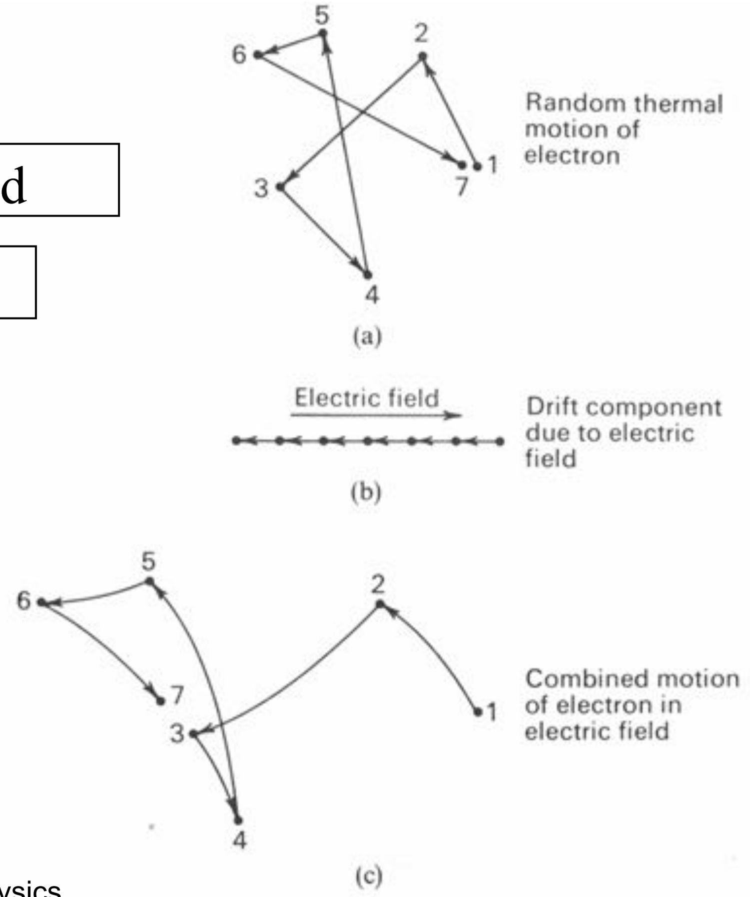
Charge density

Mobility

Electric field

$$\vec{J} \approx qn\mu\vec{\xi}$$

for $\vec{\xi}$ that causes velocities much less than the thermal velocity of ≈ 100 km/s



Mobility is a function of electric field

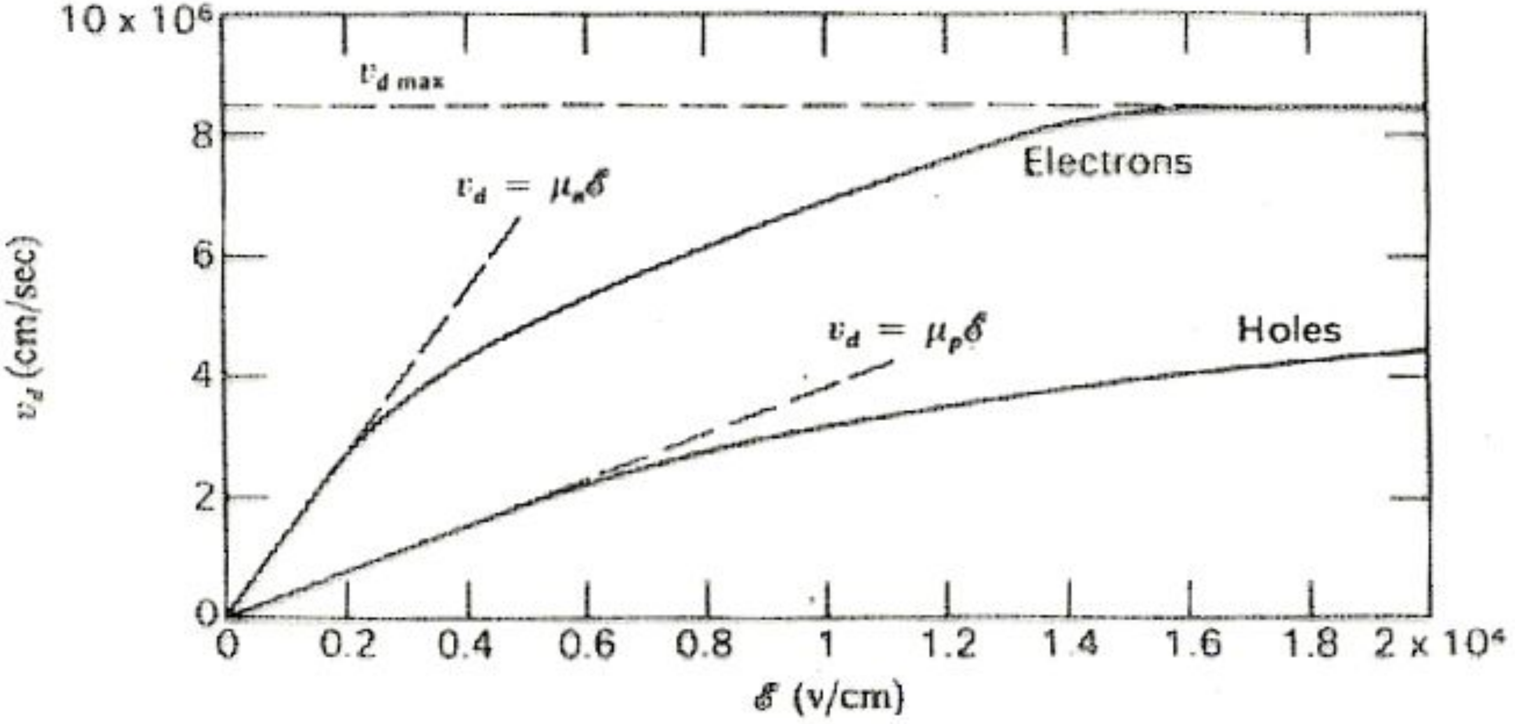
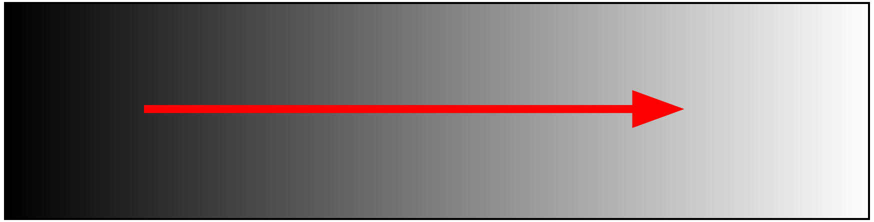


Fig. 4.10 Effect of electric field on the magnitude of the drift velocity of carriers in silicon.[3]

A density gradient causes carriers to <u>diffuse</u>



Diffusion current

$$\vec{J} = -Dq\vec{\nabla}n$$

Current Flux

Diffusion constant

Spatial gradient of charge density

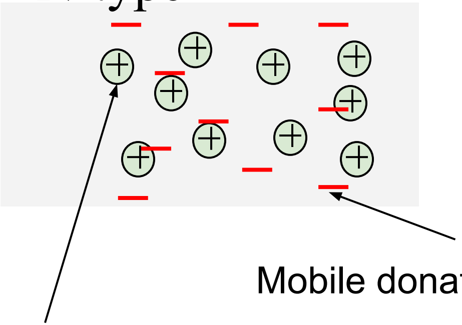
Drift and diffusion are related by the *Einstein Relation*

$$J_{diffusion} = -Dq\Delta n \qquad J_{drift} = \mu q\, n\, \xi$$

$$D = \frac{kT}{q}\mu$$

Charges, fields, and potentials in a PN junction

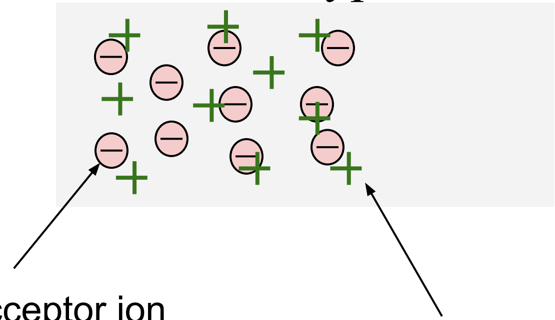
N-type



Mobile donated electron

Fixed donor ion (e.g. Phosphorus)

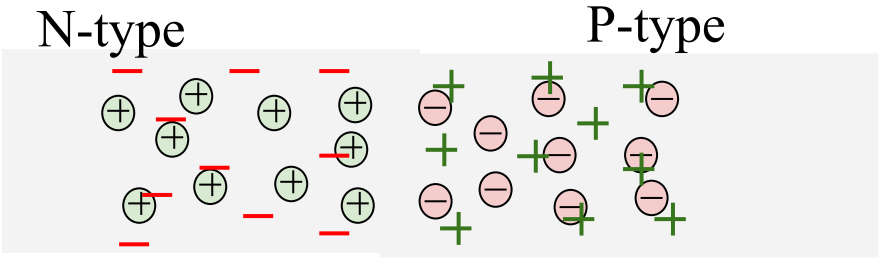
P-type



Fixed acceptor ion (e.g. Boron)

Mobile donated hole

What happens at a junction between P and N?



Lots of mobile electrons

Lots of mobile holes

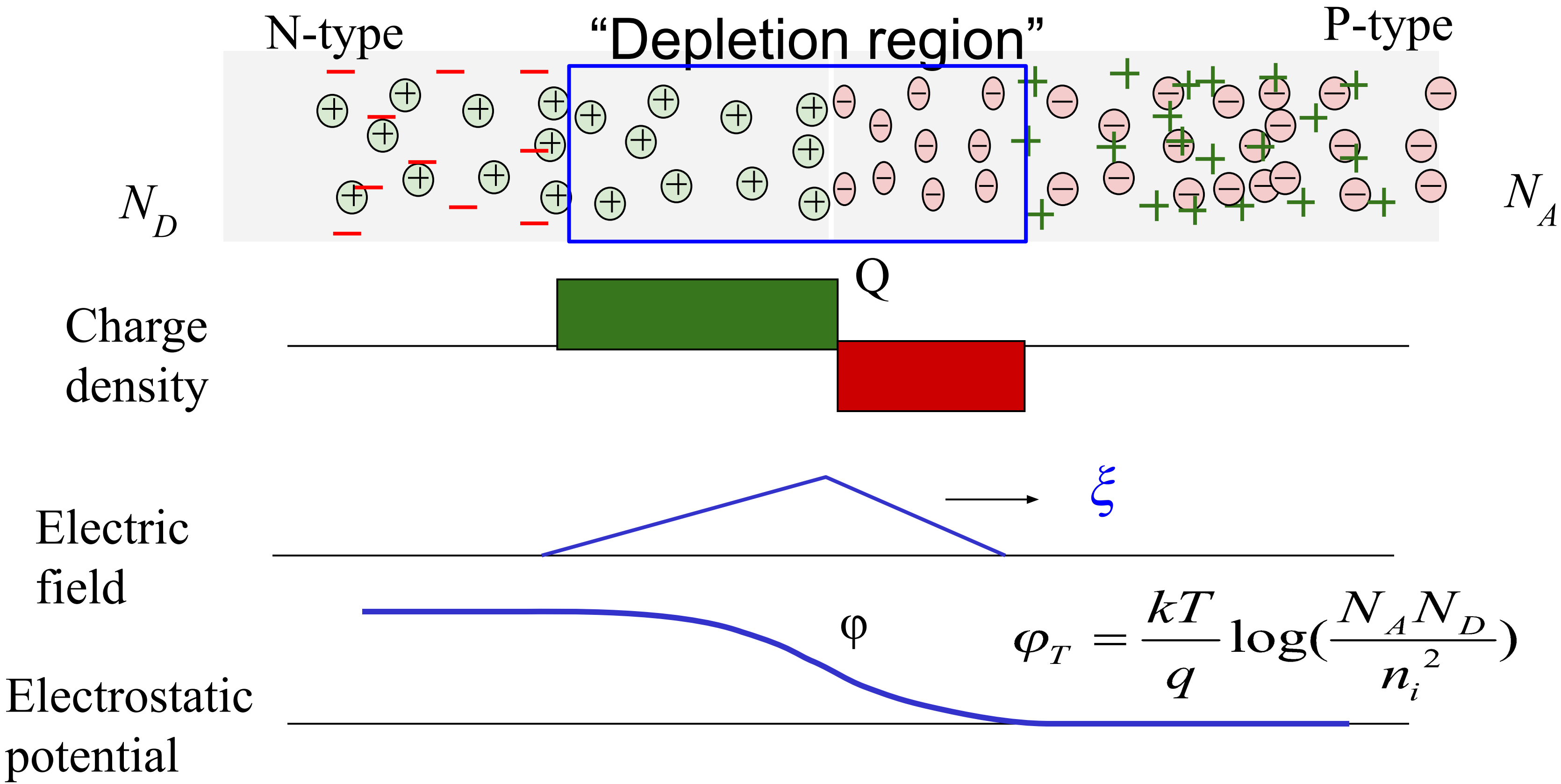
Electron density gradient:
Electrons diffuse rightwards

Hole density gradient:
Holes diffuse leftwards

The charge separation builds up an electric field to pull the carries “back home”

In a PN junction with no applied voltage, <u>drift and diffusion are balanced everywhere</u>

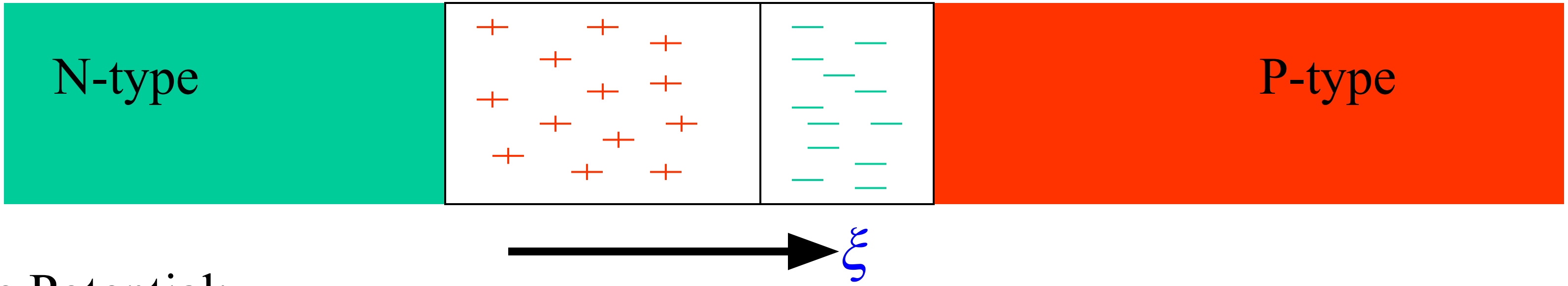
Charges, fields, and potentials in a PN junction



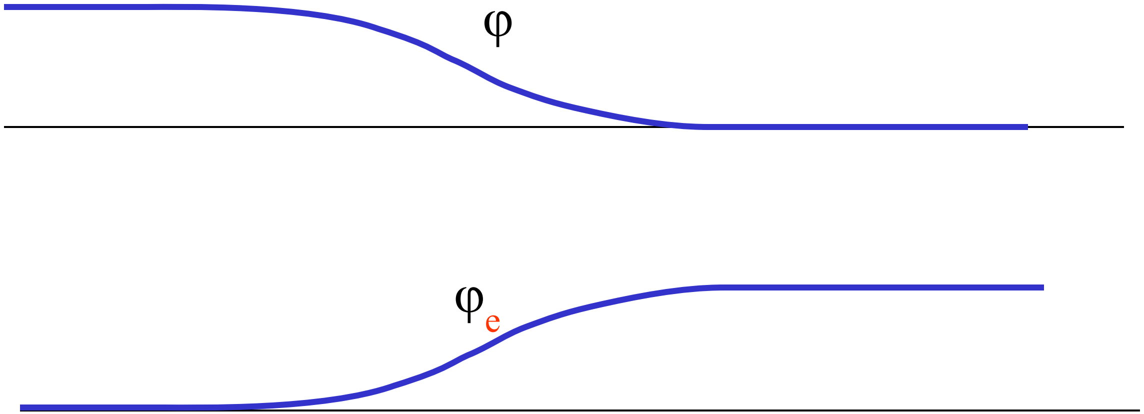
$$\varphi_T = \frac{kT}{q}\log\left(\frac{N_A N_D}{n_i^2}\right)$$

Typically, the *built-in voltage*, ϕ_T, is about 0.75V

Electrostatic potentials in a PN junction

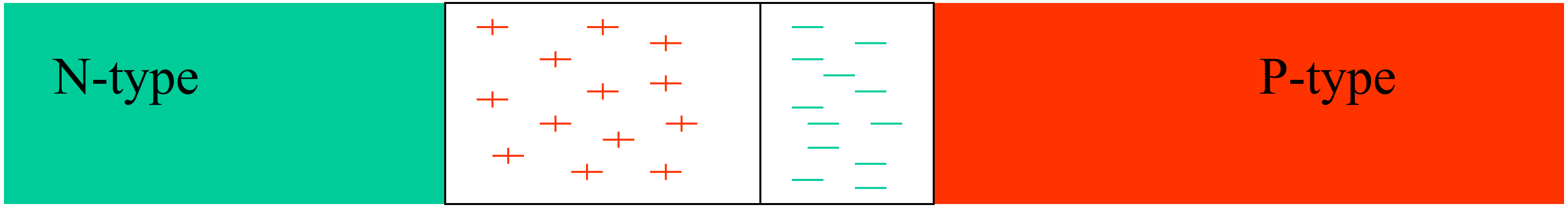


Electrostatic Potential: potential energy of positive charge

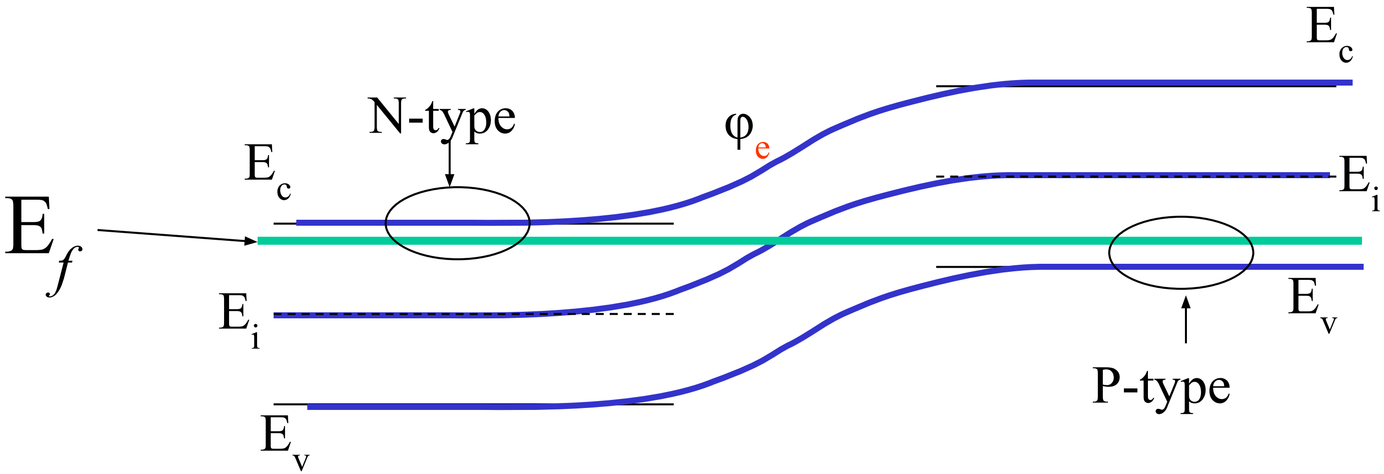


Potential energy of negatively charged electron

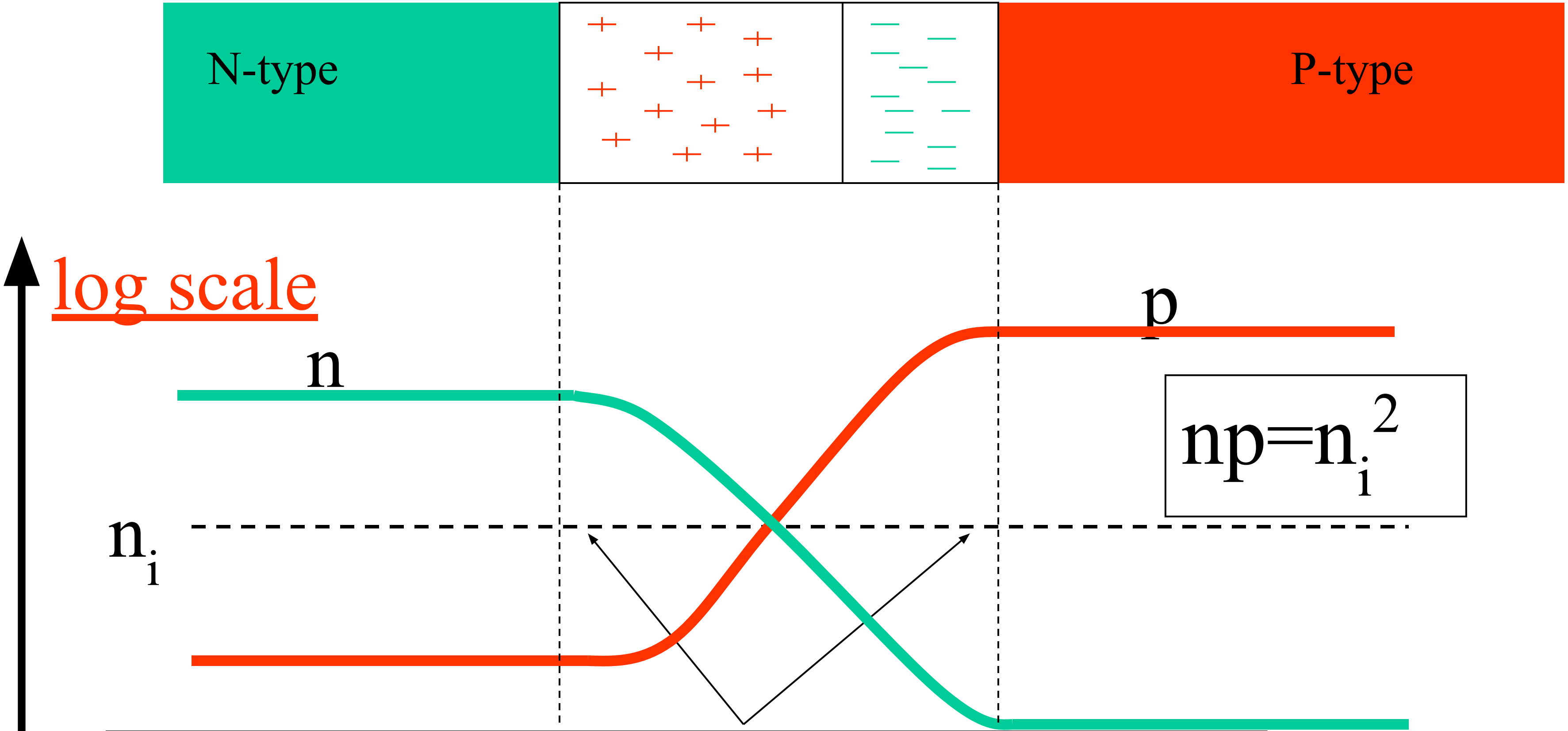
Band structure of a PN junction



Remember electron energy is UP in a band diagram

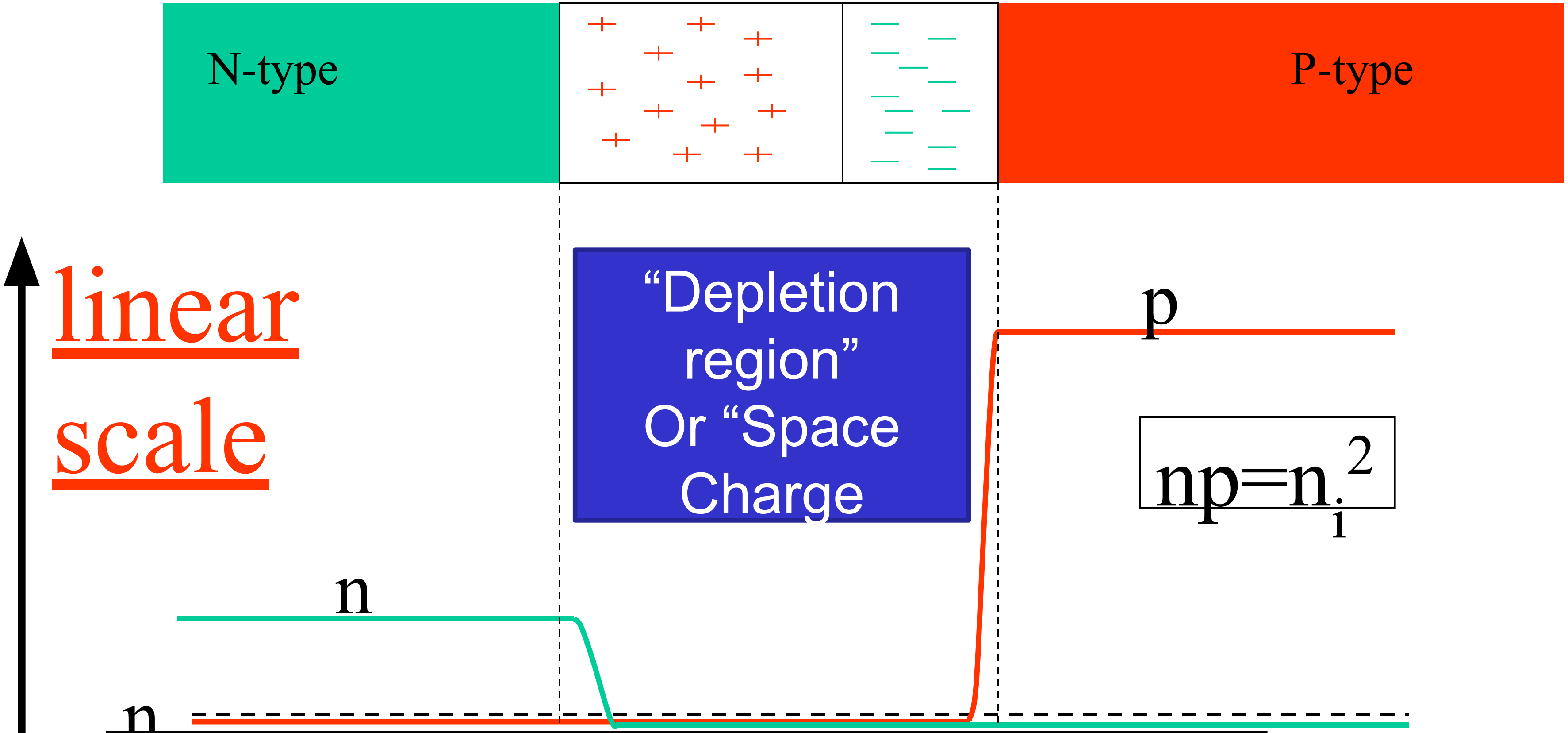


Carrier densities in a PN junction



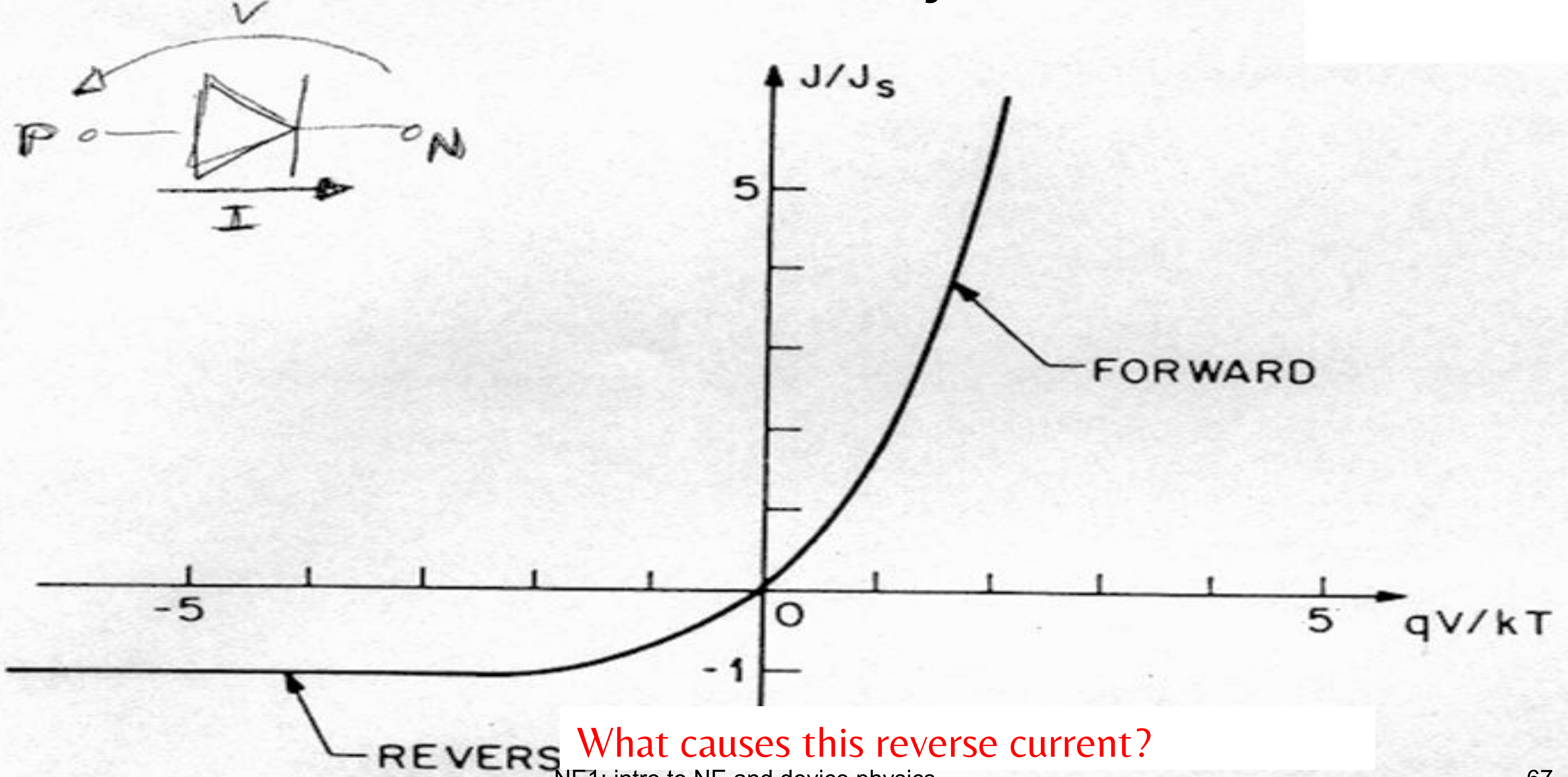
depletion region—both n and p are far below doping values

Carrier densities in a PN junction



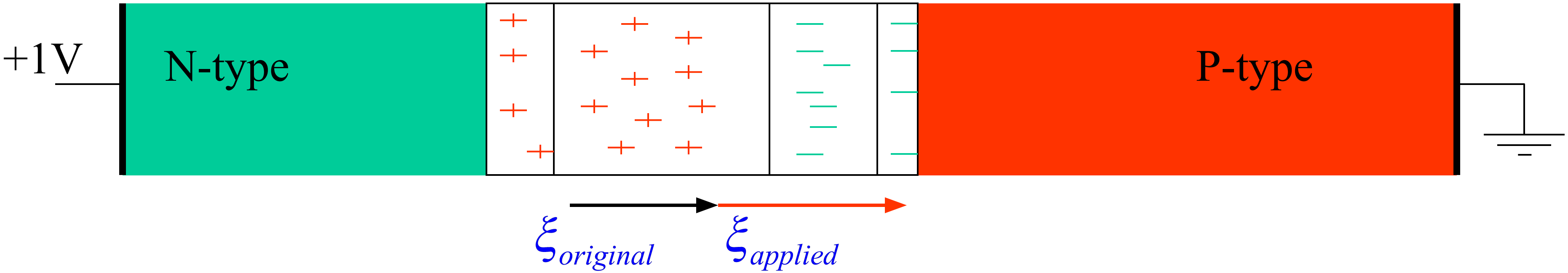
depletion region—both n and p are far below doping values

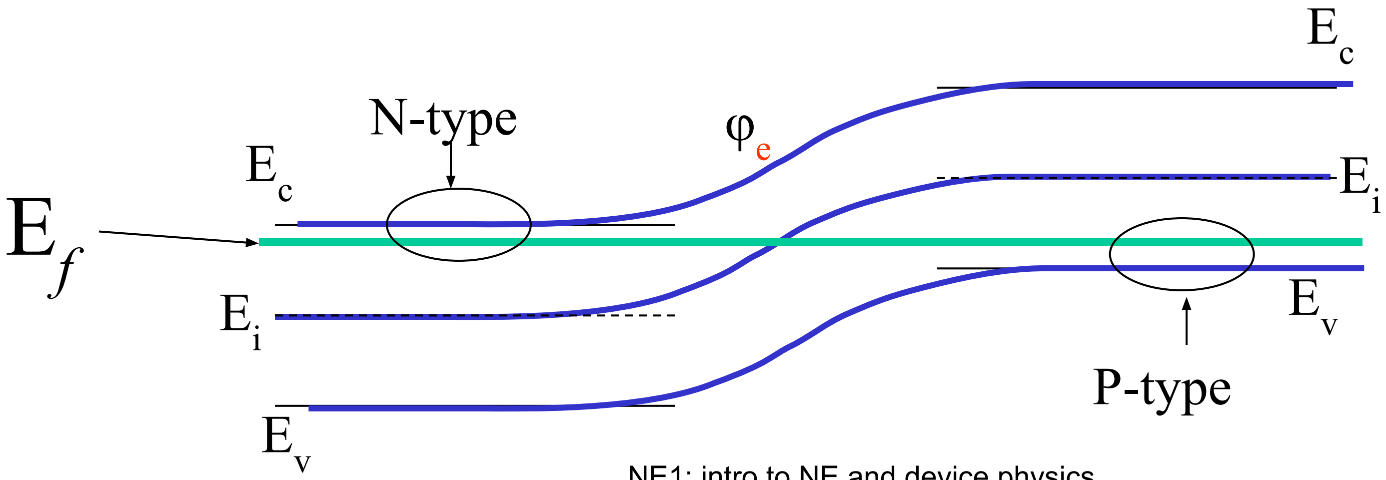
I-V characteristics of a PN junction "rectifier"



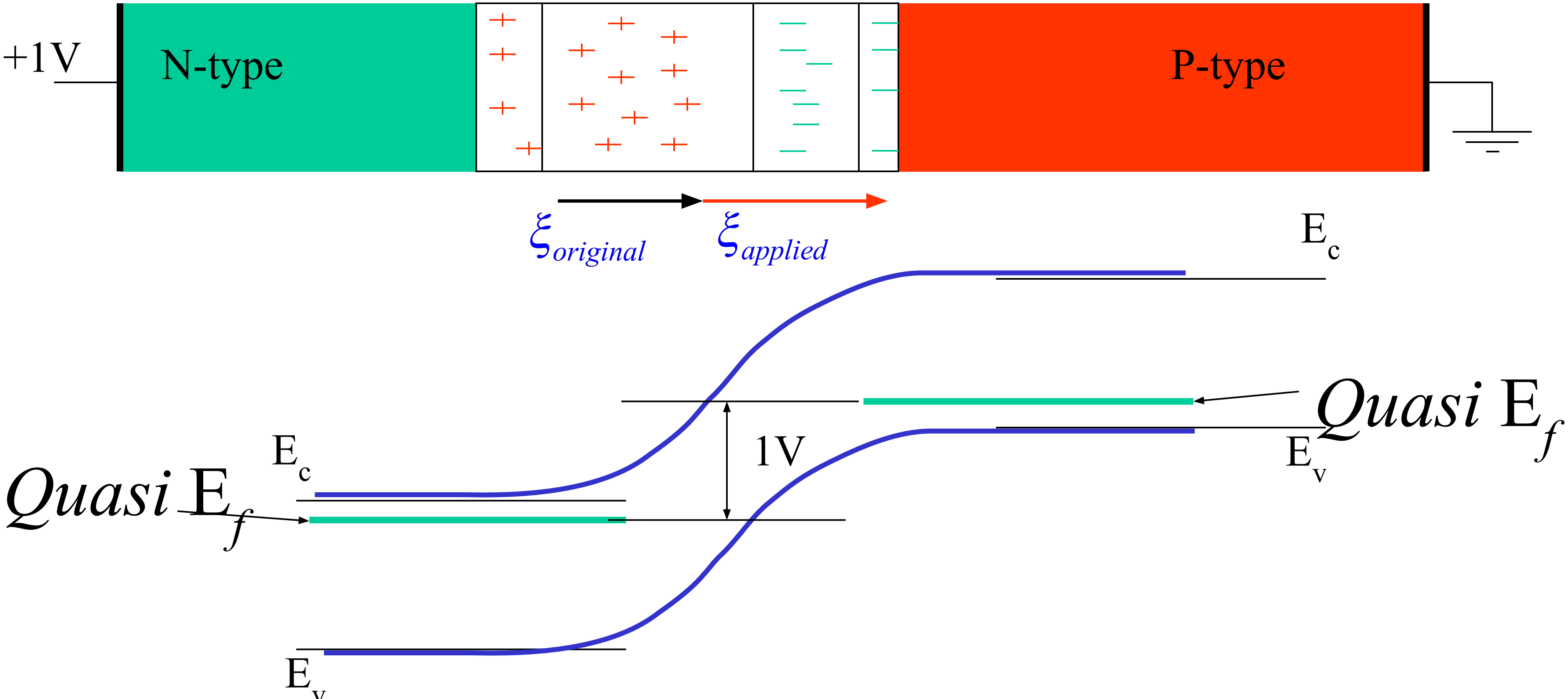
What causes this reverse current?

A reverse-biased PN junction

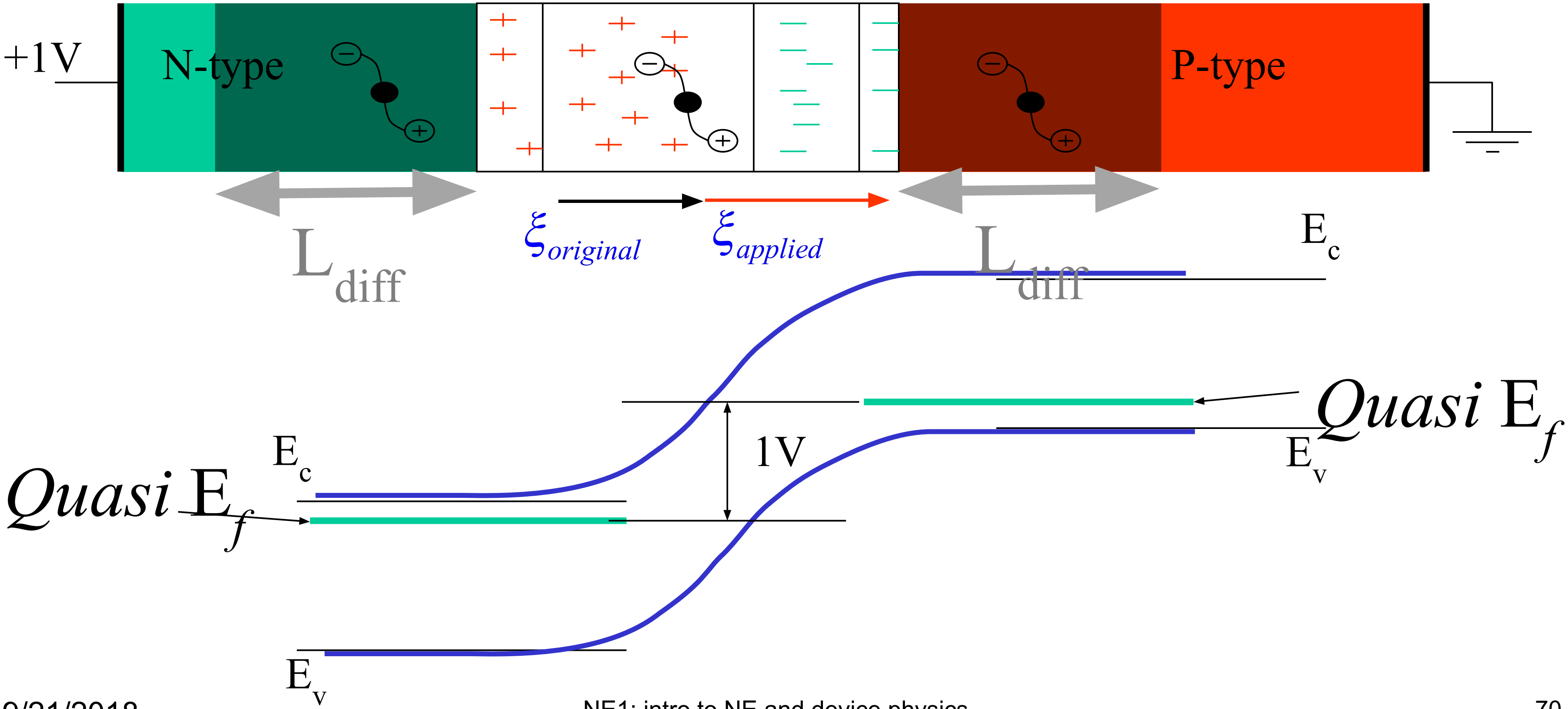




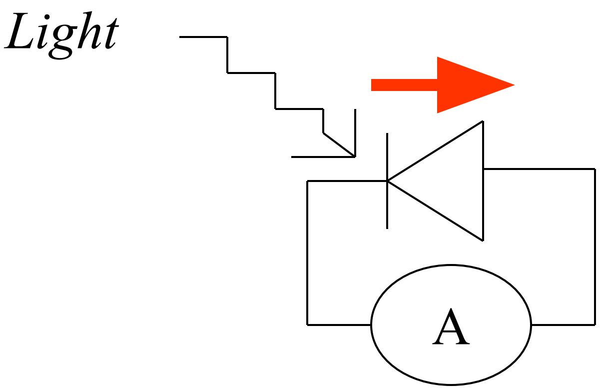
A reverse-biased PN junction



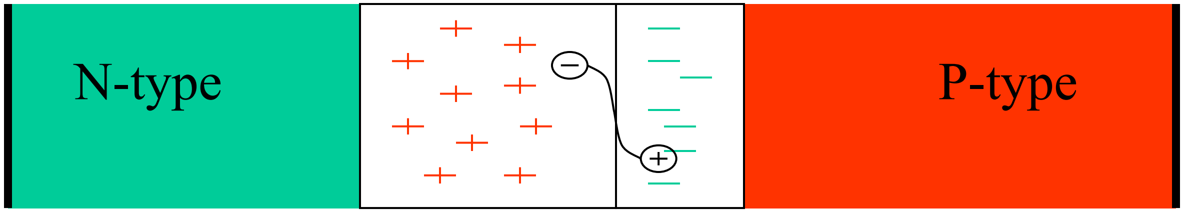
Reverse current comes from generated electron hole pairs in 3 regions



Question

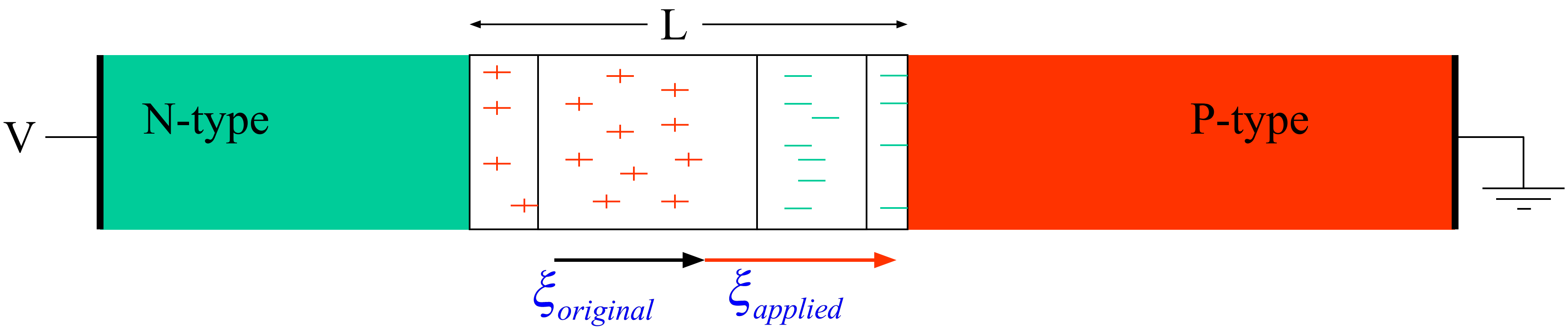


What happens when light shines on the junction?
Which way does current flow?



Answer: light tries to forward bias the junction.

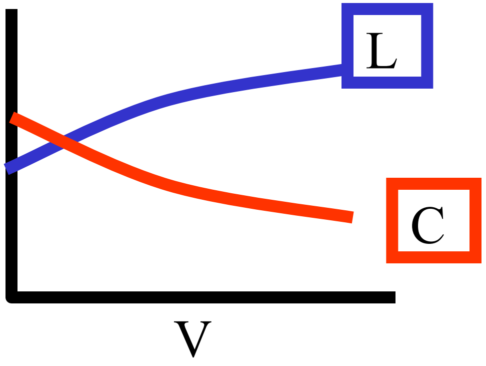
What is capacitance of reverse-biased PN junction?



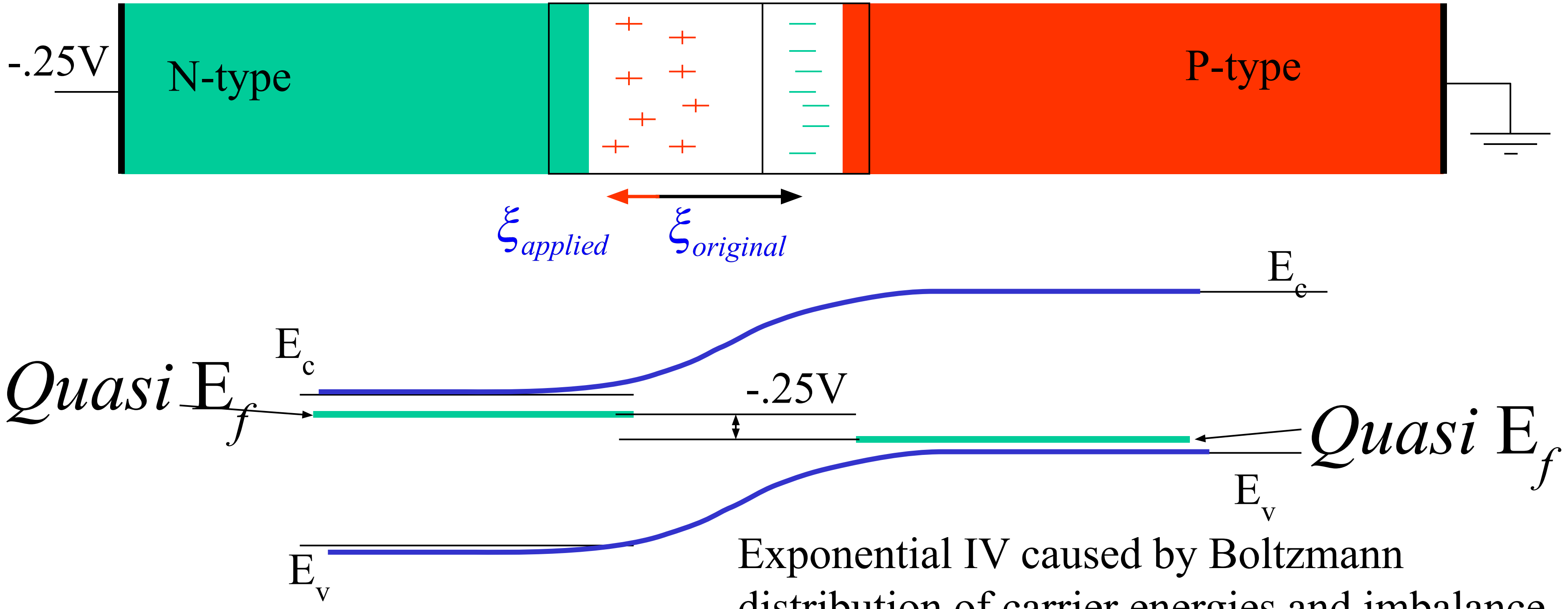
$C = \varepsilon_{Si}/L$

As V increases, L increases.

So, as V increases, C decreases



A forward-biased PN junction

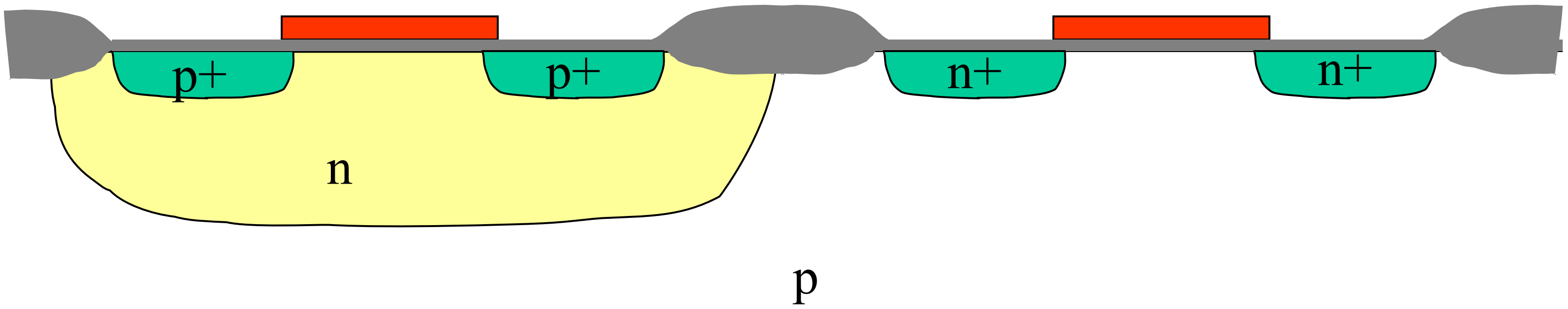


Exponential IV caused by Boltzmann distribution of carrier energies and imbalance of drift and diffusion currents

What was covered

- Insulators, conductors, semiconductors
- Crystal structure of silicon
- Band structure (valence, conduction, and forbidden bands)
- Holes and electrons
- Mechanisms of charge transport (diffusion & drift)
- Doping with donors and acceptors
- Fermi-Dirac distribution
- Law of mass action ($np=n_i^2$)
- p-n junction
- Reverse biased junction and its capacitance in reverse bias

Next week:
Understanding how MOS transistors work in the subthreshold/weak inversion regime



Properties of Materials (Si and SiO_2)

TABLE 4.1 IMPORTANT PROPERTIES OF GERMANIUM, SILICON, GALLIUM ARSENIDE, AND OF SILICON DIOXIDE AT 27°C.

	Ge	Si	GaAs	SiO_2
Atomic or molecular weight	72.60	28.09	144.63	60.08
Atoms or molecules/cm^3	4.42×10^{22}	5.00×10^{22}	2.21×10^{22}	2.3×10^{22}
Crystal structure	Diamond, 8 atoms/unit cell	Diamond, 8 atoms/unit cell	Zinc-blende, 8 atoms/unit cell	Random network of SiO_4 tetrahedra. 50% covalent, 50% ionic bonding
Lattice constant (Å)	5.66	5.43	5.65	. . .
Density, ρ (g/cm^3)	5.32	2.33	5.32	2.27
Energy gap (ev)	0.67	1.11	1.40	~8
Effective density of states conduction band N_c (cm^{-3}) valence band N_v (cm^{-3})	1.04×10^{19} 6.0×10^{18}	2.8×10^{19} 1.04×10^{19}	4.7×10^{17} 7.0×10^{18}	. . .
Intrinsic carrier concentration n_i (cm^{-3})	2.4×10^{13}	1.45×10^{10}	$\sim 9 \times 10^{6}$	. . .
Lattice (intrinsic) mobilities (cm^2/v sec) electrons holes	3900 1900	1350 480	8600 250	Insulator; $\rho > 10^{16}$ Ω-cm at 300°K.
Dielectric constant	16.3	11.7	12	3.9
Breakdown field (v/μ)	~8	~30	~35	~600
Melting point (°C)	937	1415	1238	~1700

A forward-biased PN junction