Current-mode Winner-take-all circuits

Neuromorphic Engineering I

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Outline

Current-mode circuits

Historically, analog design has been viewed as a voltage dominated form of signal processing.

With the advent of (Bi)CMOS technology, shrinking feature size, and reduction of supply voltage a new class of circuits has been developed: current-mode circuits, in which input, output signals, and state variables are represented by currents.

Examples of classical current-mode circuits include:

- translinear circuits
- current conveyors
- dynamic current mirrors
- switched current integrators
- current-feedback amplifiers

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Translinear circuits

The term translinear was coined by Barry Gilbert in 1975.
In *translinear* circuits transistors have a *trans*conductance which is *linear*ly proportional to the output current.
This applies to:

- Circuits using monolithic BJTs
- Circuits using subthreshold MOS FETs in saturation

For subthreshold MOSFETs in saturation:

$$I_{DS} = I_0 e^{(\kappa V_G - V_S)/U_T}$$

$$g_m \doteq \frac{d}{dV_G} I_{DS} = \frac{\kappa}{U_T} I_{DS}$$

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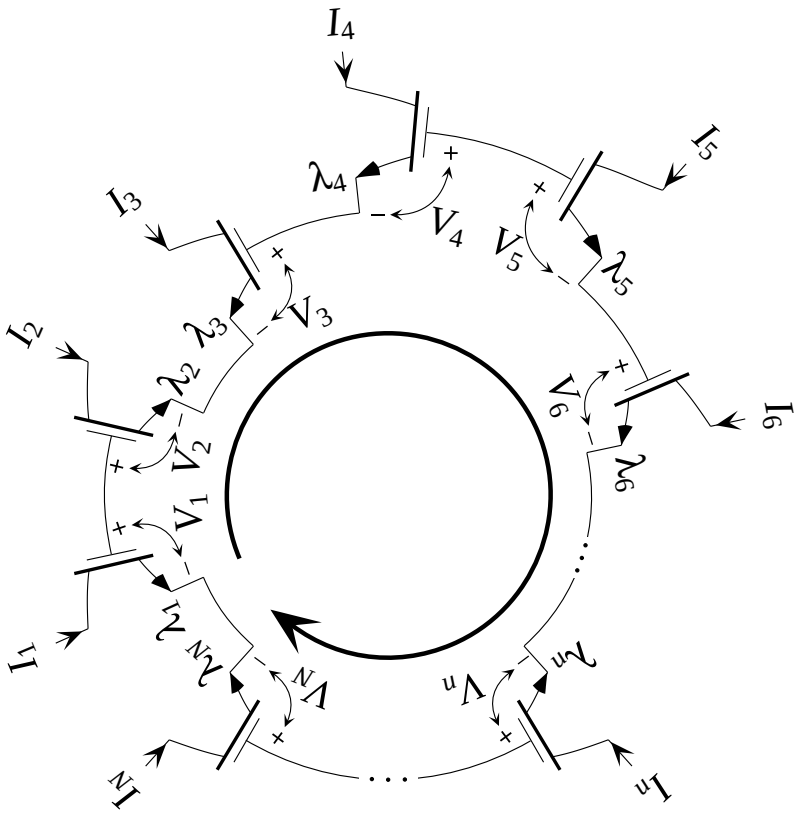
The translinear principle

Many current-mode circuits comprise transistors arranged in one or more *closed loops of junctions*.



In a closed loop containing an even number of forward-biased junctions arranged so that there are an equal number of clockwise-facing and counter clock-wise facing polarities, the product of the current densities in the clockwise direction is equal to the product o the current densities in the counter clock-wise direction.

The translinear principle

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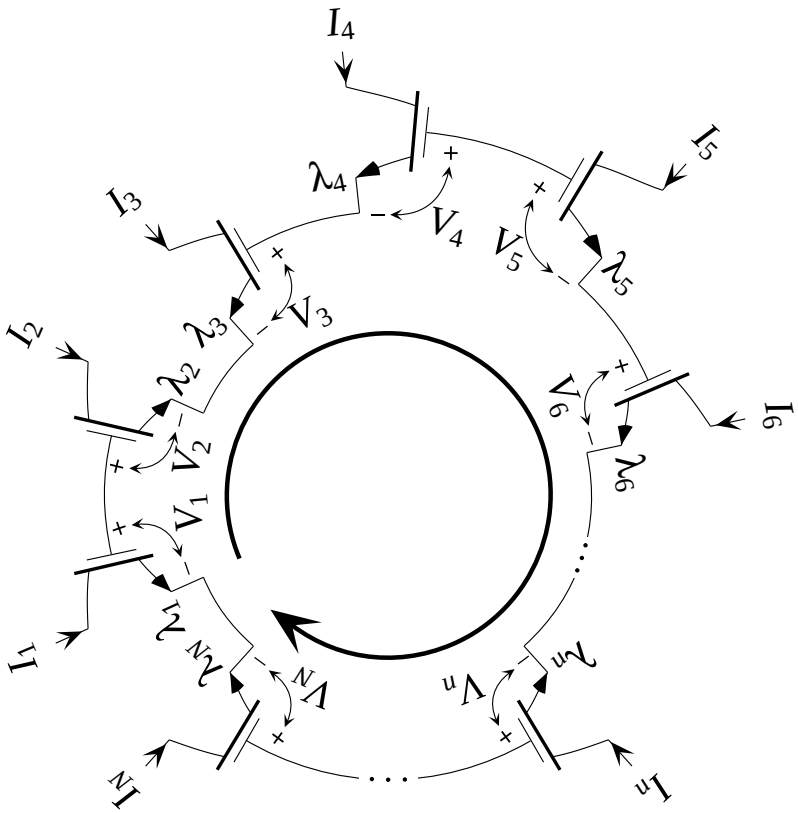


$$\sum_{k=1}^{N} V_{F_K} = 0$$

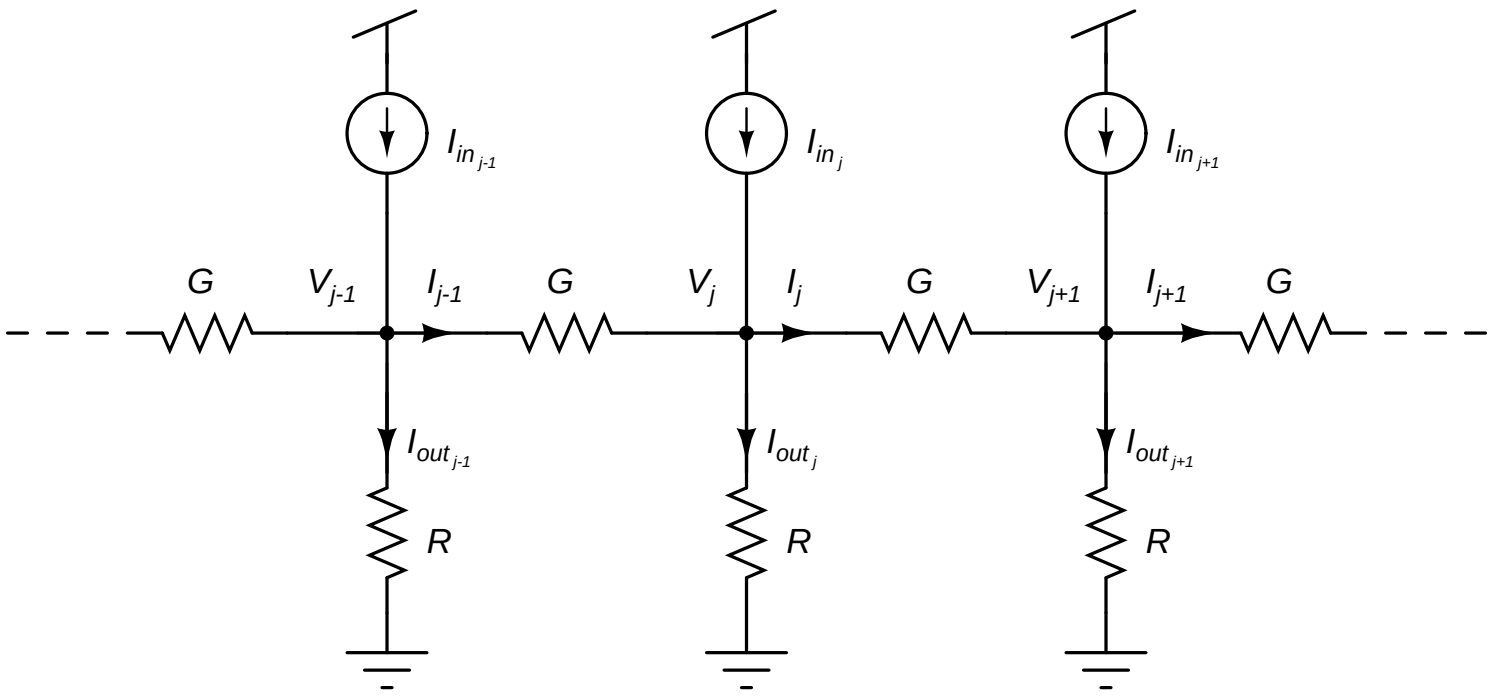
If the elements are saturated MOS subthreshold transistors (with $\kappa = 1$ for sake of clarity)

$$\sum_{k=1}^{N} U_T ln\left(\frac{I_{DS,k}}{I_0}\right) = 0$$

$$\Rightarrow \prod_{k=1}^{N} \frac{I_{DS,k}}{I_0} = 1$$

Outline

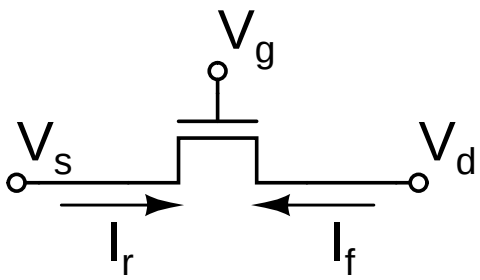
Resistive networks

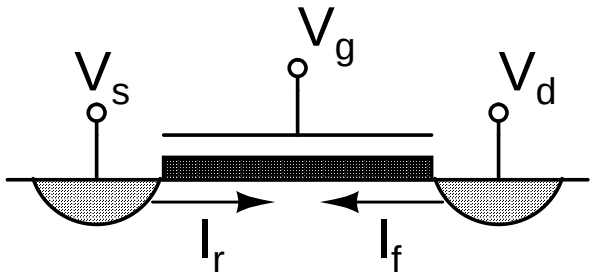


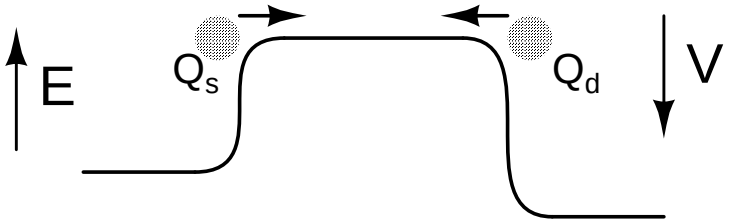
Resistors can be implemented in VLSI using single MOSFETs (but with very small dynamic range) or more complex circuits (such as the transconductance amplifier). But if we consider currents, and not voltages, to represent input and output signals of MOSFETs, then we can implement wide dynamic range resistive networks using single transistors instead of resistors.

Diffusor and pseudo-conductances

(K. Boahen and E. Vittoz, late nineties)







A conventional conductance G is defined by the relationship

$$I_{ds} = G\,(V_s - V_d)$$

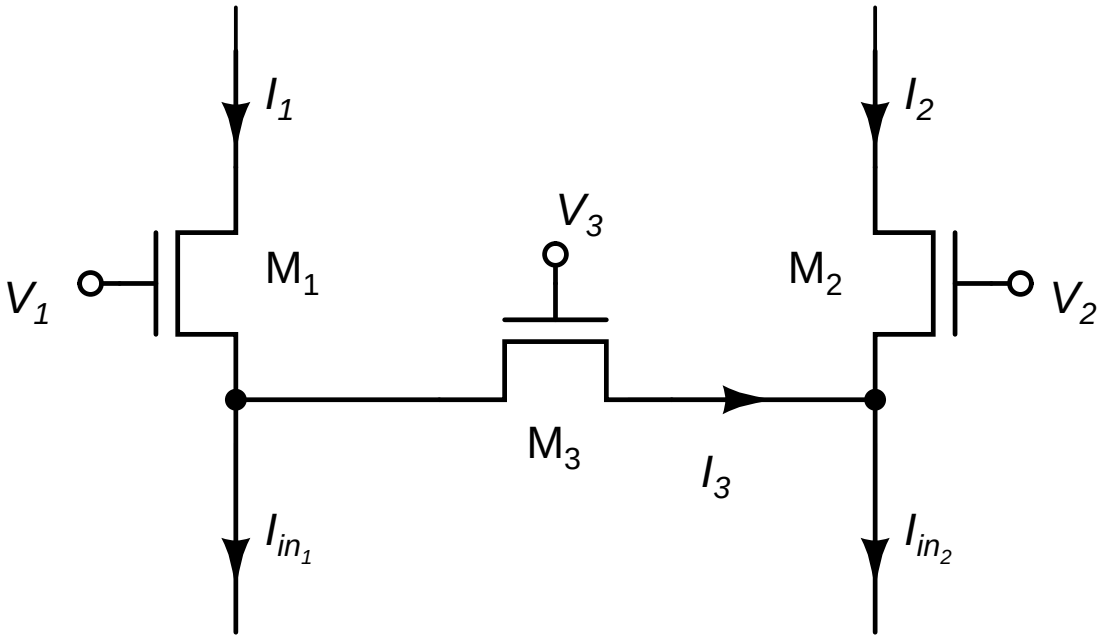
If we define $V^* \doteq V_0\, e^{-\frac{V}{U_T}}$ as a *pseudo-voltage* and $G^* \doteq \frac{I_0}{V_0}\, e^{\kappa \frac{V_g}{U_T}}$ as a *pseudo-conductance*, then

$$I_{ds} = G^*\,(V_s^* - V_d^*)$$

But this is equivalent to:

$$I_{ds} = I_0\, e^{\kappa \frac{V_g}{U_T} - \frac{V_s}{U_T}} - I_0\, e^{\kappa \frac{V_g}{U_T} - \frac{V_d}{U_T}}$$

Current divider



Inputs I_{in_1} and I_{in_2}

Outputs I_1 and I_2

Reference $V_1 = V_2 = V_{ref}$

$$I_3 = I_0 e^{\kappa \frac{V_3}{U_T}} \left(\frac{I_2}{I_0 e^{\kappa \frac{V_2}{U_T}}} - \frac{I_1}{I_0 e^{\kappa \frac{V_1}{U_T}}} \right)$$

$$\boxed{I_3 = e^{\frac{\kappa}{U_T}(V_3 - V_{ref})} (I_2 - I_1)}$$

The diffusion current I_3 through M_3 is proportional to $(I_2 - I_1)$. The proportionality factor can be modulated by V_{ref} and V_3.

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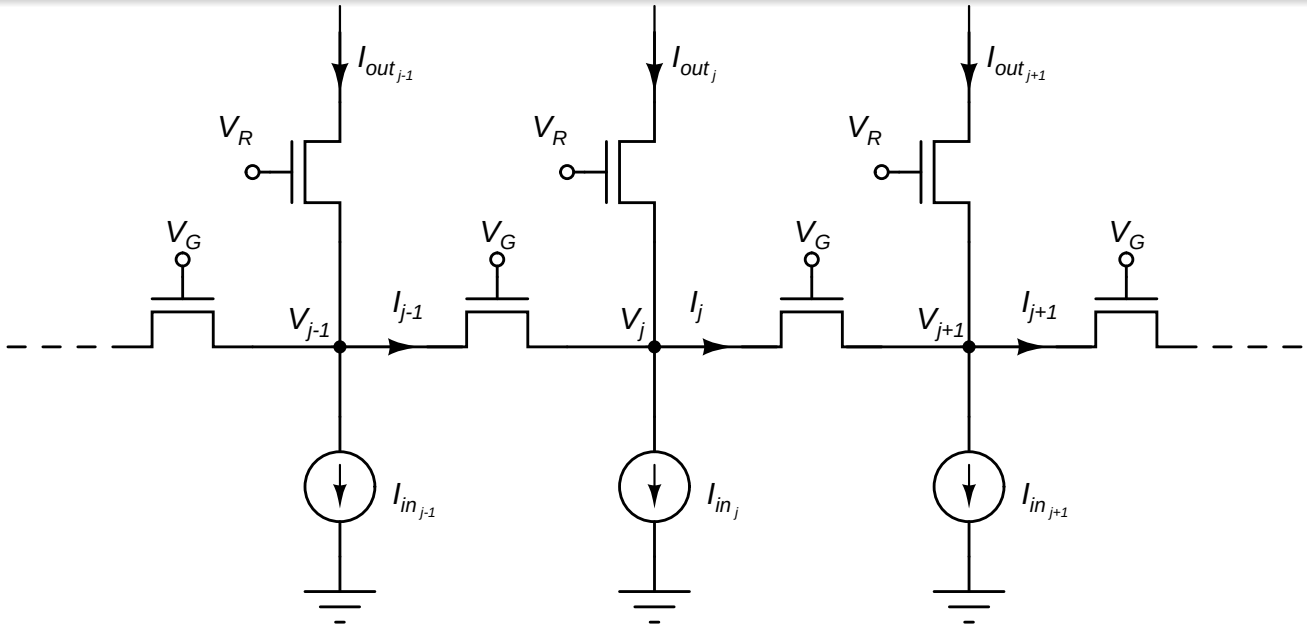
Diffusor and resistive networks

Diffusion equation

$$\lambda^2 \frac{d^2}{dx^2} V_{out}(x) = V_{out}(x) - V_{in}(x)$$



$$e^{\frac{\kappa}{U_T}(V_G - V_R)}(I_{out_{j+1}} - 2I_{out_j} + I_{out_{j-1}}) = I_{out_j} - I_{in_j}$$

$$\lambda = e^{\frac{\kappa}{2U_T}(V_G - V_R)}$$

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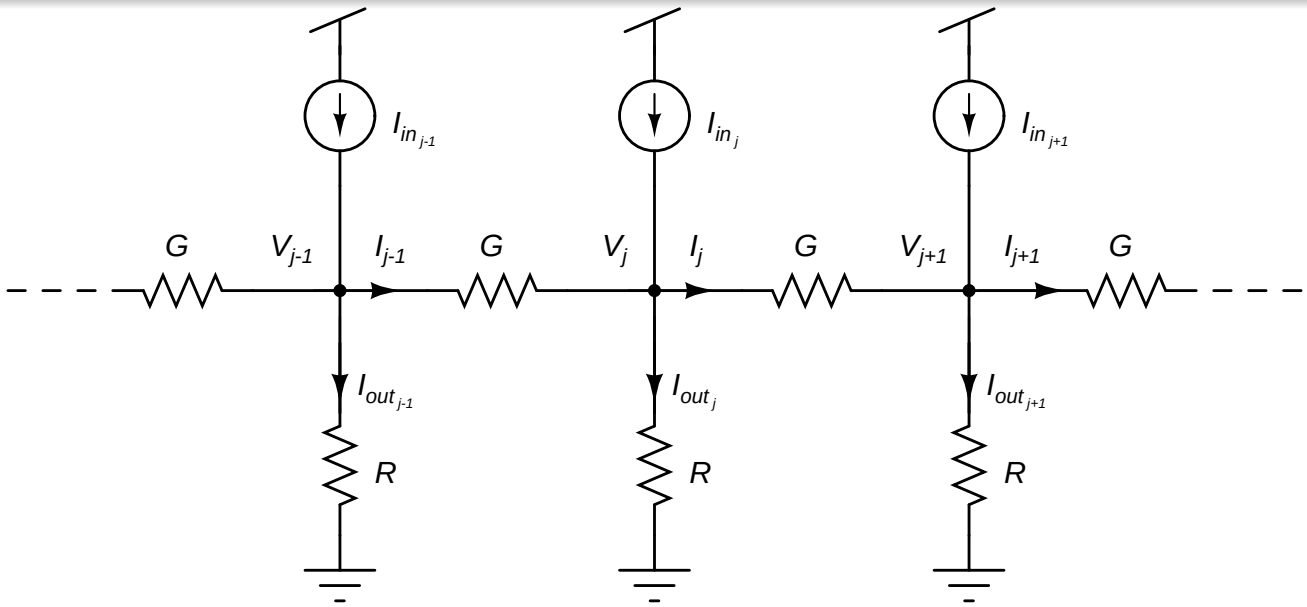


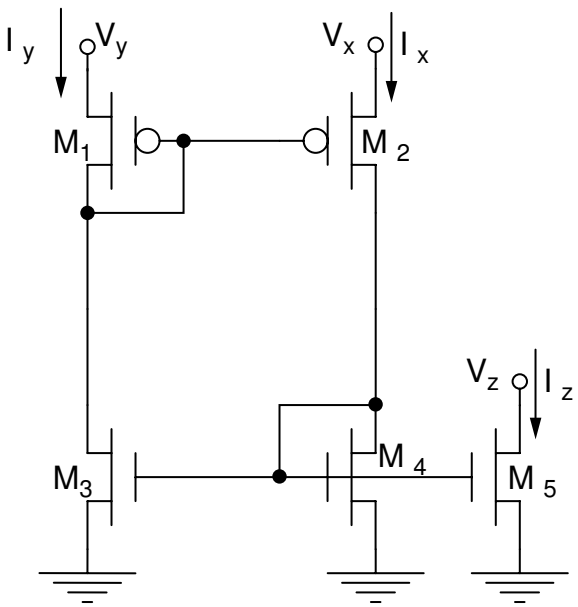
$$\frac{1}{RG}(I_{out_{j+1}} - 2I_{out_j} + I_{out_{j-1}}) = I_{out_j} - I_{in_j}$$

$\lambda = 1/\sqrt{RG}$

Outline

Current conveyor

Currents are conveyed from the input terminal (X or Y) to the output terminal (Z), while decoupling the circuits connected to these terminals.

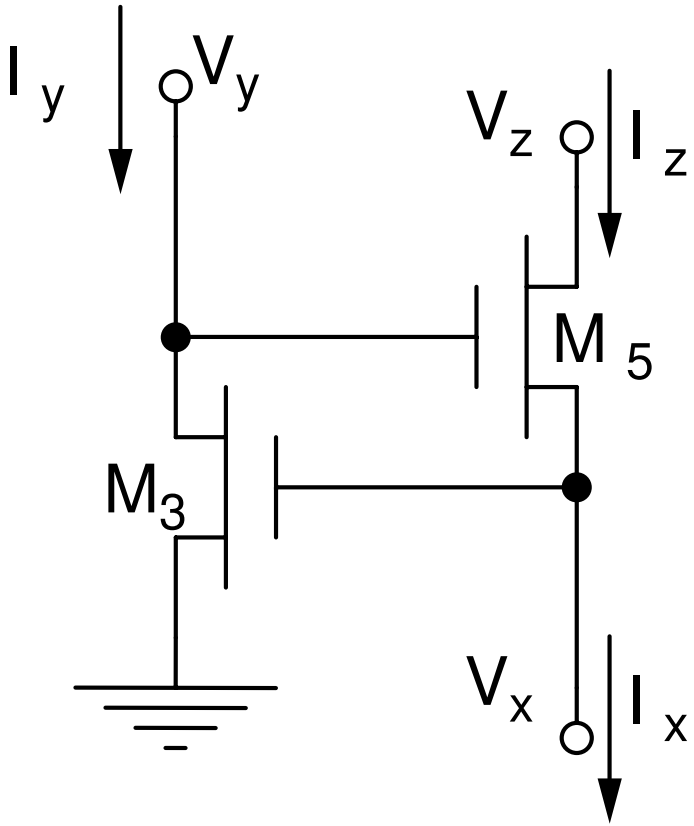


A crucial computational building block used to add, subtract, amplify, attenuate, and filter signals in the current-mode domain, analogous to the op-amp in voltage-mode (Smith and Sedra, 1968).

1. The potential at the output terminal (Z) is independent of the current applied at the node Y.
2. An input current that is forced into node X results in an equal amount of current flowing into node Y.
3. The input current flowing into node X is conveyed to node Z, which has the characteristics of a high output impedance current source.

Subthreshold current conveyor

Exploits subthreshold MOSFETs exponential characteristic.

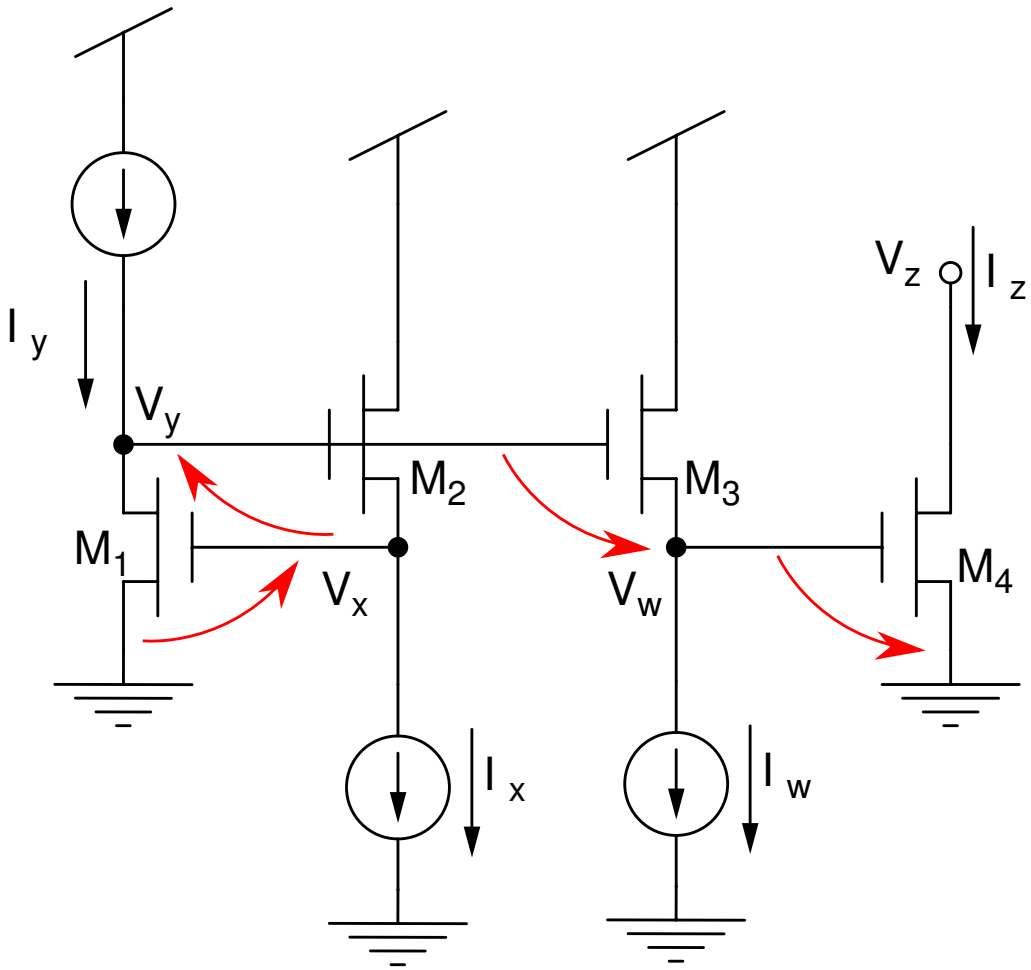


$$I_z = I_x$$
$$V_x \propto ln(I_y)$$

Used in

- Low-pass filters
- Multiplier circuits
- Winner take all circuits
- Silicon neurons
- Current-mode silicon retinas

Current conveyor as a multiplier



Exploits the translinear principle:

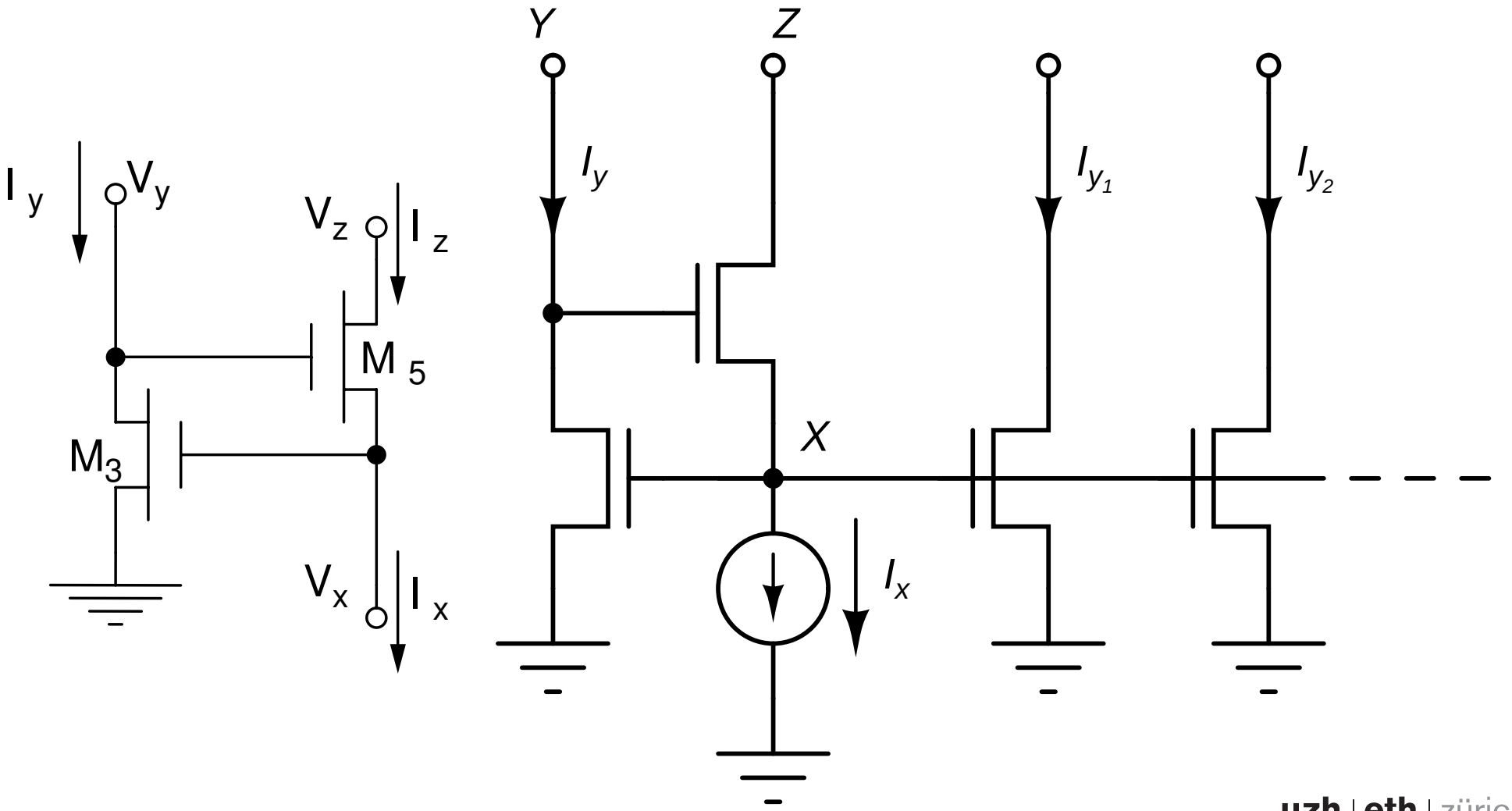
$$V_x + (V_y - V_x) + (V_w - V_y) + (0 - V_w) = 0$$

$$I_x \cdot I_y \cdot I_w^{-1} \cdot I_z^{-1} = 1$$

$$\Rightarrow I_z = \frac{I_x I_y}{I_w}$$

Current conveyor as a current mirror

As voltages at nodes Y and X are decoupled from each other, X can be clamped to a desired constant by choosing appropriate values of I_y.



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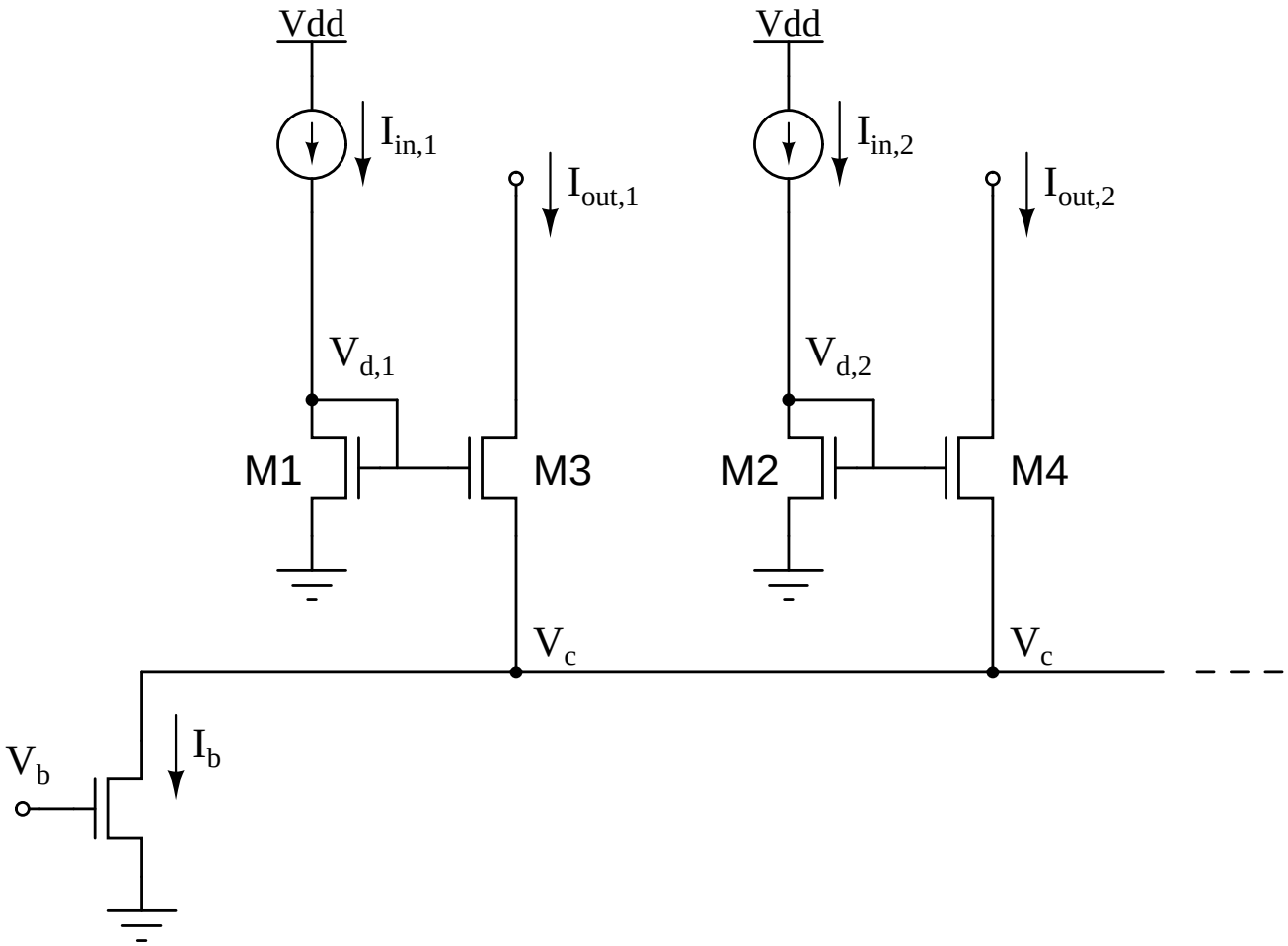
Outline

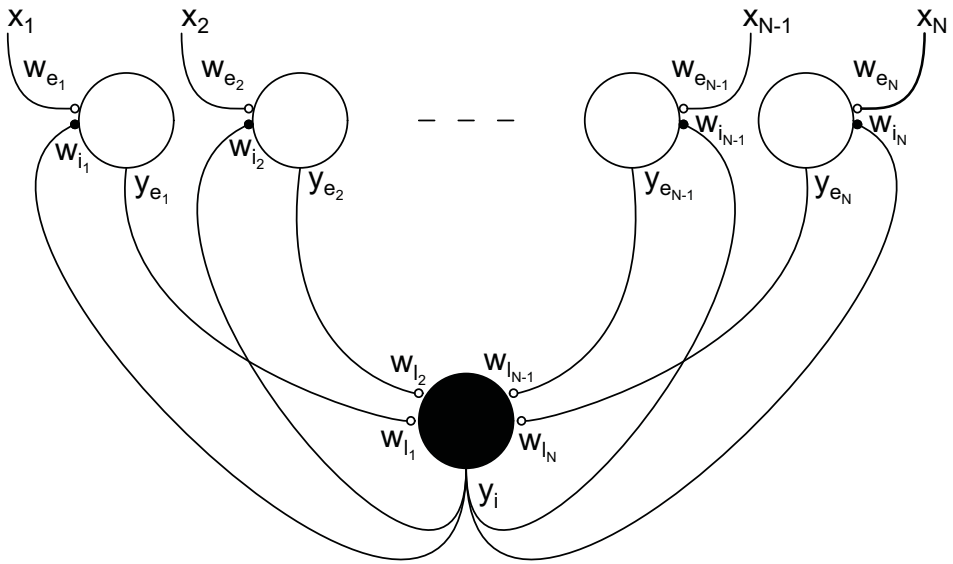
Gilbert normalizer



$$
\begin{aligned}
I_{in,i} &= I_0 e^{\kappa \frac{V_{d,i}}{U_T}} \\
I_{out,i} &= I_0 e^{\kappa \frac{V_{d,i}}{U_T} - \frac{V_c}{U_T}} \\
&= I_{in,i} e^{-\frac{V_c}{U_T}} \\
I_b &= \sum_j I_{out,j} \\
&\Downarrow \\
I_{out,i} &= I_b \frac{I_{in,i}}{\sum_j I_{in,j}}
\end{aligned}
$$

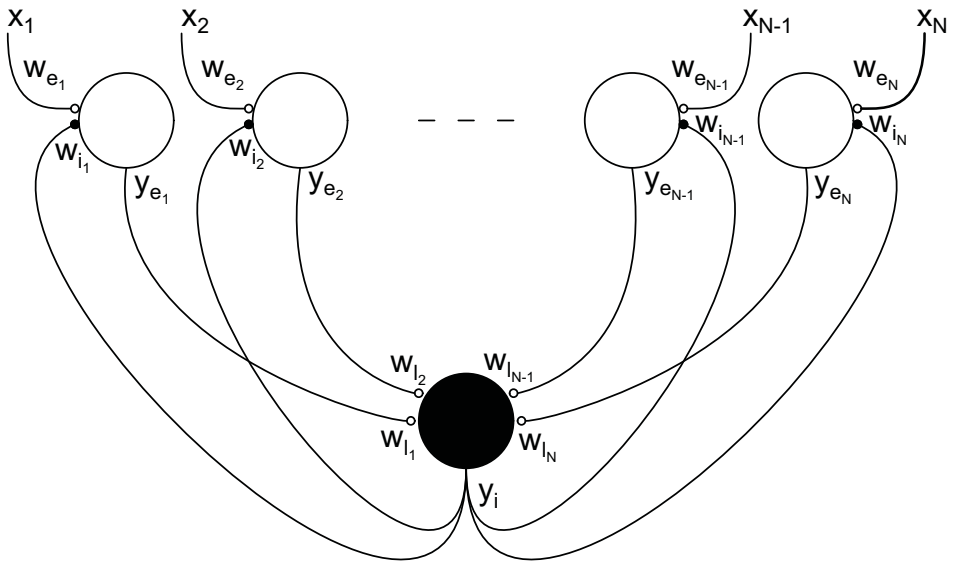
Outline

WTA networks



- Networks of competing cells (neural, software, or hardware) that report the response of the cell with the strongest activation while suppressing the responses of all other cells.
- Typically used to implement and model competitive mechanisms among populations of neurons.
- Vast literature dating to the 70s for theoretical models, software algorithms, and analog VLSI implementations.

WTA networks



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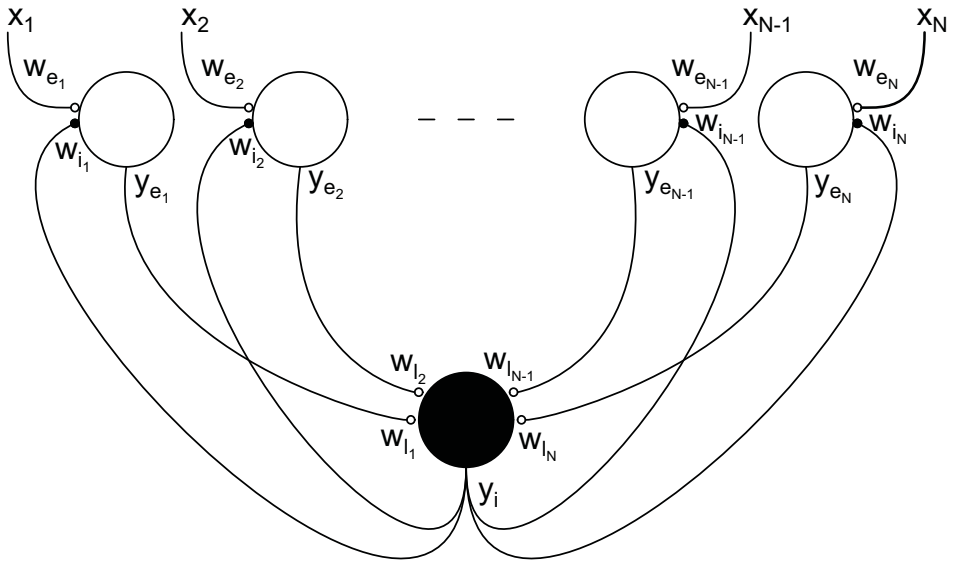

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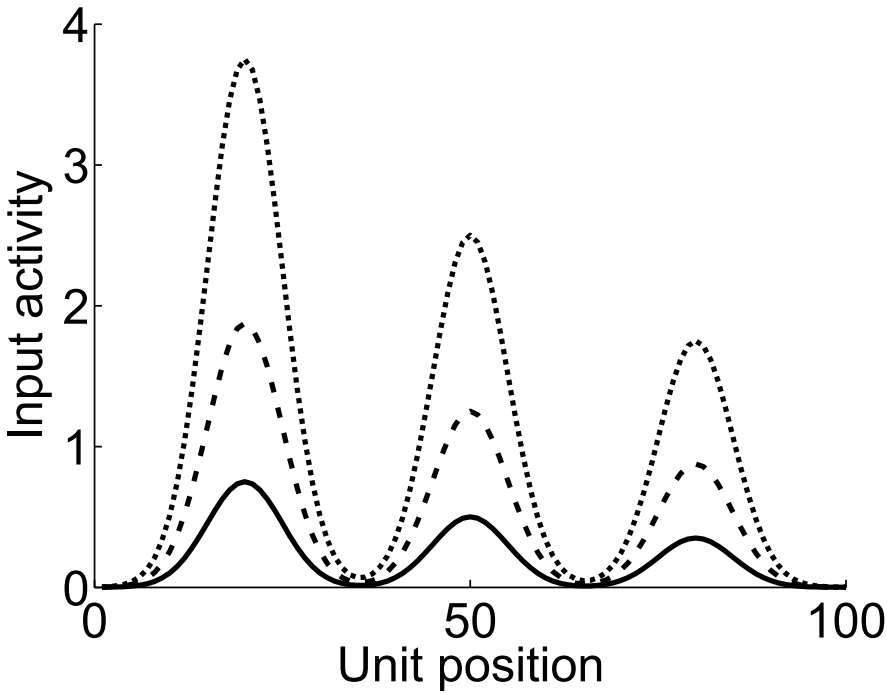
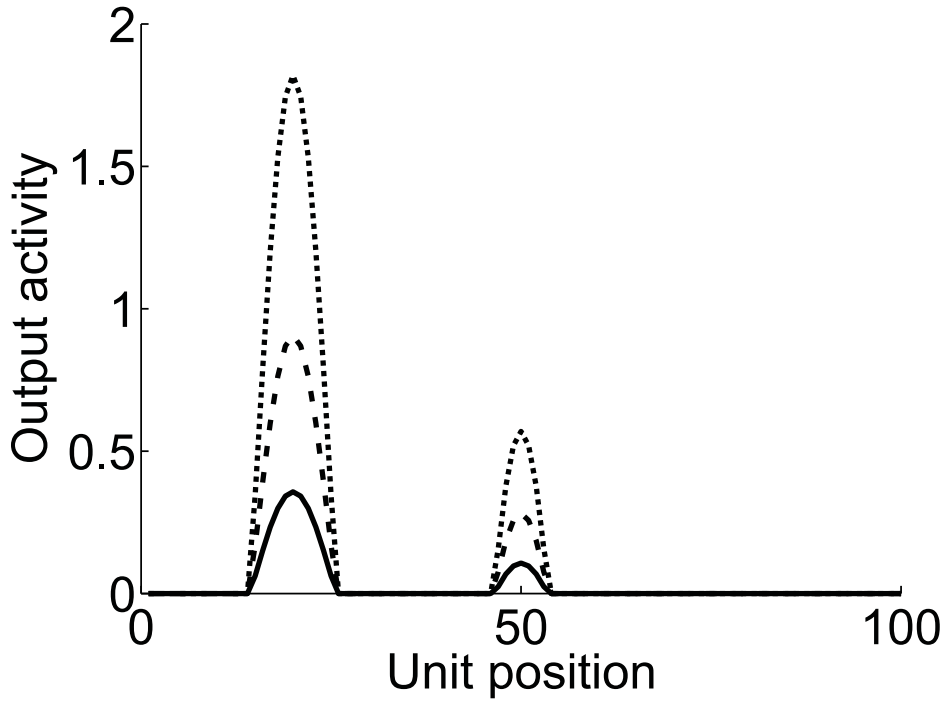
Software simulations





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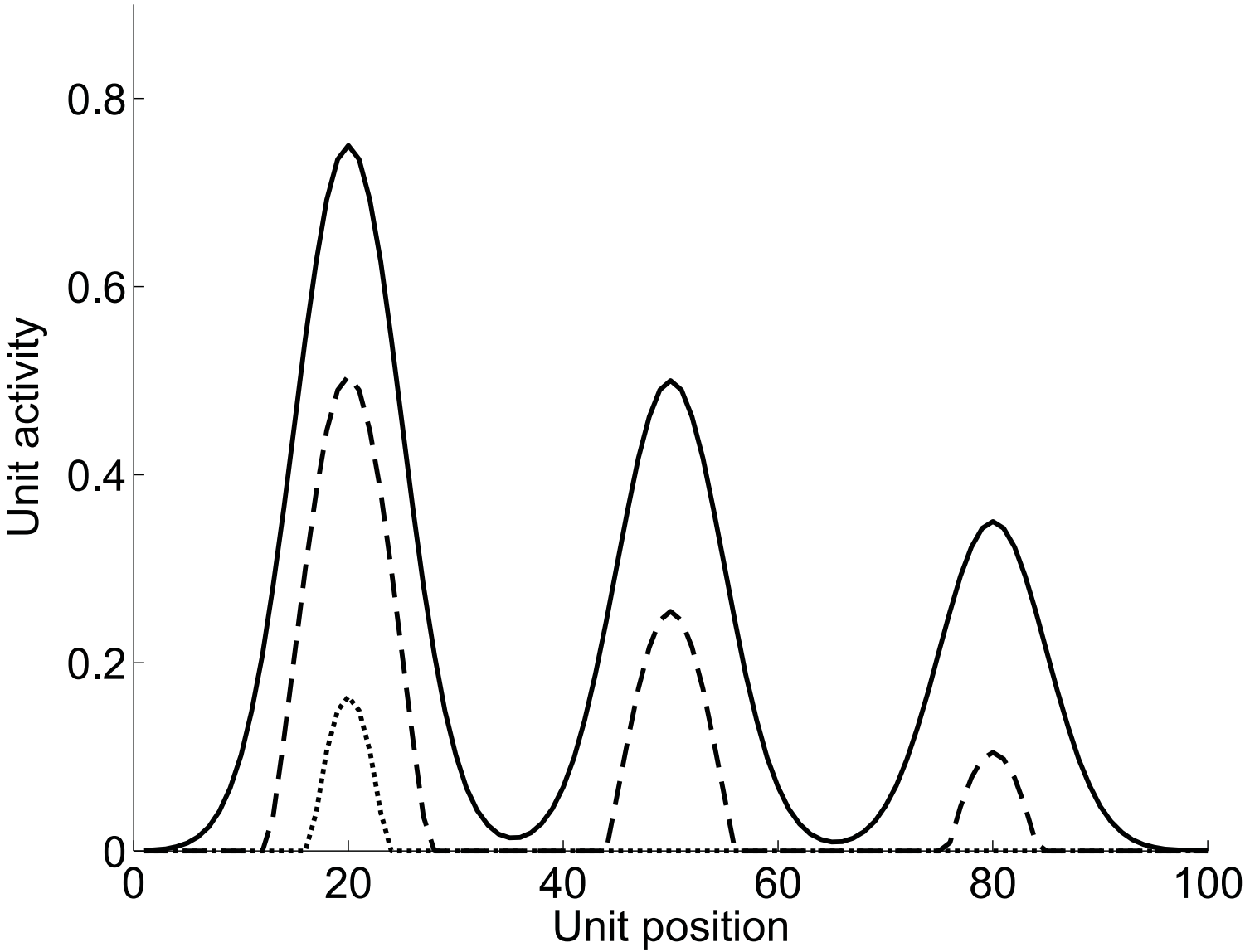

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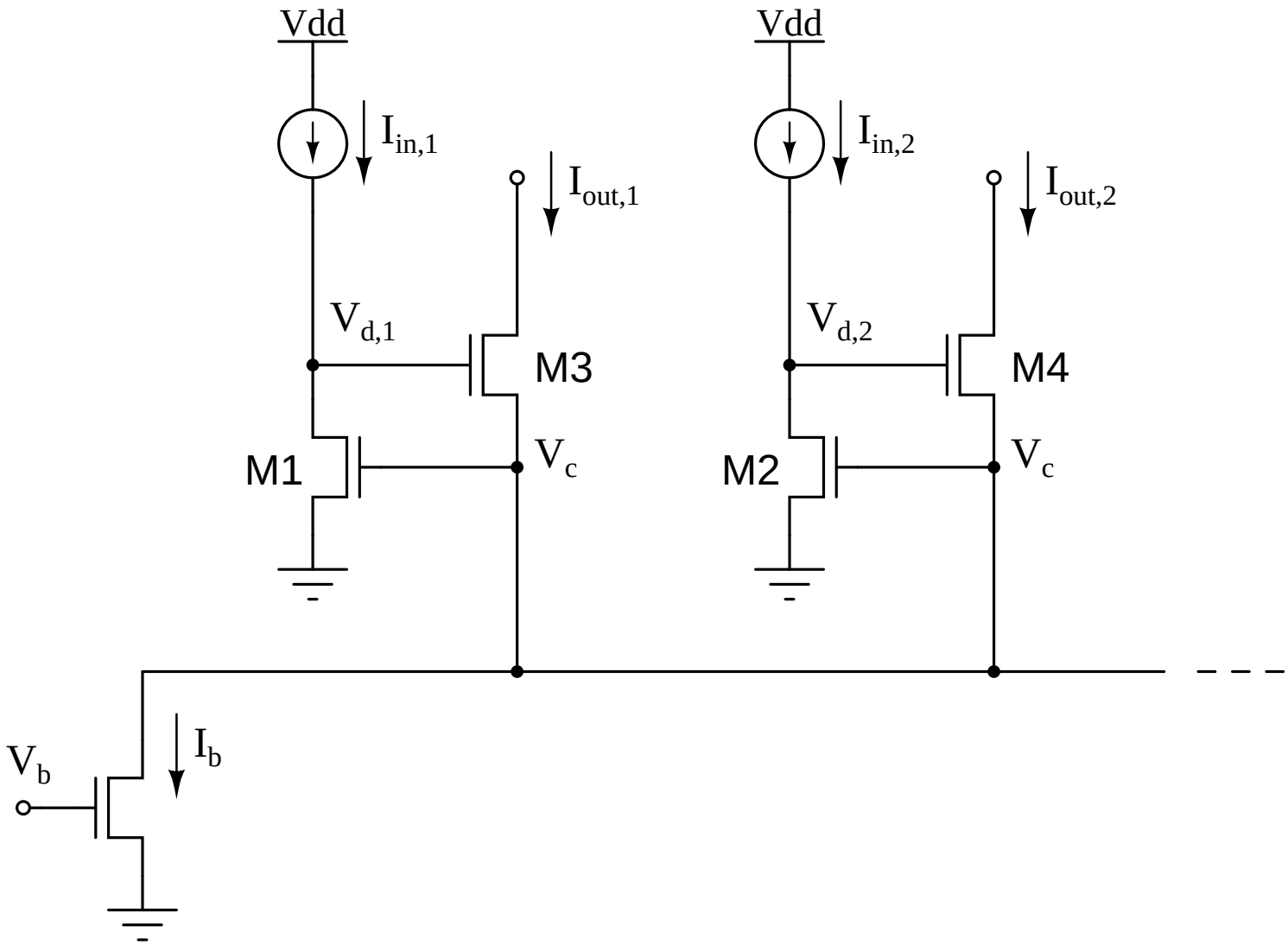
Current-mode WTA circuit



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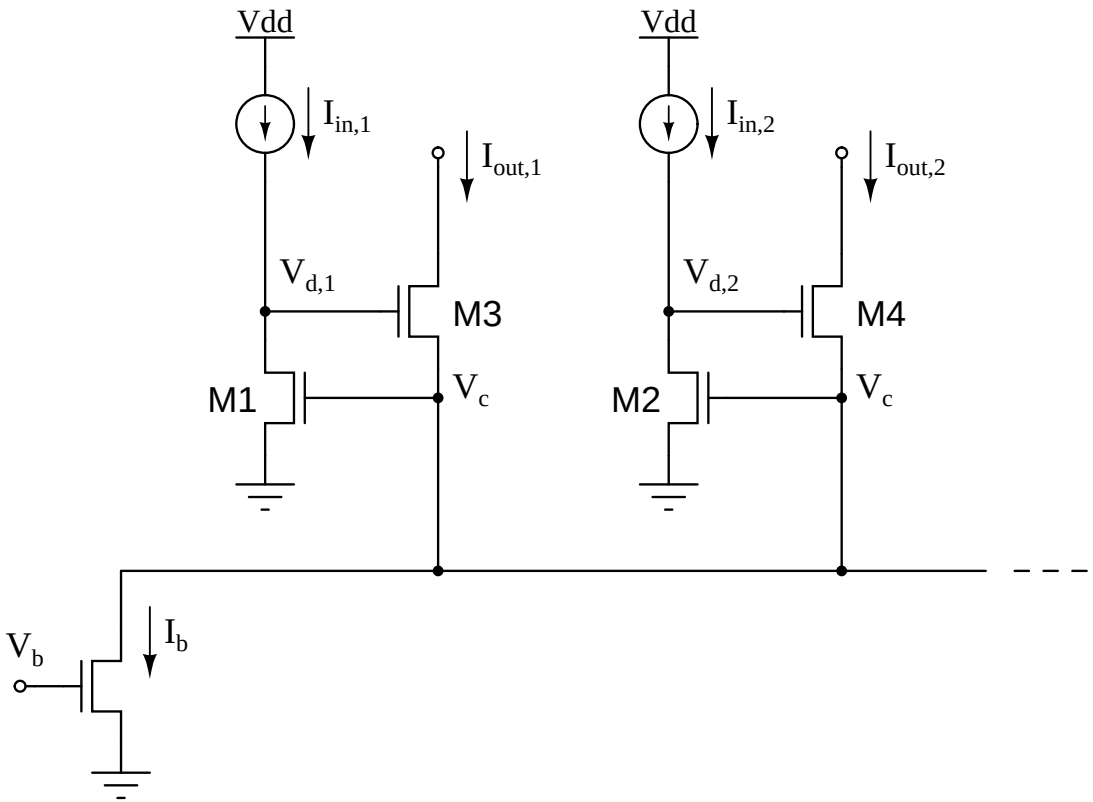

Three conditions

1. $I_{in,1} = I_{in,2} = I_{in}$
2. $I_{in,1} \gg I_{in,2}$
3. $I_{in,2} = I_{in}$
   $I_{in,1} = I_{in} + \delta I_{in}$

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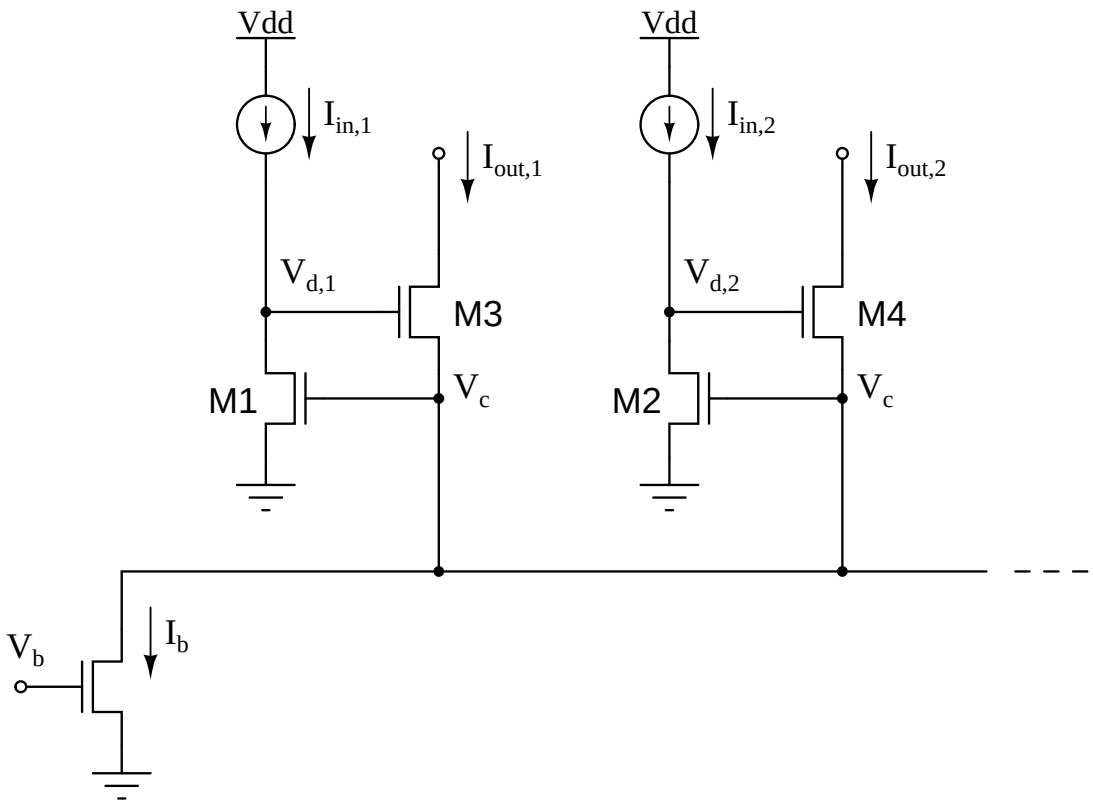
Current-mode WTA circuit



First condition

$$I_{in,1} = I_{in,2} = I_{in}$$

$$V_c = \frac{U_T}{\kappa} ln\left(\frac{I_{in}}{I_0}\right)$$

$$I_{out,1} = I_{out,2} = I_b/2$$

$$V_{d,1} = V_{d,2} \approx V_c + V_b$$

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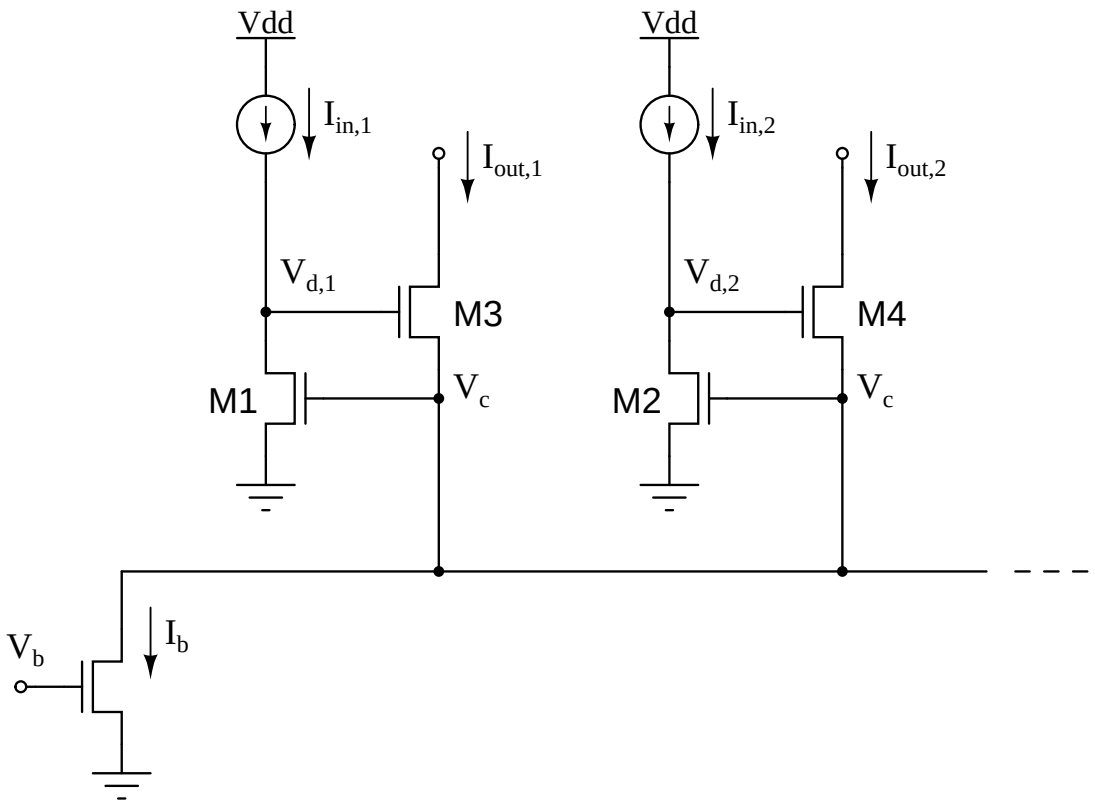
Current-mode WTA circuit



Second condition

$I_{in,1} \gg I_{in,2}$

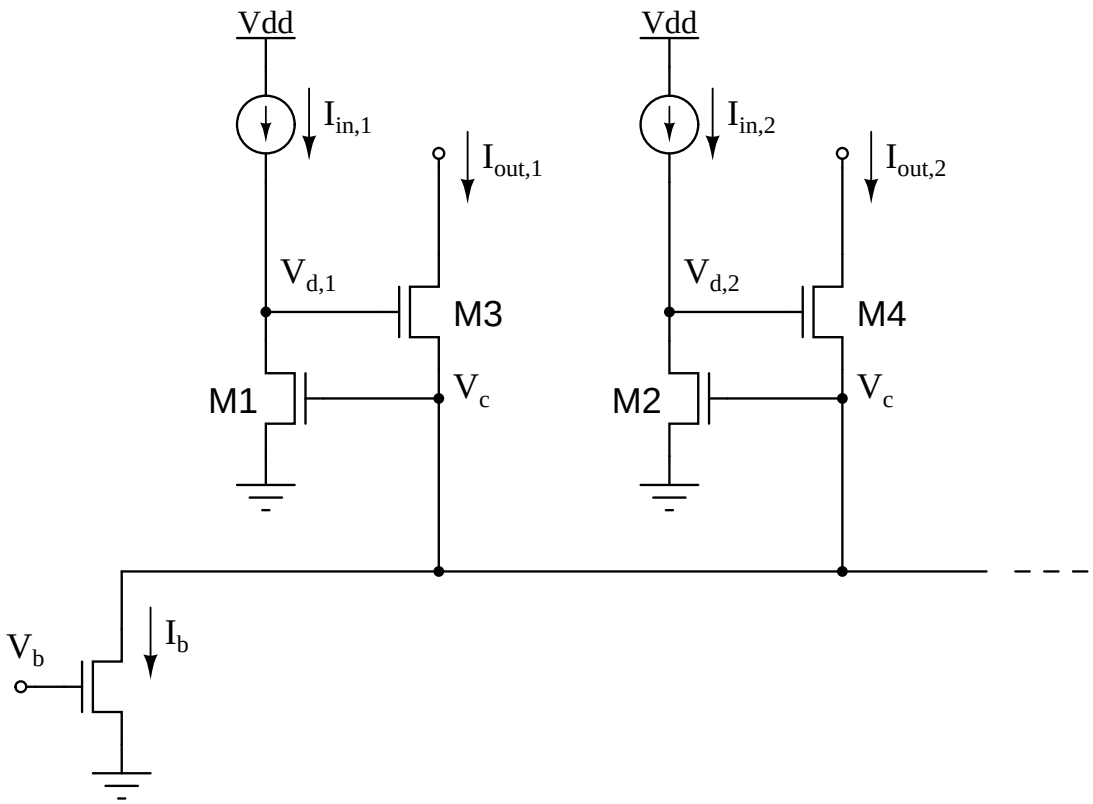
$$V_c = \frac{U_T}{\kappa} ln\left(\frac{I_{in,1}}{I_0}\right)$$

$$I_{out,1} = I_b; I_{out,2} = 0$$

$$V_{d,1} = V_c + V_b$$

$$V_{d,2} \approx 0$$

Current-mode WTA circuit

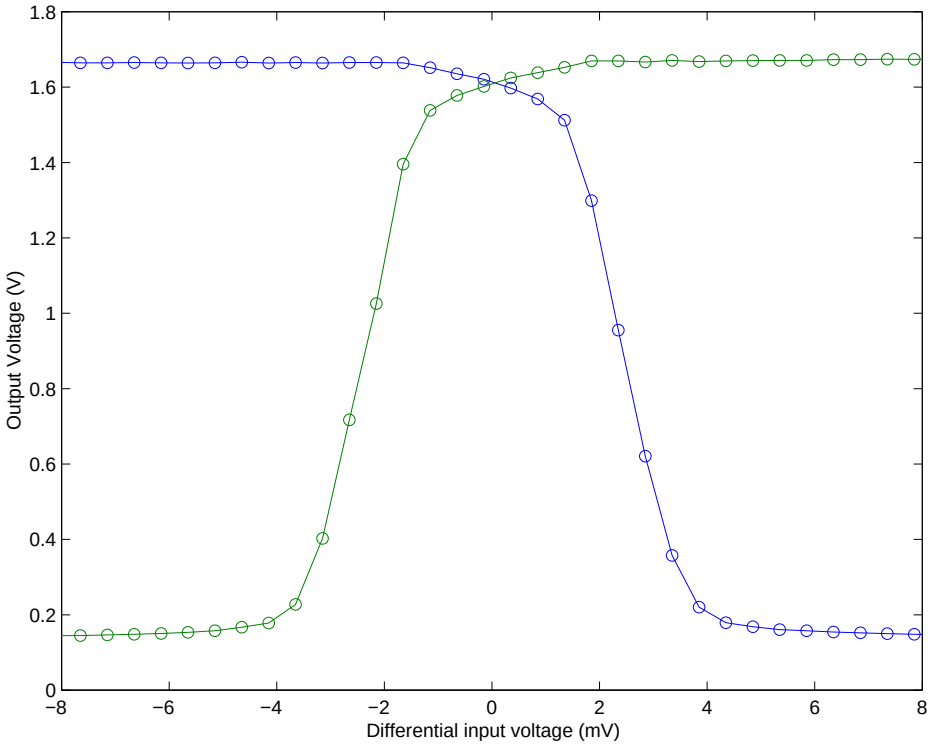


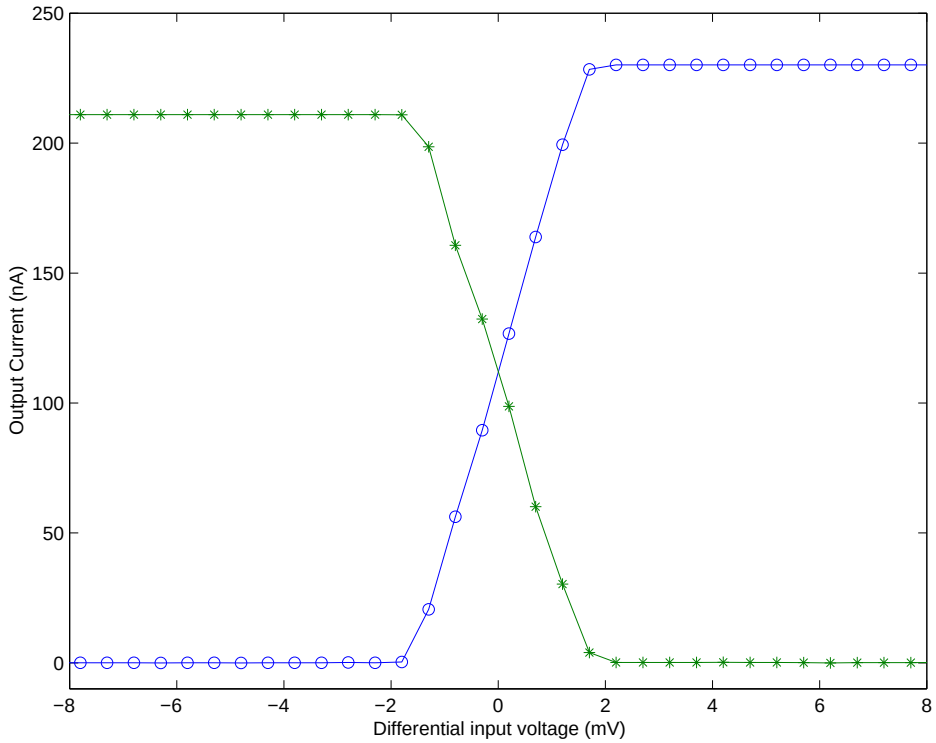
Third condition

$$I_{in,2} = I_{in}$$
$$I_{in,1} = I_{in} + \delta I_{in}$$

$$I_d = I_{sat}(1 + \frac{V_d}{V_e})$$
$$V_{d,2} = V_{d,1} - V_e \frac{\delta I_{in}}{I_{sat}}$$
$$I_{out,2} < I_{out,1}$$

WTA circuit measurements





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WTA variants

- Local inhibition
- Diode-source degeneration
- Positive feedback
- Local excitation

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Hysteretic WTA