Applying the translinear principle to the Diff-Pair Integrator (DPI) circuit

The DPI is a perfect circuit for applying the translinear principle. Complicated voltage-mode non-linear differential equations can be reduced to simple easy-to-solve equations, in current-mode.

Note that this is also one of the few circuits in which translinear loops contain both n-FETs and p-FETs. Keep in mind that the relevant signs in voltage mode (e.g. of the gate voltages) change between n- and p-FETs. So in current mode what would normally be at the numerator goes to the denominator, when using p-FETs instead of n-FETs, and vice-versa.

If we consider the circuit in Fig. 1, and assume that transistors operate in subthreshold and are in saturation, we can write:

$$I_{out} = I_0 e^{\frac{\kappa V_C}{U_T}} \tag{1}$$

$$I_{in} = I_1 + I_2 \tag{2}$$

$$I_C = C\frac{d}{dt}V_C \tag{3}$$

$$I_2 = I_\tau + I_C \tag{4}$$

where U_T is the thermal voltage and κ is the subthreshold slope factor [3]. Thanks to the properties of exponential functions, we can express I_C as a function of I_{out}:

$$I_C = C\frac{U_T}{\kappa I_{out}}\frac{d}{dt}I_{out} \tag{5}$$

Now, if we take into account the translinear loop emphasized in Fig. 1 we can write:

$$I_{th} \cdot I_1 = I_2 \cdot I_{out}. \tag{6}$$

By replacing I_1 from eq. (2) we get:

$$I_{th} \cdot (I_{in} - I_2) = I_2 \cdot I_{out} \tag{7}$$

And by expanding I_2 from eq. (4) we get:

$$I_{th} \cdot (I_{in} - I_\tau - I_C) = (I_\tau + I_C) \cdot I_{out} \tag{8}$$

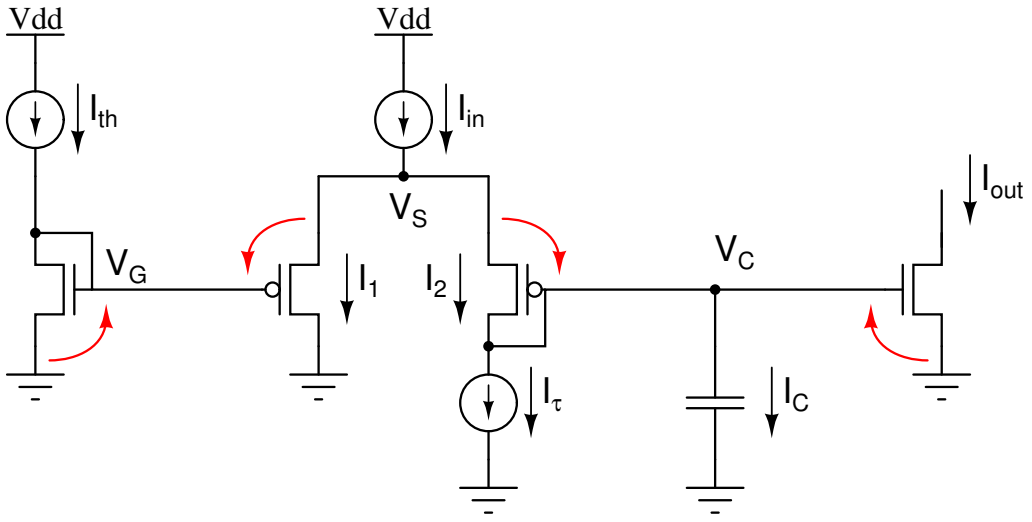

Figure 1: Schematic diagram of the diff-pair integrator circuit. Red arrows show the translinear loop considered for the analysis.

By replacing I_C from eq. (5) and dividing everything by I_τ we get:

$$\frac{I_{th}I_{in}}{I_\tau} - I_{th} \cdot \left(1 + \frac{\tau}{I_{out}}\frac{d}{dt}I_{out}\right) = \tau\frac{d}{dt}I_{out} + I_{out} \tag{9}$$

where $\tau \triangleq CU_T/\kappa I_\tau$.

This is a first-order non-linear equation that cannot be solved analytically.

But in the case of input step currents, or pulses, starting from zero initial conditions, one can safely assume that I_{out} will increase monotonically. If I_{out} becomes sufficiently large the second term in the parenthesis of eq. (9) becomes negligible with respect to 1 and the equation can be reduced to:

$$\boxed{\tau\frac{d}{dt}I_{out} + I_{out} = \frac{I_{th}}{I_\tau} \cdot I_{in} - I_{th}} \tag{10}$$

This is a first-order linear equation that has been shown to match well experimental data for input step and pulse waveforms, as is typically the case fro synapse models [1, 2].

Appendix: Translinear principle verification

We assume that the zero-sum loop of gate-to-source voltages emphasized in Fig. 1 faithfully maps to eq. (6), rewritten here for convenience:

$$I_{th} \cdot I_1 = I_2 \cdot I_{out}. \tag{11}$$

We can verify this by writing the subthreshold equations of the transistors involved in the loop, and substituting them in eq. (11):

$$I_{th} = I_0 e^{\frac{\kappa V_G}{U_T}} \tag{12}$$

$$I_1 = I_0 e^{\frac{\kappa(V_{dd}-V_G)-(V_{dd}-V_S)}{U_T}} \tag{13}$$

$$I_2 = I_0 e^{\frac{\kappa(V_{dd}-V_C)-(V_{dd}-V_S)}{U_T}} \tag{14}$$

$$I_{out} = I_0 e^{\frac{\kappa V_C}{U_T}} \tag{15}$$

Eq. (11) therefore becomes:

$$I_0 e^{\frac{\kappa V_G}{U_T}} \cdot I_0 e^{\frac{\kappa(V_{dd}-V_G)-(V_{dd}-V_S)}{U_T}} = I_0 e^{\frac{\kappa(V_{dd}-V_C)-(V_{dd}-V_S)}{U_T}} \cdot I_0 e^{\frac{\kappa V_C}{U_T}} \tag{16}$$

If all I_0 terms are equal, this equation reduces to:

$$\kappa V_G + \kappa V_{dd} - \kappa V_G - V_{dd} + V_S = \kappa V_{dd} - \kappa V_C - V_{dd} + V_S + \kappa V_C \tag{17}$$

which is obviously correct, assuming that the n-FET and p-FET κ terms are equal.

References

[1] C. Bartolozzi and G. Indiveri. Synaptic dynamics in analog VLSI. *Neural Computation*, 19(10):2581–2603, Oct 2007.

[2] C. Bartolozzi, S. Mitra, and G. Indiveri. An ultra low power current–mode filter for neuromorphic systems and biomedical signal processing. In *Biomedical Circuits and Systems Conference, BIOCAS 2006*, pages 130–133. IEEE, 2006.

[3] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbruck, and R.J. Douglas. *Analog VLSI:Circuits and Principles*. MIT Press, 2002.