Lab 4

October 14, 2018

Static Circuits: Current Mirror, Differential Pair, Current Correlator, Bump Circuit, and Transconductance Amplifier

The objectives of this lab are to understand and characterize a number of very useful standard static circuits that in subthreshold operation.

This will be a 2 week exercise which you will start the first week and then finish the second week. During the first week answer pre-lab questions 1, 2, 3, and 4. Answer questions 5, 6, and 7 after the next class. Similarly, carry out experiments 1 and 2 this week, and 3 and 4 next week.

The experimental objectives are as follows:

1. To measure and characterize the differential-pair currents as a function of the input voltages, including the mismatch-caused differential offset voltage.
2. To characterize a bump-antibump circuit and to understand something about its non-idealities.
3. To characterize a simple differential transconductance amplifier and understand its operation in terms of the behavior of the differential pair and the current mirror. Specifically, to understand the dependence of the output current on the differential input voltages.
4. To characterize single-stage 2-transistor "common-source" amplifier gain, and how it arises from transconductance and output impedance.

4.1 Reading

Read the section on the differential pair, transconductance amplifier, and bump circuit in Chapter 5 of the class book.

4.2 Prelab

This prelab must be complete individually by all partners and must be completed before coming to the lab.

1. All parts of this question refer to the differential pair shown in Fig. 4.1(a). Unless stated otherwise, assume that M_1, M_2, and M_b are in saturation, that they are operated in subthreshold, and neglect the Early effect.

   (a) When working with differential circuits, it is often advantageous to express results in terms of the *common mode* voltage (denoted by $\bar{V}$ or V_{cm}) and the *differential mode* voltage (denoted by δV or V_{dm}). These voltages are defined in terms of V_1 and V_2 by $\bar{V} \equiv 1/2(V_1 + V_2)$ and $\delta V \equiv V_1 - V_2$. Solve for V_1 and V_2 in terms of $\bar{V}$ and δV.

   (b) Compute the common source voltage V_s of M_1 and M_2 as a function of the inputs V_1 and V_2, and the bias current I_b.

   (c) What restrictions would you put on V_1 and V_2 to ensure that M_b is in saturation?

   (d) Holding V_1 constant, sketch V_s versus V_2.

   (e) How is the diff-pair related to a source-follower?

   (f) In what way does V_s approximate the maximum function $max(V_1, V_2)$? (You will see why this is relevant in the winner-take-all circuit.)

   (g) Compute the currents I_1 and I_2 as a function of V_1, V_2, and I_b.

   (h) Now compute the relationship between the differential output current $I_1 - I_2$ and the differential input voltage δV. Remember there is a trick: multiplying by $exp(-\frac{V_1+V_2}{2})$.

   (i) Sketch a graph of I_1 and I_2 versus δV. Also sketch the sum $I_1 + I_2$ and the difference $I_1 - I_2$ on the same axes.

2. For the simple current correlator in Fig. 4.1(b) show that

$$I_{out} = \frac{r_1 I_1 r_2 I_2}{r_1 I_1 + r_2 I_2}, \tag{4.1}$$

   where r_1 and r_2 denote the ratios of the W/L ratios for the transistors connected to V_1 and V_2 respectively. This means that $r_1 = w_{1out}/w_{1in}$ and $r_2 = w_{2out}/w_{2in}$, where the w's denote the W/L ratios of the corresponding transistors. Assume that M_{2out} is in saturation, but note that M_{1out} may not be.

3. Let

$$I_1 = \frac{I_t}{2}(1+x), I_2 = \frac{I_t}{2}(1-x), \tag{4.2}$$

   where $I_t \equiv I_1 + I_2$ is the total input current and $x \equiv (I_1 - I_2)/I_t$ is a dimensionless difference current.

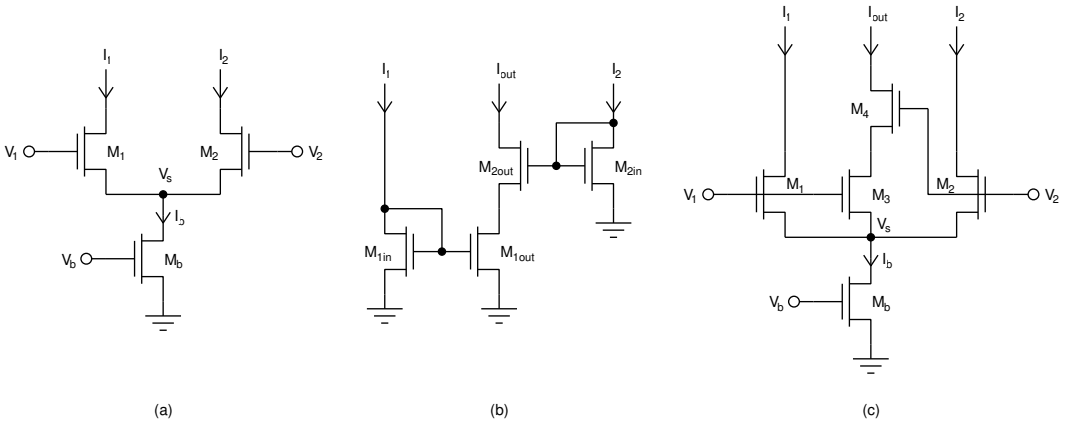

Figure 4.1: (a) Differential pair. (b) Simple current correlator. (c) Bump-antibump circuit.

(a) Substitute these expressions into (4.1) and obtain an expression for I_{out} in terms of I_t and x.

(b) Simplify your result assuming $r_1 = r_2 \equiv r$ and sketch a graph of I_{out} vs. x. How is the graph modified if $r_1 > r_2$?

(c) Show that if I_1 and I_2 are generated by a differential pair (see earlier question) then

$$x = \tanh\left(\frac{\kappa(V_1 - V_2)}{2U_T}\right) \tag{4.3}$$

and I_t is the differential pair's bias current.

4. Now consider the bump-antibump circuit shown in Fig. 4.1(c).

(a) Assume that $r_1 = r_2 \equiv r$ and that x is given by (4.3). Compute I_{out} in terms of x, r, and I_b by substituting $I_t = I_b - I_{out}$ in equation 4.1 and solving for I_{out}.

(b) Express your result in terms of the hyperbolic cosine function (cosh). You may want to use the hyperbolic function relationships

$$\cosh^2(x) - \sinh^2(x) = 1 \tag{4.4}$$

$$\tanh^2(x) = 1 - \frac{1}{\cosh^2(x)} \tag{4.5}$$

You should end up with the result

$$I_{out} = \frac{I_b}{1 + \frac{4}{r}\cosh^2(\frac{\kappa\Delta V}{2U_T})} \tag{4.6}$$

(c) What fraction of I_b will flow down the middle branch (the bump branch) if $V_1 = V_2$?

(d) Does the bump-antibump circuit compute "soft" or analog logic operations AND and XOR between the two voltage inputs V_1 and V_2?

5. Now consider a simple differential transconductance amplifier which is built from a differential pair and a current mirror. The output current should be equal to the the difference of the two differential pair currents, i. e. $I_{out} = I_1 - I_2$. Is this statement true? Justify your answer by stating your assumptions about transistor saturation and drain conductance.

   (a) Now consider the transconductance amplifier with the output open-circuited (i.e. no current flows into or out of the output node). Say V_2 is fixed at some voltage in the middle of the rails, e.g., Vdd/2. Explain what happens to the output voltage as V_1 is swept very slowly (i.e. slowly enough so that the output voltage reaches a steady state) from below V_2 to above V_2 for a subthreshold bias. Discuss the current through the differential pair transistors and the current mirror, and the voltage on the internal node common to the differential pair transistors. Try to keep the discussion concise.

   (b) What is the transconductance $g_m = dI_{out}/dV_{in}$, where $V_{in} \equiv V_1 - V_2$, in subthreshold? How does it change if the circuit is operated super-threshold?

   (c) Quantitatively, what is the relationship between transconductance, output resistance r_o, and voltage gain A of a transconductance amplifier?

6. Draw the schematic of a wide-range transconductance amplifier and explain why it does not have the simple 5-transistor transamp restriction on allowable output voltage.

7. Sketch the setups that you will use for the experiments, including voltage ranges.

4.3 This Week's Test Circuits

You will again be using the class chip. Partial schematics of this chip showing the circuits relevant to the different experiments are shown in Fig. 4.2. Don't forget to hook up ground (pin 15), V_{dd} (pins 25 and 35), and Padbias (pin 5). You can once again ground Padbias because we will not be using the analog followers in the pads for these experiements.

4.4 Fitting data

For fitting lines to some measured data, you can use the Matlab `polyfit` function to compute the slope and axis intercept, and the `polyval` function to evaluate the line on your input points to plot it, in order to see how well it fits. See the class wiki for this lab exercise to find the Matlab code, and also to find an alternative plotting routine called `plot182` that eases on-screen hand measurement of data.

Here is an example of using `polyfit`. The input is `vin`, the measured outputs are `vout`. You want to fit the line in the range of `vout` from 1.5 to 3.5. You use the `find` function to get the indices of the `vout`'s that are between these levels, then use `polyfit` to compute the coefficients of the line. Finally, you plot the data together with the fit.

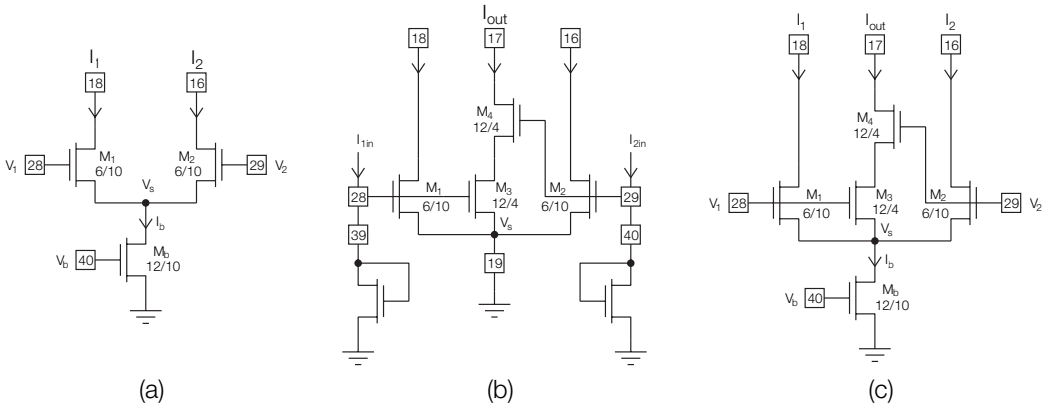

Figure 4.2: Pinouts of the transamps used in the experiments. The numbers in the squares denote the pin numbers. The sizes of the transistors are given as W/L in microns. Some transistors are shared between the three circuits. These are denoted with the same numbers. (a) Differential pair. (b) Simple current correlator (not used in this lab). (c) Bump-antibump circuit.

```
ind=find(vout<3.5 & vout >1.5); % find vout's in range
p=polyfit(vin(ind),vout(ind),1); % fit order 1 polynomial (line)
ameas=p(1) % slope is p(1), y intercept is p(2)
figure(1);clf;
vfit=polyval(p,vin); % compute values of fit at all points
plot(vin,vout,'bo',vin,vfit,'b-');
xlabel 'V_{in} (V)'% TeX formatting for subscripts
ylabel 'V_{out} (V)'
legend('Vout','linear fit for Vout');
title('Output voltage vs. input voltage');
```

4.5 Experiments

You will use almost exactly the same setup of all of the following experiments.

Experiment 1: Differential pair

In this experiment, you will measure the dependence of the differential pair currents I_1 and I_2 on the differential input voltage δV. Use a pot to bias V_b. Tie the Keithley 230 between V_1 and V_2 (use one of the isolated BNCs) so that the applied voltage corresponds to the differential voltage. In order to keep the common mode voltage $\bar{V}$ constant during the sweep, connect equally-sized resistors (approx. 10 kΩ) from a second pot to both inputs V_1 and V_2 as shown in Fig. 4.3(a). Set the pot to a common mode voltage of 2 V. To measure I_1, tie the triax lead of the Keithley 236 SMU to the drain of M_1 and its BNC lead to V_{dd}; M_2's drain should be tied directly to V_{dd}. Set the 236 voltage to zero. This setup will keep M_1, M_2 and M_b in saturation for the subthreshold measurements.

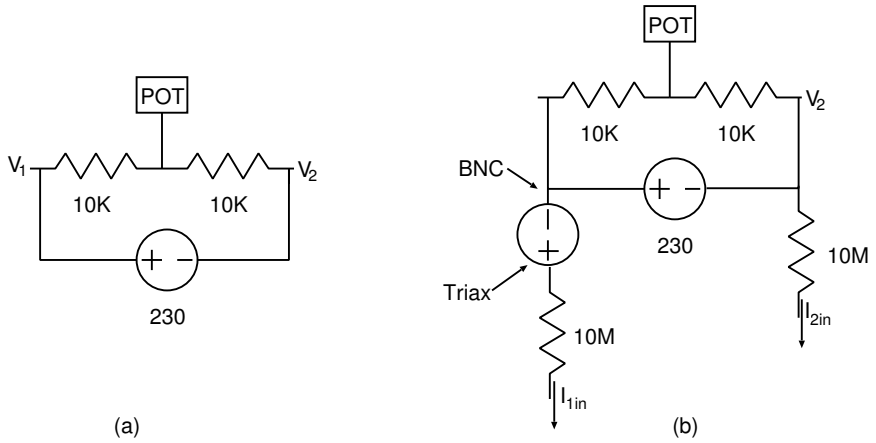

Figure 4.3: Setup for Experiments 1 to 2 so that a differential input can be applied to the circuits. (a) Circuit to apply a differential input voltage. (b) Circuit to apply a differential input voltage and to measure the corresponding input currents (not used in this lab).

After sanity checking by manually entering differential voltages, use `iv` to sweep the 230 and measure I_1. Do this for a subthreshold value on V_b. The voltage range of the sweep should be large enough to cover the full range over which the current varies. Now switch the connections between M_1 and M_2 and repeat the sweep, measuring I_2 instead of I_1. Hand in a well-annotated plot (it's fine to write on the plot) with your subthreshold curves showing I_1, I_2, $I_1 - I_2$, and $I_1 + I_2$ with appropriate fits. Comment on the range of linearity and on the measured offset voltage (the voltage that makes $I_1 = I_2$). What determines the linear range of input voltage? If you were to run the differential pair in strong inversion, what voltage would determine the linear range of operation? Hint: In weak inversion the thermal voltage is the natural voltage scale. In strong inversion, what is the most natural voltage scale?

Experiment 2: Bump-antibump circuit

In this experiment, we will measure the input-output relationship of the bump-antibump circuit, and will look for non-idealities. You will use exactly the same setup as for the diff-pair experiment except that you will now connect the middle leg to allow current to flow in it.

Choose a subthreshold value for the bias current and measure I_1, I_2, and I_{out} as you did for the diff-pair. Again, use the same sweep parameters for each curve with a sweep range of ± 250 mV. Hand in a well-annotated plot showing I_1, I_2, I_{out}, $I_1 + I_2$, and $I_1 + I_2 + I_{out}$.

Based on prelab question 4c and the transistor W/L ratios shown in Figure 4.2, does the measured ratio of maximum bump current to bias current accord with your measurement? Comment on possible reasons for any discrepancy between the fit and what you expect from the known transistor geometry. These effects are known to the logic guys as the short- and narrow-channel threshold shift effects.

Hand in the plotted subthreshold curves along with the fit to the antibump current.

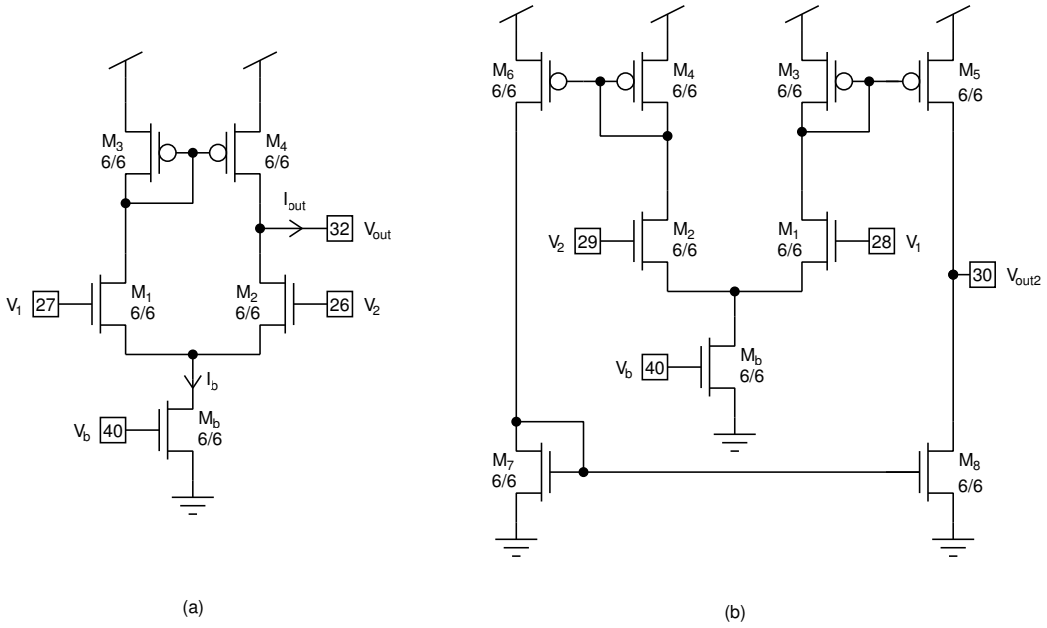

Figure 4.4: Pinouts of the different circuits used in the experiments. The numbers in the squares denote the pin numbers. The sizes of the transistors are given as W/L in microns. The input pins are shared between the two circuits. (a) Simple transconductance amplifier. (b) Wide-output-range transconductance amplifier. Note that the dimensions of the output transistors are actually $W/L = 3/58$ and not $6/6$.

Experiment 3: Transconductance amplifier output current vs. input voltage

Both transconductance amplifiers you will be taking measurements from are also on the class chip. Their pinout is shown in Fig. 4.4. Note that some pins are shared with the previous experiments so you will only need to change a few connections.

The purpose of this experiment is to explore the transfer characteristics of a simple transconductance amplifier. In particular, you will measure the effects of the bias current and input voltages on the output current. This is done by sweeping the differential input voltage for each bias current.

Use a pot to set V_b to a subthreshold value, and another pot to set V_1 to a value that is sufficient to keep M_b in saturation. Use the 236 SMU to set V_{out} to approximately 3.5 V. Reference the 236 SMU to ground. Use the 230 to apply a differential input voltage $\delta V \equiv V_1 - V_2$ and measure the output current as a function of the differential input voltage, sweeping over a large enough range to ensure that the output current saturates at each extreme. Do this experiment for two values of V_b below threshold and one value above threshold.

Show the subthreshold sweeps on one subplot and the above- threshold sweep on a different subplot. Remember to label the x and y axes appropriately and use the legend command in Matlab to label the two subthreshold plots. Fit a line to one of your subthreshold sweeps in the linear region. What characteristics can you extract from the fit? Explain any asymmetries in the amplifier's I-V curve and the offset voltage in terms of mismatch between

devices in the mirror and differential pair, and the Early effect. How can you distinguish the effects of mismatch in the mirror and in the differential pair? The main point here is to recognize that there *will* be non-idealities, to understand where they arise, and to quantify them in the simplest manner possible.

Experiment 4: Transconductance amplifier voltage gain, output conductance, transconductance

First, you will measure the open-circuit voltage gain $A \equiv \partial V_{out}/\partial V_{in}$, then the output conductance $g_d \equiv -\partial I_{out}/\partial V_{out}$, and finally, the transconductance $g_m \equiv \partial I_{out}/\partial V_{in}$. From these measurements, you will see how well the gain A is predicted by the formula $A = g_m/g_d$.

In this series of experiments, use the same measurement configuration as for the previous ones. Again, for the current measurements, set the SMU 236 to a voltage that keeps all transistors in saturation (about 3.5 V). For the voltage measurements, use the 236 SMU in I-V mode, and put the output current to zero, and use the Matlab script `vv`. Do all measurements below threshold and use the same value of V_b throughout. Once you have set this up, you will not need to change any connections between the three measurements. They are done directly from `iv`.

Do all the following experiments for the simple transamp.

If you have time in the end (doubtful!), measure the voltage gain for the wide-output-range transamp to see how it compares. You can have fun seeing how transistor length sizing clearly affects voltage gain, especially in the wide range configuration where the input and output stages are essentially decoupled.

Voltage gain *A*

Set one of the two inputs to approximately 1.5V. Locate the differential input voltage range where the output voltage changes rapidly (it will be quite small, around 2 mV, and could be away from zero by some tens of millivolts, due to random or systematic mismatch). Find the range by manually entering voltages into the 230. The circuit will be driving the electrometer directly, and at a subthreshold bias the currents available to charge capacitances will be very small. Notice how long the output takes to settle, especially in the high gain region. Knowing this, *make your sweeps small*, otherwise you will be sitting around a long time! Remember that you are only interested in the high-gain transition region. You should use a large delay time ($> 500ms$) between setting the input voltage and measuring the output (*e.g.* see the `delay` variable in `matlab>help vv`).

Once you have taken a satisfactory curve, fit a linear function to it to compute the gain. (Resist the temptation to obtain the gain by differentiating the curve, since this operation is very sensitive to noise.) Plot the data and the fit on the same graph.

Output conductance g_d

Now measure the output conductance of the amplifier at the same bias voltage. First of all, fix one input to the transconductance amplifier to a constant voltage (approximately 1.5V will still do). Now find where to set the 230 so that the output current is zero (measure current with the 236 SMU). Then sweep the output voltage (the 236 SMU voltage source) over the high gain output voltage region while measuring the output current. Do a linear fit to determine the output conductance from your data.

Transconductance g_m

Now measure the transconductance at the same bias voltage. Sweep the 230 to get a curve of I_{out} vs. $V_1 - V_2$. Extract the value of g_m from this curve.

Compute the expected voltage gain using g_m and g_d and compare with the measured voltage gain. How well do these measurements agree?

4.6 Postlab

1. When we set the output voltage of the transconductance amplifier to about 3.5 V and measured its output current, we found that at some nonzero input voltage (the offset voltage) the output current was zero. Will we get a different input offset voltage if we change the output voltage? Explain why.

2. Draw a simple transconductance amplifier like the one in Fig. 4.4(a). This transamp has an n-type bias transistor. Now draw another one "upside-down," i.e. with a pFET used to bias a pFET differential pair, and label the noninverting $(+)$ input (makes the amplifier push out more current when it is made more positive) and the inverting $(-)$ inputs (makes the amplifier suck in more current when it is made more positive).

   What are the conditions for keeping M_b in saturation for the p-type transamp? How do they differ from the n-type transamp?

3. What are the advantages and disadvantages of the wide-output-range transconductance amplifier vs. a standard transconductance amplifier? Consider layout area, output voltage swing, offset voltage, current asymmetries, and the gain A. Why is the wide-output-range transamp better suited for construction of a high-gain single-stage amplifier? *Hint: think about the necessary symmetries between pairs of transistors.*

The remainder of this postlab is not required for the completion of your lab. However, we suggest that you look over these questions as this material could be covered in the final exam.

1. Consider a current correlator with three inputs and three stacked transistors. How does I_{out} depend on the three input currents I_1, I_2, and I_3?

2. We have seen that I_{out} in the bump-antibump circuit is large when V_1 and V_2 are similar and its complement, $I_{sum} \equiv I_1 + I_2$, is large when they are dissimilar. How would you modify the device geometries to get a larger fraction of the bias current to go to I_{out} in the first case and to I_{sum} in the second case?

3. In the prelab, we suggested using a differential pair to generate the inputs to a current correlator. Draw a circuit that does this and use your results from the prelab (with $r_1 = r_2 \equiv r$) to derive an expression for I_{out} as a function of $V_1 - V_2$. Write this expression in terms of the sech≡1/cosh function. Sketch the output current as a function of differential input voltage.

4.7 What we expect

Can you sketch a transamp, a wide range transamp, a current correlator, and a bump circuit in both n- and p-type varieties?

How does a differential pair work? How does the common-node voltage change with the input voltages? How can you compute the differential tail currents from the subthreshold equations, and how do you obtain the result in terms of the differential input voltage?

How does a current-correlator work? How does a bump circuit work?

The I-V characteristics of a transconductance amplifier below threshold. What's the functional difference between simple and wide-output-range transamp? The subthreshold transconductance g_m. The relation between gain A, transistor drain conductances g_d, and transconductances g_m.

Can you reason through all the node voltages in these circuits? I.e., if we draw the circuit and provide specific power supply and input voltages, can you reason to estimate all the other node voltages, at least to first order approximations, assuming $\kappa = 1$?