LM7321/LM7321Q Single/ LM7322/LM7322Q Dual Rail-to-Rail Input/Output ±15V, High Output Current and Unlimited Capacitive Load Operational Amplifier

Check for Samples: LM7321, LM7322

FEATURES

- **(V_S = ±15, T_A = 25°C, Typical Values Unless Specified.)**
- **Wide Supply Voltage Range 2.5V to 32V**
- **Output Current +65 mA/−100 mA**
- **Gain Bandwidth Product 20 MHz**
- **Slew Rate 18 V/µs**
- **Capacitive Load Tolerance Unlimited**
- **Input Common Mode Voltage 0.3V Beyond Rails**
- **Input Voltage Noise 15 nV/√Hz**
- **Input Current Noise 1.3 pA/√Hz**
- **Supply Current/Channel 1.1 mA**
- **Distortion THD+Noise −86 dB**
- **Temperature Range −40°C to 125°C**
- **Tested at −40°C, 25°C and 125°C at 2.7V, ±5V, ±15V.**
- **LM7321Q/LM7322Q are Automotive Grade Products that are AEC-Q100 Grade 1 Qualified.**

APPLICATIONS

- **Driving MOSFETs and Power Transistors**
- **Capacitive Proximity Sensors**
- **Driving Analog Optocouplers**
- **High Side Sensing**
- **Below Ground Current Sensing**
- **Photodiode Biasing**
- **Driving Varactor Diodes in PLLs**
- **Wide Voltage Range Power supplies**
- **Automotive**
- **International Power Supplies**

DESCRIPTION

The LM7321/LM7321Q/LM7322/LM7322Q are rail-to-rail input and output amplifiers with wide operating voltages and high output currents. The LM7321/LM7321Q/LM7322/LM7322Q are efficient, achieving 18 V/µs slew rate and 20 MHz unity gain bandwidth while requiring only 1 mA of supply current per op amp. The LM7321/LM7321Q/LM7322/LM7322Q performance is fully specified for operation at 2.7V, ±5V and ±15V.

The LM7321/LM7321Q/LM7322/LM7322Q are designed to drive unlimited capacitive loads without oscillations. All LM7321/LM7321Q and LM7322/LM732Q parts are tested at −40°C, 125°C, and 25°C, with modern automatic test equipment. High performance from −40°C to 125°C, detailed specifications, and extensive testing makes them suitable for industrial, automotive, and communications applications.

Greater than rail-to-rail input common mode voltage range with 50 dB of common mode rejection across this wide voltage range, allows both high side and low side sensing. Most device parameters are insensitive to power supply voltage, and this makes the parts easier to use where supply voltage may vary, such as automotive electrical systems and battery powered equipment. These amplifiers have true rail-to-rail output and can supply a respectable amount of current (15 mA) with minimal head- room from either rail (300 mV) at low distortion (0.05% THD+Noise). There are several package options for each part. Standard SOIC versions of both parts make upgrading existing designs easy. LM7322LM7322Q are offered in a space saving 8-Pin VSSOP package. The LM7321/LM7321Q are offered in small SOT-23 package, which makes it easy to place this part close to sensors for better circuit performance.

TYPICAL PERFORMANCE CHARACTERISTICS

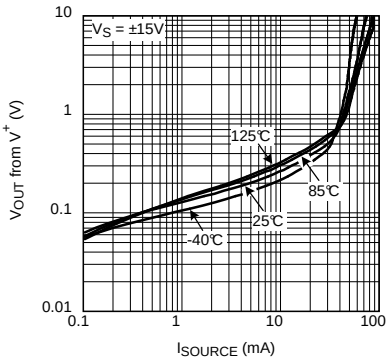


Figure 1. Output Swing vs. Sourcing Current

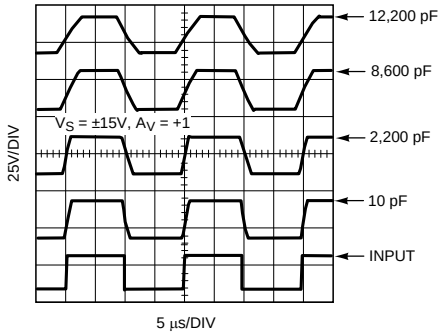


Figure 2. Large Signal Step Response

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2 kV
	Machine Model	200V
	Charge-Device Model	1 kV
V_{IN} Differential		±10V
Output Short Circuit Current		See (4)
Supply Voltage ($V_S = V^+ - V^-$)		35V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Storage Temperature Range		−65°C to 150°C
Junction Temperature (5)		150°C
Soldering Information:	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5 ms.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings

Supply Voltage ($V_S = V^+ - V^-$)		2.5V to 32V
Temperature Range (1)		−40°C to 125°C
Package Thermal Resistance, θ_{JA}, (1)	5-Pin SOT-23	325°C/W
	8-Pin VSSOP	235°C/W
	8-Pin SOIC	165°C/W

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}) - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

2.7V Electrical Characteristics (1)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_{OUT} = 1.35V, and R_L > 1 MΩ to 1.35V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 2.2V	−5 **−6**	±0.7	+5 **+6**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = 0.5V & V_{CM} = 2.2V (4)		±2		µV/C
I_B	Input Bias Current	V_{CM} = 0.5V (5)	−2.0 **−2.5**	−1.2		µA
		V_{CM} = 2.2V (5)		0.45	1.0 **1.5**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V and V_{CM} = 2.2V		20	200 **300**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.0V	70 **60**	100		dB
		0V ≤ V_{CM} ≤ 2.7V	55 **50**	70		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V	78 **74**	104		dB
CMVR	Common Mode Voltage Range	CMRR > 50 dB		−0.3	−0.1 **0.0**	V
			2.8 **2.7**	3.0		
A_{VOL}	Open Loop Voltage Gain	0.5V ≤ V_O ≤ 2.2V R_L = 10 kΩ to 1.35V	65 **62**	72		dB
		0.5V ≤ V_O ≤ 2.2V R_L = 2 kΩ to 1.35V	59 **55**	66		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 1.35V V_{ID} = 100 mV		50	150 **160**	mV from either rail
		R_L = 2 kΩ to 1.35V V_{ID} = 100 mV		100	250 **280**	
	Output Voltage Swing Low	R_L = 10 kΩ to 1.35V V_{ID} = −100 mV		20	120 **150**	
		R_L = 2 kΩ to 1.35V V_{ID} = −100 mV		40	120 **150**	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = 0V (6)	30 **20**	48		mA
		Sinking V_{ID} = −200 mV, V_{OUT} = 2.7V (6)	40 **30**	65		
I_S	Supply Current	LM7321		0.95	1.3 **1.9**	mA
		LM7322		2.0	2.5 **3.8**	
SR	Slew Rate (7)	A_V = +1, V_I = 2V Step		8.5		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF		7.5		MHz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

2.7V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_{OUT} = 1.35V, and R_L > 1 MΩ to 1.35V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
GBW	Gain Bandwidth	f = 50 kHz		16		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz		11.9		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 2 kHz		0.5		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	V^+ = 1.9V, V^- = −0.8V f = 1 kHz, R_L = 100 kΩ, A_V = +2 V_{OUT} = 210 mV_{PP}		−77		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ		60		dB

±5V Electrical Characteristics (1)

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = 0V, V_{OUT} = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −4.5V and V_{CM} = 4.5V	−5 **−6**	±0.7	+5 **+6**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −4.5V and V_{CM} = 4.5V (4)		±2		µV/°C
I_B	Input Bias Current	V_{CM} = −4.5V (5)	−2.0 **−2.5**	−1.2		µA
		V_{CM} = 4.5V (5)		0.45	1.0 **1.5**	
I_{OS}	Input Offset Current	V_{CM} = −4.5V and V_{CM} = 4.5V		20	200 **300**	nA
CMRR	Common Mode Rejection Ratio	−5V ≤ V_{CM} ≤ 3V	80 **70**	100		dB
		−5V ≤ V_{CM} ≤ 5V	65 **62**	80		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V, V_{CM} = −4.5V	78 **74**	104		dB
CMVR	Common Mode Voltage Range	CMRR > 50 dB		−5.3	−5.1 **−5.0**	V
			5.1 **5.0**	5.3		
A_{VOL}	Open Loop Voltage Gain	−4V ≤ V_O ≤ 4V R_L = 10 kΩ to 0V	74 **70**	80		dB
		−4V ≤ V_O ≤ 4V R_L = 2 kΩ to 0V	68 **65**	74		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = 0V, V_{OUT} = 0V, and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (2)	Typ (3)	Max (2)	Units
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV			100	250 **280**	mV from either rail
		R_L = 2 kΩ to 0V V_{ID} = 100 mV			160	350 **450**	
	Output Voltage Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV			35	200 **250**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV			80	200 **250**	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = −5V (6)		35 **20**	70		mA
		Sinking V_{ID} = −200 mV, V_{OUT} = 5V (6)		50 **30**	85		
I_S	Supply Current	V_{CM} = −4.5V	LM7321		1.0	1.3 **2**	mA
			LM7322		2.3	2.8 **3.8**	
SR	Slew Rate (7)	A_V = +1, V_I = 8V Step			12.3		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF			9		MHz
GBW	Gain Bandwidth	f = 50 kHz			16		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz			14.3		nV/√Hz
i_n	Input Referred Current Noise Density	f = 2 kHz			1.35		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, R_L = 100 kΩ, A_V = +2 V_{OUT} = 8 V_{PP}			−79		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ			60		dB

(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.
(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

±15V Electrical Characteristics (1)

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 15V, V^- = −15V, V_{CM} = 0V, V_{OUT} = 0V, and R_L > 1MΩ to 15V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −14.5V and V_{CM} = 14.5V	−6 **−8**	±0.7	+6 **+8**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	V_{CM} = −14.5V and V_{CM} = 14.5V (4)		±2		µV/°C
I_B	Input Bias Current	V_{CM} = −14.5V (5)	−2 **−2.5**	−1.1		µA
		V_{CM} = 14.5V (5)		0.45	1.0 **1.5**	
I_{OS}	Input Offset Current	V_{CM} = −14.5V and V_{CM} = 14.5V		30	300 **500**	nA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) All limits are ensured by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.

±15V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limited ensured for T_A = 25°C, V^+ = 15V, V^- = −15V, V_{CM} = 0V, V_{OUT} = 0V, and R_L > 1MΩ to 15V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (2)	Typ (3)	Max (2)	Units
CMRR	Common Mode Rejection Ratio	−15V ≤ V_{CM} ≤ 12V		80 **75**	100		dB
		−15V ≤ V_{CM} ≤ 15V		72 **70**	80		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V, V_{CM} = −14.5V		78 **74**	100		dB
CMVR	Common Mode Voltage Range	CMRR > 50 dB			−15.3	−15.1 **−15**	V
				15.1 **15**	15.3		
A_{VOL}	Open Loop Voltage Gain	−13V ≤ V_O ≤ 13V R_L = 10 kΩ to 0V		75 **70**	85		dB
		−13V ≤ V_O ≤ 13V R_L = 2 kΩ to 0V		70 **65**	78		
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV			150	300 **350**	mV from either rail
		R_L = 2 kΩ to 0V V_{ID} = 100 mV			250	550 **650**	
	Output Voltage Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV			60	200 **250**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV			130	300 **400**	
I_{OUT}	Output Current	Sourcing V_{ID} = 200 mV, V_{OUT} = −15V (6)		40	65		mA
		Sinking V_{ID} = −200 mV, V_{OUT} = 15V (6)		60	100		
I_S	Supply Current	V_{CM} = −14.5V	LM7321		1.1	1.7 **2.4**	mA
			LM7322		2.5	4 **5.6**	
SR	Slew Rate (7)	A_V = +1, V_I = 20V Step			18		V/µs
f_u	Unity Gain Frequency	R_L = 2 kΩ, C_L = 20 pF			11.3		MHz
GBW	Gain Bandwidth	f = 50 kHz			20		MHz
e_n	Input Referred Voltage Noise Density	f = 2 kHz			15		nV/√Hz
i_n	Input Referred Current Noise Density	f = 2 kHz			1.3		pA/√Hz
THD+N	Total Harmonic Distortion +Noise	f = 1 kHz, R_L 100 kΩ, A_V = +2, V_{OUT} = 23 V_{PP}			−86		dB
CT Rej.	Crosstalk Rejection	f = 100 kHz, Driver R_L = 10 kΩ			60		dB

(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Short circuit test is a momentary test. Output short circuit duration is infinite for V_S ≤ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5 ms.

(7) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

CONNECTION DIAGRAMS

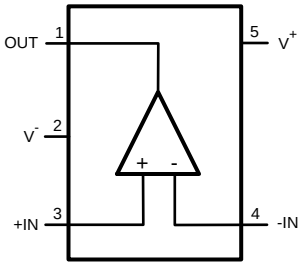


Figure 3. 5-Pin SOT-23
Top View

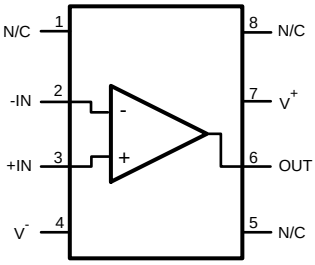


Figure 4. 8-Pin SOIC
Top View

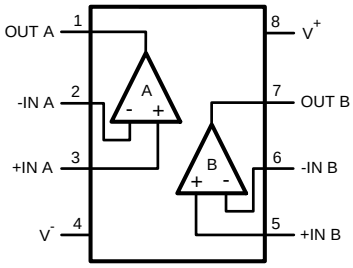


Figure 5. 8-Pin VSSOP/SOIC
Top View

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C.

Output Swing vs. Sourcing Current

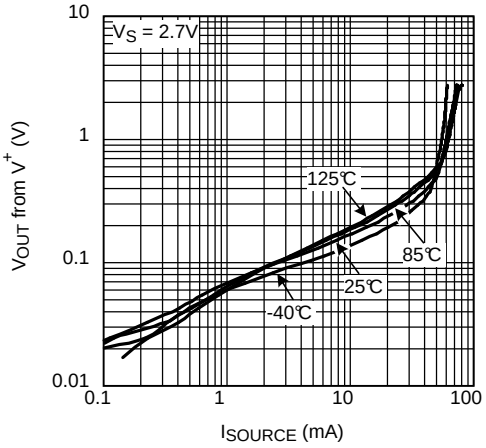


Figure 6.

Output Swing vs. Sinking Current

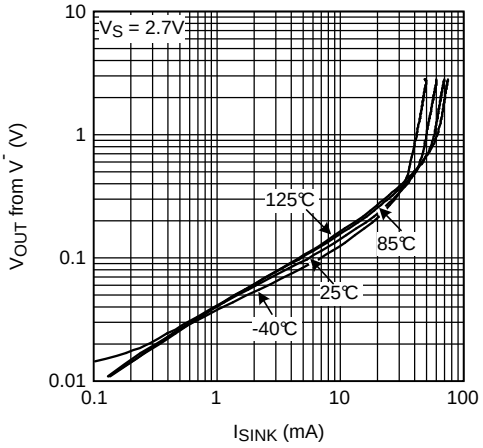


Figure 7.

Output Swing vs. Sourcing Current

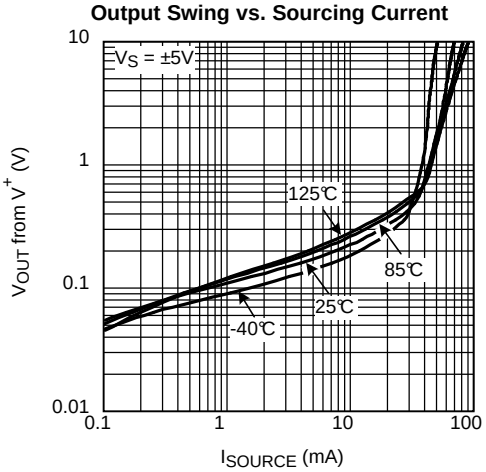


Figure 8.

Output Swing vs. Sinking Current

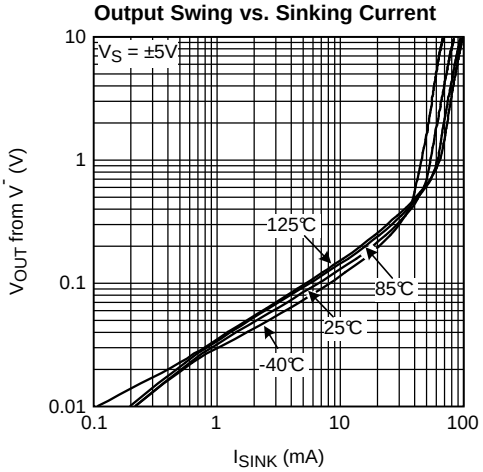


Figure 9.

Output Swing vs. Sourcing Current

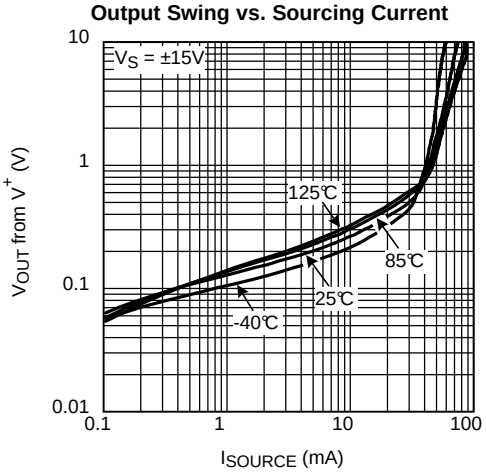


Figure 10.

Output Swing vs. Sinking Current

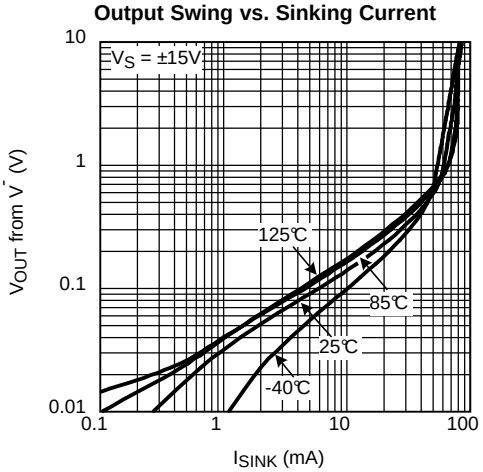


Figure 11.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

V_{OS} Distribution

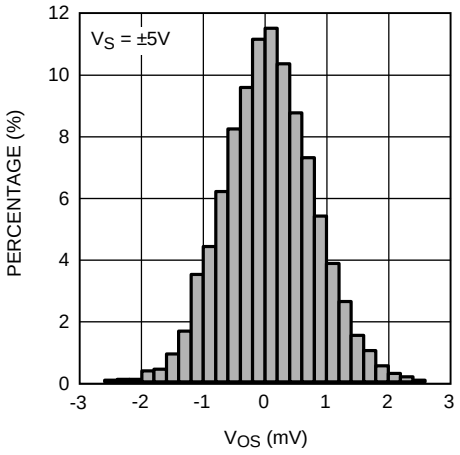


Figure 12.

V_{OS} vs. V_{CM} (Unit 1)

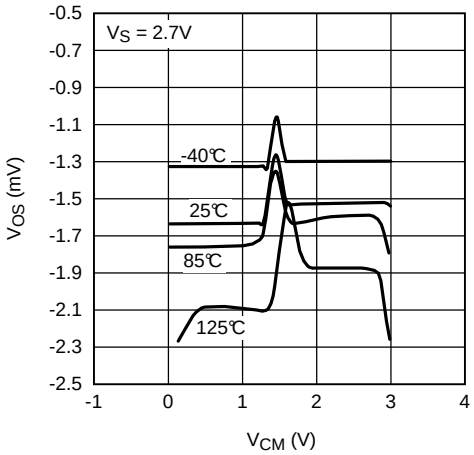


Figure 13.

V_{OS} vs. V_{CM} (Unit 2)

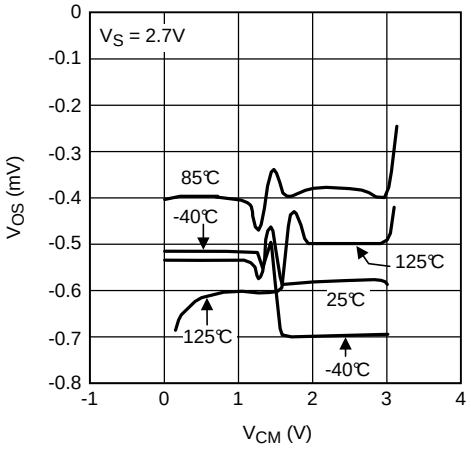


Figure 14.

V_{OS} vs. V_{CM} (Unit 3)

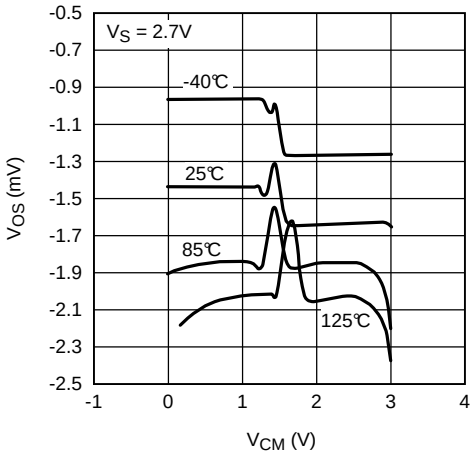


Figure 15.

V_{OS} vs. V_{CM} (Unit 1)

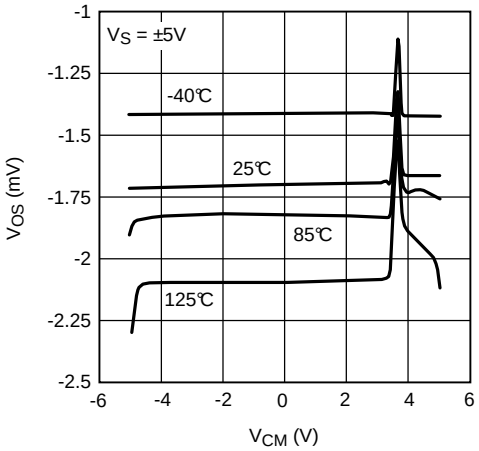


Figure 16.

V_{OS} vs. V_{CM} (Unit 2)

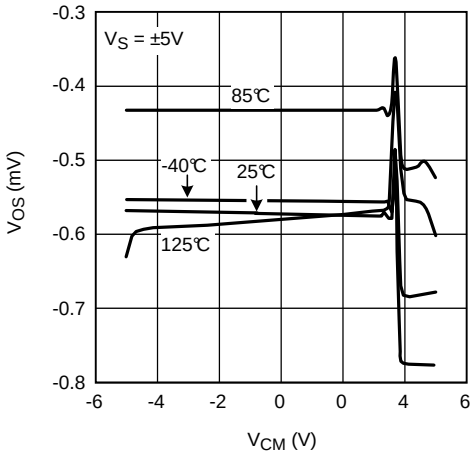


Figure 17.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

V_{OS} vs. V_{CM} (Unit 2)

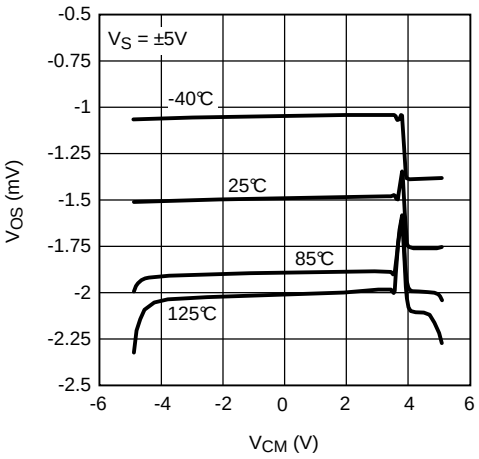


Figure 18.

V_{OS} vs. V_{CM} (Unit 1)

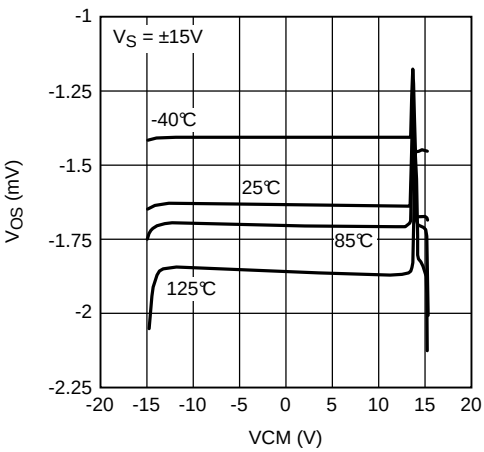


Figure 19.

V_{OS} vs. V_{CM} (Unit 2)

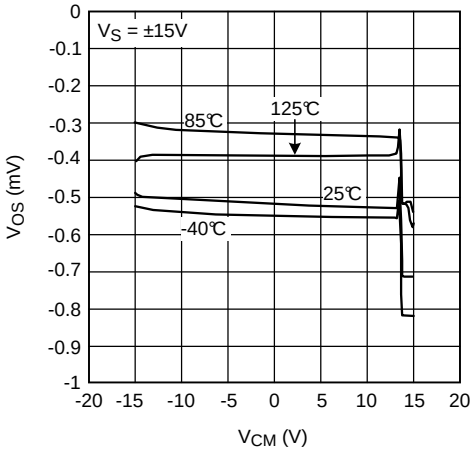


Figure 20.

V_{OS} vs. V_{CM} (Unit 3)

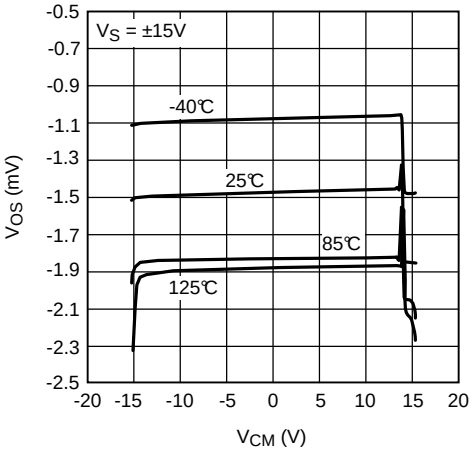


Figure 21.

V_{OS} vs. V_S (Unit 1)

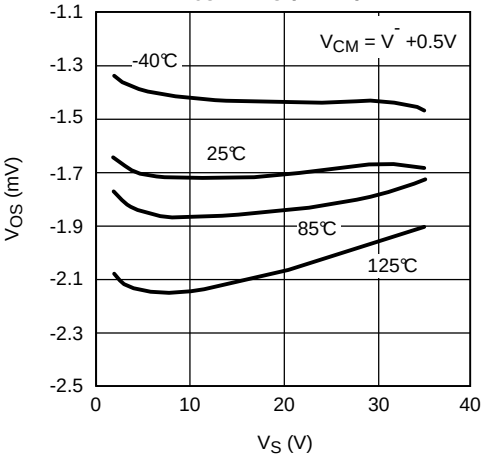


Figure 22.

V_{OS} vs. V_S (Unit 2)

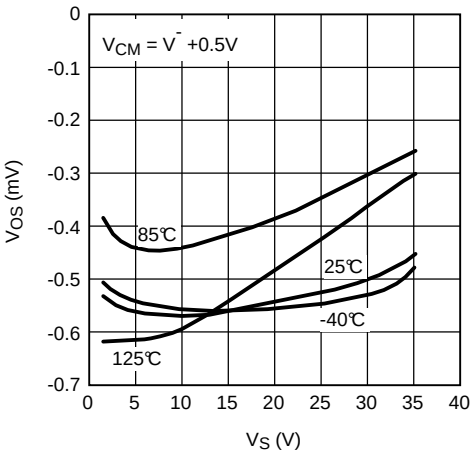


Figure 23.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

V_{OS} vs. V_S (Unit 3)

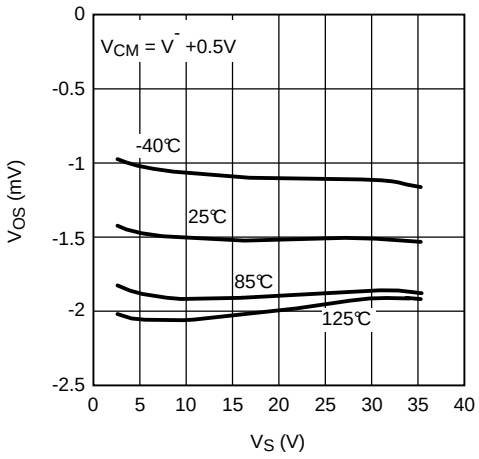


Figure 24.

V_{OS} vs. V_S (Unit 1)

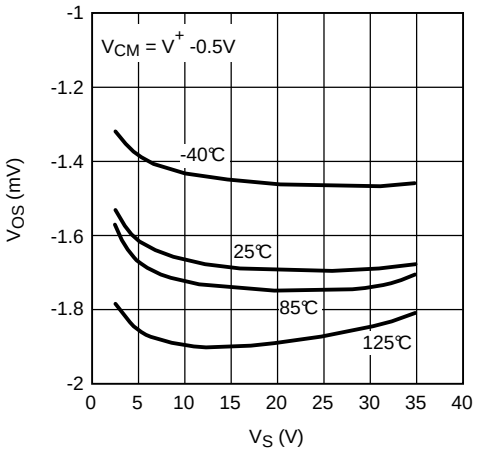


Figure 25.

V_{OS} vs. V_S (Unit 2)

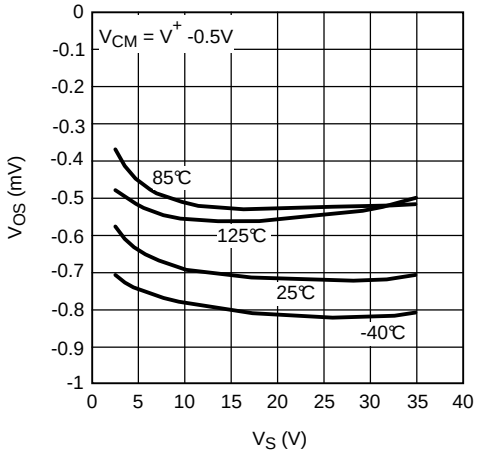


Figure 26.

V_{OS} vs. V_S (Unit 3)

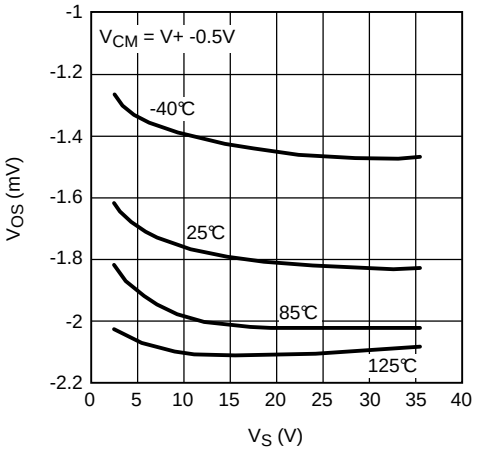


Figure 27.

I_{BIAS} vs. V_{CM}

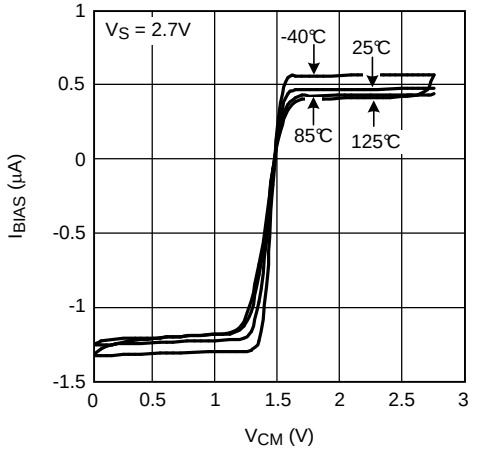


Figure 28.

I_{BIAS} vs. V_{CM}

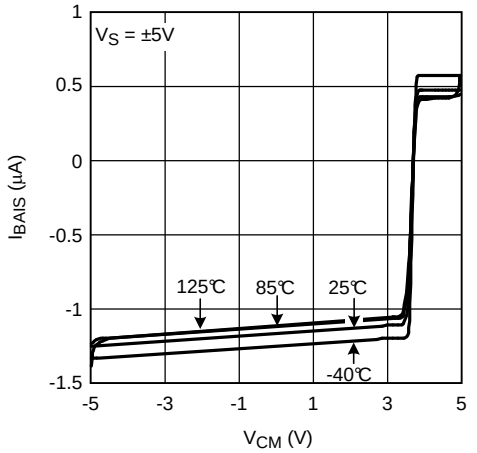


Figure 29.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

I_{BIAS} vs. V_{CM}

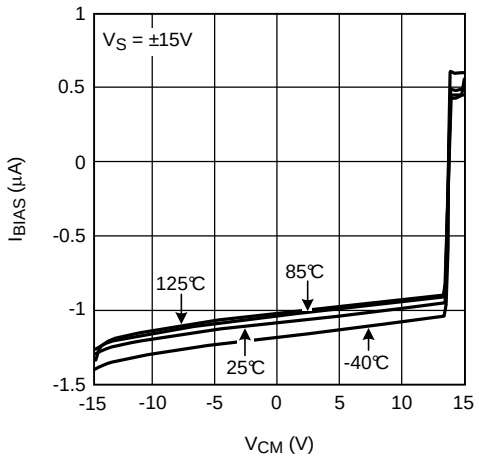


Figure 30.

I_{BIAS} vs. V_S

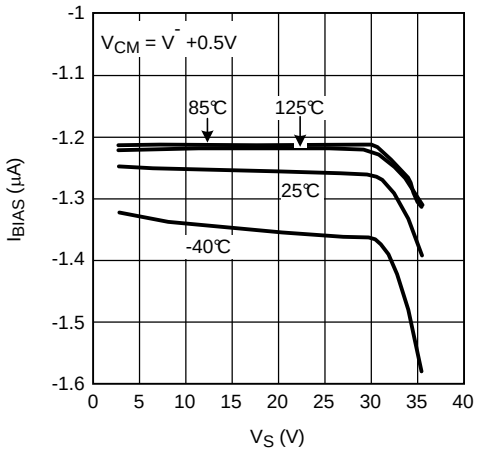


Figure 31.

I_{BIAS} vs. V_S

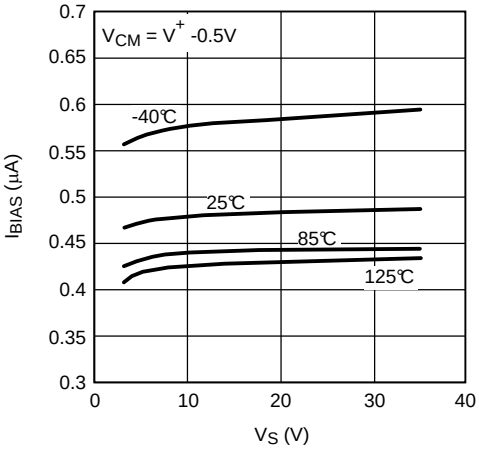


Figure 32.

I_S vs. V_{CM} (LM7321)

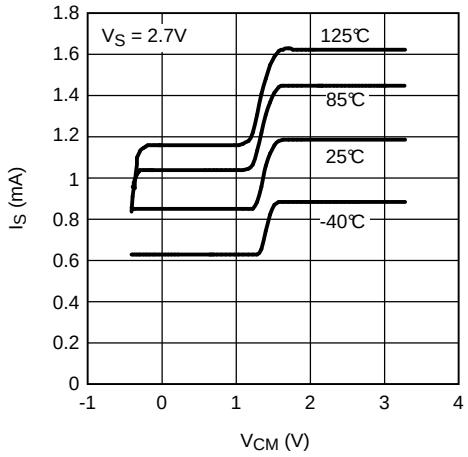


Figure 33.

I_S vs. V_{CM} (LM7322)

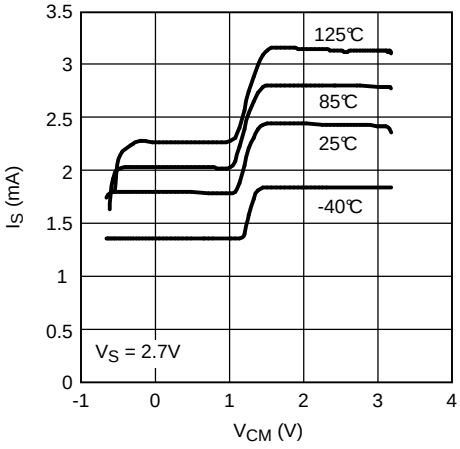


Figure 34.

I_S vs. V_{CM} (LM7321)

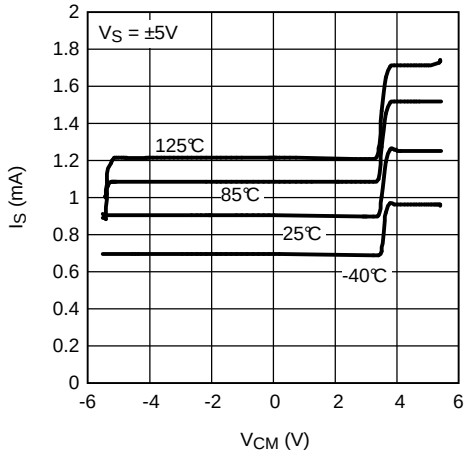


Figure 35.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

I_S vs. V_{CM} (LM7322)

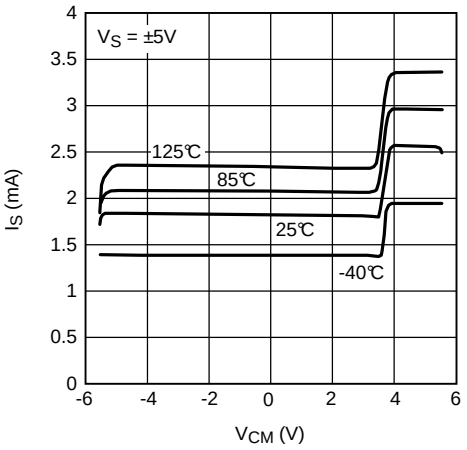


Figure 36.

I_S vs. V_{CM} (LM7321)

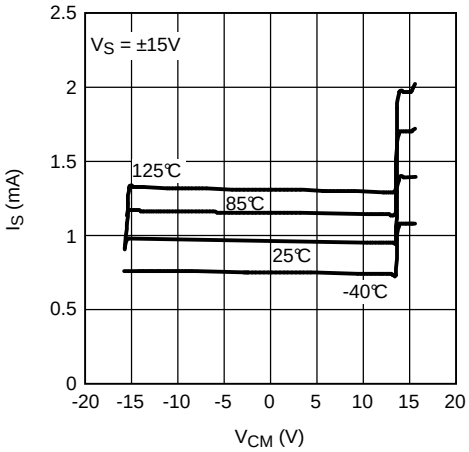


Figure 37.

I_S vs. V_{CM} (LM7322)

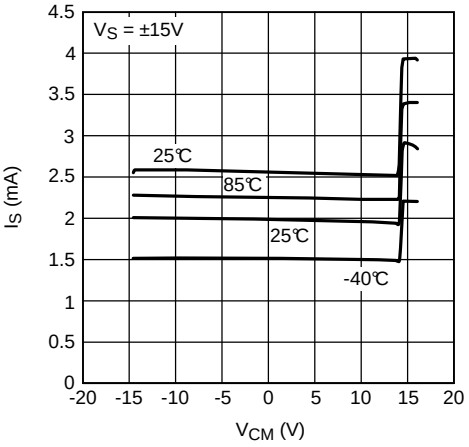


Figure 38.

I_S vs. V_S (LM7321)

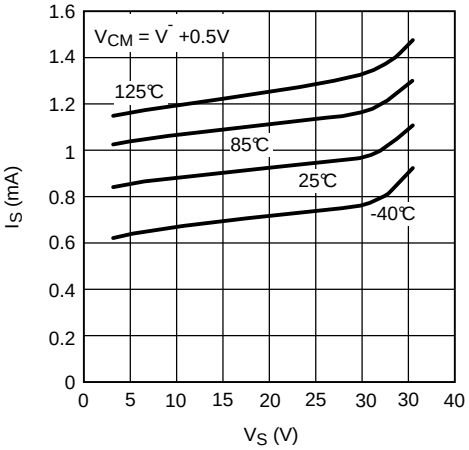


Figure 39.

I_S vs. V_S (LM7322)

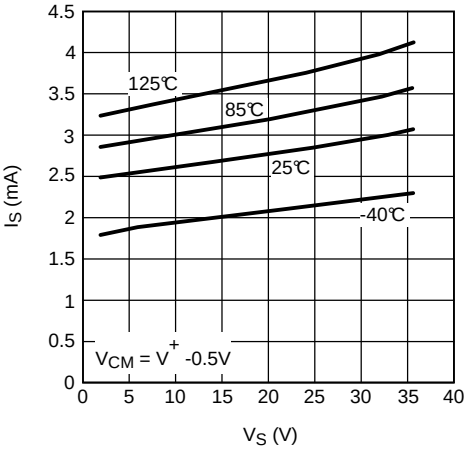


Figure 40.

I_S vs. V_S (LM7321)

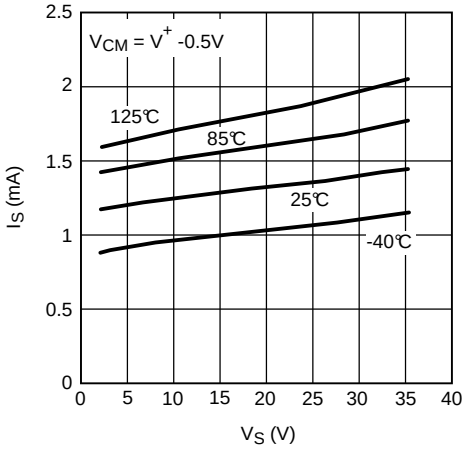


Figure 41.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

I_S vs. V_S (LM7322)

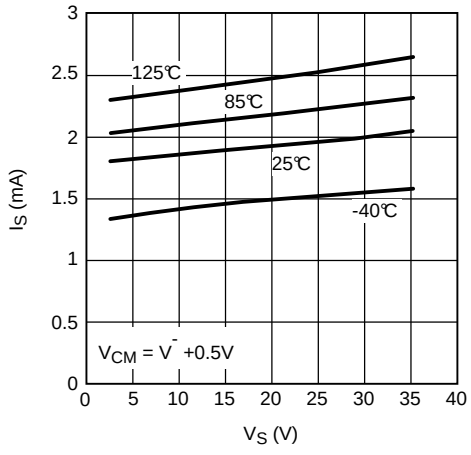


Figure 42.

Positive Output Swing vs. Supply Voltage

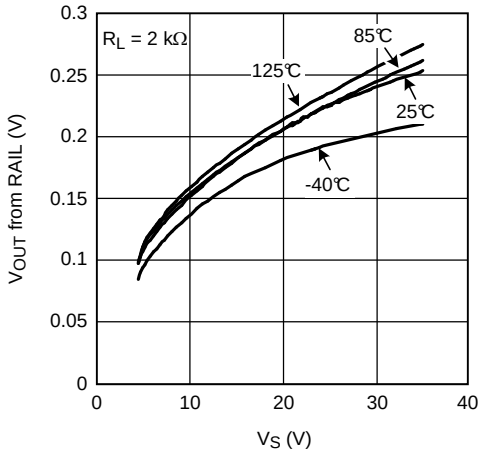


Figure 43.

Positive Output Swing vs. Supply Voltage

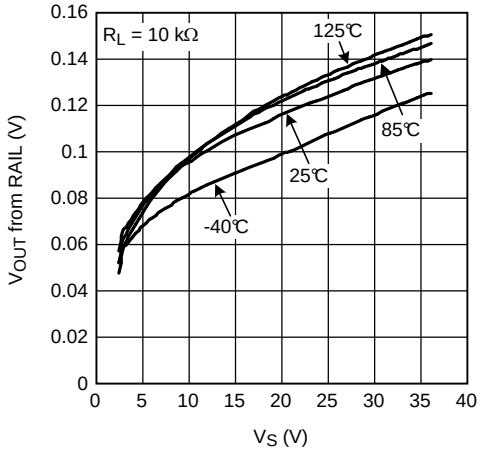


Figure 44.

Negative Output Swing vs. Supply Voltage

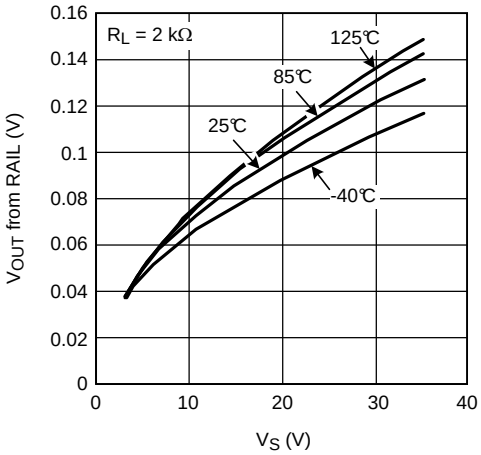


Figure 45.

Negative Output Swing vs. Supply Voltage

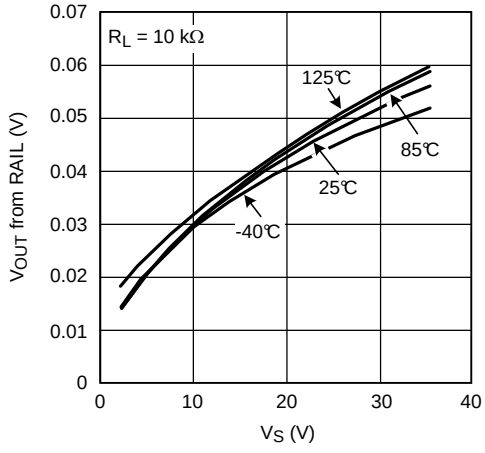


Figure 46.

Open Loop Frequency Response with Various Capacitive Load

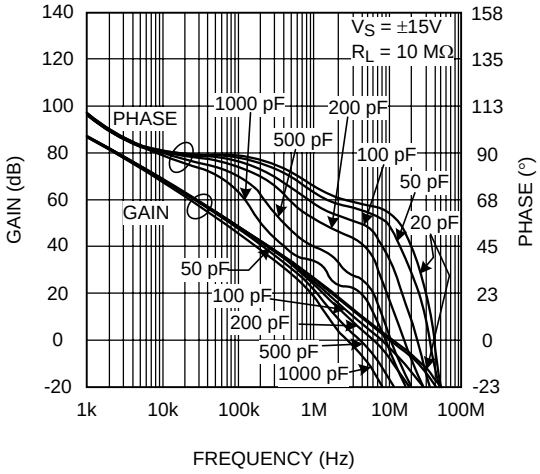


Figure 47.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

Open Loop Frequency Response with Various Resistive Load

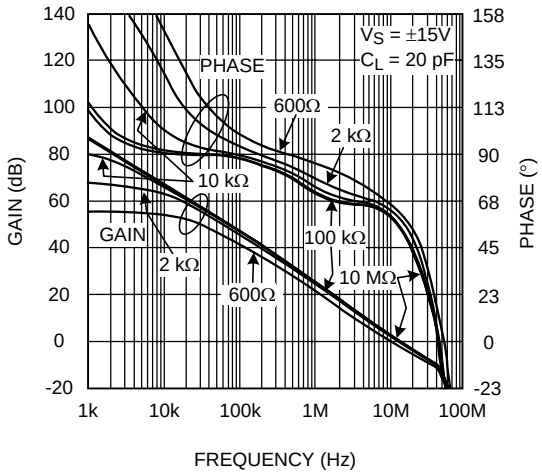


Figure 48.

Open Loop Frequency Response with Various Supply Voltage

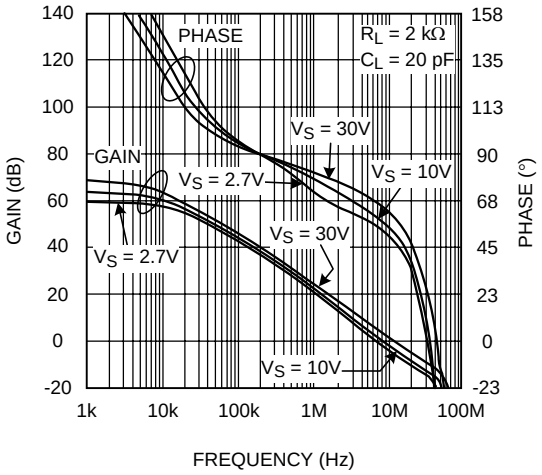


Figure 49.

Phase Margin vs. Capacitive Load

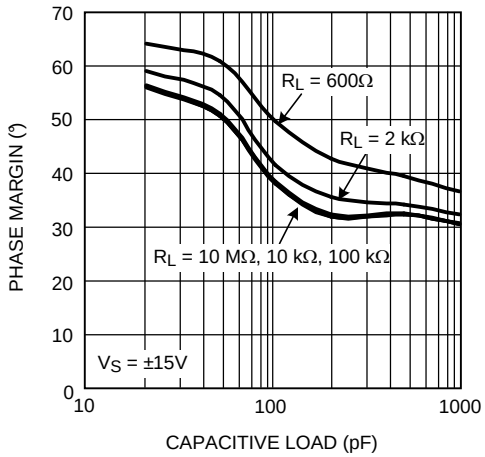


Figure 50.

CMRR vs. Frequency

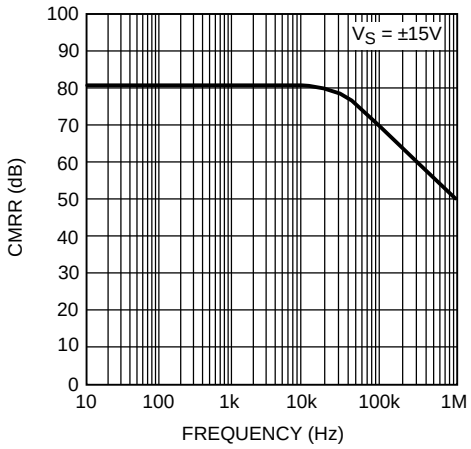


Figure 51.

+PSRR vs. Frequency

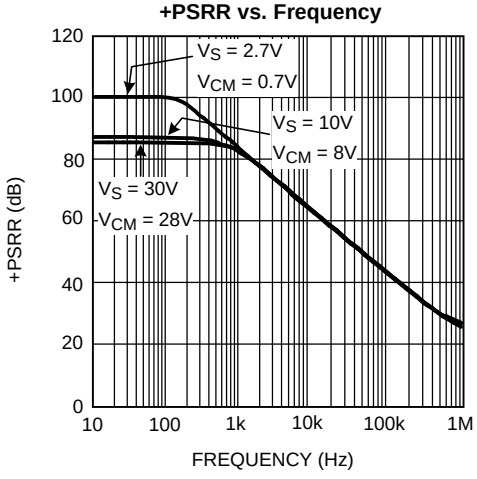


Figure 52.

−PSRR vs. Frequency

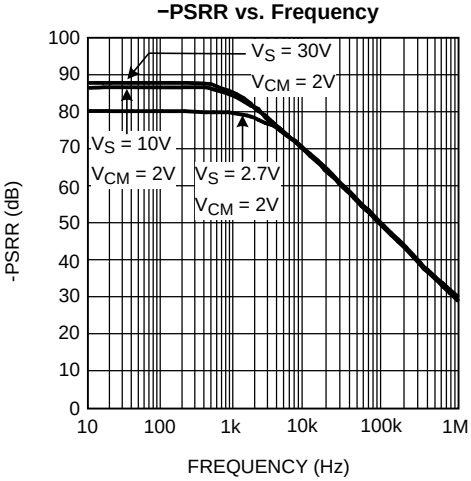


Figure 53.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

Small Signal Step Response

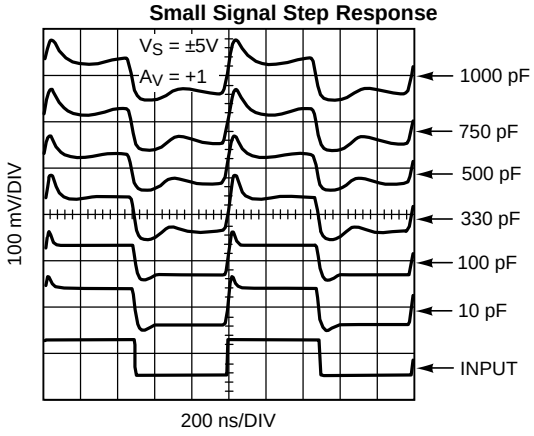


Figure 54.

Large Signal Step Response

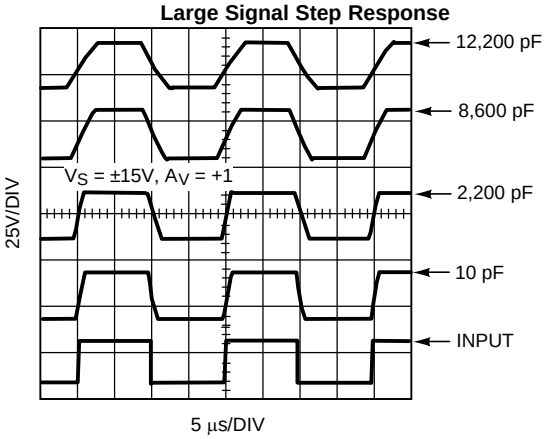


Figure 55.

Input Referred Noise Density vs. Frequency

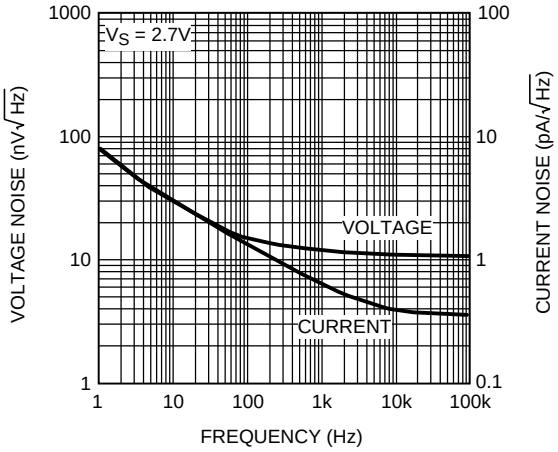


Figure 56.

Input Referred Noise Density vs. Frequency

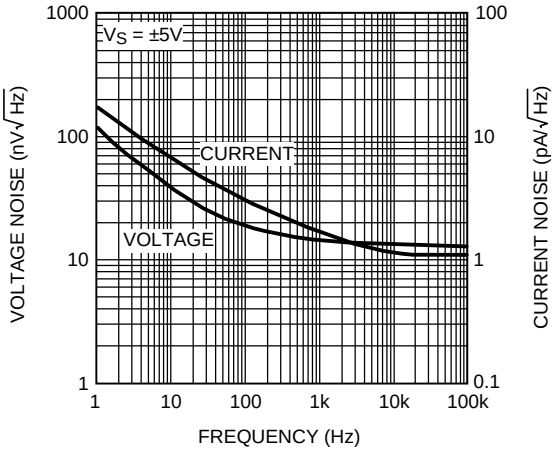


Figure 57.

Input Referred Noise Density vs. Frequency

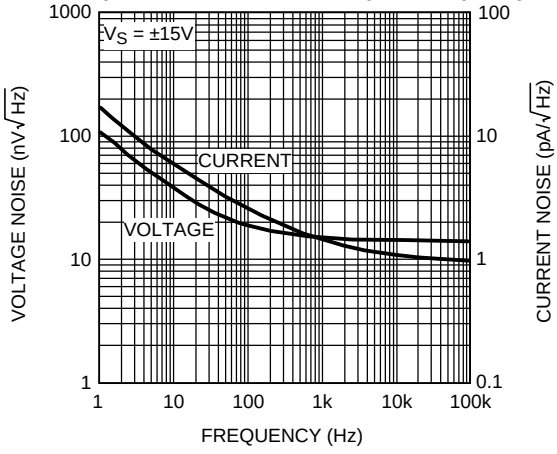


Figure 58.

THD+N vs. Frequency

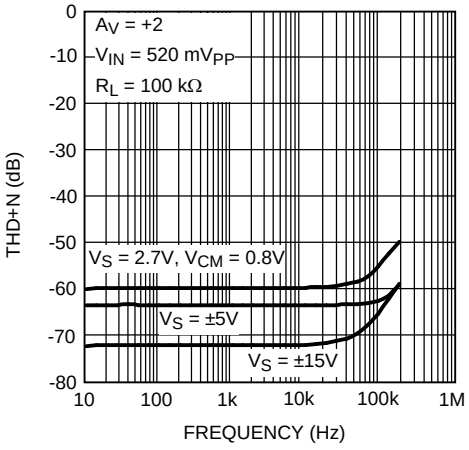


Figure 59.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_A = 25°C.

THD+N vs. Output Amplitude

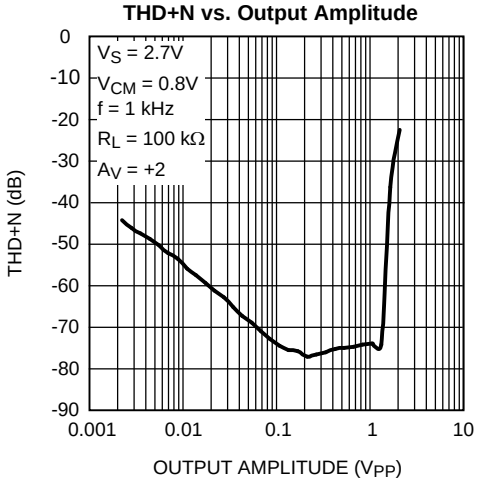


Figure 60.

THD+N vs. Output Amplitude

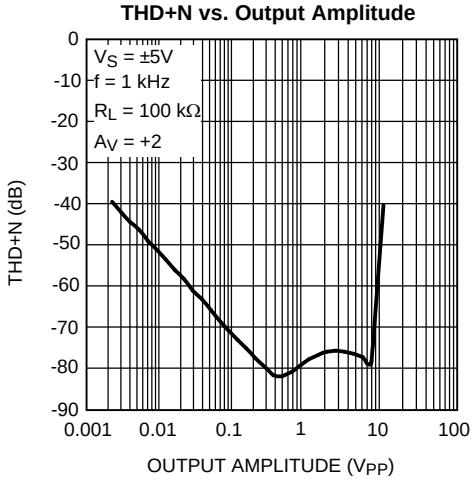


Figure 61.

THD+N vs. Output Amplitude

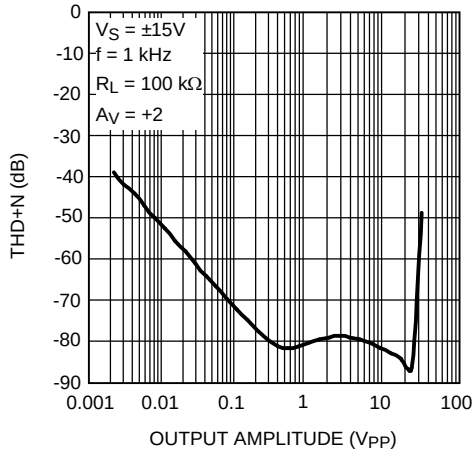


Figure 62.

Crosstalk Rejection vs. Frequency

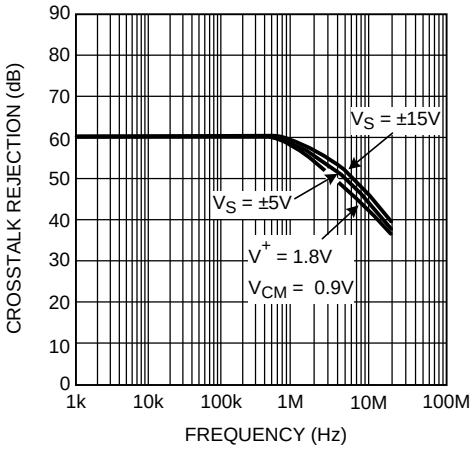


Figure 63.

APPLICATION INFORMATION

DRIVING CAPACITIVE LOADS

The LM7321/LM7321Q/LM7322/LM7322Q are specifically designed to drive unlimited capacitive loads without oscillations as shown in Figure 64.

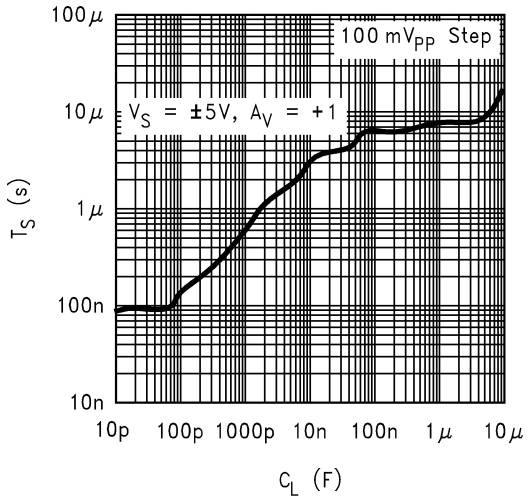


Figure 64. ±5% Settling Time vs. Capacitive Load

In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads as shown in Figure 65 and Figure 66.

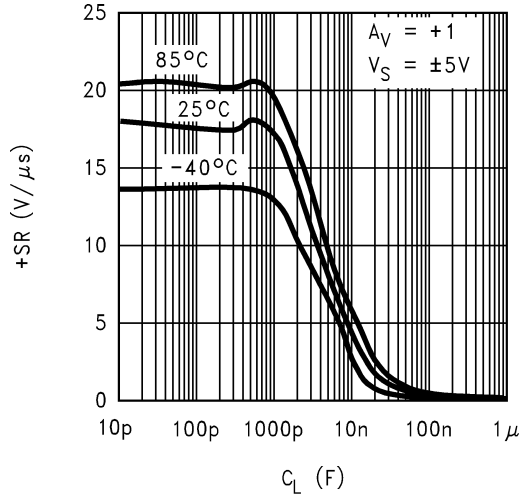


Figure 65. +SR vs. Capacitive Load

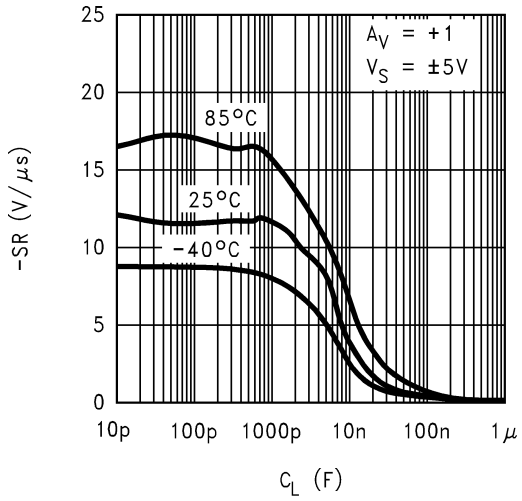


Figure 66. −SR vs. Capacitive Load

The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, etc.

However, as in most op amps, addition of a series isolation resistor between the op amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Slew Rate vs. Capacitive Load Plots (Typical Performance Characteristics section), two distinct regions can be identified. Below about 10,000 pF, the output Slew Rate is solely determined by the op amp's compensation capacitor value and available current into that capacitor. Beyond 10 nF, the Slew Rate is determined by the op amp's available output current. Note that because of the lower output sourcing current compared to the sinking one, the Slew Rate limit under heavy capacitive loading is determined by the positive transitions. An estimate of positive and negative slew rates for loads larger than 100 nF can be made by dividing the short circuit current value by the capacitor.

For the LM7321/LM7321Q/LM7322/LM7322Q, the available output current increases with the input overdrive. Referring to Figure 67 and Figure 68, Output Short Circuit Current vs. Input Overdrive, it can be seen that both sourcing and sinking short circuit current increase as input overdrive increases. In a closed loop amplifier configuration, during transient conditions while the fed back output has not quite caught up with the input, there will be an overdrive imposed on the input allowing more output current than would normally be available under steady state condition. Because of this feature, the op amp's output stage quiescent current can be kept to a minimum, thereby reducing power consumption, while enabling the device to deliver large output current when the need arises (such as during transients).

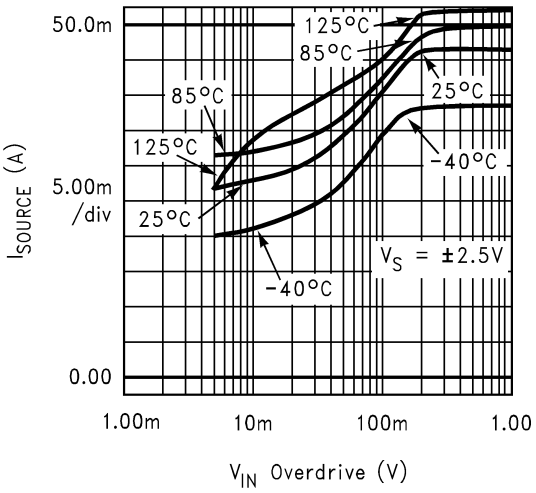


Figure 67. Output Short Circuit Sourcing Current vs. Input Overdrive

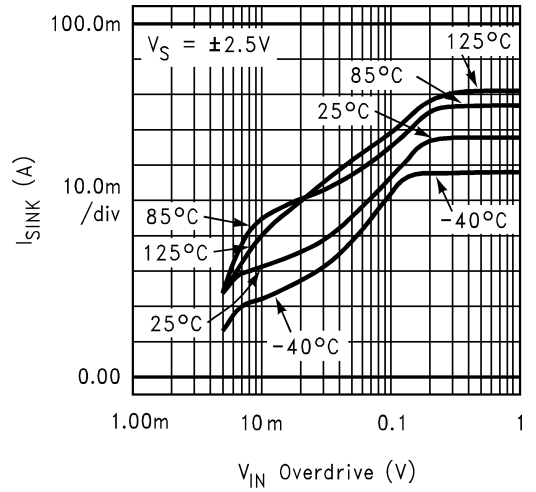


Figure 68. Output Short Circuit Sinking Current vs. Input Overdrive

Figure 69 shows the output voltage, output current, and the resulting input overdrive with the device set for A_V = +1 and the input tied to a 1 V_{PP} step function driving a 47 nF capacitor. As can be seen, during the output transition, the input overdrive reaches 1V peak and is more than enough to cause the output current to increase to its maximum value (see Figure 67 and Figure 68 plots). Note that because of the larger output sinking current compared to the sourcing one, the output negative transition is faster than the positive one.

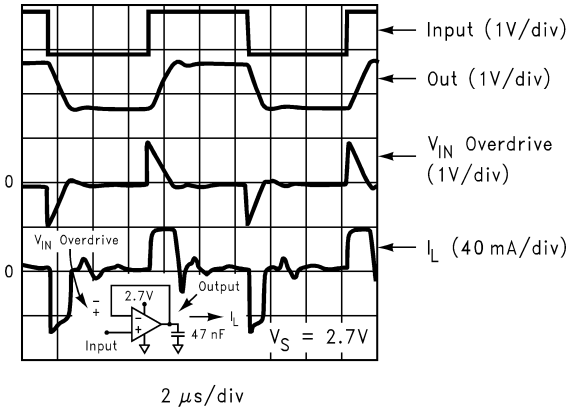


Figure 69. Buffer Amplifier Scope Photo

ESTIMATING THE OUTPUT VOLTAGE SWING

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, the Output Voltage vs. Output Current plot (Typical Performance Characteristics section) can be used to predict the output swing. Figure 70 and Figure 71 show this performance along with several load lines corresponding to loads tied between the output and ground. In each cases, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 1 kΩ load can accommodate an output swing to within 250 mV of V^- and to 330 mV of V^+ (V_S = ±15V) corresponding to a typical 29.3 V_{PP} unclipped swing.

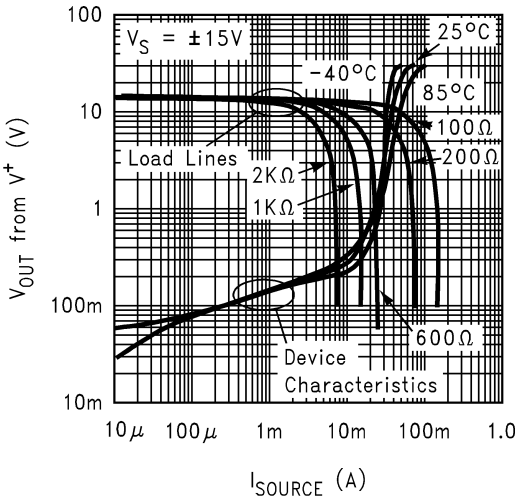


Figure 70. Output Sourcing Characteristics with Load Lines

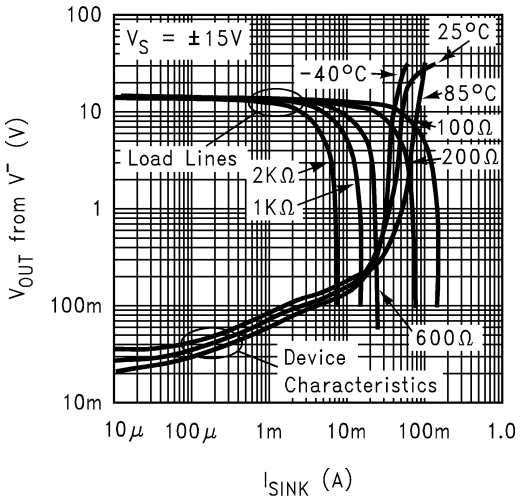


Figure 71. Output Sinking Characteristics with Load Lines

SETTLING TIME WITH LARGE CAPACITIVE LOADS

Figure 72 below shows a typical application where the LM7321/LM7321Q/LM7322/LM7322Q is used as a buffer amplifier for the V_{COM} signal employed in a TFT LCD flat panel:

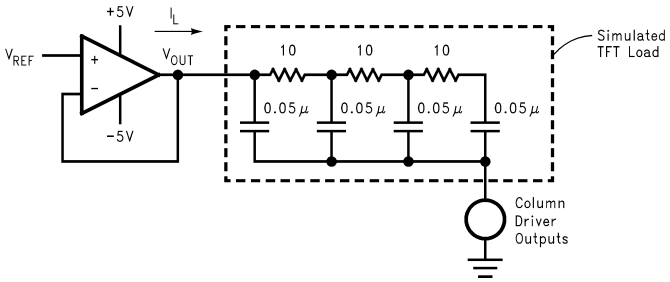


Figure 72. V_{COM} Driver Application Schematic

Figure 73 shows the time domain response of the amplifier when used as a V_{COM} buffer/driver with V_{REF} at ground. In this application, the op amp loop will try and maintain its output voltage based on the voltage on its non-inverting input (V_{REF}) despite the current injected into the TFT simulated load. As long as this load current is within the range tolerable by the LM7321/LM7321Q/LM7322/LM7322Q (45 mA sourcing and 65 mA sinking for ±5V supplies), the output will settle to its final value within less than 2 µs.

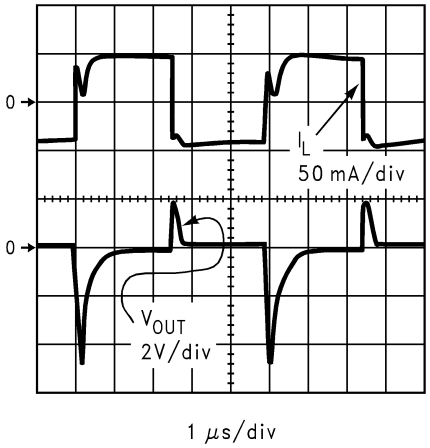


Figure 73. V_{COM} Driver Performance Scope Photo

OUTPUT SHORT CIRCUIT CURRENT AND DISSIPATION ISSUES

The LM7321/LM7321Q/LM7322/LM7322Q output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6V, the output short circuit condition can be tolerated indefinitely.

With the op amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the op amp operates in a single supply application where the output is maintained somewhere in the range of linear operation.

Therefore:

$P_{TOTAL} = P_Q + P_{DC} + P_{AC}$	
$P_Q = I_S \cdot V_S$	Op Amp Quiescent Power Dissipation
$P_{DC} = I_O \cdot (V_r - V_o)$	DC Load Power
P_{AC} = See Table 1	AC Load Power

where:

I_S: Supply Current

V_S: Total Supply Voltage ($V^+ - V^-$)

V_O: Average Output Voltage

V_r: V^+ for sourcing and V^- for sinking current

Table 1 shows the maximum AC component of the load power dissipated by the op amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} ($W.\Omega/V^2$)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/R_L. To figure out the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/R_L. For example, with ±12V supplies, a 600Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot (242/600) = 45.0 \text{ mW} \quad (1)$$

The maximum power dissipation allowed at a certain temperature is a function of maximum die junction temperature ($T_{J(MAX)}$) allowed, ambient temperature T_A, and package thermal resistance from junction to ambient, θ_{JA}.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (2)$$

For the LM7321/LM7321Q/LM7322/LM7322Q, the maximum junction temperature allowed is 150°C at which no power dissipation is allowed. The power capability at 25°C is given by the following calculations:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{235℃/W} = 0.53W \quad (3)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 25℃}{165℃/W} = 0.76W \quad (4)$$

Similarly, the power capability at 125°C is given by:

For VSSOP package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{235℃/W} = 0.11W \quad (5)$$

For SOIC package:

$$P_{D(MAX)} = \frac{150℃ - 125℃}{165℃/W} = 0.15W \quad (6)$$

Figure 74 shows the power capability vs. temperature for VSSOP and SOIC packages. The area under the maximum thermal capability line is the operating area for the device. When the device works in the operating area where P_{TOTAL} is less than $P_{D(MAX)}$, the device junction temperature will remain below 150°C. If the intersection of ambient temperature and package power is above the maximum thermal capability line, the junction temperature will exceed 150°C and this should be strictly prohibited.

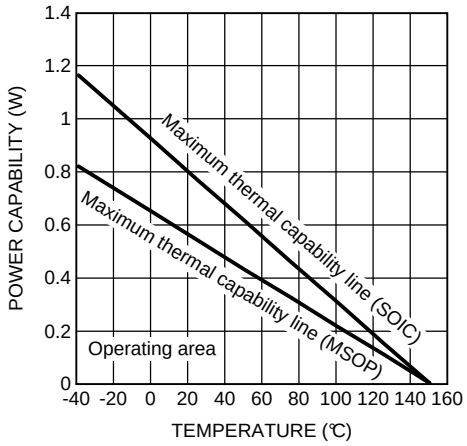


Figure 74. Power Capability vs. Temperature

When high power is required and ambient temperature can't be reduced, providing air flow is an effective approach to reduce thermal resistance therefore to improve power capability.

Other Application Hints

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01 µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the op amp output. The combination of these capacitors will provide supply decoupling and will help keep the op amp oscillation free under any load.

SIMILAR HIGH OUTPUT DEVICES

The LM7332 is a dual rail-to-rail amplifier with a slightly lower GBW capable of sinking and sourcing 100 mA. It is available in SOIC and VSSOP packages.

The LM4562 is dual op amp with very low noise and 0.7 mV voltage offset.

The LME49870 and LME49860 are single and dual low noise amplifiers that can work from ±22 volt supplies.

OTHER HIGH PERFORMANCE SOT-23 AMPLIERS

The LM7341 is a 4 MHz rail-to-rail input and output part that requires only 0.6 mA to operate, and can drive unlimited capacitive load. It has a voltage gain of 97 dB, a CMRR of 93 dB, and a PSRR of 104 dB.

The LM6211 is a 20 MHz part with CMOS input, which runs on ±12 volt or 24 volt single supplies. It has rail-to-rail output and low noise.

The LM7121 has a gain bandwidth of 235 MHz.

Detailed information on these parts can be found at www.ti.com.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM7321MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM732 1MA	Samples
LM7321MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM732 1MA	Samples
LM7321MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU4A	Samples
LM7321MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU4A	Samples
LM7321MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AU4A	Samples
LM7321QMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AR8A	Samples
LM7321QMFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AR8A	Samples
LM7321QMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AR8A	Samples
LM7322MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM732 2MA	Samples
LM7322MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM732 2MA	Samples
LM7322MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AZ4A	Samples
LM7322MME/NOPB	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AZ4A	Samples
LM7322MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AZ4A	Samples
LM7322QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM732 2QMA	Samples
LM7322QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM732 2QMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF LM7321, LM7321-Q1, LM7322, LM7322-Q1 :

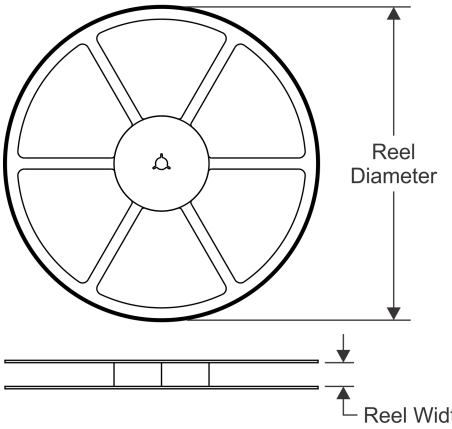
- Catalog: LM7321, LM7322
- Automotive: LM7321-Q1, LM7322-Q1

NOTE: Qualified Version Definitions:

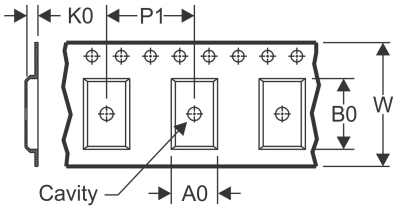
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

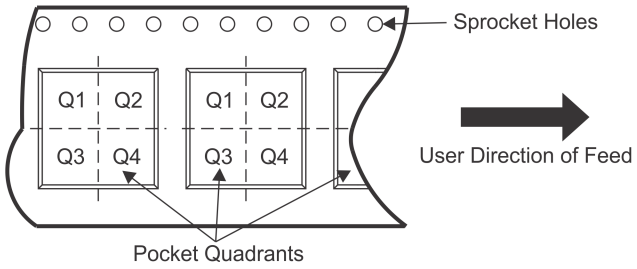


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

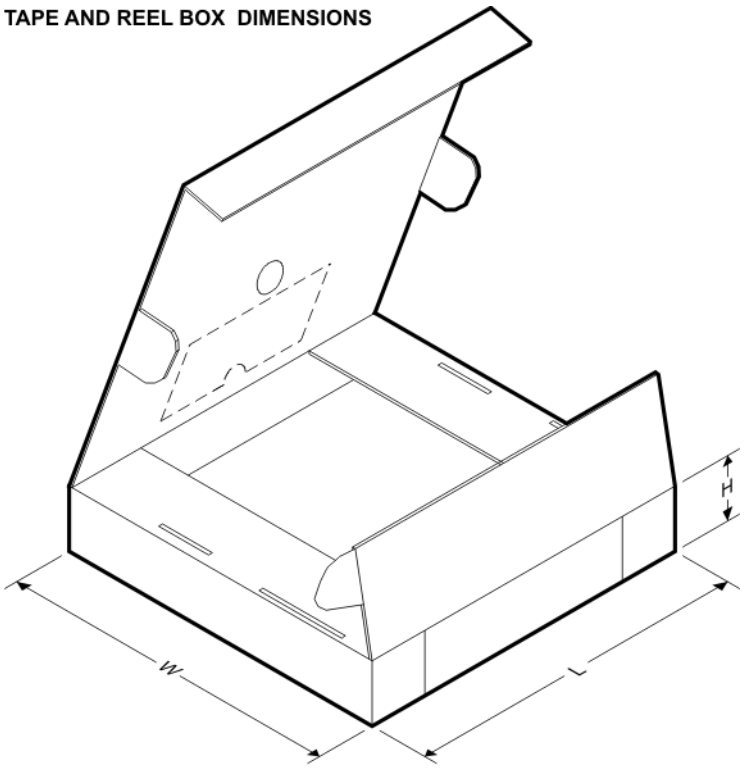
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7321MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7321MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321QMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321QMFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7322MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM7322MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7322MME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7322MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM7322QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

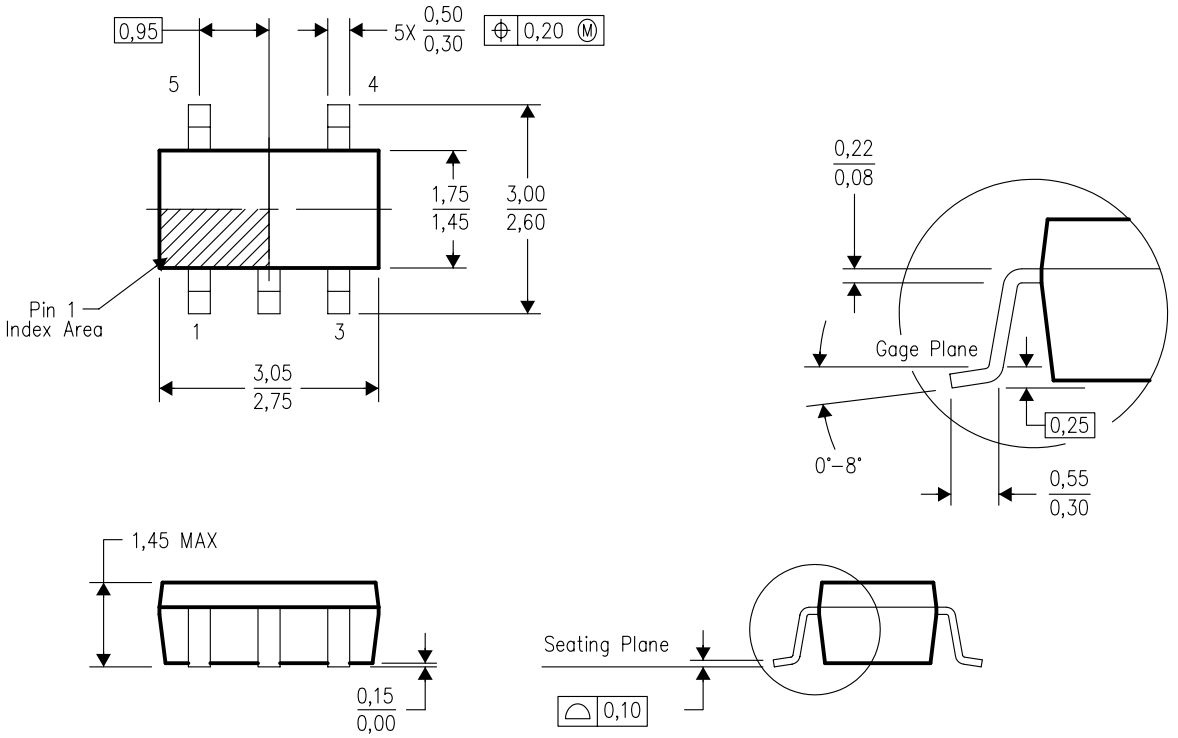
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7321MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7321MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7321MFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LM7321MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7321QMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7321QMFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LM7321QMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM7322MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM7322MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM7322MME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LM7322MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM7322QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

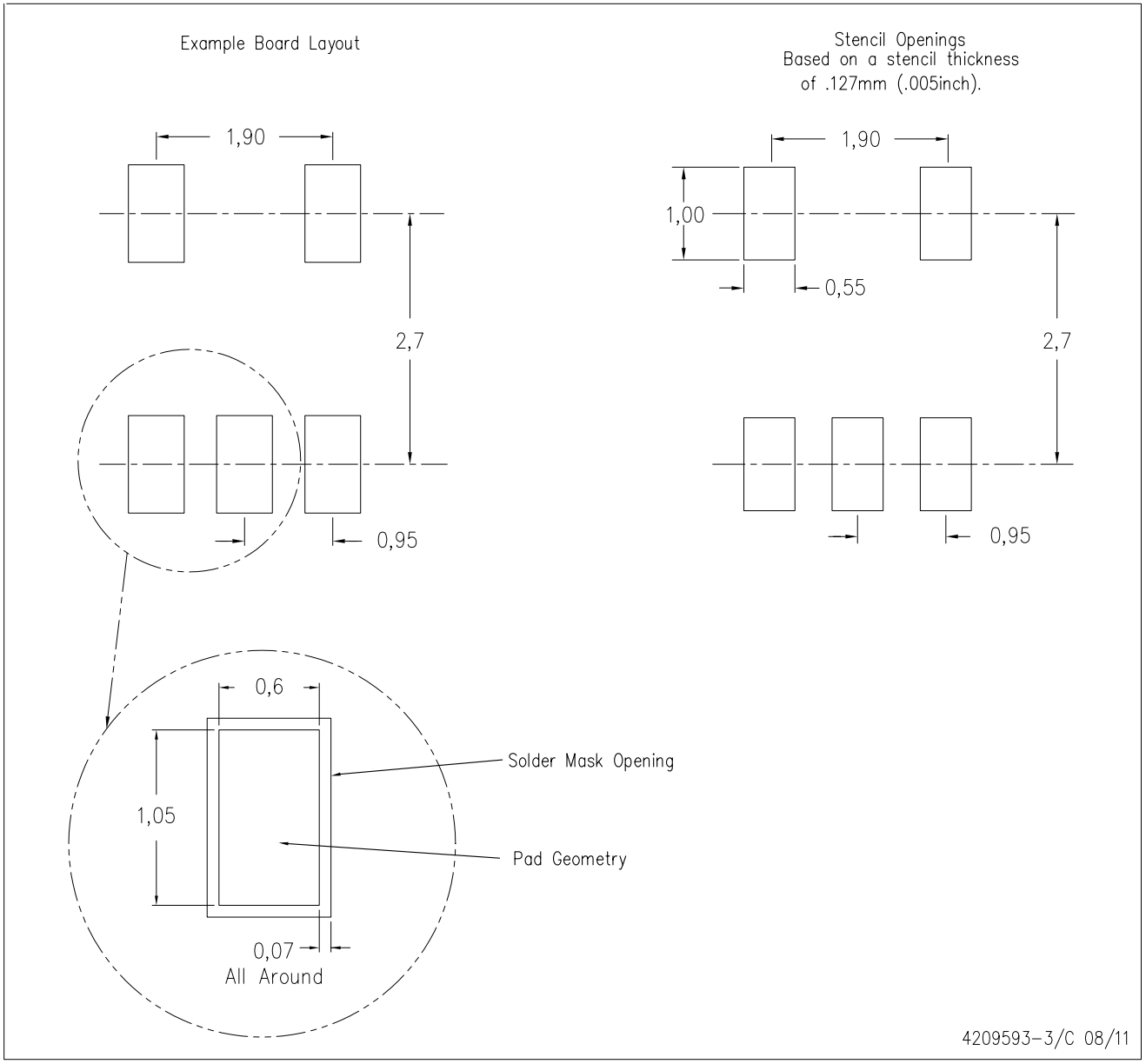
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

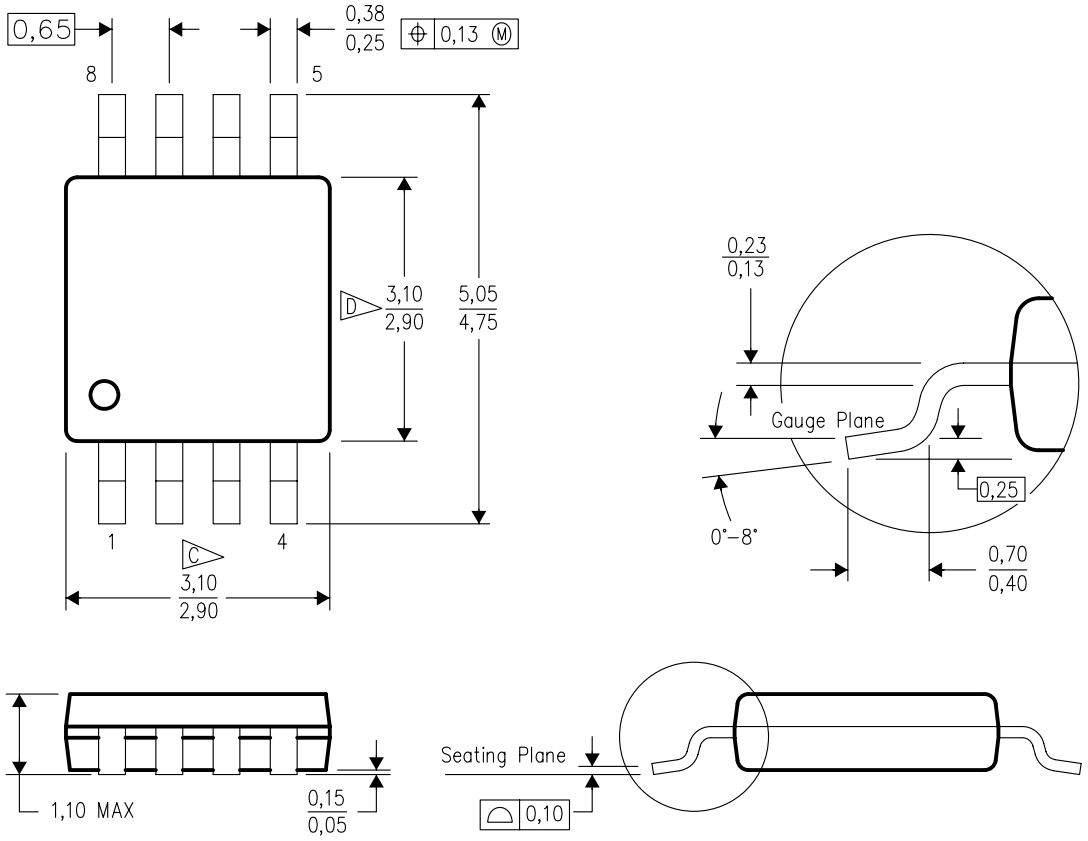
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

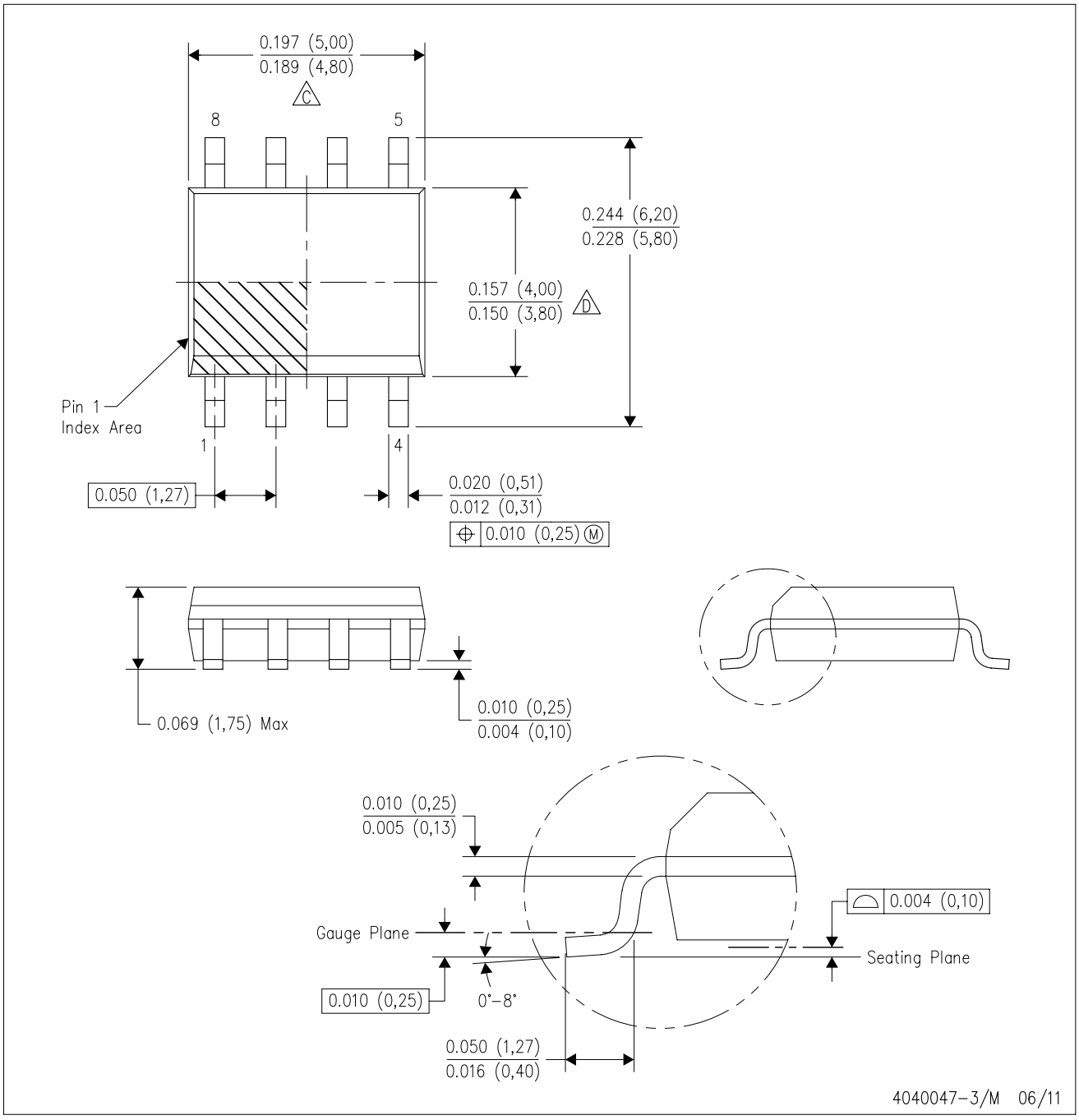
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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