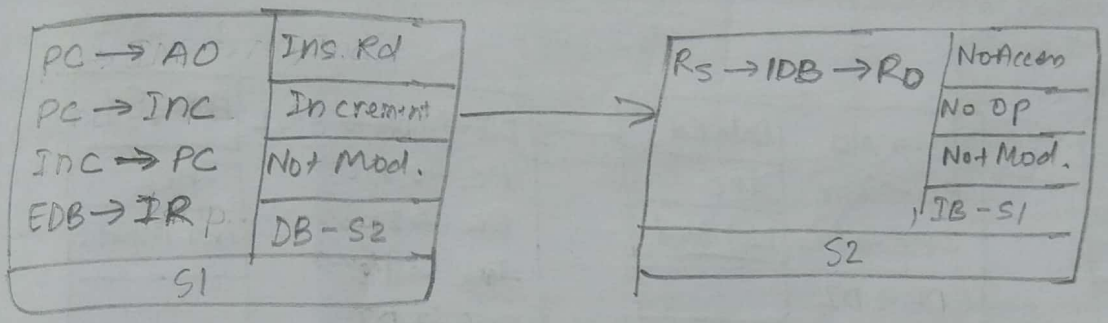
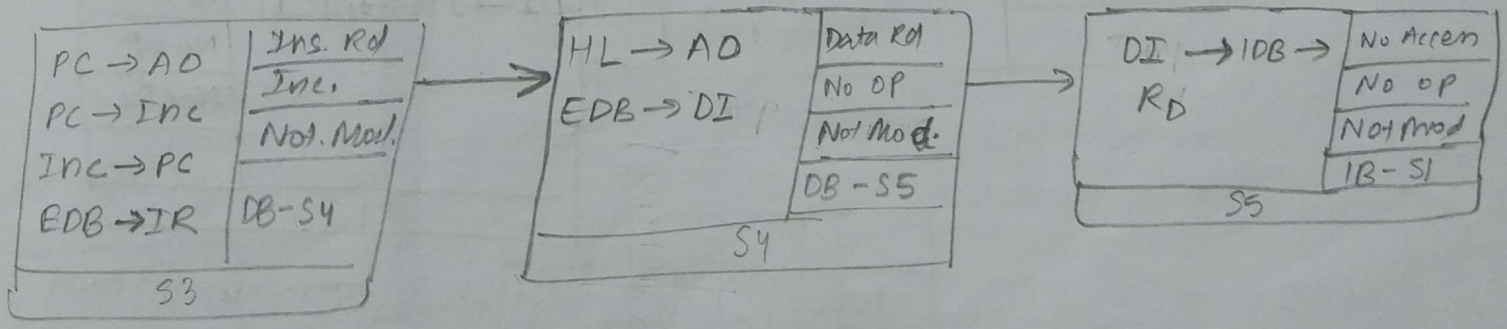
(1) MOV Rd, Rs

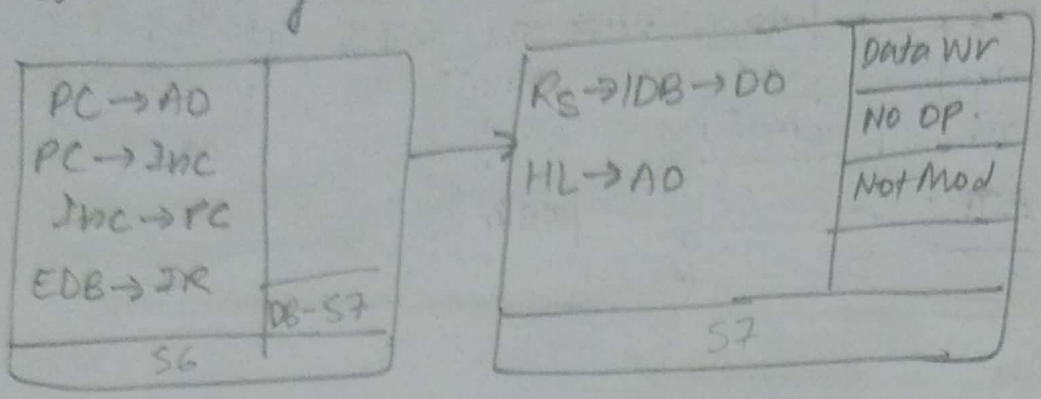
Temp ≡ DI



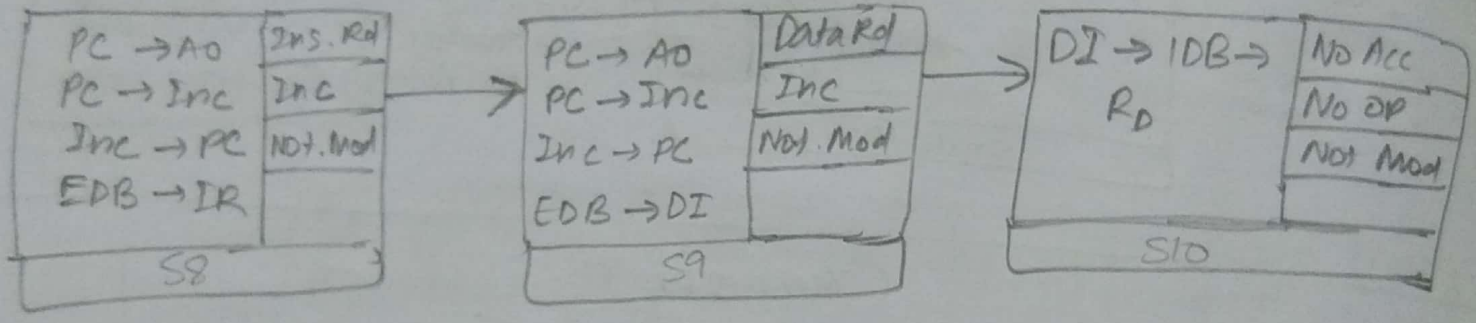
(2) MOV Rd, M



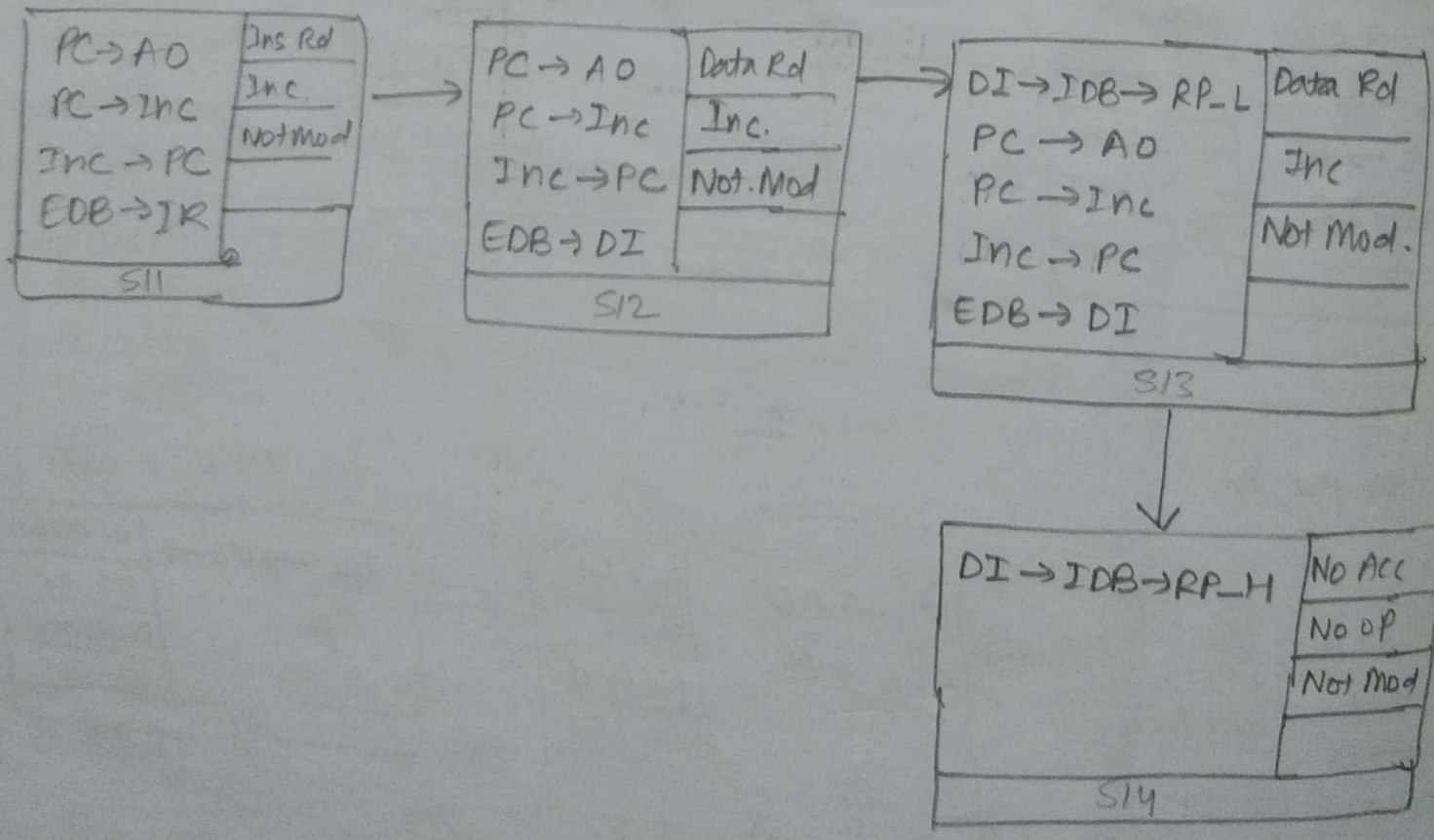
3) MOV M, Rg



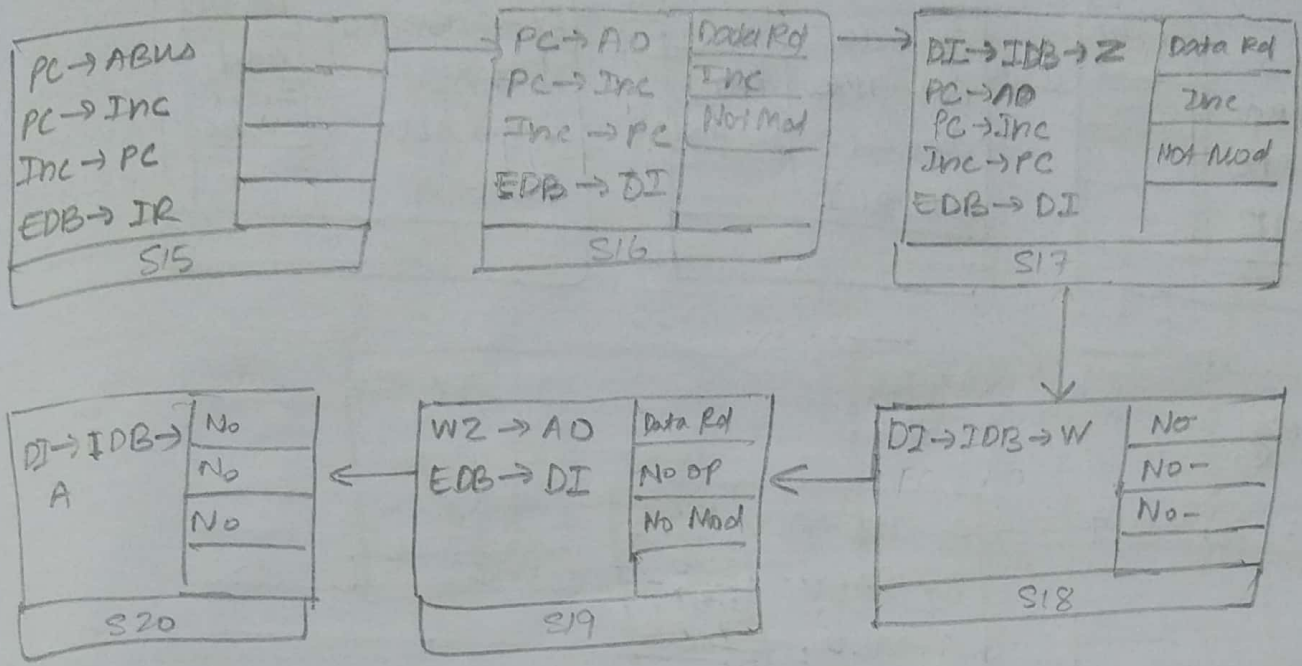
(4) MVI Rd, D08



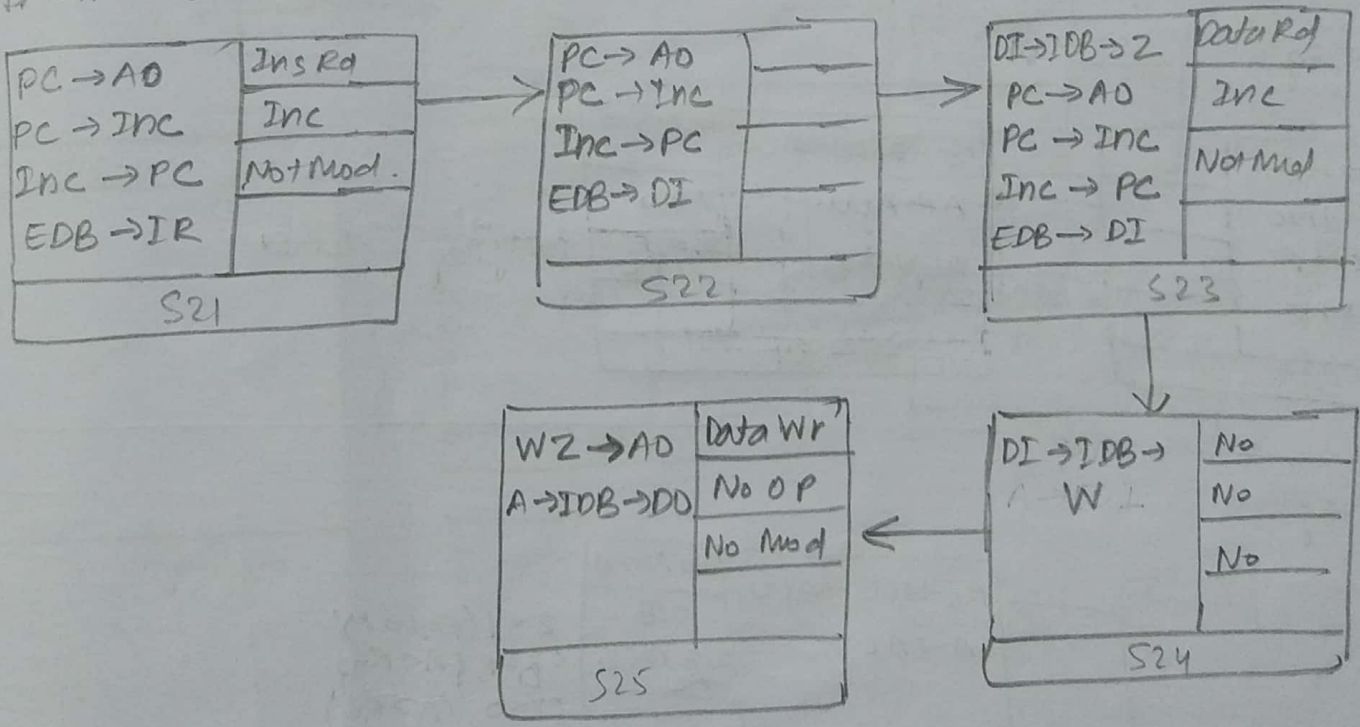
(5) LXI Rp/SP D16



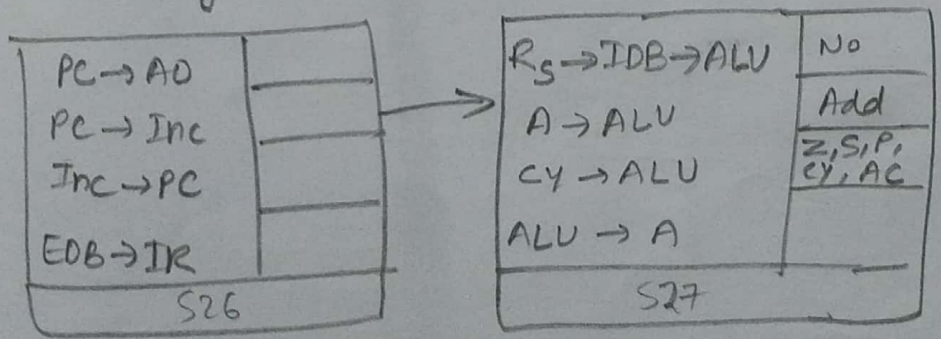
(6) LDA D16



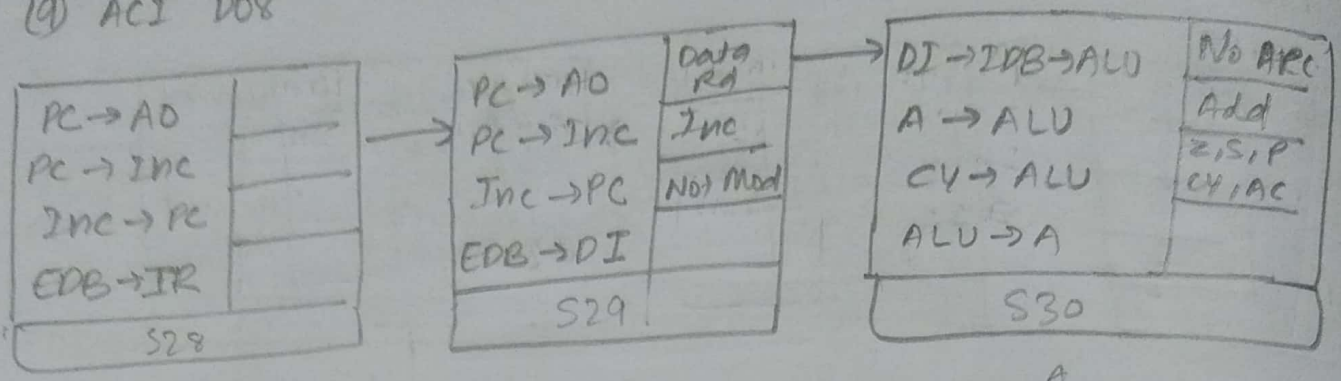
(7) STA D16



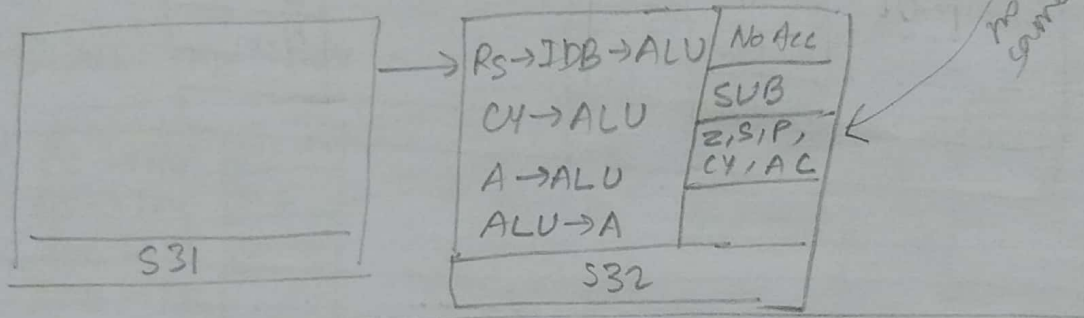
(8) ADC Rg



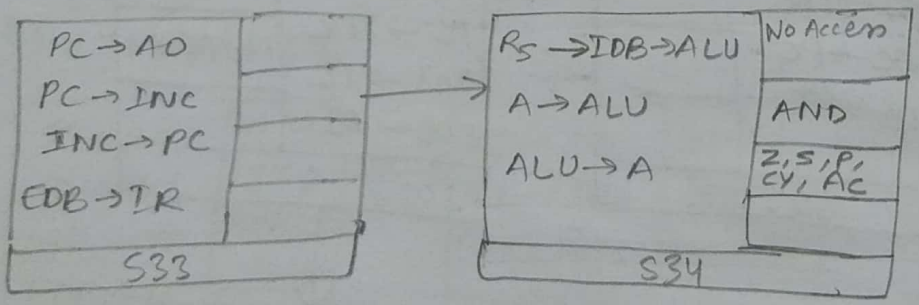
(9) ACI D08



(10) SBB Rg

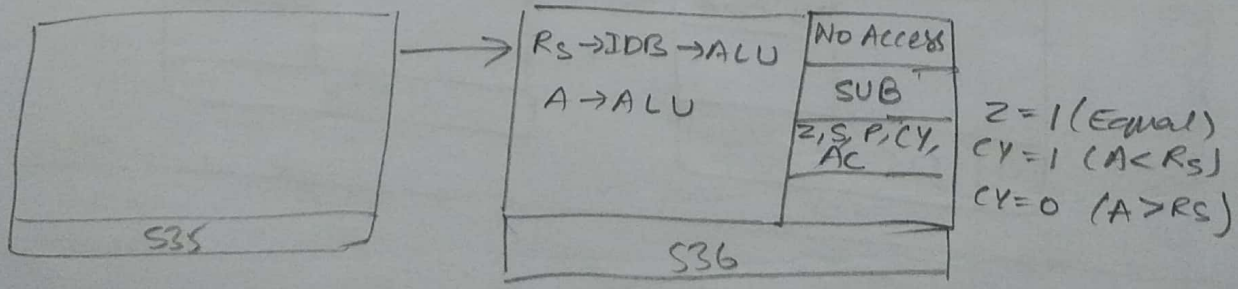


(11) ANA Rg.



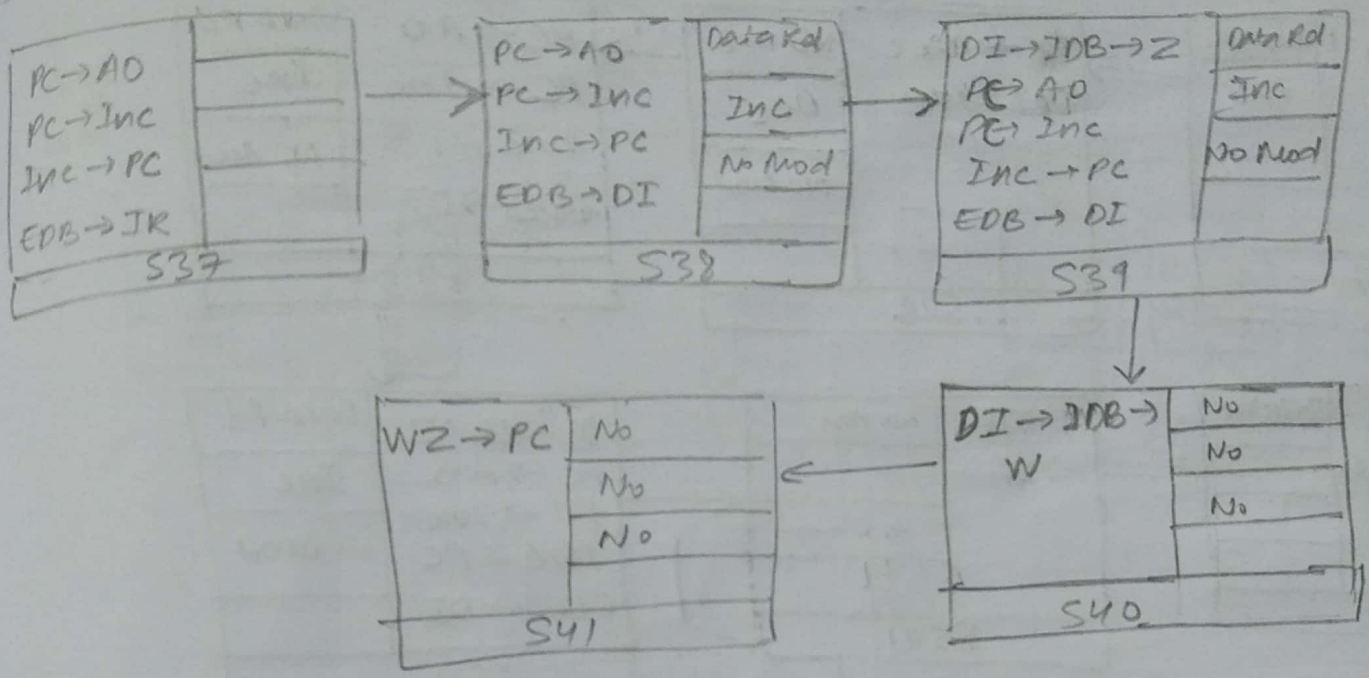
Carry flag is cleared.

(12) CMP Rg

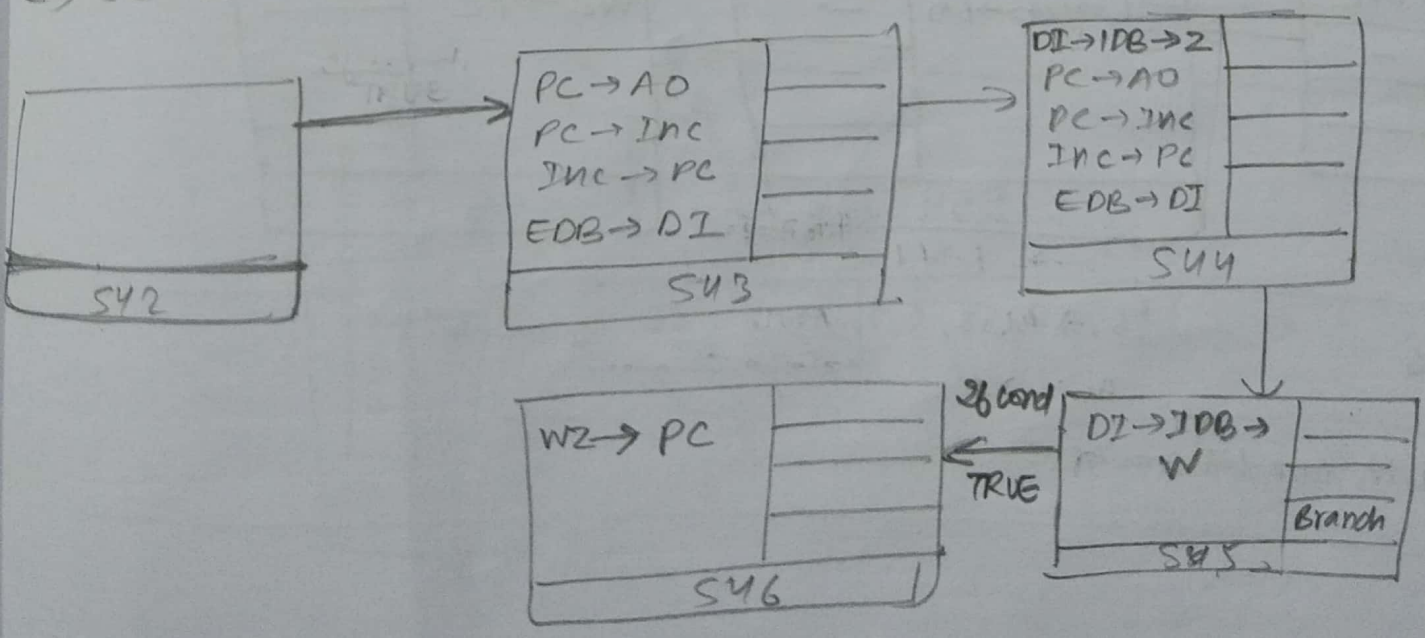


Z = 1 (Equal)
CY = 1 (A < Rs)
CY = 0 (A > Rs)

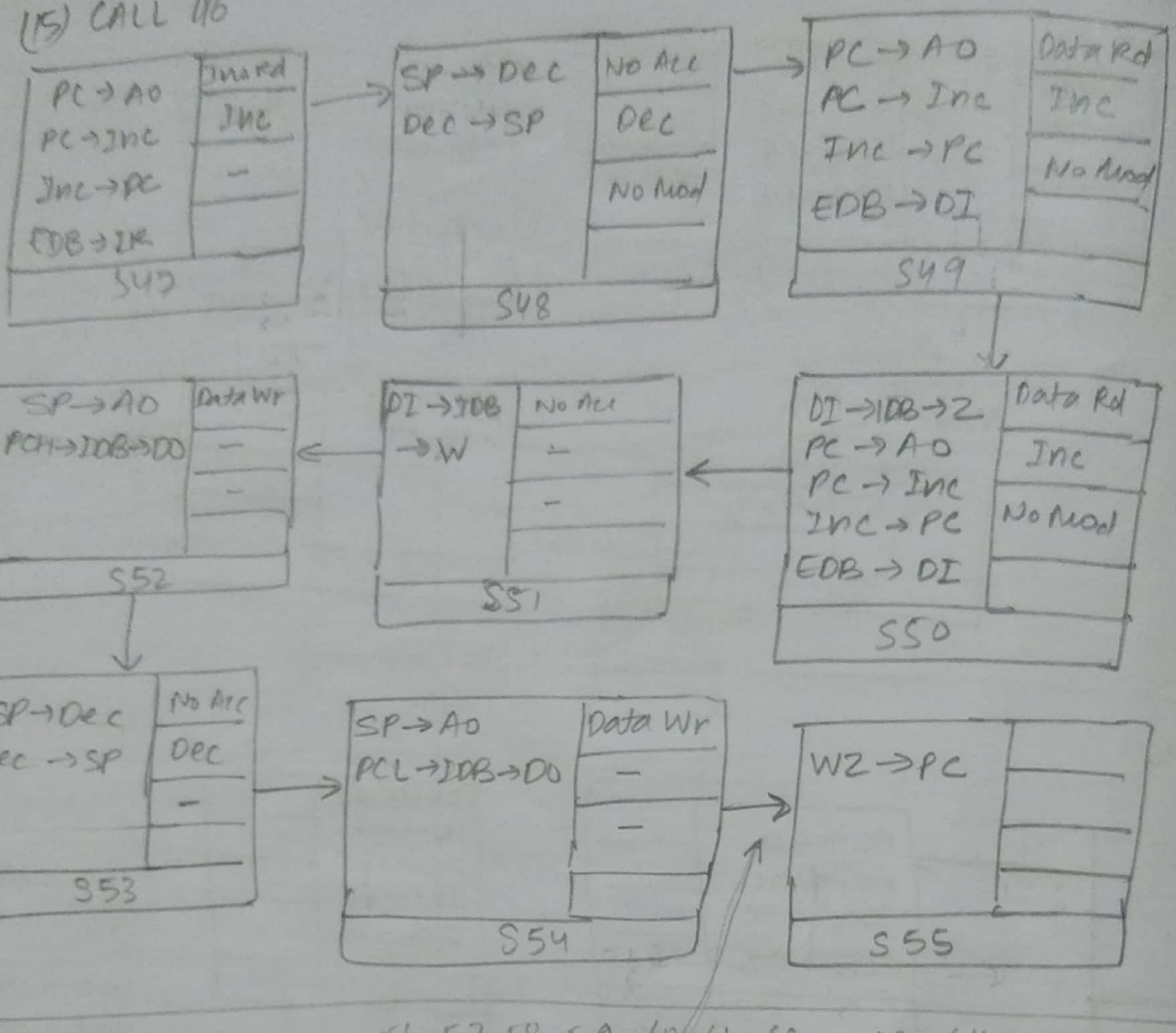
(13) JMP D16



(14) JC D16



(15) CALL D16

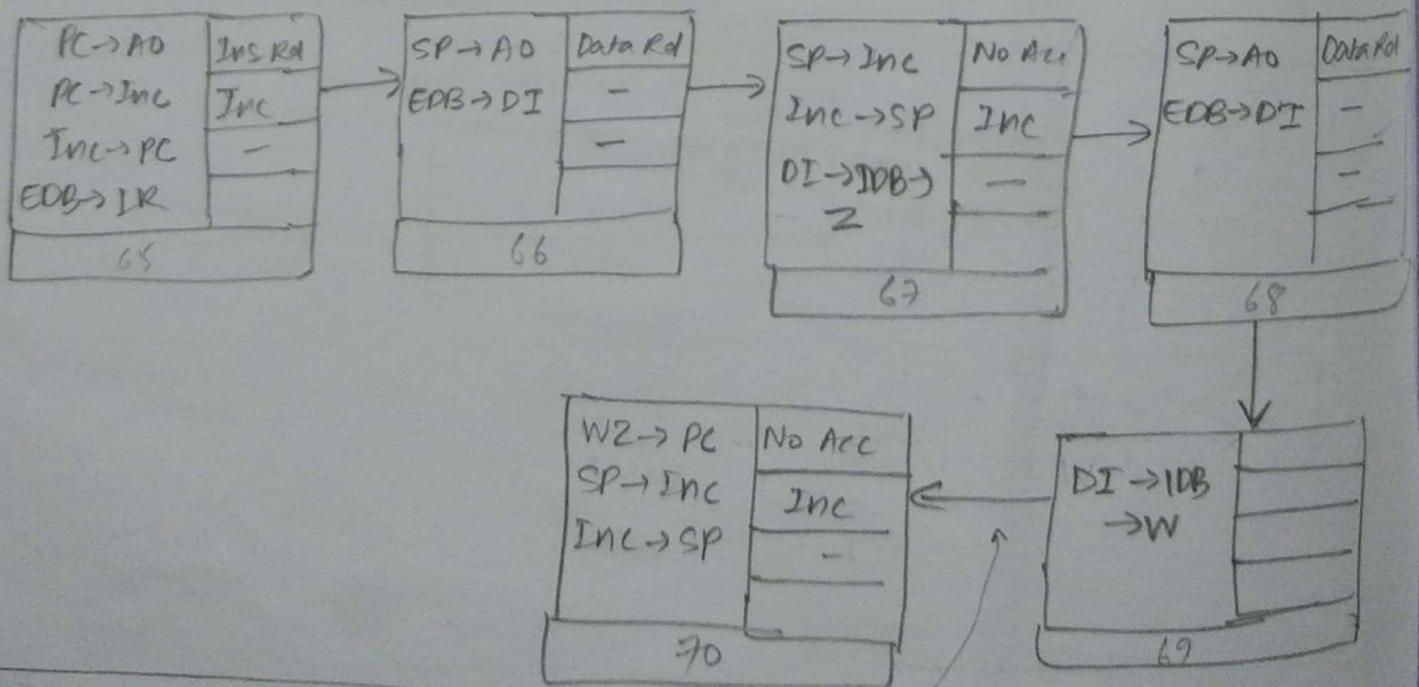


56, 57, 58, 59, 60, 61, 62, 63, 64

(16) CZ D16

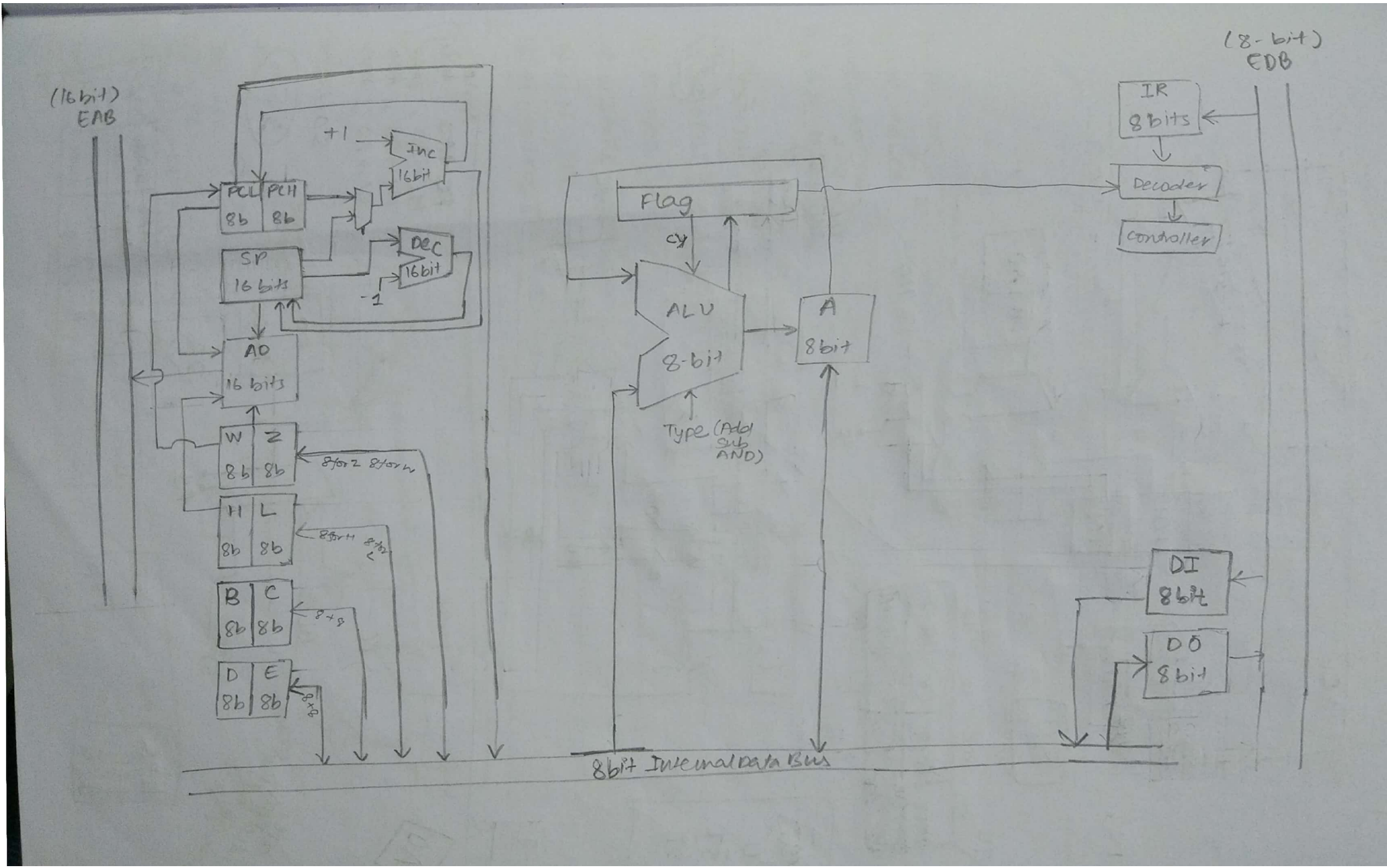
Same with condition = TRUE

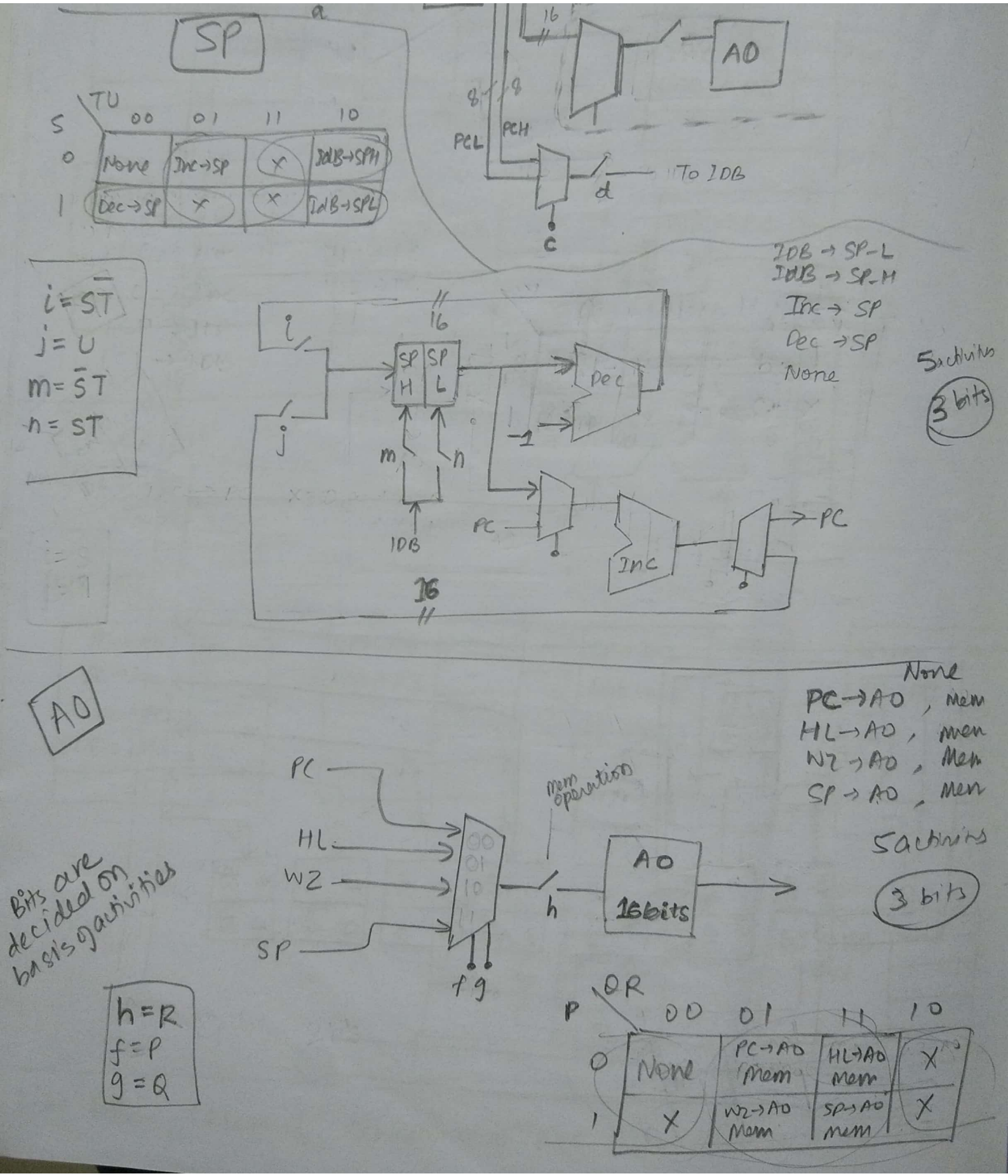
(17) RET



(18) RZ Check if condition = TRUE.

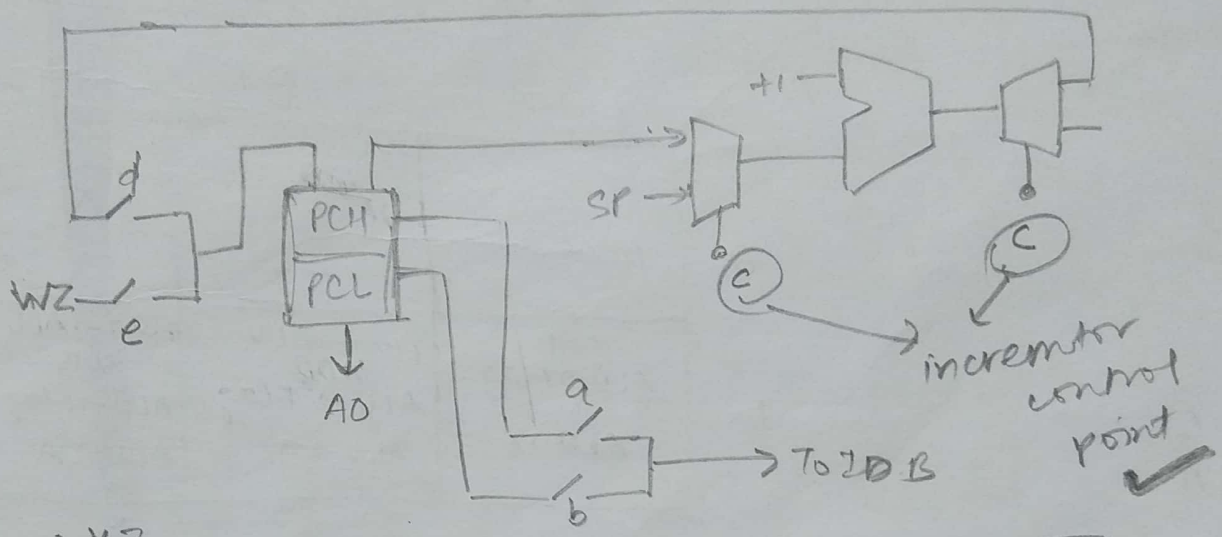
71, 72, 73, 74, 75, 76


(16 bit)
EAB
(8-bit)
EDB
+1
Inc
16bit
PCL
PCH
8b
8b
DEC
16bit
SP
16 bits
-1
AD
16 bits
W
Z
H
L
B
C
D
E
Flag
CY
ALU
8-bit
A
8bit
Type (Add Sub AND)
IR
8bits
Decoder
Controller
DI
8bit
DO
8bit
8bit Internal Data Bus


SP
a
TU
S
00
01
11
10
0
None
Inc→SP
x
IDB→SPH
1
Dec→SP
x
x
IDB→SPL
16
AO
8
8
PCL
PCH
To IDB
d
c
i = S T̄
j = U
m = S̄ T
n = ST
i
j
16
SP H
SP L
m
n
IDB
Dec
1
PC
Inc
PC
16
IDB → SP-L
IDB → SP-H
Inc → SP
Dec → SP
None
5 activities
3 bits

AO
None
PC→AO, Mem
HL→AO, Mem
WZ→AO, Mem
SP→AO, Mem
5 activities
3 bits
PC
HL
WZ
SP
mem operation
00
01
10
11
h
AO
16bits
f g
Bits are decided on basis of activities
h = R
f = P
g = Q
P
OR
00
01
11
10
0
None
PC→AO Mem
HL→AO Mem
X
1
X
WZ→AO Mem
SP→AO Mem
X

PC



none ?

Inc → PC
WZ → PC
PCH → idb
PCL → idb

Sachintha
3 bits

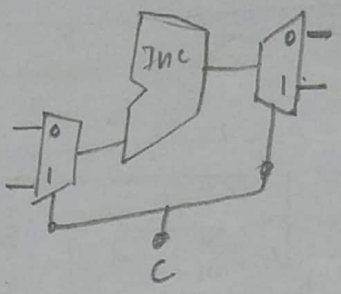
X \ YZ	00	01	11	10
0	None	Inc→PC	x	PCH→idb
1	WZ→PC	x	x	PCL→idb

$d = Z$ $\quad e = X\bar{Y}$

$a = \bar{X}Y$ $\quad b = XY$

INC

1 bit → C



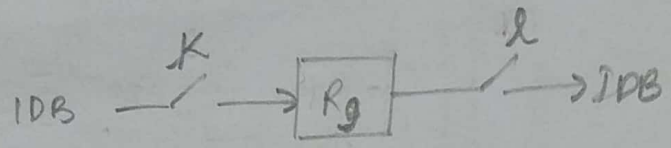
1 bit

Rg

includes Accumulator

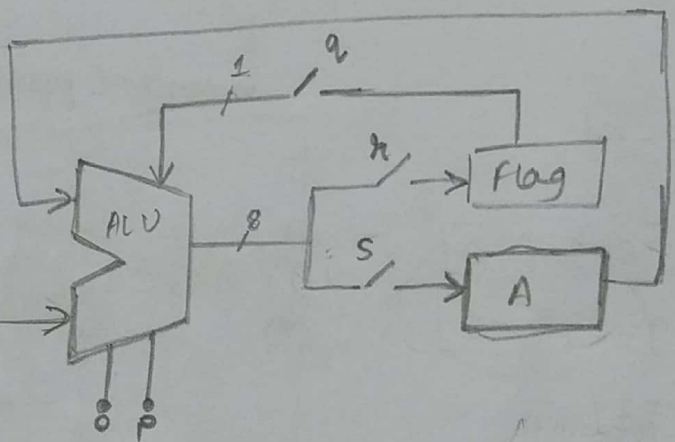
K = A
L = B

Read write none



3 actions
2 bits

ALU



ADC ACI Flag → ALU Add ALU → Flag ALU → A
SBB Flag → ALU Sub ALU → Flag ALU → A
ANA AND ALU → Flag ALU → A
CMP Sub ALU → Flag
None

5 actions
3 bits

q = A
r = C
S x

q = C
r = A
S =

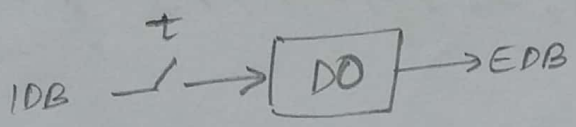
A \ BC	00	01	11	10
0	None	X	X	X
1	AND ALU → Flag ALU → A	Flag → ALU ADD ALU → Flag ALU → A	Flag → ALU SUB ALU → Flag ALU → A	SUB ALU → Flag

A \ BC	00	01	11	10
0	None	SUB ALU→Flag	AND ALU→Flag ALU→A	X
1	X	Flag→ALU SUB ALU→Flag ALU→A	Flag→ALU ADD ALU→Flag ALU→A	X

q = A
r = C
s = A+B

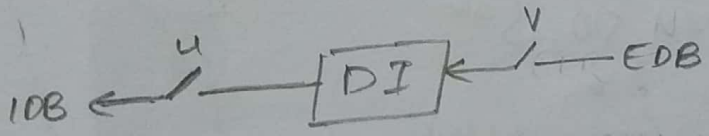
t=F

DO



1 Bit

DI



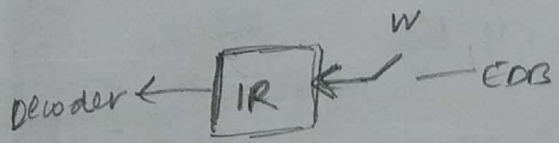
EDB → DI
DI → IDB
None

D \ E	0	1
0	None	DI→IDB
1	EDB→DI	X

u = E V = D

2 Bits

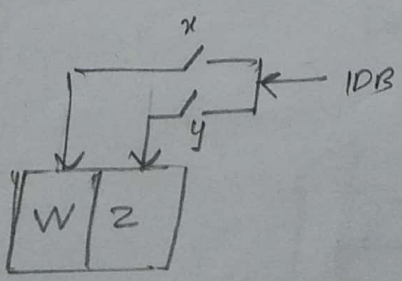
IR



W = G

1 Bit

WZ



3 Activities

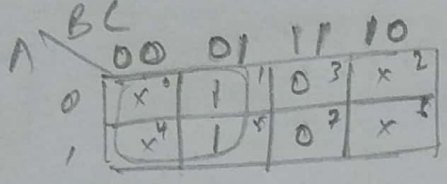
x = H

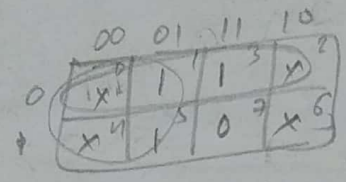
Y = I

2 Bits

00 - ADD
01 - AND
11 - Sub
o p

A	B	C	O	P
0	0	1	1	1
1	0	1	1	1
0	1	1	0	1
1	1	1	0	0





$O = \bar{B}$; $P = \bar{A} + \bar{B}$

Compatible

→ 1, 3, 6, 8, 11, 15, 21, 26, 28, 31, 33, 35, 37, 42, 47, 56, 65, 71

→ 5, 10 (Eq)

→ 9, 12, 16, 22, 38, 43, 49, 58

→ 17, 23 (Equivalent) 39, 44, 50, 59

→ 18, 24, 40, 45, 51, 60, 69 (compatible)

→ 41, 46, 55, 64 (Equivalent)

→ 48, 57 (Eq.)

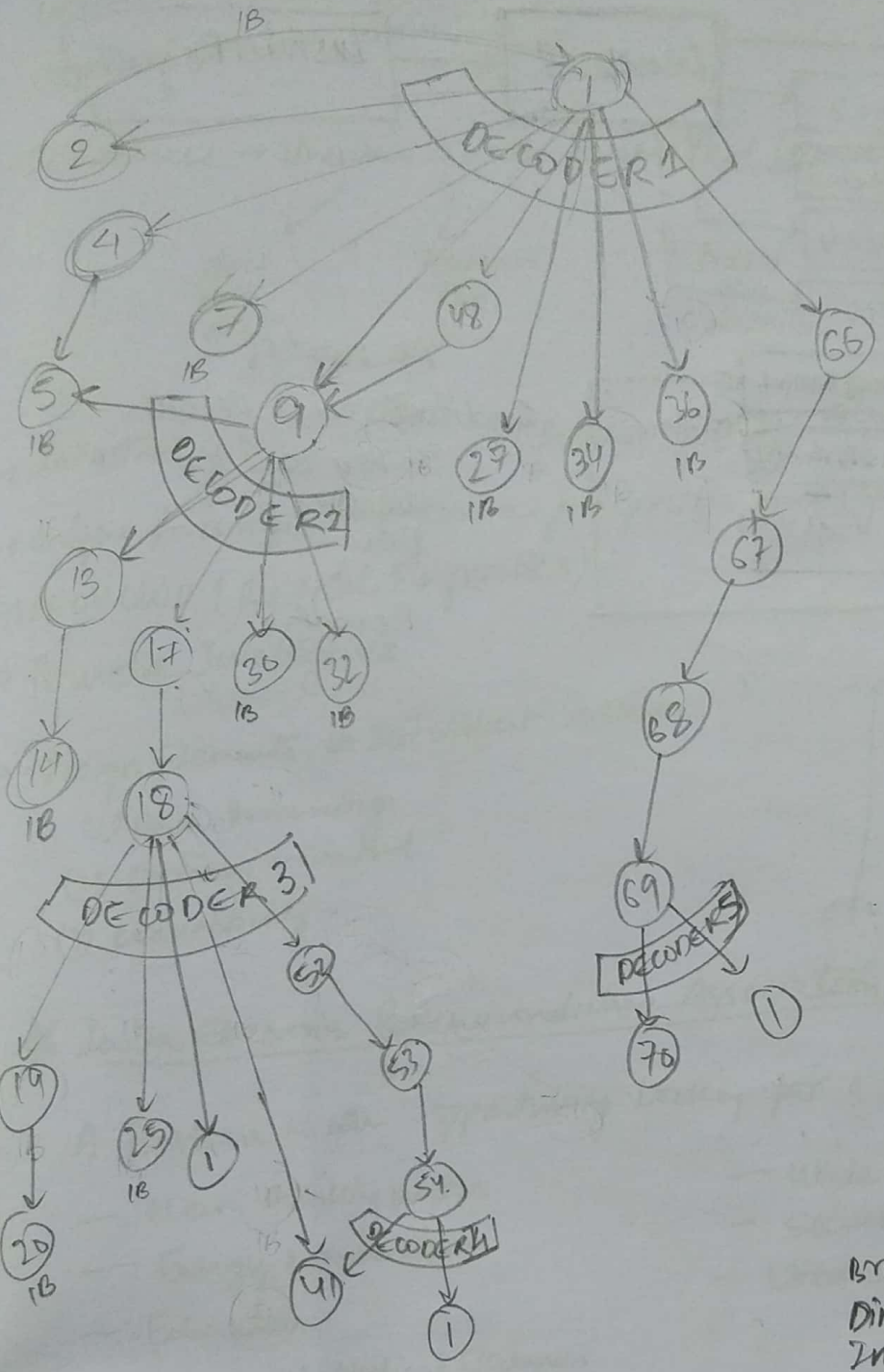
→ 52, 61 (Eq.)

→ 53, 62

→ 54, 63

→ 66, 72 → 67, 73 → 68, 74 → 69, 75 (compat.)

→ 70, 76



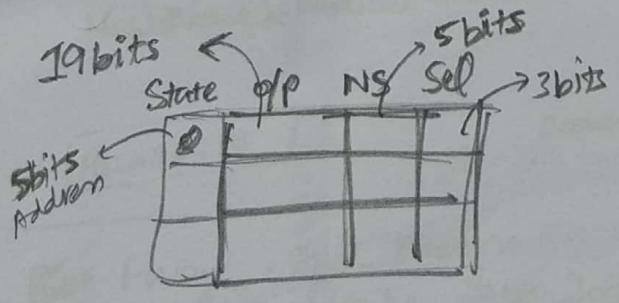
48 22 34 36

52
53
54

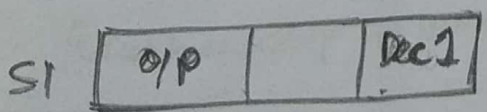
25 1B
41 1B
1

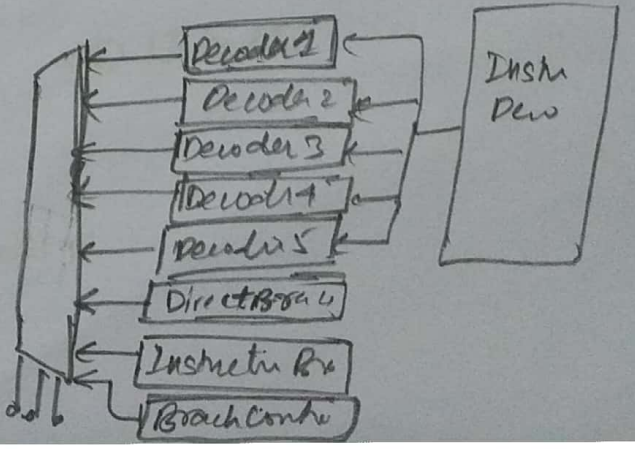
28 States (5 bits)

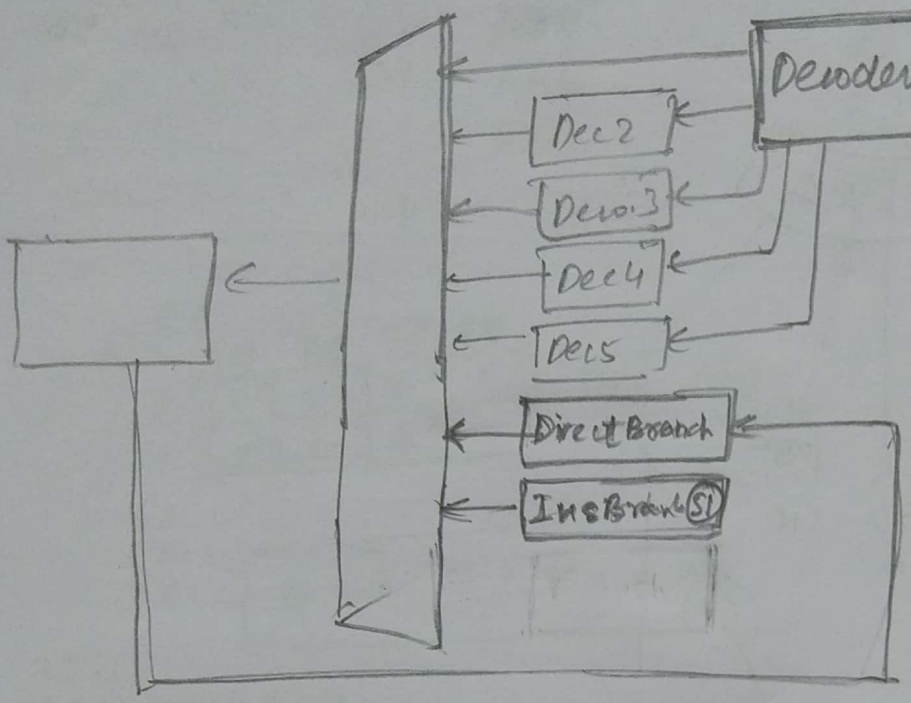
5 Decoders



Branch Control
Direct Branch
Instruction Branch
Decoder 1
Decoder 2
Decoder 3
Decoder 4
Decoder 5







No need of
Conditional Branch Decoder
Taken care by
Decoder 3
Decoder 4
&
Decoder 5.