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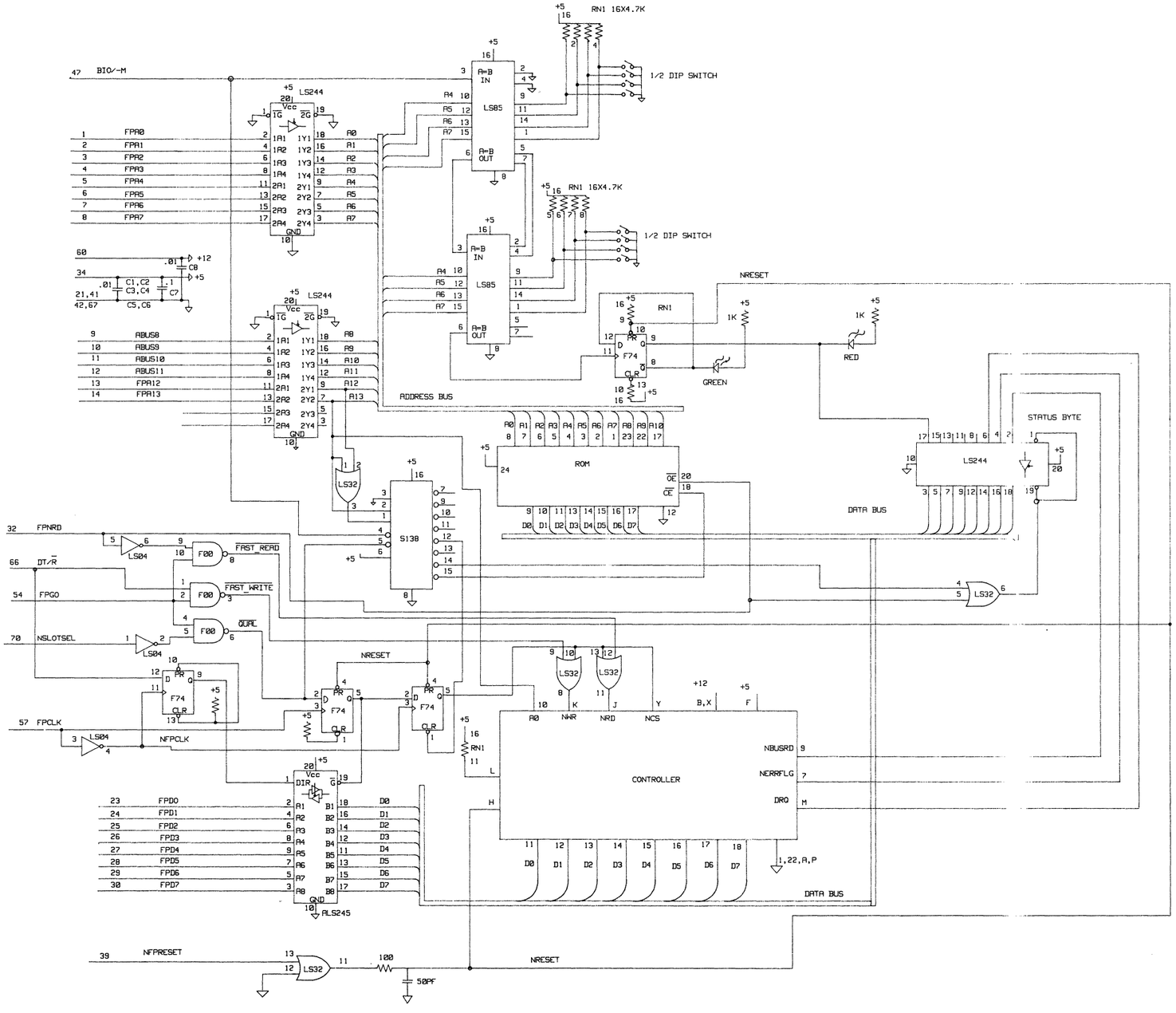


Figure 3-31. Typical Accessory Card Schematic

MEMORY AND I/O MAPPING

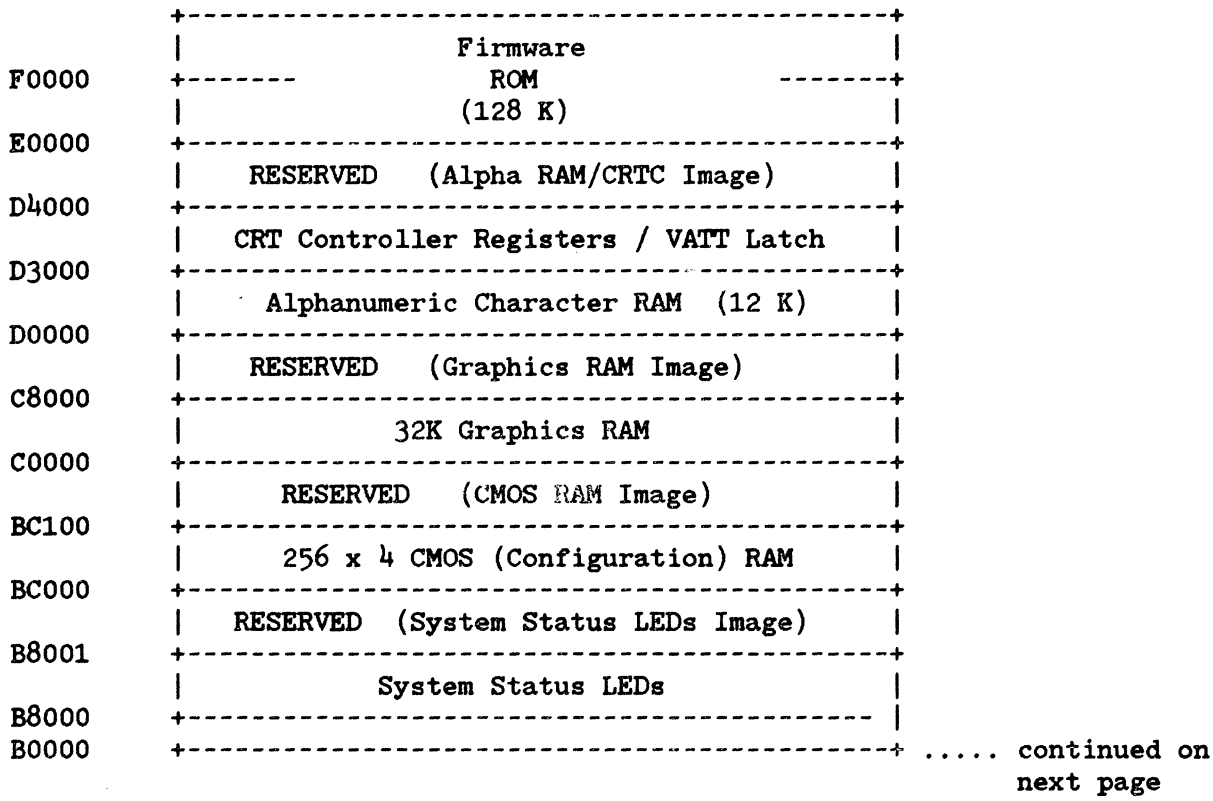
SECTION 4

This section contains memory and input/output maps for the HP 150 memory and input/output address spaces. Included is information describing the register and bit mappings of all devices which consume a portion of the 8088 processor's address space for both memory and input/output instruction types. More information regarding the functionality of the devices themselves may be found in Section 3, Hardware Subsystems.

CONTENTS

MEMORY MAPPED DEVICES

HP 150 Memory Map



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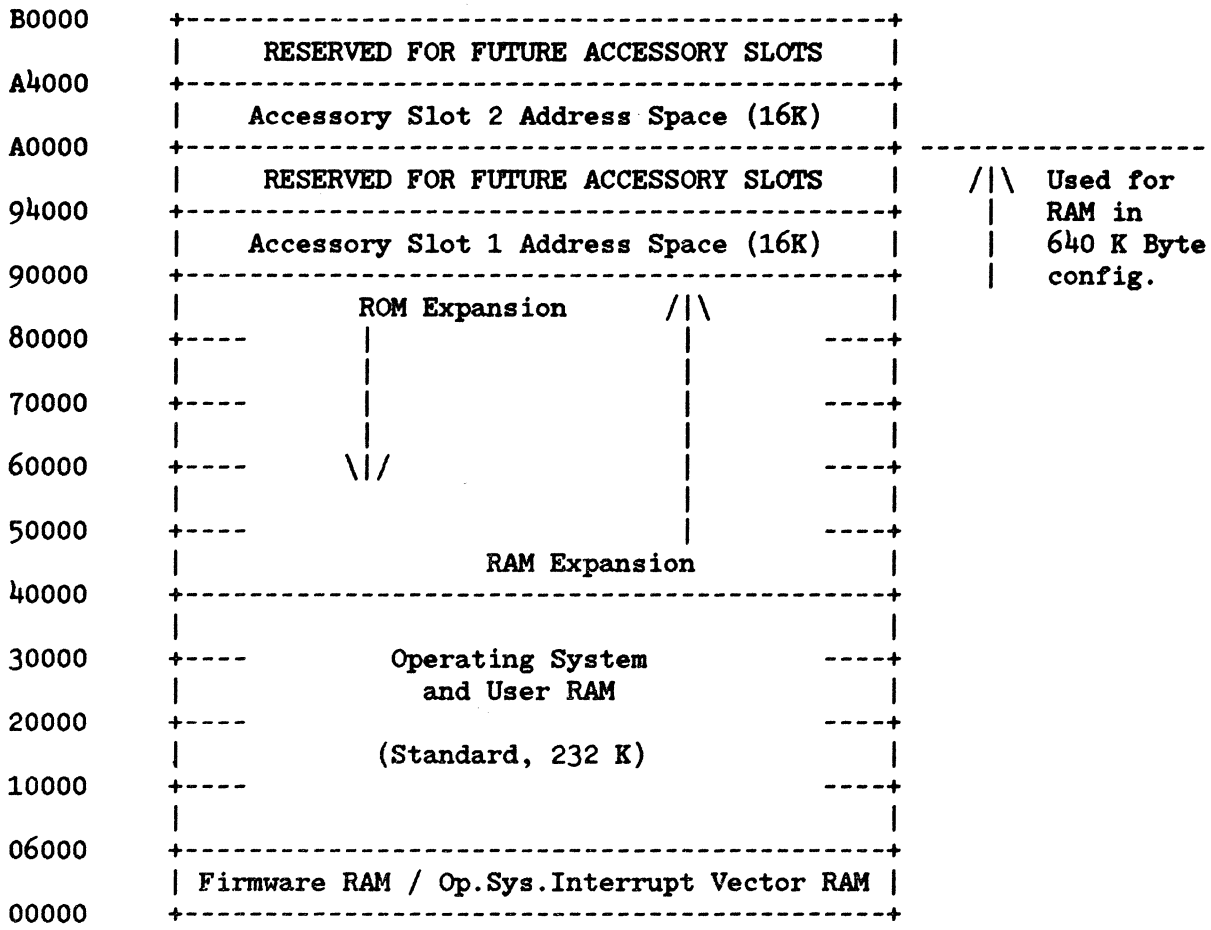
HP 150 Memory Map continued



NOTE

For a more detailed map of Operating System, User, and Firmware RAM useage, refer to System Software (Section 5), Operating System Memory Map.

CRT Controller Registers

Register Type / Bit Definition D7	D6	D5	D4	D3	D2	D1	D0	Register #	Initialization Register Data (hex)	8088-Addr (hex)	Read/Write
MSB	CHARS./HORIZONTAL PERIOD						LSB	R0 #	73	D3000	WRITE
MSB	CHARACTERS/ DATA ROW						LSB	R1 #	*4F	D3002	WRITE
MSB	HORIZONTAL DELAY						LSB	R2 #	2E	D3004	WRITE
MSB	HORIZONTAL SYNC WIDTH						LSB	R3 #	07	D3006	WRITE
MSB	VERTICAL SYNC WIDTH						LSB	R4 #	13	D3008	WRITE
MSB	VERTICAL DELAY						LSB	R5 #	20	D300A	WRITE
PIN CONFG	CURSOR SKEW			BLANK SKEW				R6 #	C9	D300C	WRITE
MSB	VISIBLE DATA ROWS/ FRAME						LSB	R7 #	*1A #	D300E	WRITE
SCAN LINES/FRM (B10)	(B8)	SCAN LINES/DATA ROW (MSB)					(LSB)	R8 #	2D	D3010	WRITE
(B7)	SCAN LINES / FRAME						(B0)	R9 #	9F	D3012	WRITE
DMA DISABLE	DMA BURST DLY MSB		LSB	DMA BURST COUNT MSB			LSB	RA #	70	D3014	WRITE
X	PB/SS	INTERLACE MODES		OPERATION MODES			2XC/1XC	RB #	41	D3016	WRITE
MSB	TABLE START REGISTER(LS BYTE)						LSB	RC #	91	D3018	WRITE
ADDRESS MODE	TABLE START REG (MS BYTE) (MSB)						(LSB)	RD #	97	D301A	WRITE
MSB	AUX. ADDRESS REG.1 (LS BYTE)						LSB	RE #	FF	D301C	WRITE
ROW ATTR'S	AUX ADDR REG 1(MS BYTE) (MSB)						(LSB)	RF #	3F	D301E	WRITE
MSB	SEQUENTIAL BREAK REG. 1						LSB	R10 +	FF	D3020	WRITE
MSB	DATA ROW START REGISTER						LSB	R11	FF	D3022	WRITE
MSB	DATA ROW END/SEQU. BRK REG 2						LSB	R12	FF	D3024	WRITE
MSB	AUX. ADDRESS REG.2 (LS BYTE)						LSB	R13 +	00	D3026	WRITE
ROW ATTR'S	AUX ADDRESS REG 2 (MS BYTE) (MSB)						(LSB)	R14 +	00	D3028	WRITE
START COMMAND								R15	00	D302A	READ/WRITE
RESET COMMAND								R16 +	00	D302C	READ/WRITE
OFST OVR-FLOW	OFFSET VALUE (MSB)					(LSB)	0	R17	00	D302E	WRITE
VERTICAL CURSOR REGISTER (ROW COORD.) (MSB)							(LSB)	R18	FF	D3030	WRITE
								R38 +	--	D3070	READ
HORIZONTAL CURSOR REG. (COL. COORD.) (MSB)							(LSB)	R19	00	D3032	WRITE
								R39 +	--	D3072	READ
	VERT RE-TRCE	LGHT PEN	INTERRUPT ENABLE REG X	X	X	X	FRM TIM-ER	R1A #	40	D3034	WRITE
INT PEN-DING	VERT RE-TRCE	LGHT PEN	STATUS REGISTER		ODD/EVEN	X	FRM TMER	R3A	--	D3074	READ
MSB	VERT LIGHT PEN REG(ROW COORD)						LSB	R3B +	--	D3076	READ
MSB	HOR LIGHT PEN REG (COL COORD)						LSB	R3C +	--	D3078	READ
		VIDEO ATTRIBUTES REGISTR									
X	X	X	DISP ON		CURS BLRT	BLRT	BLOB GREN	"VATT"	00	D30BE	WRITE

* These registers are programmed with N -1.
\# These registers must have these initialization values.
\+ These registers may not be accessible on future HP 150 revisions and must not be written to or read from.

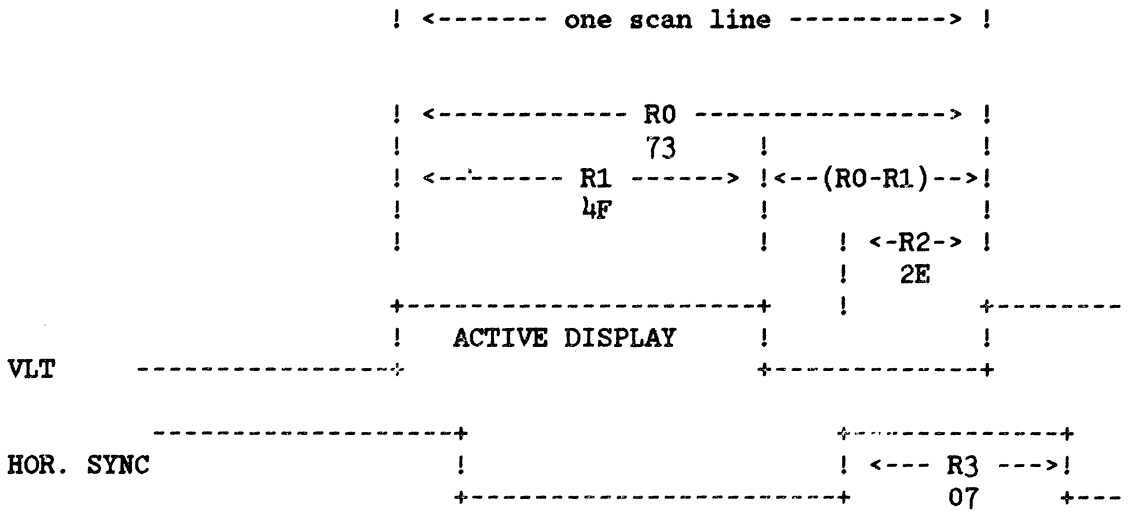
NOTE

For a full description of the CRT Controller registers, refer to the SMC9007 data in Standard Microsystems Corporation 1982 Data Book. Use of registers noted as being not accessible on future HP 150 revisions is not recommended and such access may result in software incompatibilities with certain HP 150 units. All addresses not specifically shown are reserved and should not be used.

A description of CRT controller registers as those registers are used and supported by the HP 150 follows.

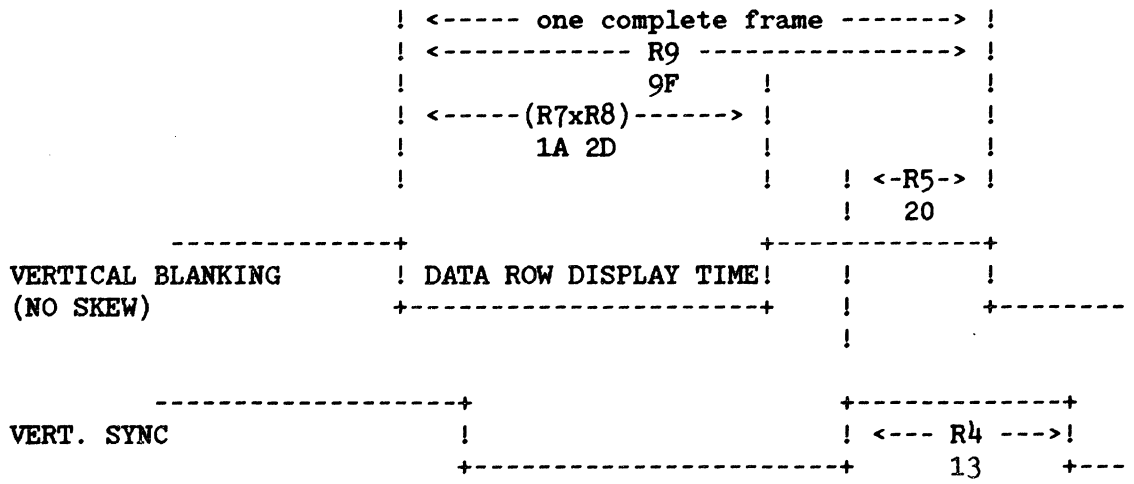
HORIZONTAL TIMING REGISTERS (R0, R1, R2 AND R3)

These registers define the horizontal scan line timing. They must contain the (hexadecimal) values shown.



VERTICAL TIMING REGISTERS (R4, R5, R7, R8 AND R9)

These registers define the vertical frame timing. They must contain the (hexadecimal) values shown.



PIN CONFIGURATION/SKEW BITS REGISTER (R6)

- Contains pin configuration information (bit 7,6)
- Cursor skew (bits 5,4,3) define the number of character clocks the cursor signal is delayed from VLT
- Blank skew (bits 2,1,0) define the number of character clocks the horizontal blank component of the CBLANK signal is delayed from VLT.
- Both cursor skew and blank skew are the value "001" for the 1 character skew.
- Must contain C9 Hex.

DMA CONTROL REGISTER (RA)

- DMA disable (bit 7). A logic "1" on this pin forces the SMC9007 DMA request into the inactive state, and the address bus will enter its high impedance state.
- DMA burst delay (bits 6,5,4). This register is loaded with "111" for zero delay, allowing all characters to be retreived from video RAM in one burst.
- DMA Burst Count (bits 3,2,1,0). Not Used.
- Must contain 70 Hex.

CONTROL REGISTER (RB)

- 7 bit register
- Smooth scroll mechanism is enabled by writing a "1" to bit 6.
- Interlace, (bits 5,4). "00" - non interlaced mode.
- Operation mode (bits 3,2,1). "000" for repetitive memory addressing.
- Single/double height cursor (bit 0). "1" = single.
- Must contain 41 Hex.

TABLE START REGISTER (RC AND RD)

- These registers point to the address where the row table begins.
- The registers are set up the following way for contiguous row table mode:
  - * register D (bits 7,6) = "10"
  - * register D (bits 5-0) = upper 6 bits of the 14 bit address
  - * register C (bits 7-0) = lower 8 bits of the 14 bit address.
- RC must contain 91 Hex, RD must contain 97 Hex.

AUXILIARY REGISTER 1 (RE AND RF)

- Not used, except for bits 7,6 in register F which must be "00" for single height, single width characters.
- RE must contain FF Hex, RF must contain 3FH.

SEQUENTIAL BREAK REGISTER 1 (R10)

- This register may not be accessible on certain HP 150 revisions and must not be used.

DATA ROW START REGISTER (R11)

- Defines the first data row number at which a smooth scroll operation begins.
- Is initialized by the system firmware to FF Hex.

DATA ROW END REGISTER (R12)

- The row numerically one less than the row defined by this register is the last data row on which a smooth scroll will occur.
- Is initialized by the system firmware to FF Hex.

AUXILIARY ADDRESS REGISTER 2 (R13 AND R14)

- This register may not be accessible on certain HP 150 revisions and must not be used.

START COMMAND (R15)

- During initialization of the SMC9007, after all vital screen parameters are loaded, a start command can be initiated by addressing this dummy register location.

RESET COMMAND (R16)

- This register may not be accessible on certain HP 150 revisions and must not be used.

SMOOTH SCROLL OFFSET REGISTER (R17)

- This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter to start at the programmed value rather than zero for the data row that starts the smooth scroll interval.
- Must have data bit 7 (most significant) cleared (0).

VERTICAL CURSOR REGISTER (R18)

- This register specifies the data row in which the cursor appears.

HORIZONTAL CURSOR REGISTER (R19)

- This register specifies the character position in which the cursor appears.

CURSOR REGISTERS R38 AND R39 (READ)

- These registers may not be accessible on some revisions of the HP 150 and must not be used.

INTERRUPT ENABLE REGISTER (R1A)

- This 3 bit write only register allows each of the 3 SMC9007 interrupts to be enabled or disabled.
- Bit 6 is set to "1" to enable vertical retrace interrupts.
- Must contain 40 Hex.

STATUS REGISTER (R3A)

- This register is only used to clear the interrupt bit. The value read is irrelevent.

VERTICAL LIGHT PEN REGISTER (R3B)

- This register may not be accessible on certain revisions of the HP 150 and must not be used.

HORIZONTAL LIGHT PEN REGISTER (R3C)

- This register may not be accessible on certain revisions of the HP 150 and must not be used.

VIDEO ATTRIBUTE LATCH

This latch stores 5 bits of video data, and can be updated during the blank portions of the video frame. It is a memory mapped I/O register with the 8088 address D30BE hexadecimal. The register is actually decoded as a non-existent SMC9007 register.

VIDEO ATTRIBUTE LATCH PIN DEFINITION

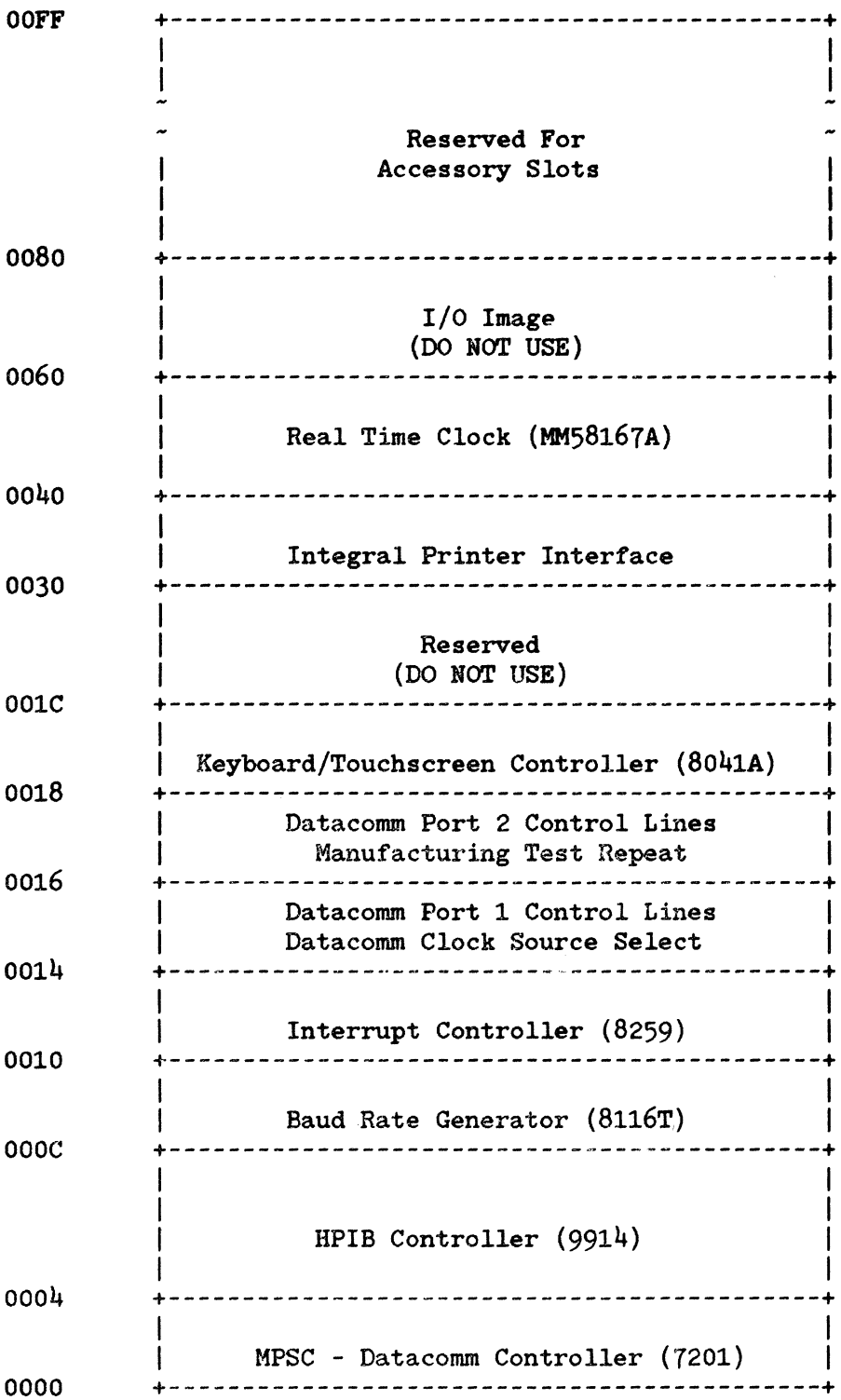
DISPON	BLRT	CBLRT	BLOB	GREN
D4	D3	D2	D1	D0

note: - positive logic is used (1 = on, 0 = off)
- when writing to this register, D5-D7 are don't cares

DISPON	:	Alpha Display On
BLRT	:	Character Blink Rate Characters with BL (blink) enhancement set will be blanked on the screen while BLRT is a "1."
CBLRT	:	Cursor Blink Rate The character for which CURS from the SMC9007 is active high, the cursor will be blinked when CBLRT is a "1."
BLOB	:	Blob Cursor Select (otherwise double scan line cursor)
GREN	:	Graphics Display Enable

I/O MAPPED DEVICES

HP 150 I/O Map



NOTE

I/O mapped devices at 0000 Hex through 0080 Hex are not exclusively decoded to 16 bits. Rather they may be accessed through any combination of high order byte bits. For future hardware compatibility it is highly recommended that programs which access I/O mapped devices directly at these addresses do so with a high order byte address of 00 Hex. Accessory cards may exclusively decode a 16 bit address. See the accessory card specifications for more information.

Real Time Clock (MM58167A)

Address	Register	Type
0056-005FH	Not Used	reserved
0055H	"GO" Comamand Register	write
0054H	Status Bit	read
0053H	RAM Register Reset	write
0052H	Counter Register Reset	write
0051H	Interrupt Control Register	write
0050H	Interrupt Status Register	read
004FH	Month RAM Register	read/write
004EH	Date RAM Register	read/write
004DH	Day RAM Register	read/write
004CH	Hour RAM Register	read/write
004BH	Minutes RAM Register	read/write
004AH	Seconds RAM Register	read/write
0049H	Tenth/Hundreth Sec RAM Reg	read/write
0048H	Millisecond RAM Register	read/write
0047H	Month Counter Register	read/write
0046H	Date Counter Register	read/write
0045H	Day Counter Register	read/write
0044H	Hour Counter Register	read/write
0043H	Minutes Counter Register	read/write
0042H	Seconds Counter Register	read/write
0041H	Tenth/Hundreth Sec Counter	read/write
0040H	Millisecond Counter Register	read/write

For more information on this part, see the MM58167A Data Sheet, National Semiconductor Corporation.

Integral Printer Interface

Address	Register	Type
0030H	Status/Data	read/write

Bit:	7	6	5	4	3	2	1	0
READ	-	-	-	-	-	NPAPER OUT	ONLINE	ACK
WRITE	D7	D6	D5	D4	D3	D2	D1	D0

Keyboard / Touchscreen Controller (8041A)

Address	Register	Type
0019H	Status / Command Register	read/write
0018H	Data Register	read/write

For more information on the use of these registers, see the "Hardware Subsystems" section, "Keyboard and Touchscreen".

Datacomm Port 2 Control Lines / Manuf Test Repeat

Address	Register	Type
0016H	OCR1/OCD1, OCR2/OCD2, DM Ctrl. Lines, Port 1 detect, Manufac. test bit	read/write

Bit:	7	6	5	4	3	2	1	0
READ	----	----	----	POD	DM	MTST	OCR2	OCR1
WRITE	----	----	----	----	----	----	OCD2	OCD1

In the above:

POD = 0 if Port 1 datacomm PCA is not present.
POD = 1 if Port 1 datacomm PCA is in place.
MTST = 0 if jumper wire is not grounding U62 pin 14.
MTST = 1 if U62 pin 14 is grounded causing repetition of manufacturing test segment that failed.

Datacomm Port 1 Control Lines / Clock Source Select

Address	Register	Type
0014H	OCR1/OCD1, OCR2/OCD2, DM Ctrl. Lines, Clock Source Select	read/write

Bit:	7	6	5	4	3	2	1	0
READ	0	0	0	1	DM	0	OCR2	OCR1
WRITE	Clock Source		----	----	----	----	OCD2	OCD1

Clock source select bits are defined as follows:

Bits 7	Bits 6	Receive Clock	Transmit Clock
0	0	x16	x16
0	1	x1	x1
1	0	RT	ST
1	1	RT	ST

Interrupt Controller (8259A)

Address	Register	Type
0010,0011H	Interrupt Controller Registers	read/write

For more information on this part, see the 8259A Data Sheet, Intel Corporation.

Baud Rate Generator (8116T)

Address	Register	Type
000CH	Baud Rate Select	write

Baud Rate Select Coding:

Port 2 Control D7 D6 D5 D4	Port 1 Control D3 D2 D1 D0	Clock Output (Hz.)	Baud Rate
0 0 0 0	0 0 0 0	800	50 *
0 0 0 1	0 0 0 1	1200	75 *
0 0 1 0	0 0 1 0	1760	110
0 0 1 1	0 0 1 1	2152	134.5 *
0 1 0 0	0 1 0 0	2400	150
0 1 0 1	0 1 0 1	4800	300
0 1 1 0	0 1 1 0	9600	600
0 1 1 1	0 1 1 1	19200	1200
1 0 0 0	1 0 0 0	28800	1800 *
1 0 0 1	1 0 0 1	32000	2000 *
1 0 1 0	1 0 1 0	38400	2400
1 0 1 1	1 0 1 1	57600	3600 *
1 1 0 0	1 1 0 0	76800	4800
1 1 0 1	1 1 0 1	115200	7200 *
1 1 1 0	1 1 1 0	153600	9600
1 1 1 1	1 1 1 1	307200	19200

* Denotes baud rates not configurable through the HP 150 Config menus.

HPIB Controller (9914)

Address	Register	Type
000BH	Command Pass Thru /Parallel Poll	read/write
000AH	Address Status Register	read
0009H	Address Switch / Address Reg	read/write
0008H	Interrupt Status 0/Interrupt Mask 0	read/write
0007H	Data In / Data Out	read/write
0006H	Bus Status / Auxiliary Command	read/write
0005H	Serial Poll register	read
0004H	Interrupt Status 1/Interrupt Mask 1	read/write

For more information on this part, see the TMS9914 Data Sheet, Texas Instruments Incorporated.

MPSC - Datacomm Controller (7201/8274)

Address	Register	Type
0003H	Channel B Control Reg	read/write
0002H	Channel B Data Reg	read/write
0001H	Channel A Control Reg	read/write
0000H	Channel A Data Reg	read/write

For more information on programming this part, see the "PD7201 Multiprotocol Serial Communications Controller Technical Manual", NEC Electronics U.S.A. Incorporated, or 8274 Data Sheet, Intel Corporation.