

TCCxxxx Auto.CE

Common SDK

User Guide for LPDDR4 Configuration

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TABLE OF CONTENTS

Contents

1 Introduction.....	3
1.1 Config Platform	3
1.2 Supported Speed	3
1.3 Available List.....	3
2 Configuration	4
2.1 Provide Config File for DRAM Setting	4
2.1.1 Magic number	4
2.1.2 DRAM Org. Config	4
2.1.3 DRAM Setting Config.....	5
2.1.4 SoC Setting Config.....	7
2.1.5 Timing Setting	8
2.1.6 Training Option Config	9
2.2 How to change config.....	10
2.2.1 To change LPDDR4 speed.....	10
2.2.2 To change Membus clock.....	11
2.2.3 To change SoC DIC/ODT.....	11
2.2.4 To change DRAM DIC/ODT	12
2.2.5 To change other configs	13
3 Training.....	14
3.1 Read Training.....	14
3.2 Write Training	16
3.3 PRBS Training.....	17
3.4 Soc VREF Training.....	18
3.5 DRAM VREF Training	19
4 Verification	20
4.1 U-boot mtest.....	20
4.2 Memtester	20
5 Margin Tool.....	22
5.1 Read DQ/DQS Valid Window Margin	22
5.2 Write DQ/DQS Valid Window Margin	22
5.3 Soc (Read) VREF Valid Window Margin	23
5.4 DRAM (Write) VREF Valid Window Margin	24
5.5 Read Impedance Valid Window Margin.....	25
5.6 Write Impedance Valid Window Margin.....	26
6 References	27
7 Revision History.....	28
7.1 Rev. 0.10: 2018-08-22.....	28

Figures

Figure 3.1. Read Path	14
Figure 3.2. Read Training#1	15
Figure 3.3. Read Training #2.....	15
Figure 3.4. Write Path	16
Figure 3.5. Write Training #1	16
Figure 3.6. Write Training #2	17
Figure 3.7. SoC VREF Training.....	18
Figure 3.8. DRAM VREF Training	19
Figure 4.1. mtest usage	20
Figure 4.2. mtest	20
Figure 4.3. memtester	21

Tables

Table 1.1 Available List.....	3
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1 INTRODUCTION

This document describes the configurable components and how to set up LPDDR4 for TCC899x and TCC803x.

1.1 Config Platform

The following platforms are supported.

- TCC899x for STB platform
- TCC803x for Automotive platform

Caution: LPDDR4 is very sensitive and you must follow the hardware design guide[1]. If you do not follow the hardware design guide, LPDDR4 operation can be incorrect.

1.2 Supported Speed

The following speeds are supported depending on the platform.

- TCC899x – Supports LPDDR4 3200 (1.6GHz) Speed
 - PLL Clock for PHY is 3.2GHz, and it is divided into 1.6GHz inside the PHY.
- TCC803x – Supports LPDDR4 3200 (1.6GHz) Speed
 - PLL Clock for PHY is 3.2GHz, and it is divided into 1.6GHz inside the PHY.

Note: 1.2GHz is available for testing purpose. Speeds below 1.2GHz affect the system and cannot be used. Refer to Chapter 2.2.1 for the clock change.

1.3 Available List

Table 1.1 Available List

Vendor	Part number	Interface	Speed	Size
Samsung	K4F8E3S4HB-MF(H)CJ	32Bits	3200	1Gbyte
	K4F6E3D4HB-MF(H)CJ	32Bits	3200	2Gbyte
	K4FBE3D4HM-GHCL	32Bits	3200	4Gbyte
Hynix	H9HCNNNBKUMLHR	32Bits	3200	2Gbyte
	H9HCNNNCPUMLHR	32Blts	3200	4Gbyte

2 CONFIGURATION

2.1 Provide Config File for DRAM Setting

Bootloader (U-Boot) has configure file for DRAM setting in the following folder.

```
[S237 u-boot]$ cd tools/lpddr4_param/
[S237 lpddr4_param]$ ls
lpddr4_param.py
[S237 lpddr4_param]$
```

- lpddr4_param_py
 - This file is python language file.
 - When this file is executed, the binary file "BL20.bin" is created.
 - The binary file is used to set in DRAM initialization.
 - If the file does not run, initialize the DRAM using default config.
- The lpddr4_param_py file consists of five parts, excluding the magic number.
 - DRAM Org. Config
 - DRAM Setting Config
 - SoC Setting Config
 - Timing Setting
 - Training Option Config

2.1.1 Magic number

Field	Description
magic_num = 40404040	Magic number to check valid DRAM parameters

2.1.2 DRAM Org. Config

Field	Description
manual_config = 0	config part is set manually 0: Default 1: Manual
data_width = 32	DRAM Bandwidth Default: 32bits Note: Other bandwidths are not yet supported.
channel = 1	Count of DRAM Controller and PHY
speed = 3200	LPDDR4 Speed Available speed: 3200 and 2400
membus_clock = 700	Membus Clock Speed(MHz) Available maximum clock: 700MHz
intlv_size = 8	Interleaving size when DRAM Controllers are two 128Mbyte by 1 (8 -> 1024Mbyte)
debug = 0	Print debug information Note: This config is not supported for security reason.
total_size = 2048	DRAM total size Note: This config is not supported for security reason.
channel0_size = 1024	DRAM size of channel 0 Note: This config is not supported for security reason.
channel1_size = 1024	DRAM size of channel 1 Note: This config is not supported for security reason.
num_chip = 2	Number of DRAM RANK Note: This config is not supported for security reason.
chip_size = 16	DRAM size of RANK Note: This config is not supported for security reason.
chip_num_row = 16	Number of row address Note: This config is not supported for security reason.
chip_num_col = 10	Number of column address Note: This config is not supported for security reason.
density = 8	Density information of DRAM RANK Note: This config is not supported for security reason.

2.1.3 DRAM Setting Config

Field	Description
manual_dramvalue = 0	Dram value part is set manually 0: Default 1: Manual
dram_vref_range = 0	DRAM VREF(DQ) range: 0 or 1
rclk_freq = 26	
reqq_depth = 32	
wdq_depth = 128	
rank_interleaving = 0	DRAM RANK interleaving On/Off Note: This config is not yet supported
channel_interleaving = 0	DRAM channel interleaving On/Off Note: This config is not yet supported
meso_synchroizer = 1	Unused value
mrr_byte_lane = 5	Mark the byte lane where DQ[7:0] of each DRAM device is connected to
byte_lane_inversion = 0	When the data wires are in bitwise reverse-order at the package or PCB, mark the byte lane where MRR data is delivered by writing '1' to the corresponding lane. 1: The bitwise order of the MRR byte lane is reversed. 0: NOP
initial_dram_vref = 20	DRAM VREF value during DRAM initialization
lpddr4_rpst = 0	RD Post-Amble length 0: 0.5*tCK 1: 1.5*tCK
lpddr4_wpst = 0	WR Post-Amble Length 0: 0.5*tCK 1: 1.5*tCK
lpddr4_rpre = 1	RD Pre-preamble Type 0: Static 1: Toggle
lpddr4_wpre = 1	WR Pre-preamble Length 0: Reserved 1: 2*tCK
lpddr4_ca_odi = 6	DRAM On-die-termination for CA
lpddr4_dq_odi = 5	DRAM On-die-termination for DQ
lpddr4_dq.dds = 6	DRAM Drive strength for DQ
read_dbi = 1	DBI-Read Enable
write_dbi = 1	DBI-Write Enable
write_odi = 1	Option of DQ ODT 0: Disable 1: Enable
ca_odi = 1	Option of CA ODT 0: Disable 1: Enable
single_cke = 0	1: Control CKE to all the ranks at the same time. 0: Control CKE to each rank independently.
init_zq_calibration = 1	ZQ Calibration during DRAM initialization 0: Disable 1: Enable
t_refipb = 3904000	Per-bank refresh interval in OSC clock cycles for each of eight MR4 values.
t_refiab = 488000	All-bank refresh interval in OSC clock cycles for each of eight MR4 values.
t_zqcal = 1000000	Register value of DRAM Controller (TIMING_PARAM_RCLK)
t_fc = 200000	tRC as defined in JEDEC
t_vrcg_disable = 100000	tVRCG_DISABLE ad defined in JEDEC
mr4_sensing = 1	mr4 sensing function 0: Off 1: On
mr4_sensing_period = 32000	mr4 sensing period
zq_calibration = 1	Periodic ZQ Calibration 0: Off 1: On
zq_calibration_period = 48000	Periodic ZQ Calibration(Interval)
periodic_training = 1	Periodic DQ Calibration 0: Off 1: On
periodic_training_period = 640000	Periodic DQ Calibration(Interval)
dynamic_power_down = 1	Dynamic Power Down Function

Field	Description
	0: Off 1: On
dynamic_self_refresh = 1	Dynamic Self Refresh Function 0: Off 1: On
regional_clock_gating = 1	Each block clock gating 0: Off 1: On
phy_clock_gating = 1	PHY clock gating On/Off
dram_clock_gating = 1	Reserved

2.1.4 SoC Setting Config

Field	Description
manual_socvalue = 0	Soc value part is set manually 0: Default 1: Manual
initial_soc_vref = 0x28	SoC VREF value during dram initialization
clock_dds = 4	Clock Signal Strength value It can be set from 0 to 7, and it consists of a combination of resistors. 3'b100: 48Ω Impedance output driver 3'b101: 40Ω Impedance output driver 3'b110: 34Ω Impedance output driver 3'b111: 30Ω Impedance output driver Note: This config is not yet supported.
cs_dds = 4	CS Signal Strength value It can be set from 0 to 7, and it consists of a combination of resistors. 3'b100: 48Ω Impedance output driver 3'b101: 40Ω Impedance output driver 3'b110: 34Ω Impedance output driver 3'b111: 30Ω Impedance output driver Note: This config is not yet supported.
cpu_ds_dds = 4	DQ/DQS Signal Strength value It can be set from 0 to 7, and it consists of a combination of resistors. 3'b100: 48Ω Impedance output driver 3'b101: 40Ω Impedance output driver 3'b110: 34Ω Impedance output driver 3'b111: 30Ω Impedance output driver
cpu_odt = 4	On-die-termination resistor value It can be set from 0 to 7, and it consists of a combination of resistors. 3'b100: 60Ω Far end VSSQ termination 3'b010: 120Ω Far end VSSQ termination 3'b001: 240Ω Far end VSSQ termination
dll_start_point	Initial DLL lock start point
dll_ctrl_ref = 8	The period of time when ctrl_locked is cleared
zq_clk_div = 7	ZQ Clock(=U_PHYIO_WRAPPER/U_ZQ_CTRL_IO_DS1/ZCTRL_CLK) divider setting value. The frequency will be determined by the following formula. This field should be set before the first ZQ calibration and should not be changed afterwards. ctrl_zq_clk_div should be between 1 to 7. Frequency of U_PHYIO_WRAPPER/U_ZQ_CTRL_IO_DS1/ZCTR L_CLK" = "clk_dfi frequency"(MHz) / ((ctrl_zq_clk_div+1)*2) (MHz)
dq_slew_control = 1	IO Driver slew control

2.1.5 Timing Setting

Field	Description
freq = 0	The frequency at which the timing parameter is based. Timing related parameters are determined by density, and the platform automatically obtains density information from LPDDR4 and automatically determines the parameter values for density. Therefore, the timing parameter cannot be inserted manually. However, if you want to force the timing parameter directly, you must put the value 0x800 in the frequency and the value in the rest of the parameter.
timing_param0 = 0	Timing parameter - t_ckcke, t_cmdcke, t_rppb, t_rpab
timing_param1 = 0	Timing parameter - t_cke, t_ckesr, t_ckelck, t_xp
timing_param2 = 0	Timing parameter - t_rc, t_ras, t_rtp, t_rcd
timing_param3 = 0	Timing parameter - t_wr_a, t_wtr_a, t_rrd, t_faw
timing_param4 = 0	Timing parameter - t_rtrrd, t_wrwtr, read_latency, write_latency
timing_param6 = 0	Timing parameter - t_ccdmw, t_mrw, t_mrd, t_mrr
timing_param7 = 0	Timing parameter - t_rdidle, t_add_wr_p, t_wtwcr, t_rtrcr
timing_param8 = 0	Timing parameter - t_ccd_gap, t_xsr, t_xp_mrri, t_refpdr
timing_param_derate0 = 0	Timing parameter derate- t_rcd_derate, t_rc_derate, t_ras_derate, t_rrd_derate
timing_param_derate1 = 0	Timing parameter derate- t_rpab_derate, t_rppb_derate
timing_zqcal0 = 0	t_zqcl
timing_zqcal1 = 0	t_zqcl
timing_configure = 0	Reserved
trddata_en1 = 0	trddata_en when read_dbi is 0
trddata_en2 = 0	trddata_en when read_dbi is 1
tphy_rdlat = 0	Read Latency
tphy_wrlat = 0	Write Latency
tphy_wrdata = 0	dfi_tphy_wrdata
t_wtwcr1 = 0	t_wtwcr Additional minimum gap between write CAS commands across ranks.
t_wtwcr2 = 0	t_wtwcr Additional minimum gap between write CAS commands across ranks.
t_rtw1_1 = 0	t_rtw
t_rtw1_2 = 0	t_rtw
t_rtw2_1 = 0	t_rtw
t_rtw2_2 = 0	t_rtw
t_rdidle1 = 0	t_rdidle
t_rdidle2 = 0	t_rdidle
t_rtrrd1 = 0	t_rtrrd
t_rtrrd2 = 0	t_rtrrd
t_wtrcr1 = 0	t_wtrcr Gap from write in rank A to read in rank B to avoid DQ & DQS bus collision.
t_wtrcr2 = 0	t_wtrcr Gap from write in rank A to read in rank B to avoid DQ & DQS bus collision.
t_rfocab1 = 0	t_rfocab
t_rfocab2 = 0	t_rfocab
t_rfocab3 = 0	t_rfocab
t_rfcpb1 = 0	t_rfcpb
t_rfcpb2 = 0	t_rfcpb
t_rfcpb3 = 0	t_rfcpb
t_xsr1 = 0	t_xsr
t_xsr2 = 0	t_xsr
t_xsr3 = 0	t_xsr
r1 = 0	Read latency
r2 = 0	Read latency
wl = 0	Write latency
lpddr4_rl = 0	Read Latency For MR setting
lpddr4_wl = 0	Write Latency For MR setting

2.1.6 Training Option Config

Field	Description
manual_option = 0	option part is set manually 0: Default 1: Manual
ca_train = 0	Command/Address Line Training On/Off Note: This config is not supported.
rd_train = 1	Read Training On/Off
wr_train = 1	Write Training On/Off
prbs_train = 1	PRBS (Pseudo Random Binary Sequence) Training On/Off
soc_vref_train = 1	SoC VREF Training On/Off
dram_vref_train = 1	DRAM VREF Training On/Off

2.2 How to change config

The platform was configured to initialize the DRAM with no config changes.

Therefore, there is no need for the DRAM-related settings (such as size, row, column, bit) except under special occasion.

The following chapters describe how to change the settings for test purposes or special cases.

By default, the config file consists of five parts, each with a manual variable. The value of this manual variable must be set to 1 for that part. If it is 0, the default value is set. (except timing config)

2.2.1 To change LPDDR4 speed

- Find lpddr4 config file(in bootloader(u-boot))

```
[S237 u-boot]$ cd tools/lpddr4_param/  
[S237 lpddr4_param]$ ls  
lpddr4_param.py  
[S237 lpddr4_param]$
```

- Edit that(lpddr_param_py) file

```
manual_config = 0 -> 1  
speed = 3200 -> 2400
```

*Currently, supported speeds are 3200(1.6GHz), and 2400(1.2GHz). Other speeds are not available and it will be supported in the future.

- Execute config file

```
[S237 lpddr4_param]$ ./lpddr4_param_py  
[S237 lpddr4_param]$
```

- Check update time of BL20.bin file

```
[S237 lpddr4_param]$ls -l ..//tcmkimage/images/BL20.bin  
-rw-r--r-- 1 B100196 Default_Group 12 May 29 16:51 ..//tcmkimage/images/BL20.bin
```

- re-build u-boot

2.2.2 To change Membus clock

- Find lpddr4 config file(in bootloader(u-boot))

```
[S237 u-boot]$ cd tools/lpddr4_param/
[S237 lpddr4_param]$ ls
lpddr4_param.py
[S237 lpddr4_param]$
```

- Edit that(lpddr_param_py) file

*manual_config = 0 -> 1
membus_clock = 700 -> 400 or 500 or 600*

**Currently, supported speeds are 400MHz, 500MHz, 600MHz and 700MHz. Other speeds are not available and it will be supported in the future.*

- Execute config file

```
[S237 lpddr4_param]$ ./lpddr4_param.py
[S237 lpddr4_param]$
```

- Check update time of BL20.bin file

```
[S237 lpddr4_param]$ls -l ..tcmkimage/images/BL20.bin
-rw-r--r-- 1 B100196 Default_Group 12 May 29 16:51 ..tcmkimage/images/BL20.bin
```

- re-build u-boot

2.2.3 To change SoC DIC/ODT

■ SoC DIC consists of clock, cs, and ds. And ODT consists of dq related one.

- clock_dds: LPDDR4 Clock Strength
- cs_dds: CS and Address Strength
- cpu_ds_dds:DQ Strength
- cpu_odt: DQ termination

- Find lpddr4 config file(in bootloader(u-boot))

```
[S237 u-boot]$ cd tools/lpddr4_param/
[S237 lpddr4_param]$ ls
lpddr4_param.py
[S237 lpddr4_param]$
```

- Edit that(lpddr_param_py) file

manual_socvalue = 0 -> 1

a. Clock Strength

clock_dds = 6 -> 0~7 if you want.

b. CS and Address Strength

cs_dds = 5 -> 0~7 if you want.

c. DQ Strength

cpu_ds_dds = 5 -> 0~7 if you want.

d. DQ Termination

cpu_odt = 4 -> 0~7 if you want.

- Execute config file

```
[S237 lpddr4_param]$ ./lpddr4_param.py
[S237 lpddr4_param]$
```

- Check update time of BL20.bin file

```
[S237 lpddr4_param]$ls -l ..tcmkimage/images/BL20.bin
-rw-r--r-- 1 B100196 Default_Group 12 May 29 16:51 ..tcmkimage/images/BL20.bin
```

- re-build u-boot

2.2.4 To change DRAM DIC/ODT

- The DRAM DIC consists of dq, and the ODT consists of dq and ca.
 - lpddr4_ca_0dt: CA Termination
 - lpddr4_dq_0dt: DQ Termination
 - lpddr4_dq_dds: DQ Strength

- Find lpddr4 config file(in bootloader(u-boot))

```
[S237 u-boot]$ cd tools/lpddr4_param/
```

```
[S237 lpddr4_param]$ ls
```

```
lpddr4_param.py
```

```
[S237 lpddr4_param]$
```

- Edit that(lpddr_param_py) file

```
manual_dramvalue = 0 -> 1
```

a. LPDDR4 CA ODT

```
lpddr4_ca_0dt = 6 -> 0~7 if you want.
```

b. LPDDR4 DQ ODT

```
lpddr4_dq_0dt = 4 -> 0~7 if you want.
```

c. LPDDR4 DQ Strength

```
lpddr4_dq_dds = 6 -> 0~7 if you want.
```

- Execute config file

```
[S237 lpddr4_param]$ ./lpddr4_param_py
```

```
[S237 lpddr4_param]$
```

- Check update time of BL20.bin file

```
[S237 lpddr4_param]$ls -l ..//tcmkimage/images/BL20.bin
```

```
-rw-r--r-- 1 B100196 Default_Group 12 May 29 16:51 ..//tcmkimage/images/BL20.bin
```

- re-build u-boot

2.2.5 To change other configs

- Other configs can be modified for testing purposes though it is not recommended.

- **Find lpddr4 config file(in bootloader(u-boot))**

```
[S237 u-boot]$ cd tools/lpddr4_param/
```

```
[S237 lpddr4_param]$ ls
```

```
lpddr4_param.py
```

```
[S237 lpddr4_param]$
```

- **Edit that(lpddr_param_py) file**

a. find manual setting of part and set to 1 ex)manual_socvalue = 0 -> 1

- The manual_xxxx option for that part must be 1 for the fix to be applied

b. modify the item you want to modify.

- **Execute config file**

```
[S237 lpddr4_param]$ ./lpddr4_param_py
```

```
[S237 lpddr4_param]$
```

- **Check update time of BL20.bin file**

```
[S237 lpddr4_param]$ ls -l ..tcmkimage/images/BL20.bin
```

```
-rw-r--r-- 1 B100196 Default_Group 12 May 29 16:51 ..tcmkimage/images/BL20.bin
```

- **re-build u-boot**

3 TRAINING

The platform supports three auto training and two manual training functions.

- Auto Training
 - Read Training
 - Write Training
 - PRBS Training
- Manual Training
 - SoC VREF Training
 - DRAM VREF Training

Read training, Write training, and PRBS training automatically calculate the distance between signals by hardware to obtain left, right, and center. Use the delay value based on the obtained center value. Although it is possible to set the offset in software, it is not recommended to use offset setting of IP vendor.

3.1 Read Training

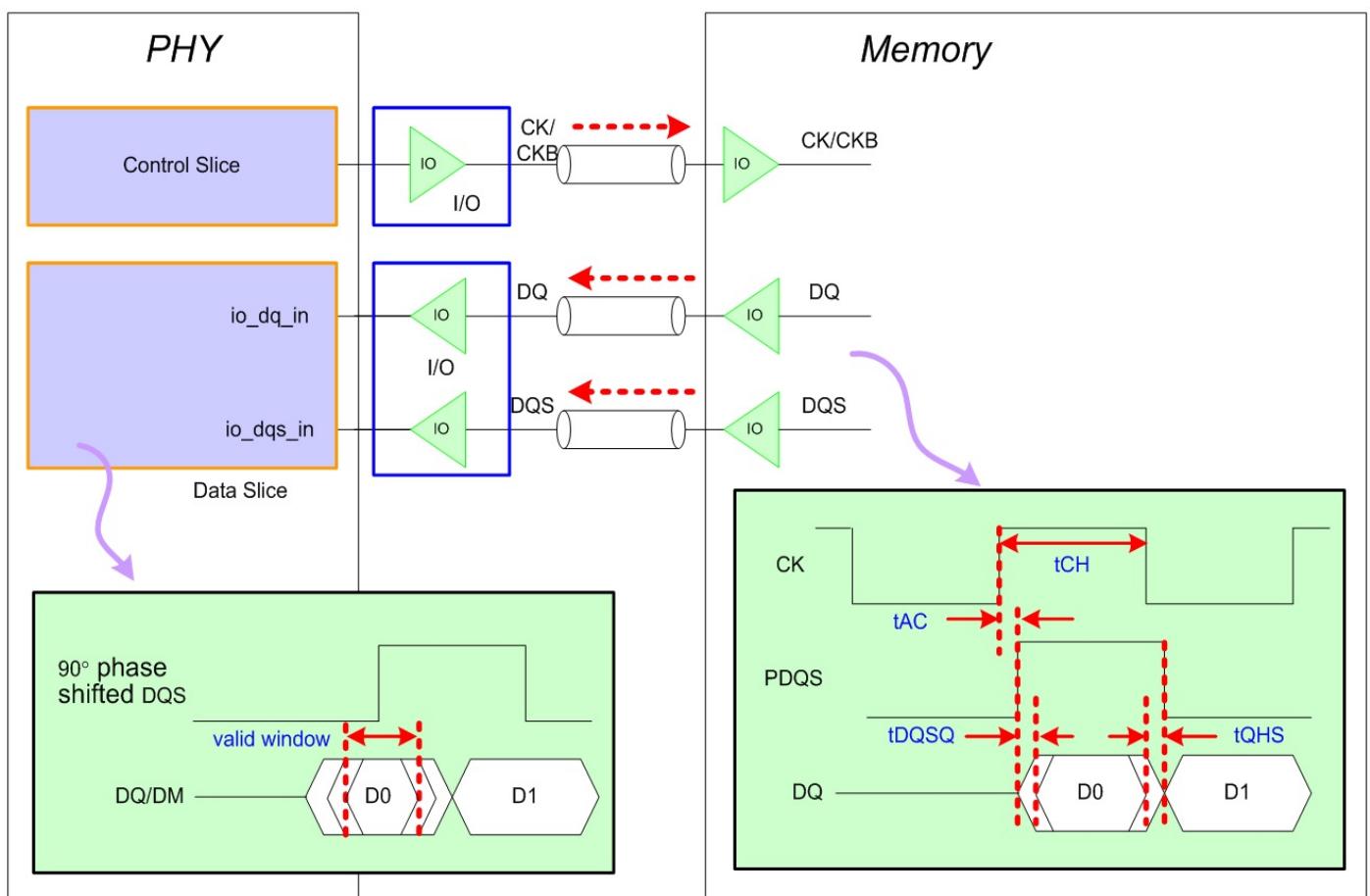


Figure 3.1. Read Path

- PHY reads pre-defined DQ pattern from memory after setting DQ DLL code.
- The valid window location is found by adjusting delay to DQS and by checking that read data from the memory equals to the pre-defined DQ pattern.
 - Add delay to DQS and capture DQ/DM using DQS as clock
 - vvmc, vwml, vwmr are found by checking “pass” region

DQS —Add delay→

DQ0

DQ1

DQ3

DQ4

...
DQ7

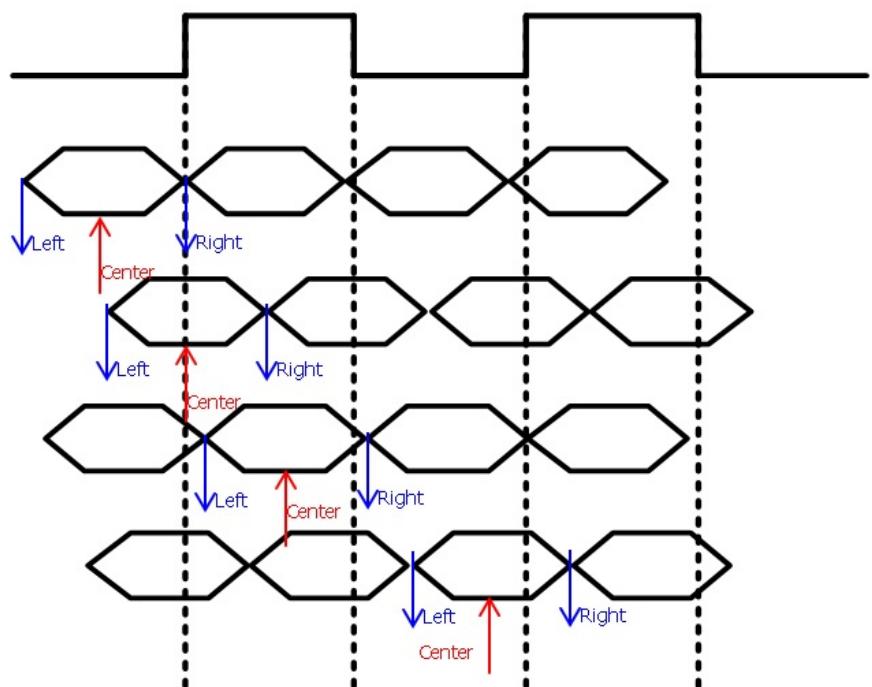


Figure 3.2. Read Training#1

- After Read Training, vwmr for each DQ will be found and each DQ bit will be edge-aligned with each other.

DQS —Add delay→

DQ0

DQ1

DQ3

DQ4

DQ5 ...

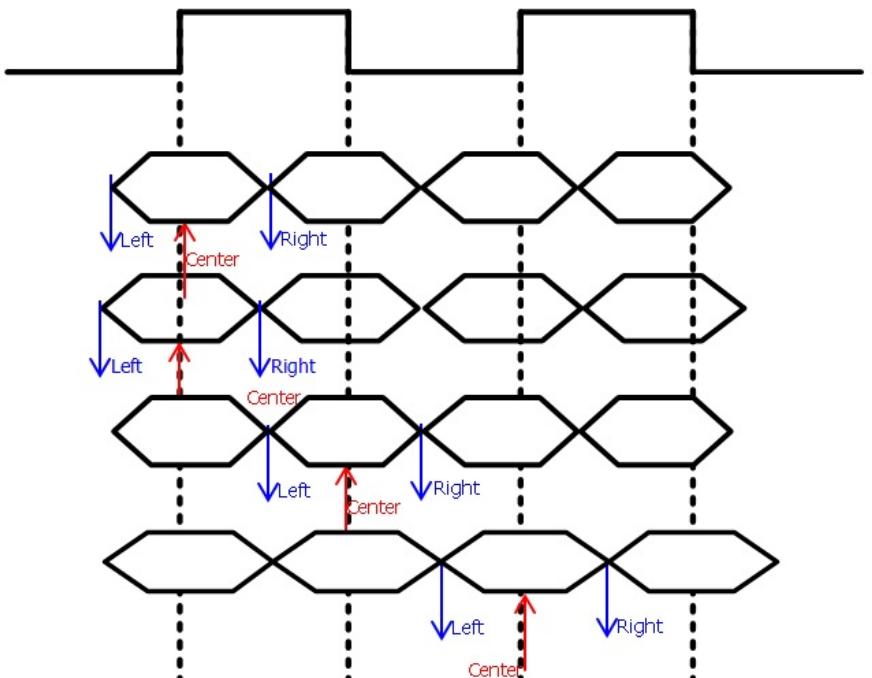


Figure 3.3. Read Training #2

3.2 Write Training

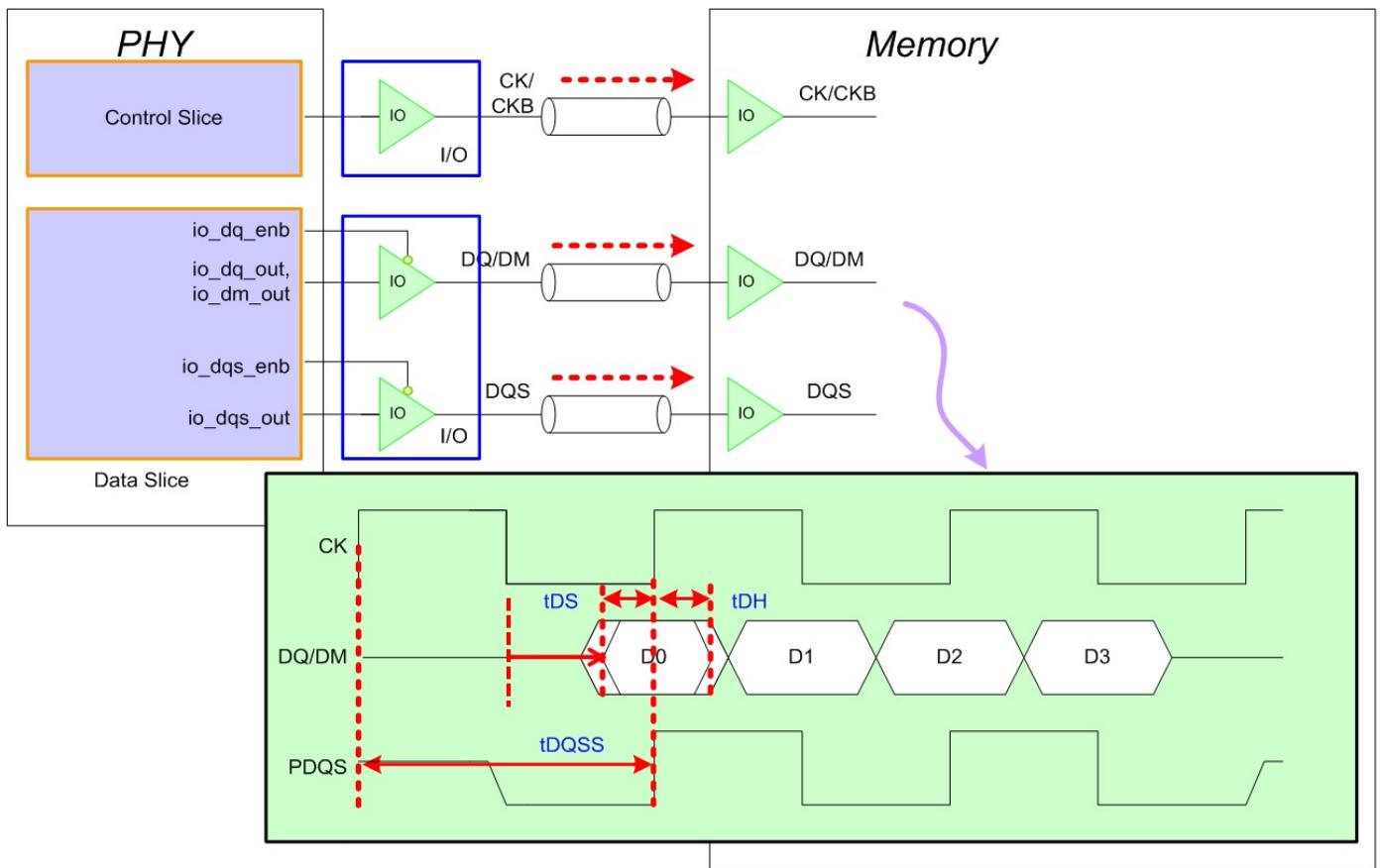


Figure 3.4. Write Path

- PHY writes pre-defined DQ pattern to memory after setting DQ DLL code.
- The valid window location is found by adjusting delay to DQ and by checking that read data from the memory equals to the pre-defined DQ pattern.

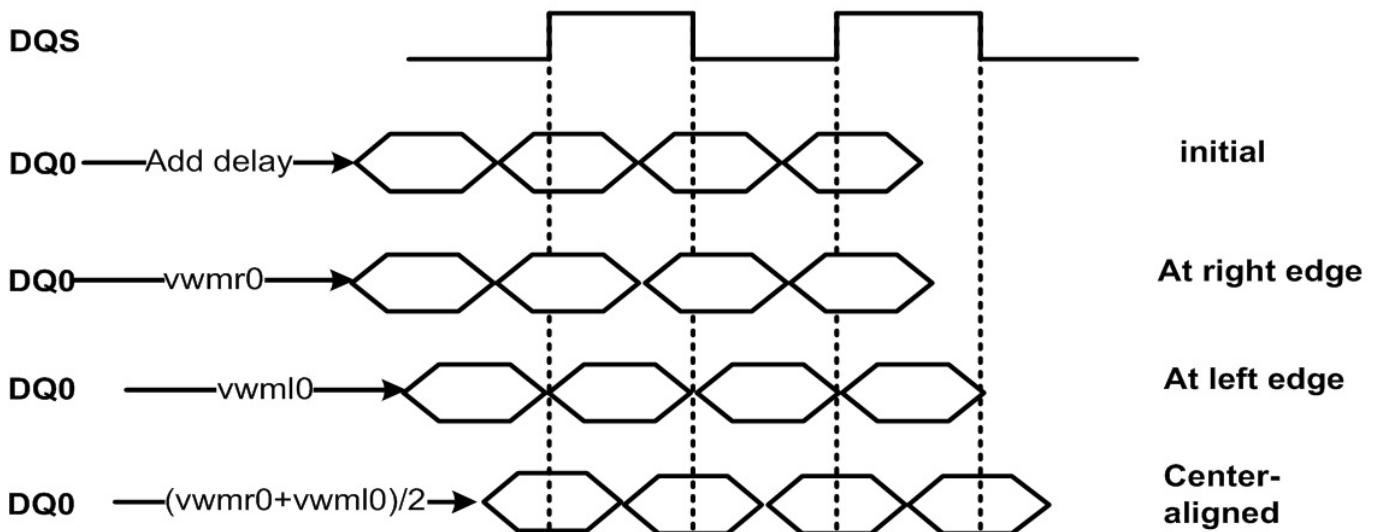


Figure 3.5. Write Training #1

- After Write Training, vwmc for each DQ will be found and each DQ bit will be center-aligned with DQS.

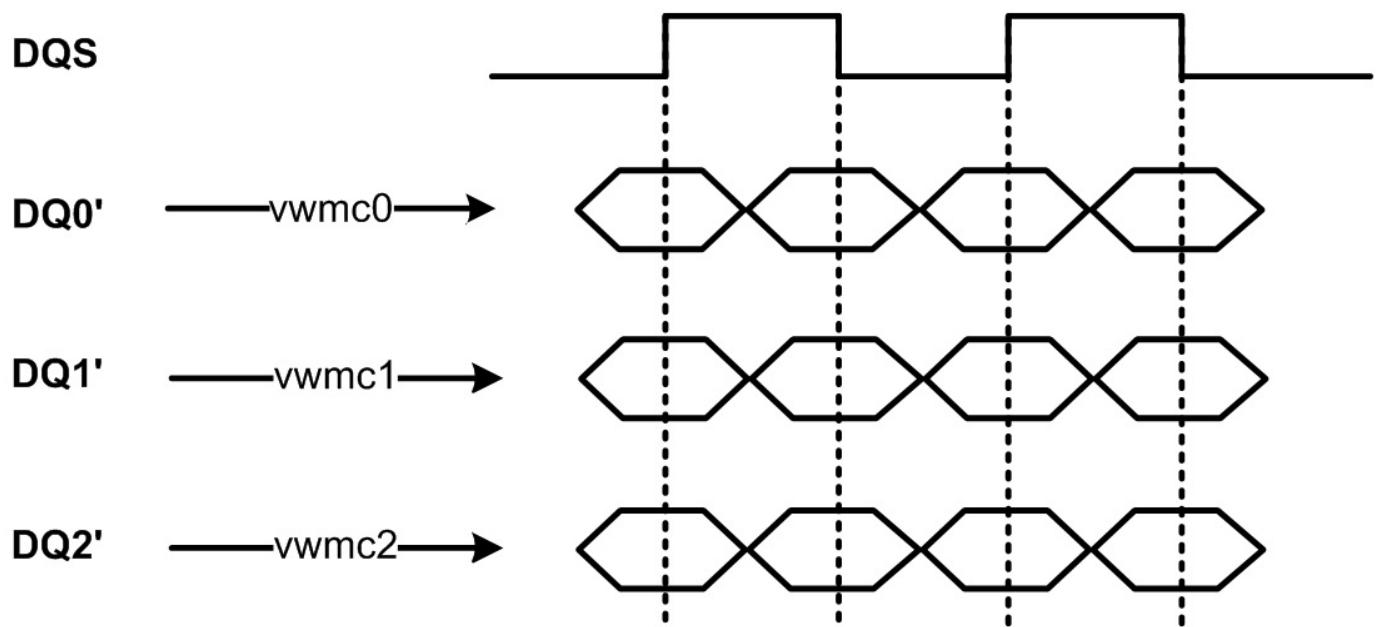


Figure 3.6. Write Training #2

3.3 PRBS Training

PRBS (Pseudo Random Binary Sequence) training compensates Read/Write center shift caused by DQ/DM patterns. Initial Read/Write training should be completed before PRBS training. This training can be trained more precisely through the random pattern after the Read / Write training.

3.4 SoC VREF Training

```
:SOC vref valid margin window phy[0],channel[0]
```

```
vref 63 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 62 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 61 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 60 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 59 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 58 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 57 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 56 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 55 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 54 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 53 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 52 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 51 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 50 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 49 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 48 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 47 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 46 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 45 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 44 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 43 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 42 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 41 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 40 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 39 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 38 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 37 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 36 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 35 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 34 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 33 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 32 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 31 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 30 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 29 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 28 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 27 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 26 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 25 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 24 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 23 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 22 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 21 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 20 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 19 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 18 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 17 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 16 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 15 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 14 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 13 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 12 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  
vref 11 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
```

Figure 3.7. SoC VREF Training

SoC VREF (Voltage Reference) set in the SoC is directly configurable and has a margin in setup and hold for each setup. Therefore, in order to find the optimal setup and hold margin for read, the margin is measured by VREF to find the section with the greatest margin.

3.5 DRAM VREF Training

```
;DRAM vref valid margin window channel [0]
50 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
49 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
48 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
47 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
46 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
45 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
44 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
43 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
42 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
41 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
40 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
39 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
38 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
37 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
36 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
35 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
34 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
33 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
32 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
31 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
30 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
29 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
28 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
27 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
26 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
25 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
24 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
23 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
22 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
21 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
20 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
19 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
18 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
17 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
16 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
15 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
14 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
13 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
12 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
11 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
10 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
9 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
8 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
7 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
6 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
4 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0 -XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
```

Figure 3.8. DRAM VREF Training

DRAM VREF set in the DRAM is directly configurable and has a margin in setup and hold for each setup. Therefore, in order to find the optimal setup and hold margin for write, the margin is measured by VREF to find the section with the greatest margin.

4 VERIFICATION

Although it is automatically tuned through the training function, it is necessary to check the reliability of the DRAM operation.

4.1 U-boot mtest

U-boot basically provides a simple RAM test function.

```
TCC # mtest -help
mtest - simple RAM read/write test

Usage:
mtest [start [end [pattern [iterations]]]]
TCC #
```

Figure 4.1. mtest usage

```
TCC #
TCC # mtest 0x20000000 0x20100000 10
Testing 20000000 ... 20100000:
Pattern FFFFFFFFFFFFEF Writing... | n: 1434: 1433
```

Figure 4.2. mtest

You can specify the test area and the number of times, and if an error occurs, you can detect the problem in that area.

4.2 Memtester

Memtester is an effective user space tester for stress-testing of the memory subsystem. It is very effective at finding intermittent and non-deterministic faults. Note that problems in other hardware areas (overheating CPU, out-of-specification power supply, etc.) can cause intermittent memory faults, so it is still up to you to determine where the fault lies through normal hardware diagnostic procedures; memtester just helps to determine whether a problem exists or not.

Memtester is described in the GPL license linux APP manual page. [2] You can download it. [3]

```
console:/ # memtester 32 1
memtester version 4.3.0 (32-bit)
Copyright (C) 2001-2012 Charles Cazabon.
Licensed under the GNU General Public License version 2 (only).

pagesize is 4096
pagesizemask is 0xffffffff000
want 32MB (33554432 bytes)
got 32MB (33554432 bytes), trying mlock ...locked.

Loop 1/1:
    Stuck Address      : ok
    Random Value       : ok
    Compare XOR        : ok
    Compare SUB        : ok
    Compare MUL        : ok
    Compare DIV        : ok
    Compare OR         : ok
    Compare AND        : ok
    Sequential Increment: ok
    Solid Bits         : ok
    Block Sequential   : ok
    Checkerboard       : ok
    Bit Spread          : ok
    Bit Flip            : ok
    Walking Ones        : ok
    Walking Zeroes     : ok

Done.
console:/ #
```

Figure 4.3. memtester

5 MARGIN TOOL

The following margin tools are provided in the u-boot console environment.

- Read DQ/DQS Valid Window Margin
- Write DQ/DQS Valid Window Margin
- SoC(Read) VREF Valid Window Margin
- DRAM(Write) VREF Valid Window Margin
- Read Impedance Valid Window Margin
- Write Impedance Valid Window Margin

5.1 Read DQ/DQS Valid Window Margin

The function sweeps the offset of DQ to measure the margin between DQ and DQS (Read Operation)

- Console Command: **read_dqs_margin**

(U-Boot Console)

TCC # **read_dqs_margin**

Read DQ/DQS Valid Margin Window

*XXXXXXXXXXXXXXXXXXXXXXXXXXXX*****|*****XXXXXXXXXXXXXXXXXXXXXXXXXXXX*

Left valid offset : 18

Right valid offset : 18

Done.

TCC #

5.2 Write DQ/DQS Valid Window Margin

The function sweeps the offset of DQ to measure the margin between DQ and DQS (Write Operation)

- Console Command: **write_dqs_margin**

(U-Boot Console)

TCC # **write_dqs_margin**

Write DQ/DQS Valid Margin Window

*XXXXXXXXXXXXXXXXXXXXXXXXXXXX*****|*****XXXXXXXXXXXXXXXXXXXXXXXXXXXX*

Left max valid offset : 19

Right max valid offset : 16

Done.

TCC #

5.3 SoC (Read) VREF Valid Window Margin

The corresponding VWM (Valid Window Margin) shows Read DQS margin according to the SoC VREF change at the time of Read. This gives the optimum VREF value.

- PHY[0]: 16bits
 - PHY[1]: 16bits

- #### ■ Console Command: **soc_vref_margin**

(U-Boot Console)

TCC #

5.4 DRAM (Write) VREF Valid Window Margin

The corresponding VWM shows Write DQS margin according to the DRAM VREF change at the time of Write. This gives the optimum VREF value. DRAM VREF is divided into 0 and 1 range. You can find the appropriate value in the 0 and 1 range.

Refer to JEDEC STANDARD or the datasheet of the LPDDR4 vendor for detailed values of vref. [4]

Console Command: **dram_vref_margin**

(U-Boot Console)

TCC #

5.5 Read Impedance Valid Window Margin

The window shows the margin according to the combination of the ODT of the SoC and the strength of the DRAM at the time of reading. The optimum margin can be found and the corresponding SoC ODT and DRAM strength (DQ/DQS) can be applied with reference to Chapter 2.2.3 and 2.2.4.

Console Command: **read_impedence_margin**

(U-Boot Console)

```
TCC # read_impedence_margin
Read Impedence Valid Margin Window
CPU_ODT[7] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[7] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[7] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[7] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[7] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[6] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[6] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[6] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[6] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[6] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[5] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[5] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[5] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[5] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[5] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[4] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[4] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[4] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[4] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[4] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[3] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[3] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[3] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[3] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[3] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[2] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[2] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[2] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[2] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[2] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[1] DRAM_DDS[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[1] DRAM_DDS[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[1] DRAM_DDS[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[1] DRAM_DDS[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_ODT[1] DRAM_DDS[5] - XXXXXXXXXXXXXXXXXXXXXXXX
Done.
```

TCC #

5.6 Write Impedance Valid Window Margin

The window shows the margin according to the combination of the ODT of the DRAM and the strength of the SoC at the time of writing. The optimum margin can be found and the corresponding DRAM ODT and SoC strength (DQ/DQS) can be applied with reference to Chapter 2.2.3 and 2.2.4.

Console Command: `write_impedence_margin`

(U-Boot Console)

```
TCC # write_impedence_margin
Write Impedence Valid Margin Window
CPU_DDS[7] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[7] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[7] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[7] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[7] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[7] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[6] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[6] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[6] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[6] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[6] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[6] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[5] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[5] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[5] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[5] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[5] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[5] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[4] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[4] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[4] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[4] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[4] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[4] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[3] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[3] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[3] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[3] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[3] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[3] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[2] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[2] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[2] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[2] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[2] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[2] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[1] DRAM_ODT[1] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[1] DRAM_ODT[2] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[1] DRAM_ODT[3] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[1] DRAM_ODT[4] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[1] DRAM_ODT[5] - XXXXXXXXXXXXXXXXXXXXXXXX
CPU_DDS[1] DRAM_ODT[6] - XXXXXXXXXXXXXXXXXXXXXXXX
```

Done.

TCC #

6 REFERENCES

- [1] Contact Telechips for more details: auto_sales@telechips.com ce_sales@telechips.com
- [2] Memtester site: <https://linux.die.net/man/8/memtester>
- [3] Memtester download site: <http://pyropus.ca/software/memtester/>
- [4] JEDEC STANDARD (Low Power Double Data Rate 4) JESD209-4

7 REVISION HISTORY

7.1 Rev. 0.10: 2018-08-22

Preliminary version release.

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