Analysis and Design of a Voltage Controlled Oscillator

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Introduction and circuit operation

Abstract

In this report, a voltage controlled oscillator (VCO) will be designed, simulated, and implemented in a mask diagram. For this purpose, a Schmitt trigger will be characterized using CMOS transistor logic.

The Schmitt trigger

Introduction

The Schmitt trigger was invented by US scientist Otto H. Schmitt in 1934 as a direct result of Schmitt's study of the neural impulse propagation in squid nerves [1]. It is a comparator circuit that uses positive feedback to switch a continuous waveform into two voltage levels, effectively transforming an analog signal into a digital one. It also has hysteresis on the switching thresholds, as shown in Figure 1, making it less susceptible to noise. Schmitt triggers can additionally be used to build oscillators, as will be shown in this report.

One possible and simple schematic of a Schmitt trigger in CMOS logic is shown in Figure 3.

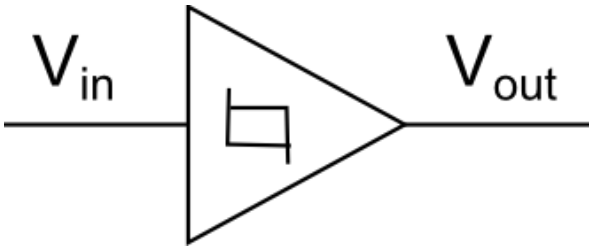

Figure 1: Schematic symbol for the Schmitt trigger

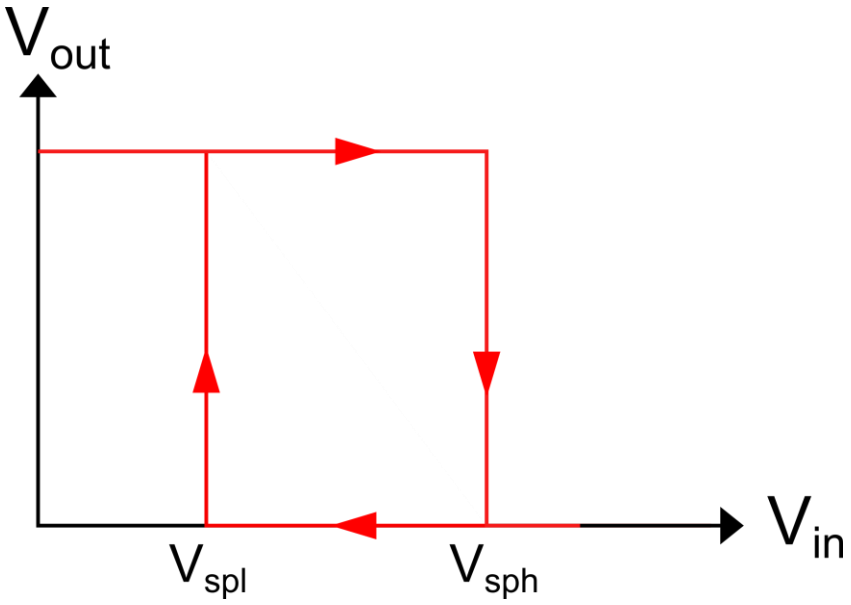

Figure 2: Ideal Schmitt trigger voltage transfer characteristic

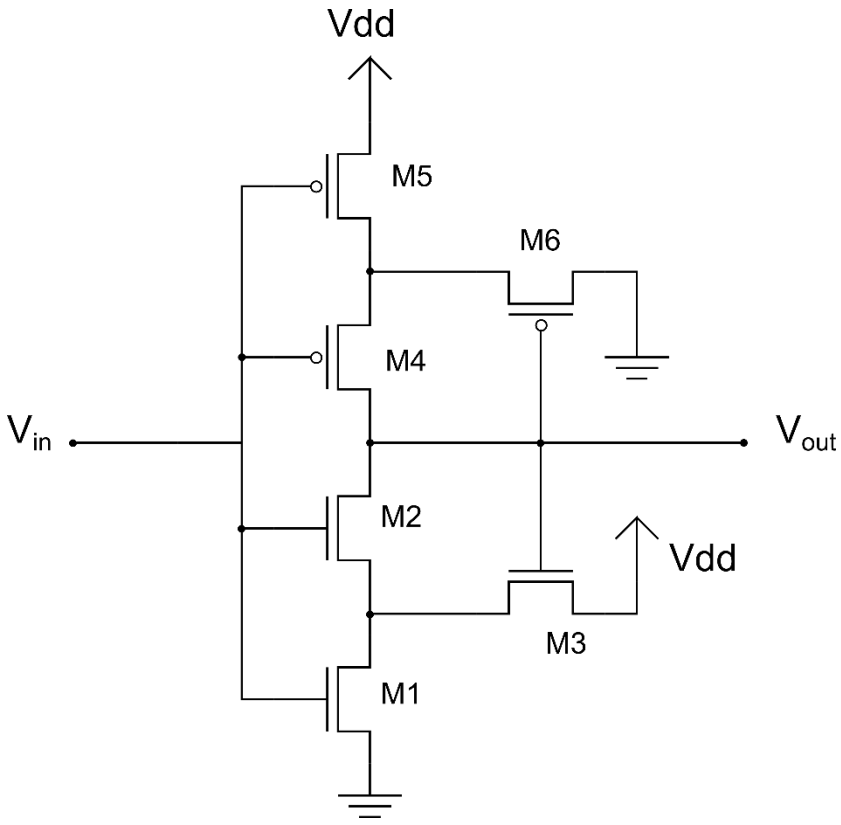

Figure 3: CMOS implementation of a Schmitt trigger

Circuit operation

In this section, a detailed description of the circuit in Figure 3 will be given, as well as the derivation for the mathematical expressions of the key parameters involved in its design. The expressions obtained will then be used to establish the transistor dimensions required to achieve the desired device specifications. For notation, the transistor gain for transistor M_i will be represented as β_i.

It is easier to begin the analysis by considering the output established at a certain level, and then understand the circuit operation from this state. For V_{out} = 0[V] and $V_{in} < V_{tn}$, none of the transistors are conductive. If V_{in} is increased to a value between V_{tn} and V_{sph}, then M2 is not conductive and current is driven through M1 and M3 (Figure 4). The output V_{out} remains unchanged, as no current path has been formed yet. Since both transistors are clearly saturated, the currents I_{M1} and I_{M3} are given by (1) - (2), respectively. Setting them equal and solving for V_x, (3) is obtained. This allows for the determination of the parameter V_{sph}, which will activate M2 and give V_{out} a discharge path through M1 and M2, effectively lowering the output voltage to 0[V] (Figure 5: NMOS sub-circuit operation with M2 conducting. Vout quickly drops and opens M3).

$$I_{M1} = \frac{\beta_1}{2}(V_{in} - V_{tn})^2 \tag{1}$$

$$I_{M3} = \frac{\beta_3}{2}(V_{dd} - V_x - V_{tn})^2 \tag{2}$$

$$V_x = -\sqrt{\frac{\beta_1}{\beta_3}}V_{in} + V_{dd} - \mathrm{V_{tn}}\left(1 - \sqrt{\frac{\beta_1}{\beta_3}}\right) \tag{3}$$

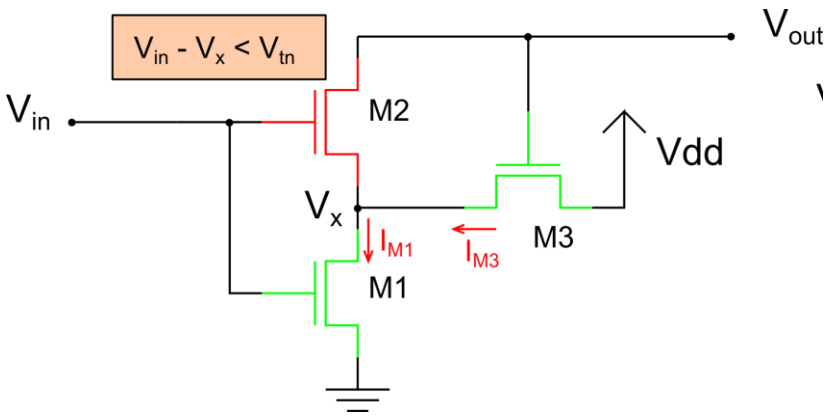

Figure 4: NMOS sub-circuit operation while Vin is still not large enough to drive M2

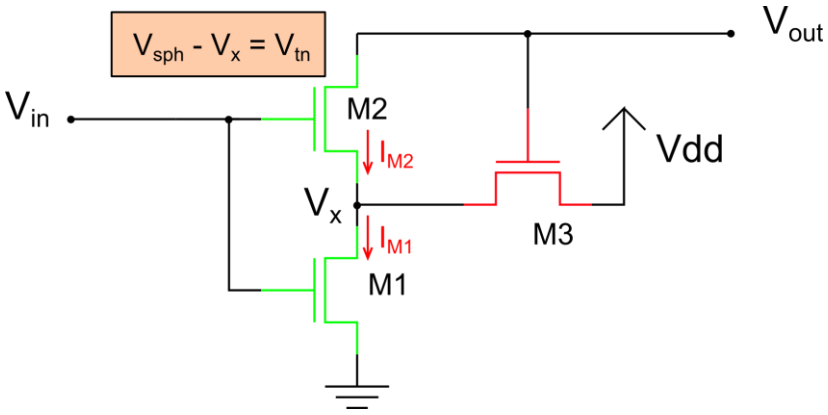

Figure 5: NMOS sub-circuit operation with M2 conducting. Vout quickly drops and opens M3

Setting $V_{in} = V_{tn} + V_x = V_{sph}$ and using (3), equation (4) is obtained. This expression relates the gain ratio between transistors M1 and M3 to the reference values, adding a restriction to the values of W/L the transistors may have.

$$\frac{\beta_1}{\beta_3} = \left(\frac{V_{dd} - V_{sph}}{V_{sph} - V_{tn}}\right)^2 \quad (4)$$

A similar analysis is done for the PMOS sub-circuit. Assuming the output is low and V_{in} is at V_{dd}, then both M4 and M5 are open - so no current is driven, even though M6 is closed. As soon as

the input becomes less than $V_{dd} - V_{tp}$, M5 begins conducting and current is driven through M5 and M6. This situation is shown in Figure 6. Since both transistors are saturated, the currents I_{M5} and I_{M6} are given by (5) and (6), respectively. Setting these two currents equal and solving for V_y, (7) is obtained.

Transistor M4 will only close once the relation $V_{in} - V_y < V_{tp}$ is satisfied. The threshold V_{spl} can be found by setting $V_{in} = V_{tp} + V_y$ and using (7) to find the gain required for the output to charge back to V_{dd} at the low threshold value of $V_{in} = V_{spl}$, thus obtaining (8).

$$I_{M5} = \frac{\beta_5}{2}\left(V_{in} - V_{dd} - V_{tp}\right)^2 \tag{5}$$

$$I_{M6} = \frac{\beta_6}{2}\left(0 - V_y - V_{tn}\right)^2 \tag{6}$$

$$V_y = \sqrt{\frac{\beta_5}{\beta_6}}\left(V_{dd} + V_{tp} - V_{in}\right) - V_{tp} \tag{7}$$

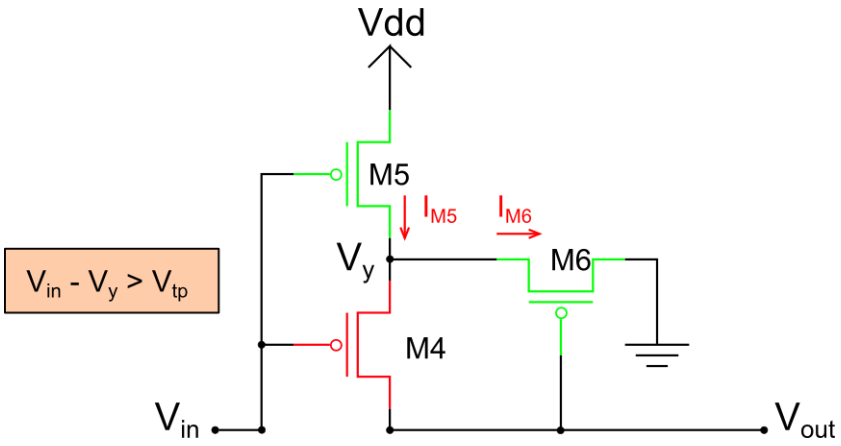

Figure 6:PMOS sub-circuit operation while Vin is still not small enough to drive M5

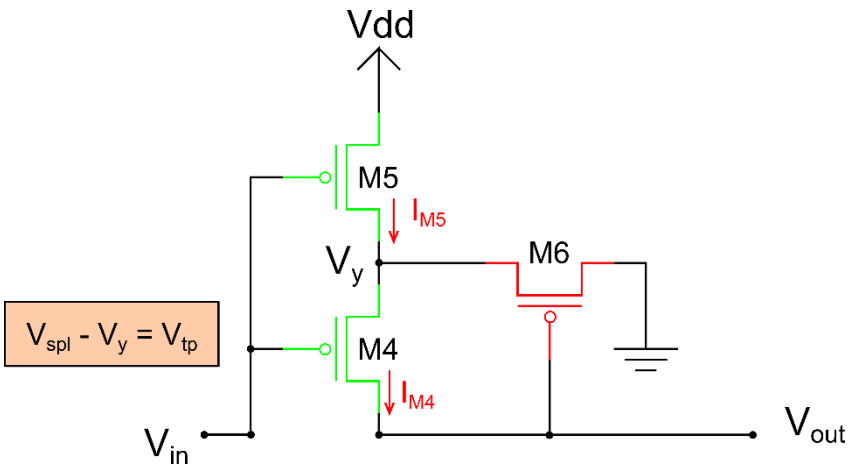

Figure 7: PMOS sub-circuit operation with M4 being conduction. Vout quickly increases back to Vdd, opening M6.

$$\frac{\beta_5}{\beta_6} = \left(\frac{V_{spl}}{V_{dd} + V_{tp} - V_{spl}}\right)^2 \quad (8)$$

When both the PMOS and CMOS sub-circuits are combined, they operate in the same manner as a Schmitt trigger. It is also clear that they do not interfere with each other, operating independently. If the output is low, then the NMOS side simply keeps it low, through transistors M1 and M2. It will only be switched high after V_{in} becomes lower than V_{spl}, which triggers the output to become high. Once the output is high, M3 is switched on and V_x is greatly increased, shutting down M2. Now, the output will stay high until V_{in} becomes greater than V_{sph}, as discussed earlier. Once that happens, M6 will turn on, decreasing the value of V_y and shutting down M4, repeating the cycle.

Timing analysis

In this section, a timing equations will be derived, concerning the rise time t_{plh} and the fall time t_{phl}. This analysis is useful to have an understanding of what is affecting the rise and fall times. The rise time is defined as the amount of time it takes for the output to go from $V_{out} = 0$ to $V_{out} =$ Vdd/2. In the same manner, the fall time is how long it takes for the output to go from V_{out} = Vdd to

V_{out} = Vdd/2. To study this problem, a common approach of using a RC-model is used, where a load capacitance is established at the output and the transistors at their operating point being modeled as voltage-controlled resistors. This model, when the PMOS sub-circuit switches the output from low to high, is shown in Figure 8. For clarity, Figure 9 and Figure 10 are shown. They represent the isolated equivalent RC model that will be used to find the switching times t_{plh} and t_{phl}.

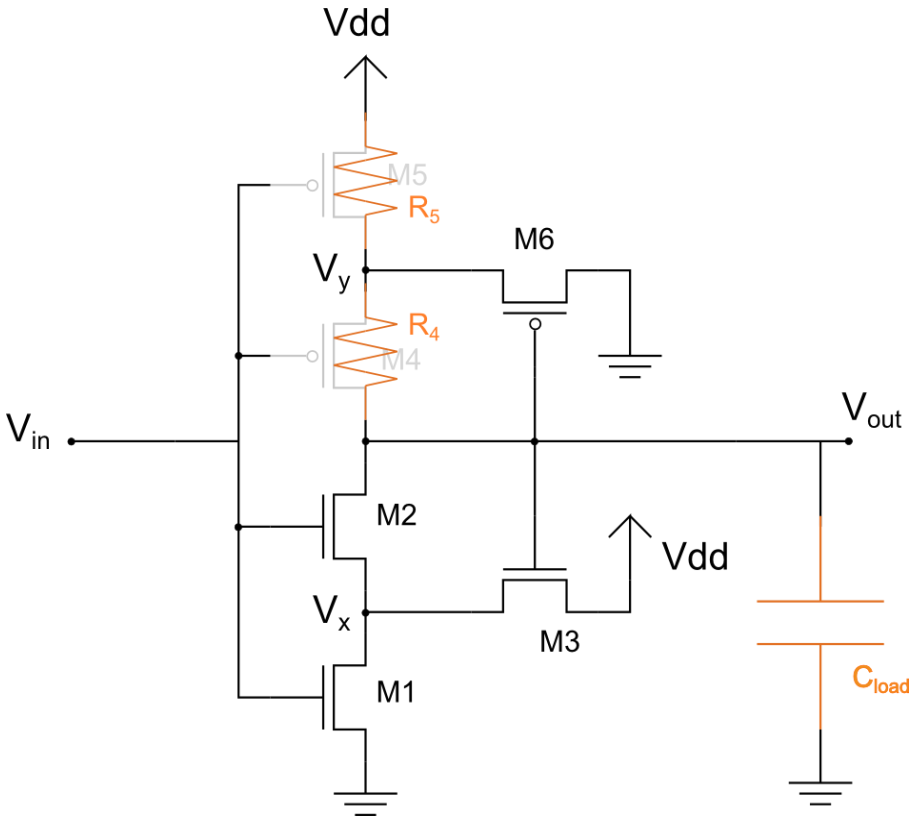

Figure 8: Schmitt trigger with load capacitance

The analysis for t_{plh} (Figure 9) is straightforward. At time 0, the value of the output voltage is 0 as well. The current $i(t)$ is given by (9), and that leads to a first-order differential equation. To solve it, the steps shown in equations (9)-(12) are shown.

$$i(t) = \frac{V_{dd} - V(t)}{R_4 + R_5} = -C_{load}\frac{dV(t)}{dt} \tag{9}$$

$$\frac{dV(t)}{V_{dd} - V(t)} = -\frac{dt}{C_{load}(R_4 + R_5)} \tag{10}$$

$$u(t) = V_{dd} - V(t) \tag{11}$$

$$-\frac{du(t)}{u(t)} = -\frac{dt}{C_{load}(R_4 + R_5)} \tag{12}$$

$$\ln\left(\frac{u(t_{plh})}{u(0)}\right) = \frac{t_{plh}}{C_{load}(R_4 + R_5)} \tag{13}$$

$$t_{plh} = \ln(2)\, C_{load}(R_4 + R_5) \approx 0.7\, C_{load}(R_4 + R_5) \tag{14}$$

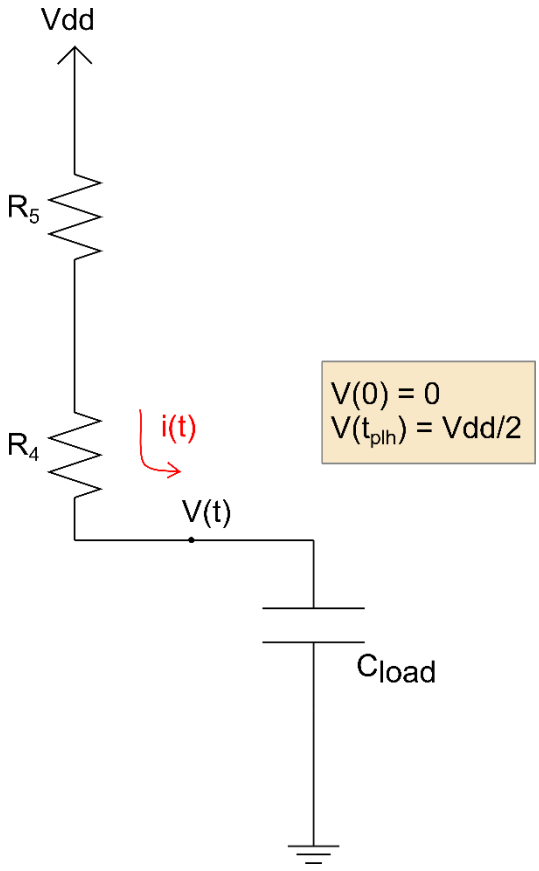

Figure 9: Equivalent RC circuit for calculating the rise time

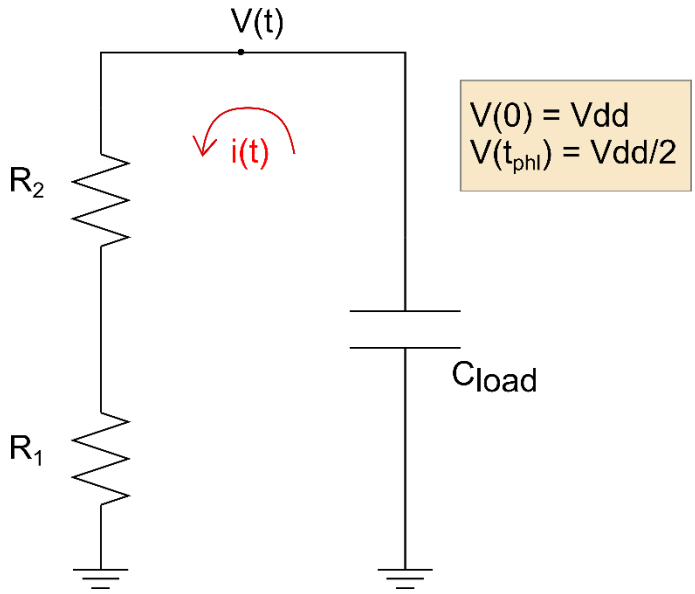

Figure 10: Equivalent RC circuit for calculating the fall time

For the calculation of t_{phl}, a similar procedure is implemented using the schematic of Figure 10: Equivalent RC circuit for calculating the fall time. The current $i(t)$ is calculated and shown in (15). Solving it in the same manner as done previously, the expression for t_{phl} is obtained in (16).

$$i(t) = -C_{load}\frac{dV(t)}{dt} = \frac{V(t)}{R_1 + R_2} \tag{15}$$

$$t_{phl} = \ln(2)\, C_{load}(R_1 + R_2) \approx 0.7\, C_{load}(R_1 + R_2) \tag{16}$$

Oscillator operation

Oscillators are extremely common and can be used in a variety of circuits. In this report, a voltage-controlled oscillator will be studied. The main goal for the oscillator of this design is to:

- Have equal “on” and “off” times. A symmetric signal is desired.
- Possess an acceptable waveform. The criteria for the timing requirements used in this report is shown in Table 1, found in an application note by Intel for the Pentium

processors [2]. This requirement puts the design in perspective. However, for it to operate as a clock signal in a real system, a vast amount of improvements are necessary and beyond the scope of this report.

Table 1: Clock signal quality specifications [2]

Symbol (5)	Parameter	Minimum	Maximum	Unit	Notes
	CLK Frequency	33.33	66.66	MHz	(1)
t2	CLK Period	15		ns	
t3	CLK High Time	4		ns	(2)
t4	CLK Low Time	4		ns	(3)
t5	CLK Rise Time	0.15	1.5	ns	(4)
t6	CLK Fall Time	0.15	1.5	ns	(4)
	CLK Stability		±250	ps	(6), (7), (8), (9)
	V_{IH}	2	V_{CC} + 0.3	V	
	V_{IL}	−0.3	0.8	V	

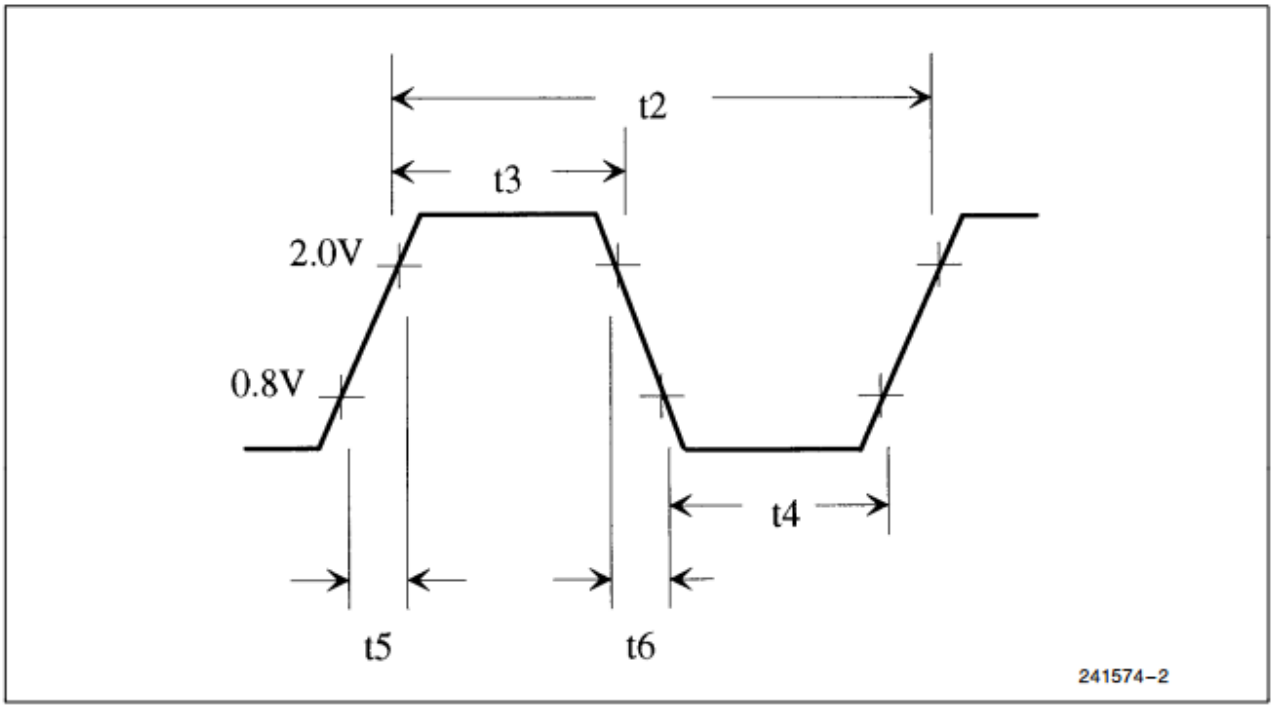

Figure 11: Clock requirements for the Pentium processor [2]

The oscillator schematic is shown in Figure 12: Voltage controlled oscillator, and consists of four different stages, which will be explained in this section.

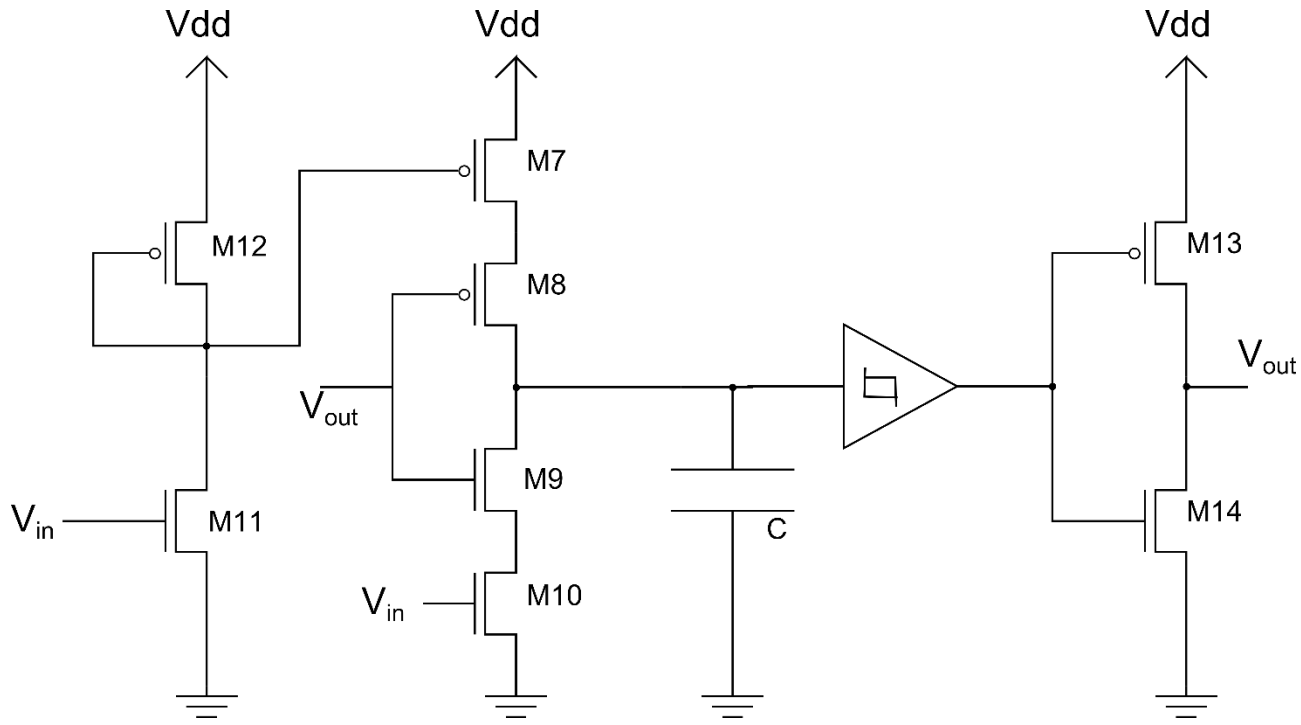

Figure 12: Voltage controlled oscillator

Voltage reference stage

The voltage reference circuit (Figure 13) is responsible for setting a constant voltage level to the next stage of the oscillator. When both transistors are saturated, a constant current flows through M11 and M12, depending only on the input voltage $V_{in.}$ It can be shown that the intermediary voltage between the two transistors is given by (17) as long as M11 is saturated, which happens as long as the conditions in (18) are met. If $\beta_1 = \beta_2$, then an increase in V_{in} will provide an equal decrease in V, which helps keep the input signals symmetric for the next stage.

$$V = -\sqrt{\frac{\beta_1}{\beta_2}}(V_{in} - V_{tn}) + V_{dd} + V_{tp} \tag{17}$$

$$\begin{matrix} V \geq V_{in} - V_{tn} \\ V_{in} \geq V_{tn} \end{matrix} \tag{18}$$

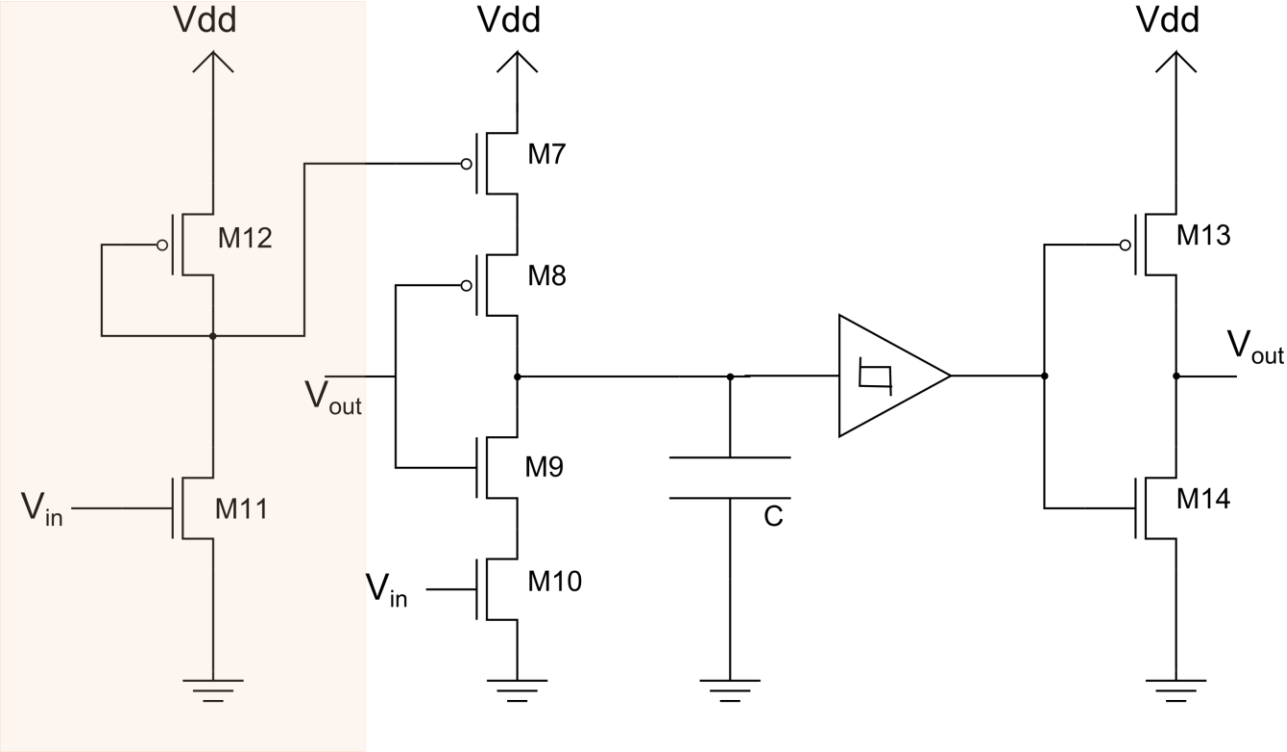

Figure 13: First stage of the oscillator

Current source stage

The second stage of the oscillator circuit provides a constant current charge/discharge path for the capacitor C. If the capacitor is discharged and V_{out} is low, then M7 and M8 will become conductive and charge the capacitor, until it reaches the Schmitt trigger voltage V_{sph}. Once this happens, the feedback signal V_{out} becomes high, and then transistors M9 and M10 are switched on, providing a discharge path. This happens until the voltage at the capacitor reaches V_{spl}, which will cause V_{out} to become high again. This illustrates the operation of the oscillator, but a few considerations must be taken into account.

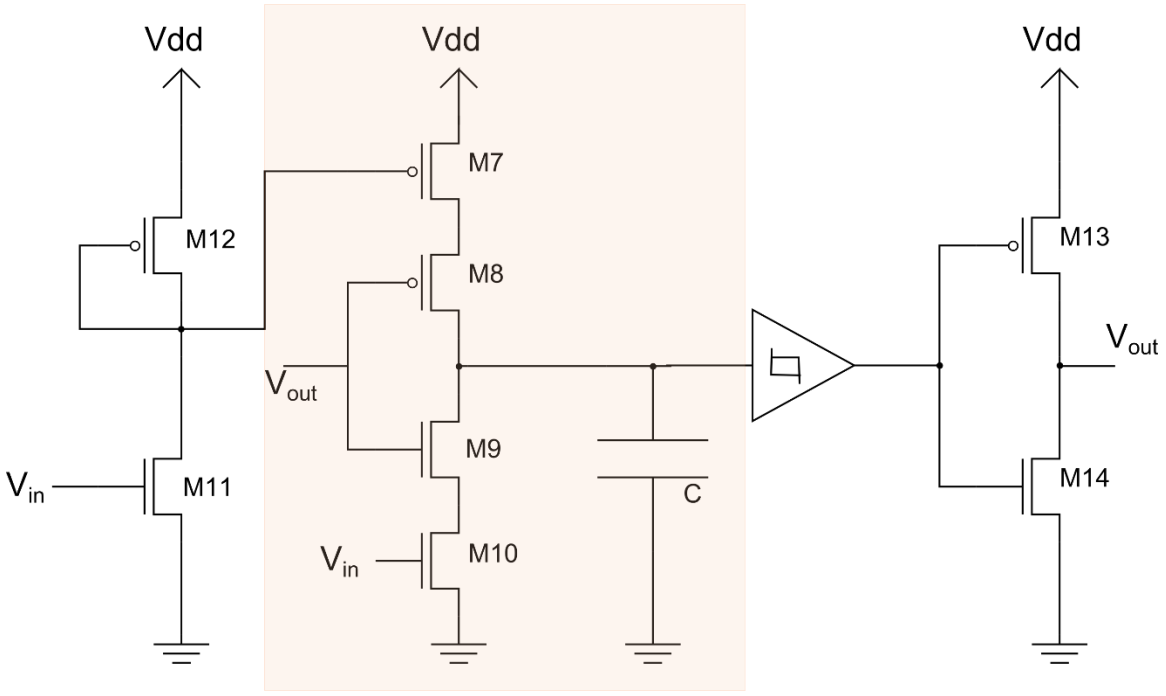

Figure 14: Second stage of the oscillator

1. **The current is not always constant.** It is only the case if the transistors M7 (or M10) are saturated. This is a strong assumption, because depending on the conditions for the voltages V_{gs}(M10) and V_{gs}(M7), this may not be the case. The expected behavior for a constant current source is that the capacitor charges/discharges uniformly, with the voltage increase/decrease following a straight line. If the transistors are operating in the resistive region, then the "equivalent resistance" of the charge/discharge path will vary with the voltage, creating an "exponential RC" kind of charge/discharge.
2. **Symmetry is not guaranteed.** In the constant-current operation, the currents for the M7-M8 and M9-M10 paths must be equal for the given V_{in}. This will cause the capacitor to charge and discharge at an equal manner. If the transistors are operating in the resistive region, then their exponential behavior also must be similar in order to produce the desired symmetric waveform. As will be seen in a future section, this becomes a design tradeoff.

Schmitt trigger stage

This stage has already been characterized previously (page 2), but a few design considerations will be included. It is important that the trigger threshold voltages V_{sph} and V_{spl} are symmetrical. They will determine the "window" of charging and discharging of the capacitor voltage of the previous stage. A well designed Schmitt trigger must be considered for this purpose. Also, it is important that the rise and fall times are small enough in order to produce quick switching response.

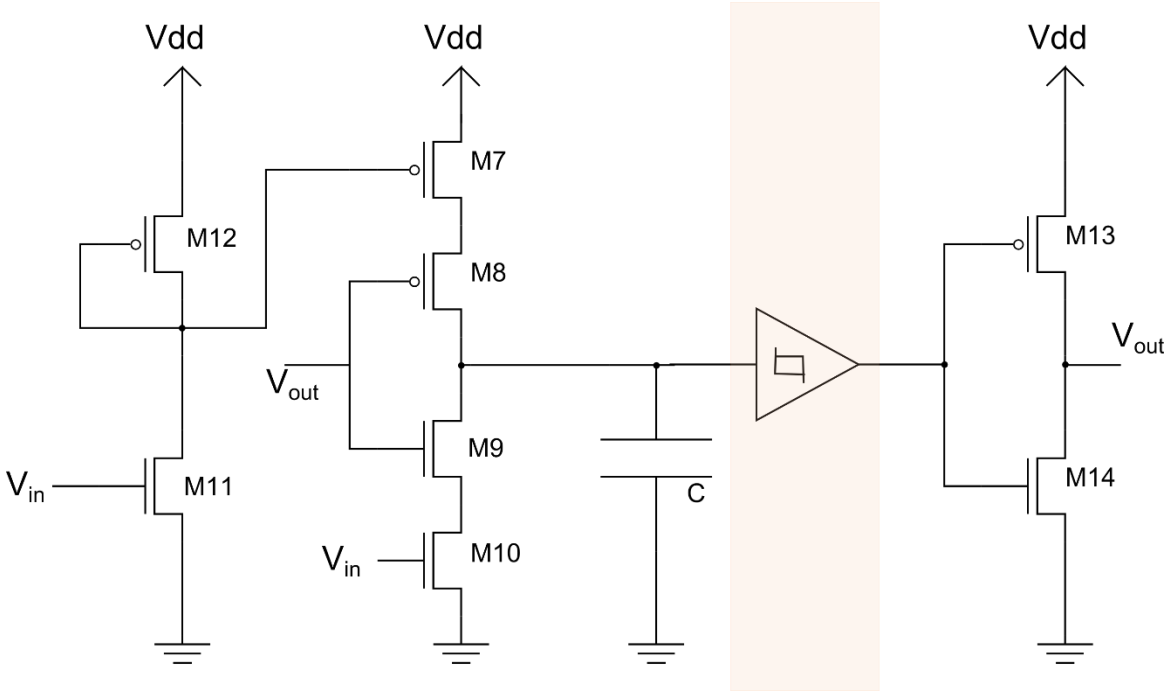

Figure 15: Third stage of the oscillator

Inverter stage

The inverter is the last stage, and is responsible for creating the positive feedback required to achieve the desired functionality. Without the inverter, the feedback signal V_{out} does not trigger the charge/discharge paths in the second stage. The most significant design requirement for this stage of the circuit is that the rise/fall times be made as low as possible.

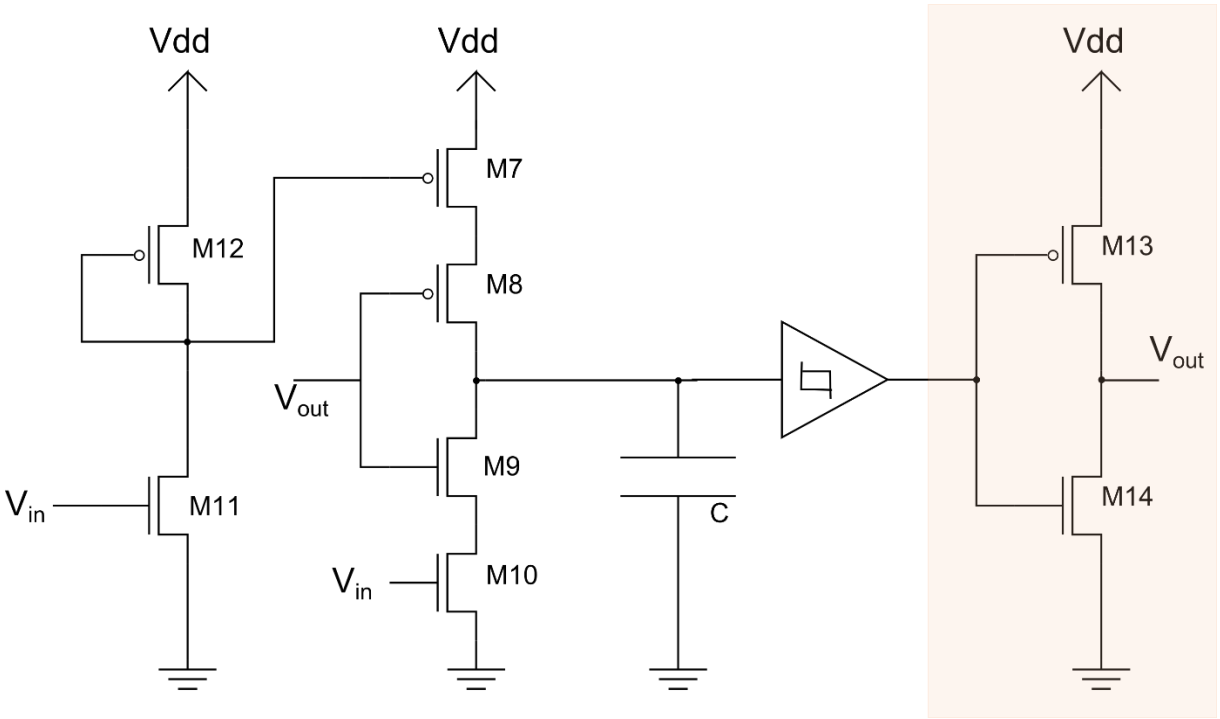

Figure 16: Fourth stage of the oscillator

Circuit Design and Simulation

With the circuit properly characterized in the previous section, the design of the circuit will be made. The entire circuit will be simulated in the LTSPICE simulation environment, using a complete model of the NMOS and PMOS transistors. Calibration in the transistor dimensions will be made in the oscillator circuit stages until the circuit waveform meets the desired specifications. Then, the circuit mask diagram will be implemented and simulated in Microwind, using 1.2um technology.

LTSPICE simulation

Schmitt trigger circuit

The Schmitt trigger was chosen to satisfy the parameters shown in Table 2. The trigger threshold voltage levels provide a symmetrical input/output transfer characteristic, and the low rise/fall times are create a satisfactory waveform response. Using these values and the transistor simulation values (Table 3) in equations (4) and (8), the transistor gain ratio is obtained, shown in (19).

$$\frac{\beta_1}{\beta_3} = 0.245\,, \frac{\beta_5}{\beta_6} = 0.271 \tag{19}$$

Table 2: Schmitt trigger specifications

Parameter	Value
Supply voltage (V_{dd})	5[V]
V_{sph}	3.5[V]
V_{spl}	1.5[V]
Rise time (t_{plh})	2[ns]
Fall time (t_{phl})	2[ns]

Table 3: LTSPICE transistor simulation parameters

Parameter	Value (V)
V_{tp}	-0.9
V_{tn}	0.6

Running the LTSPICE simulation (Figure 17) with the gain ratios calculated in (19), the response shown in Figure 18 is obtained. It is noted that the trigger voltage values are very different from the ones expected. This does not come as a surprise, given the complexity of the transistor model being used. The formulas used to obtain the expressions in equations (4) and (8) are based on greatly simplified models.

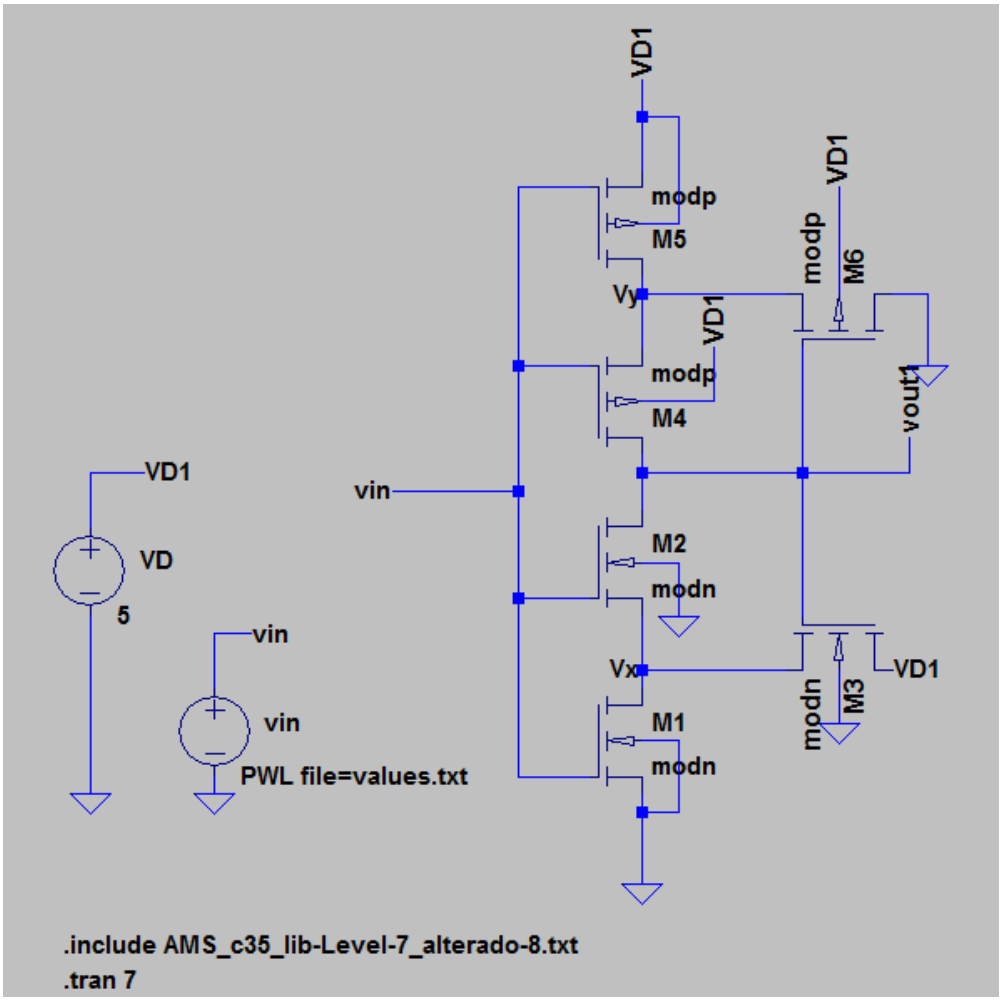

Figure 17: LTSPICE Schmitt trigger simulation

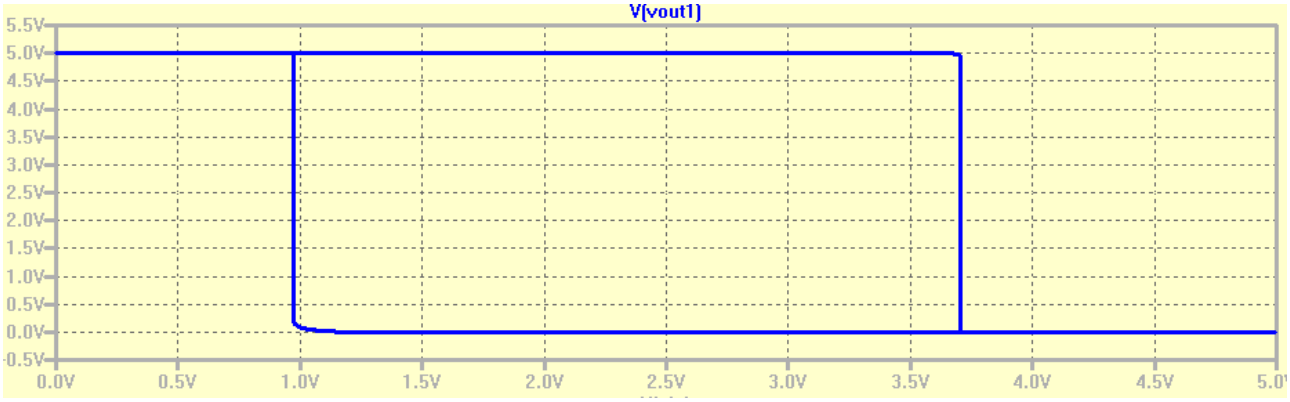

Figure 18: Schmitt trigger voltage transfer characteristic with calculated parameters

This is not the desired response. It also does not take into account the actual technology dimensions that will be simulated in Microwind. To obtain these values, a manual calibration was done in the channel width (W) and length (L) parameters. The values obtained are listed in Table 4, and the voltage transfer curve is shown in Figure 19.

Table 4: Transistor gains used in final LTSPICE simulation

Transistor	W (um)	L(um)
M1	2.4	2.4
M2	2.4	2.4
M3	2.8	6.6
M4	4.8	1.2
M5	4.8	1.2
M6	10.8	1.2

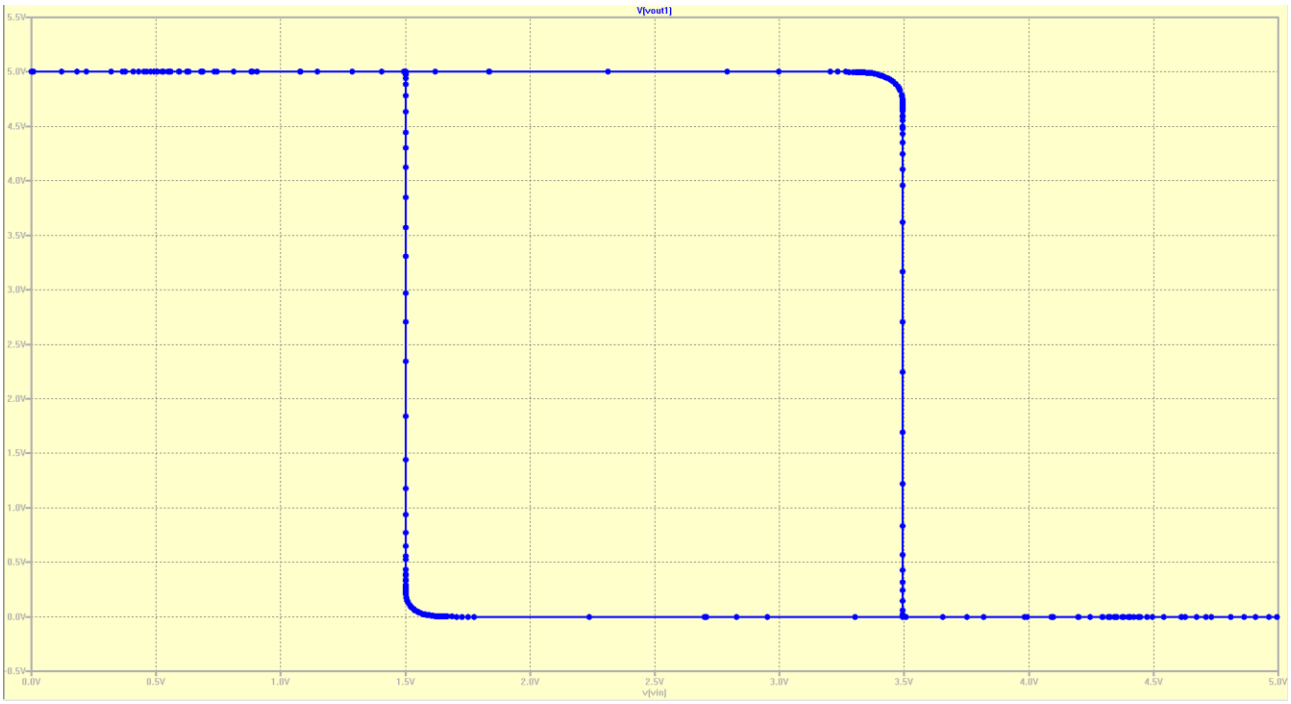

Figure 19: Final LTSPICE Schmitt trigger voltage transfer curve

Oscillator circuit

The oscillator circuit was implemented (Figure 20), and simulated. Figure 21 contains the simulation results. Even though the Schmitt oscillator is fairly symmetric (the voltage at the capacitor output switches at 1.5V and 3.5V), the resulting waveform is not. By observing the capacitor waveform, it is concluded that the capacitor is discharging too fast, which means that the NMOS transistor gains are high, when compared to the PMOS gains. To fix this, the PMOS transistor gains were increased, obtaining the result indicated in Figure 22. The choice of capacitance and the effect of altering the input Vin will be studied.

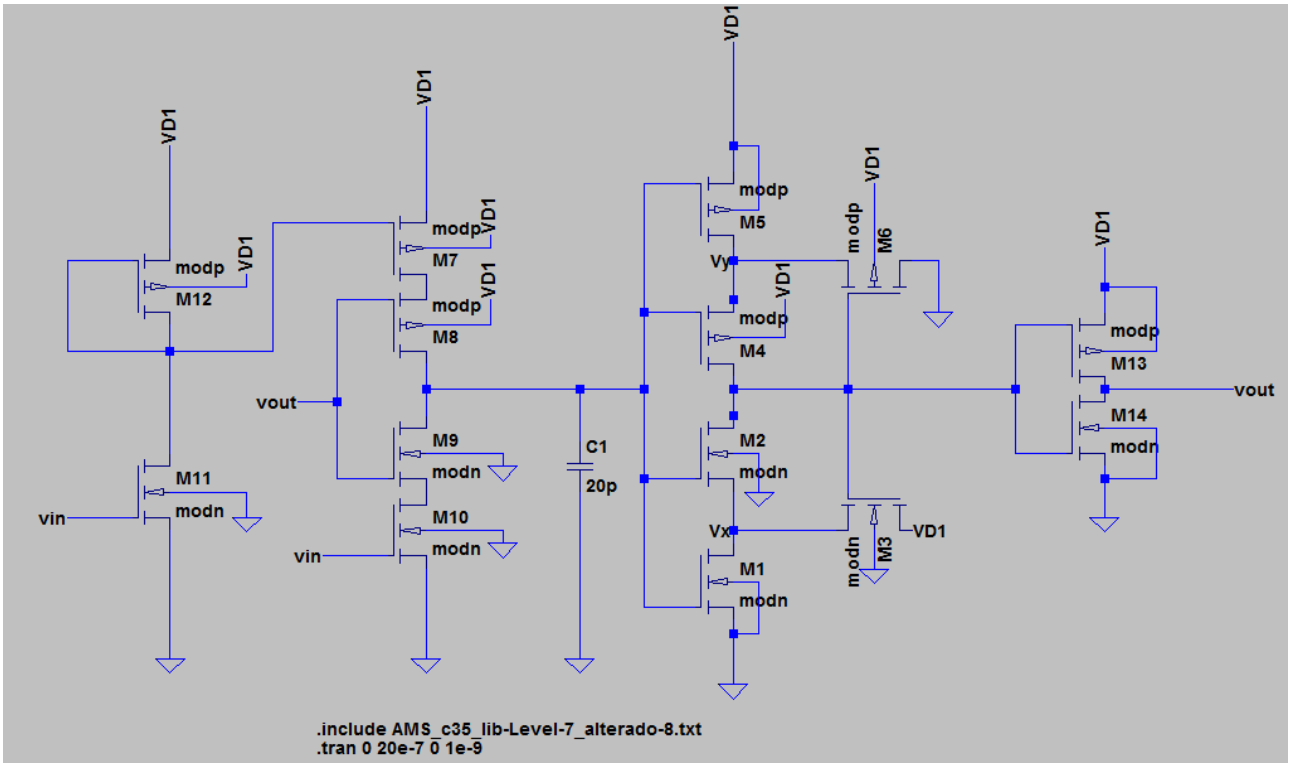

Figure 20: Oscillator circuit simulation

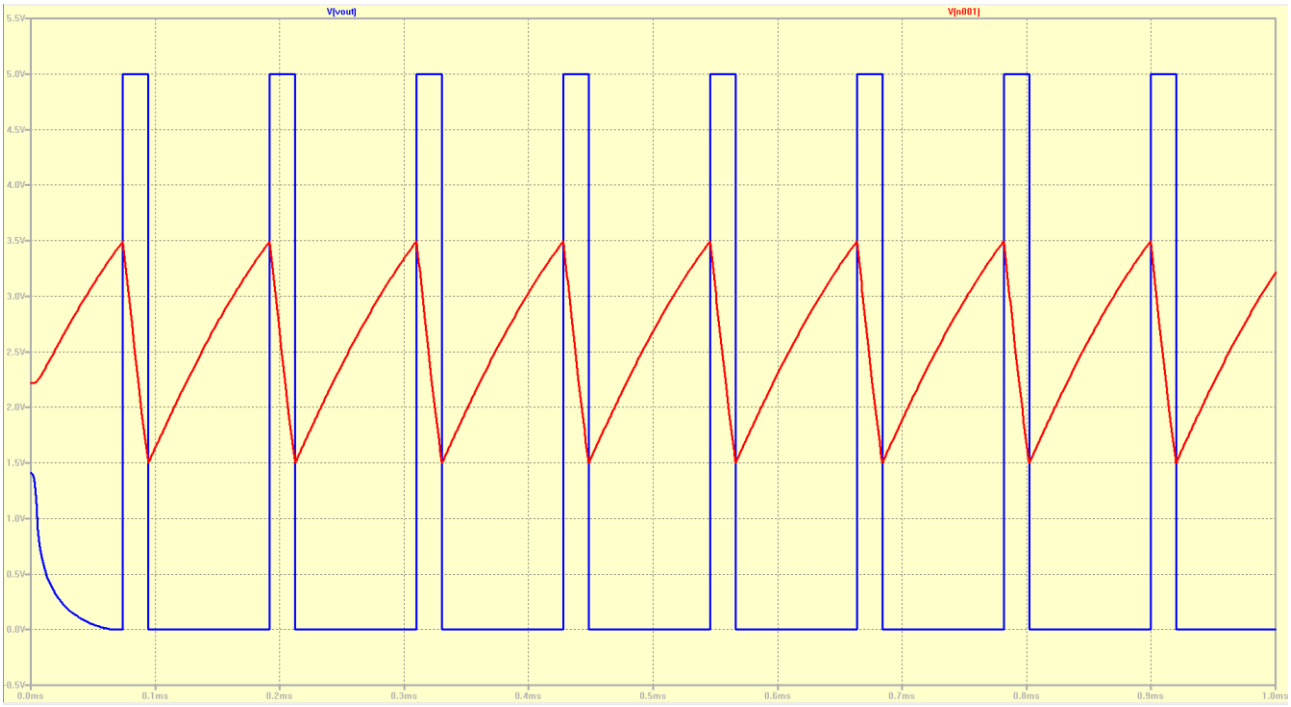

Figure 21: Resulting waveforms. Orange: voltage at capacitor, Blue: voltage at Vout

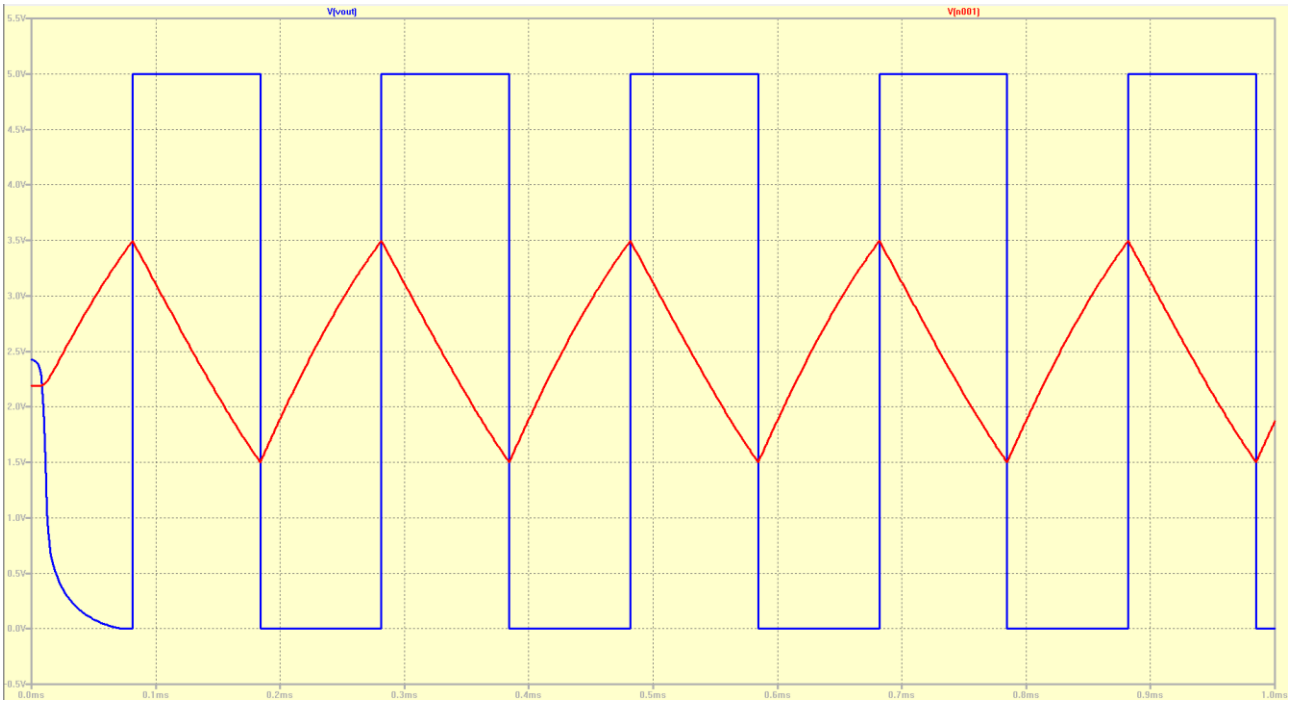

Figure 22: Waveform after transistor gain correction

1. **Effect of Vin on frequency and rise/fall times**.

The chosen values of capacitance for analysis were: C = 5pF, C = 10pF and C = 20pF. These give frequency oscillations in the MHz scale, which are close to the desired value. Table 5 was created using these simulations in order to determine the expected frequency value and the rise/fall times.

It is worth specifying how the rise/fall times were estimated. First, the time where the difference between 0[V] and 5[V] becomes 0.3[V] is recorded. Then, the approximate time when the voltage reaches 2.5[V] is captured, and the subsequent difference between these two times will yield the rise/fall time. Figure 23 indicates this procedure.

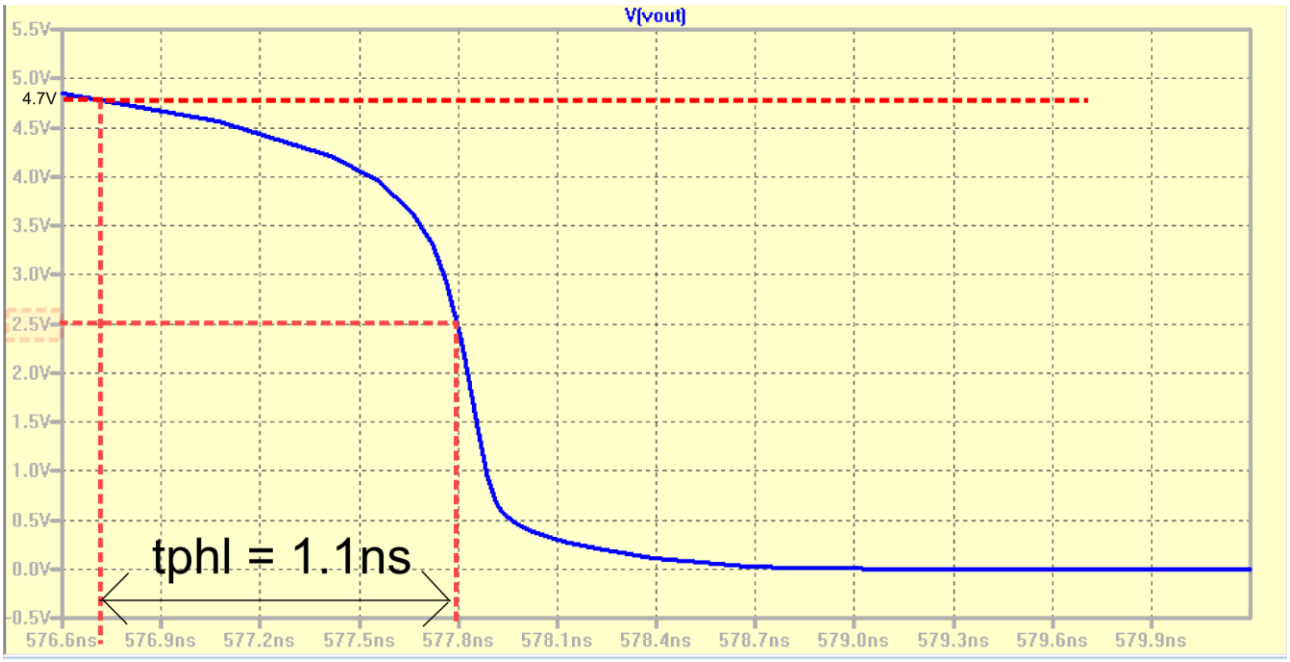

Figure 23: Example of how t_{phl} is calculated.

Table 5: Frequency and rise/fall time values based on capacitance and Vin levels

	Vin [V]	Frequency (MHz)	Fall time (ns)	Rise time (ns)
C = 5pF	1	5.95	1.0	0.5
	2	27.03	1.1	0.6
	3	38.5	0.8	0.5
	5	41.67	0.8	0.6
C = 10pF	1	3.25	0.9	0.8
	2	14.93	0.9	0.6
	3	22.7	1.1	0.7
	5	25.3	0.7	0.5
C = 20pF	1	1.72	1.1	0.8
	2	8.7	1.2	0.6
	3	12.82	0.8	0.5
	5	14.28	0.8	0.5

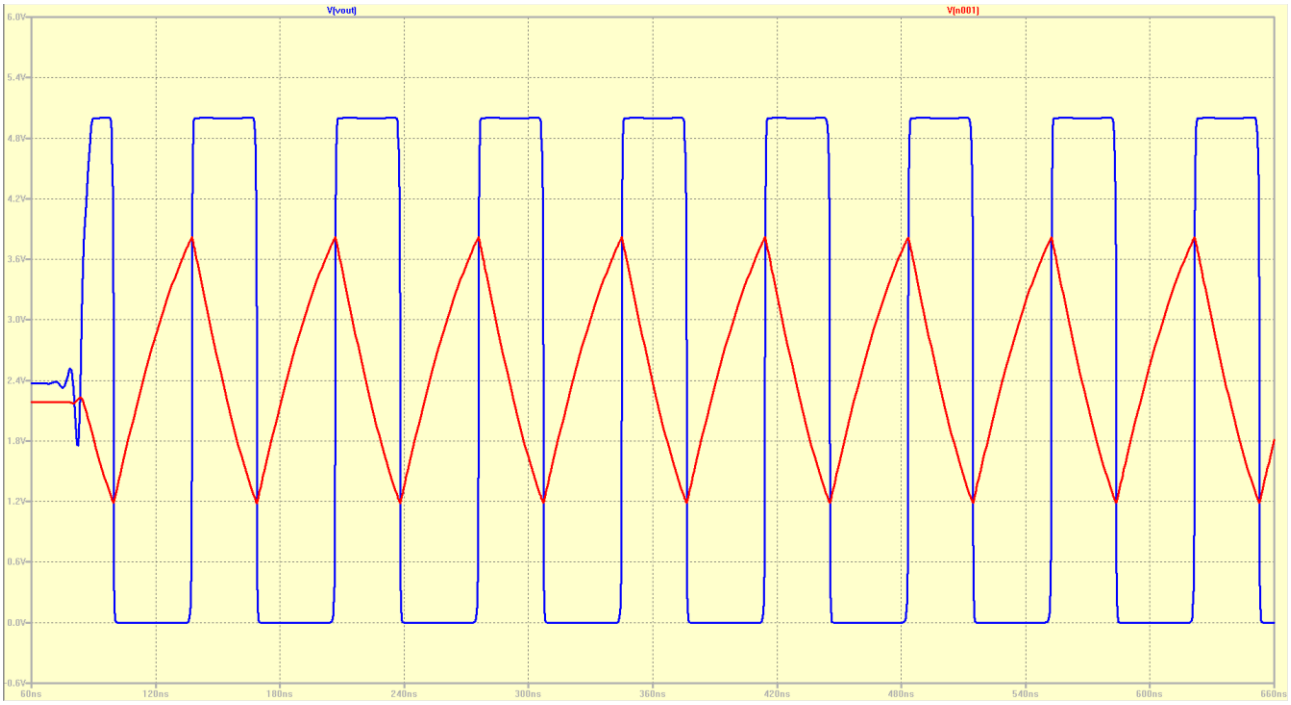

Figure 24: Simulation for Vin = 5[V]

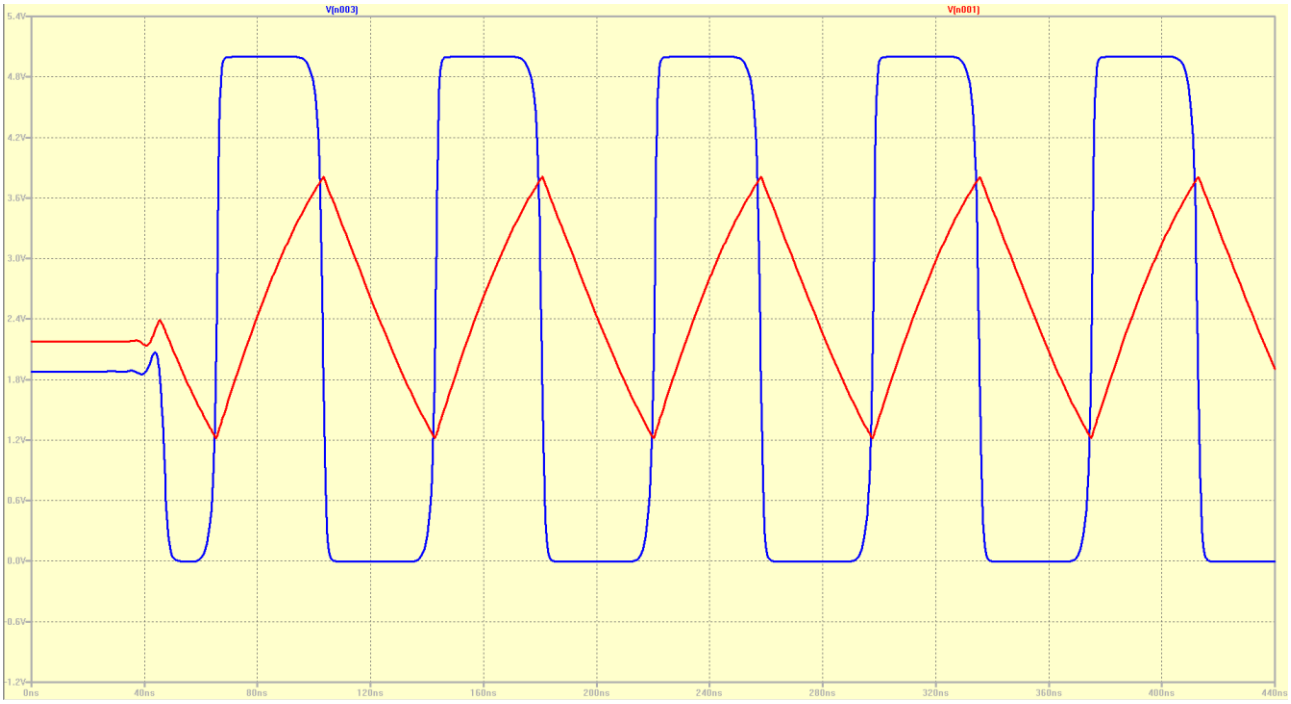

Figure 25: Simulation for Vin = 3[V]

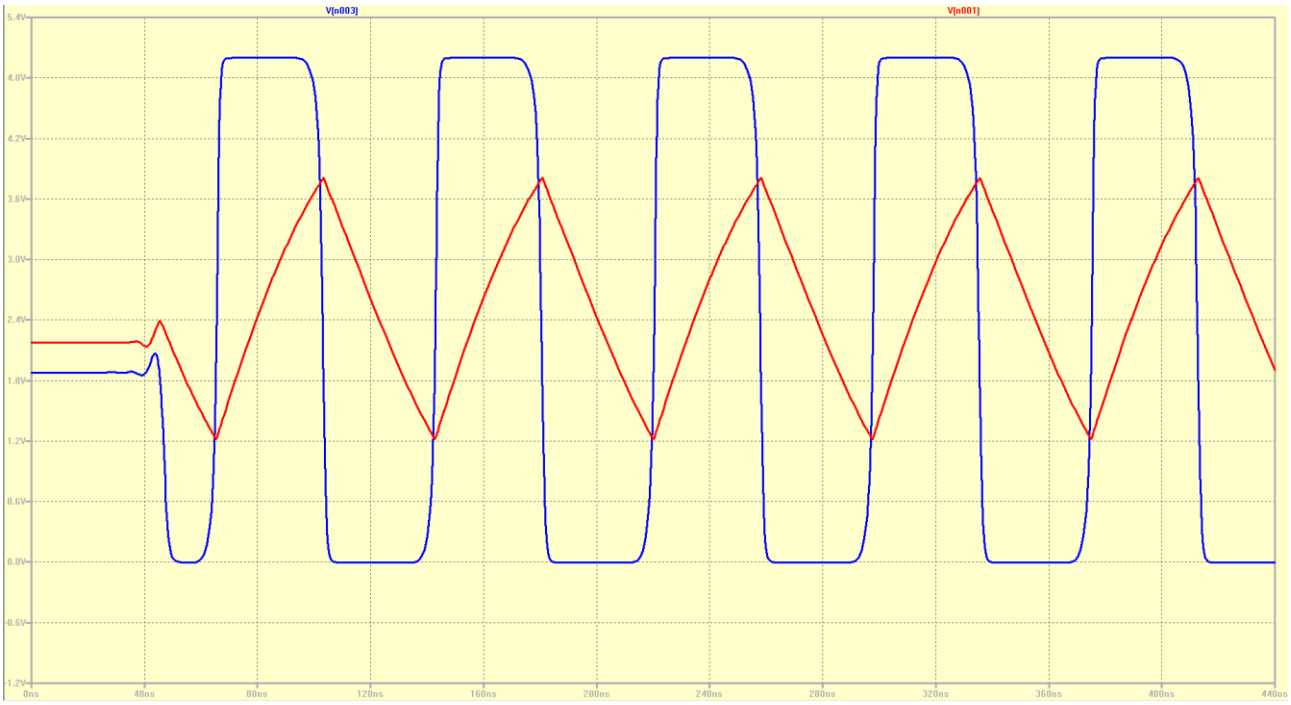

Figure 26: Simulation for Vin = 2[V]

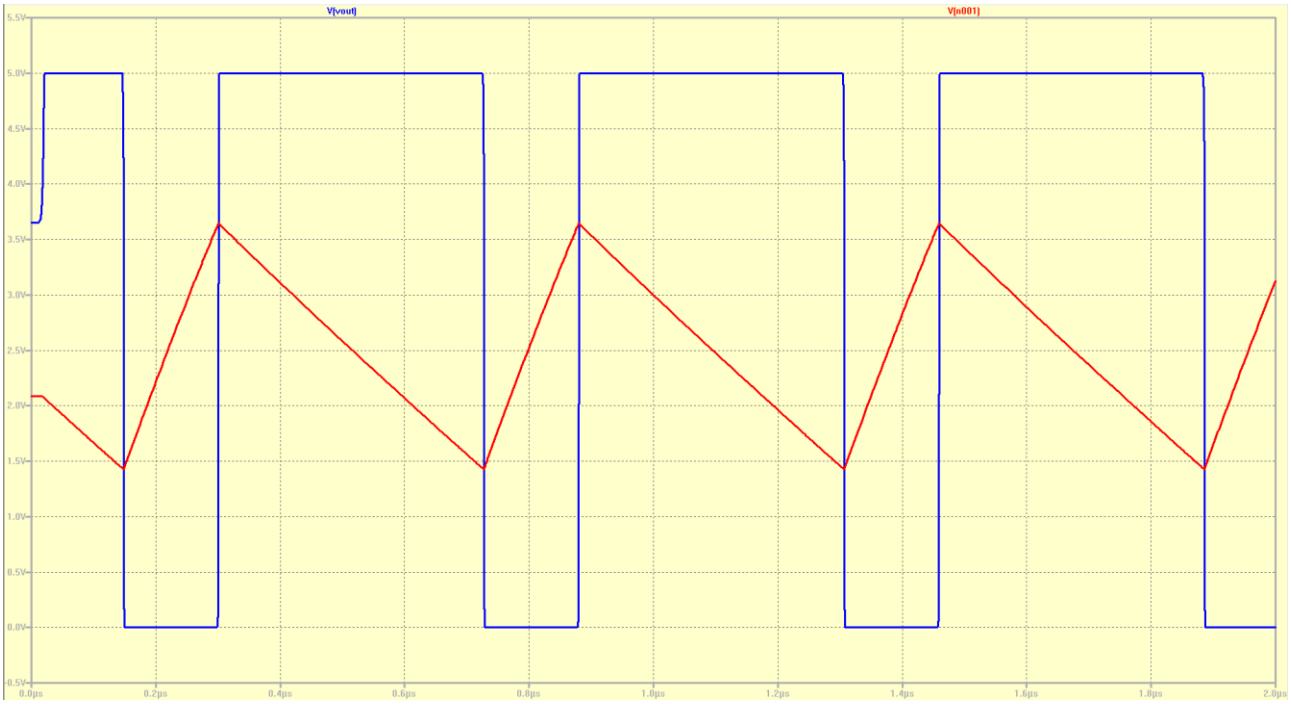

Figure 27: Simulation for Vin = 1[V]

2. Effect of Vin on signal symmetry.

It can be seen from the examples for C = 20pF (Figures 24-27) that the signal loses its symmetry as the frequency is decreased. This happens because of the transistor saturation effect discussed in the "current source" stage description (page 13). If the intended purpose of the circuit is to operate in these lower frequency regions, then a different transistor gain calibration procedure must be studied. Since higher frequencies are required for the intended application, then this procedure will not be addressed.

Remarks

Considering the results obtained by simulation, the following comments are worth making:

1) It is important to consider another possibility: drastically reduce the capacitor size, so as to operate on lower V_{in} to achieve similar frequency values. This approach was considered because the author suspected that if the capacitor is discharged with a constant current source (such as in Figure 27), then the rise/fall times would be quicker. However, no considerable difference in these transition delays were noted in the simulations, so this was not investigated further.
2) The symmetry of the Schmitt trigger may seem to not be important, since one can always compensate for the eventual asymmetries by changing the transistor gains of the preceding stage accordingly. The problem with this approach is that (a) the capacitor voltage might reach values above V_{tn} and below V_{tp}-V_{dd}, effectively stopping operation and (b) the rise/fall times would be very different from each other. It can be seen from Figure 18 that the low-high transition is not as sharp as the high-low one, while the same observation cannot be made for the curve shown in Figure 19.

Microwind Simulation

Initial Schmitt trigger implementation and discussion

With the transistor dimensions of Table 4: Transistor gains used in final LTSPICE simulation, the Schmitt trigger circuit shown in Figure 17 was implemented in Microwind, using the "CMOS12.RUL" foundry file. The circuit did not achieve the results obtained by the LTSPICE simulation. This, however, is expected - for two reasons:

1) The LTSPICE MOSFET simulation parameters are not specifically the same as the ones used in Microwind.
2) Even if they were based on the same technology, there is still a plethora of effects unaccounted for, such as transmission line dimensions, substrate dimension, metal contact capacitance, etc.

That being said, this observation does not remove the necessity of performing the LTSPICE simulations. First of all, the circuit simulation accounts for more nonlinearities and parasitic effects than the standard model used to find the gain ratio equations. If they posed a potential serious problem, then valuable time wouldn't be wasted implementing the circuit on Microwind. Secondly, a general estimate of the required transistor dimensions is achieved. As will be discussed in this section, the dimensions used in the final result were different, but they still held some basic properties (e.g. M3 having larger gain than M1 and M2, etc.), so the effort of calibrating the waveforms in Microwind was substantially reduced. Lastly, a general "intuition" is gained in the SPICE simulation. The effects of changing the transistor gains become more intuitive, making it easier to decide if the transistor gain should be increased or decreased, depending on the observed signals.

The transistor dimensions for the Schmitt trigger were then adjusted, according to the simulation results, resulting in Figure 28. The trigger voltage levels obtained are $V_{sph} = 3.525[V]$ and $V_{spl} = 1.478[V]$, which are very close to the desired result. The hysteresis curve for the designed Schmitt trigger can be seen in Figure 29.

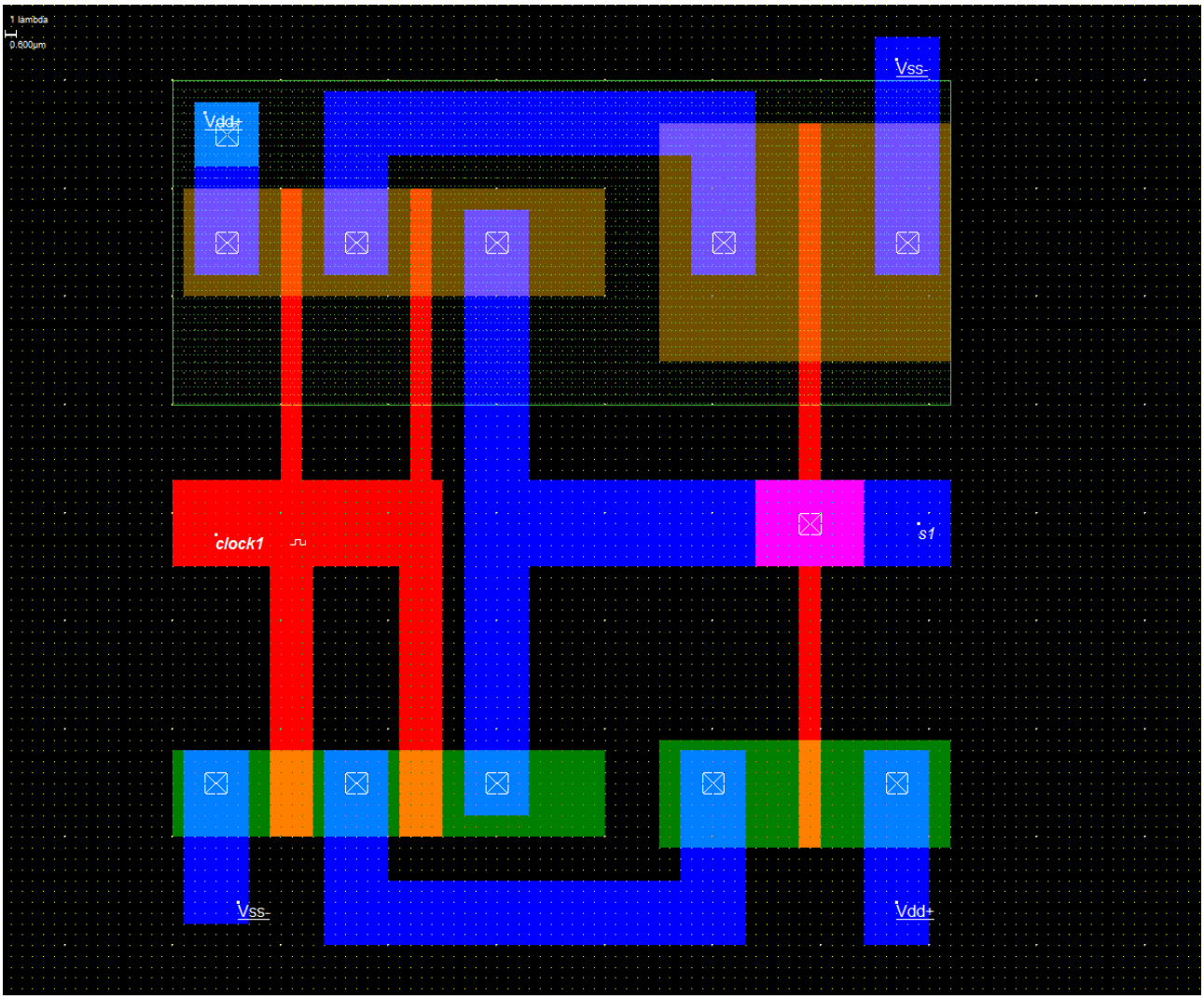

Figure 28: Mask diagram for the calibrated Schmitt trigger

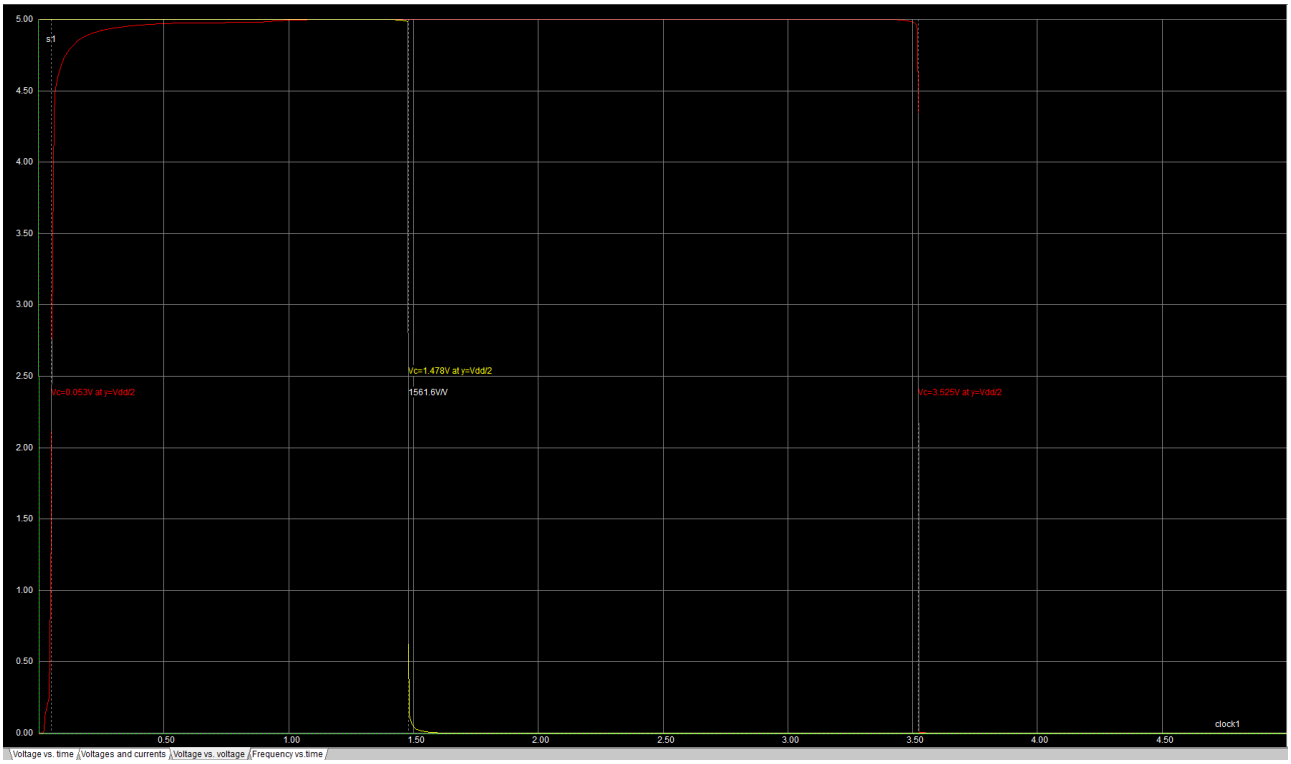

Figure 29: Values obtained: ***Vspl = 1.478[V] and Vsph = 3.525[V]***

Oscillator circuit implementation and simulation

The oscillator circuit is then implemented, shown in Figure 20. The oscillation waveforms obtained in Figure 31, Figure 32, Figure 33 for different capacitance values, for Vin = 3[V]. It is evident that the waveforms are asymmetric. Additionally, as can be estimated from Figure 34, the rise time is approximately 3.6[ns], which is larger than the established 2[ns] maximum. The circuit also occupies too much area, which is undesirable.

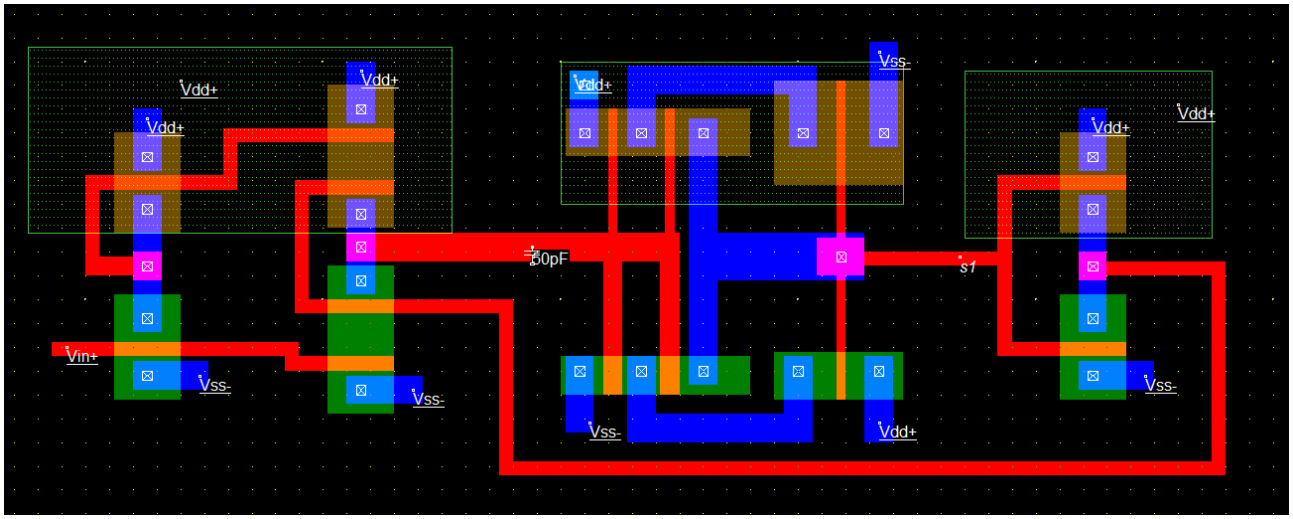

Figure 30: Oscillator circuit mask diagram

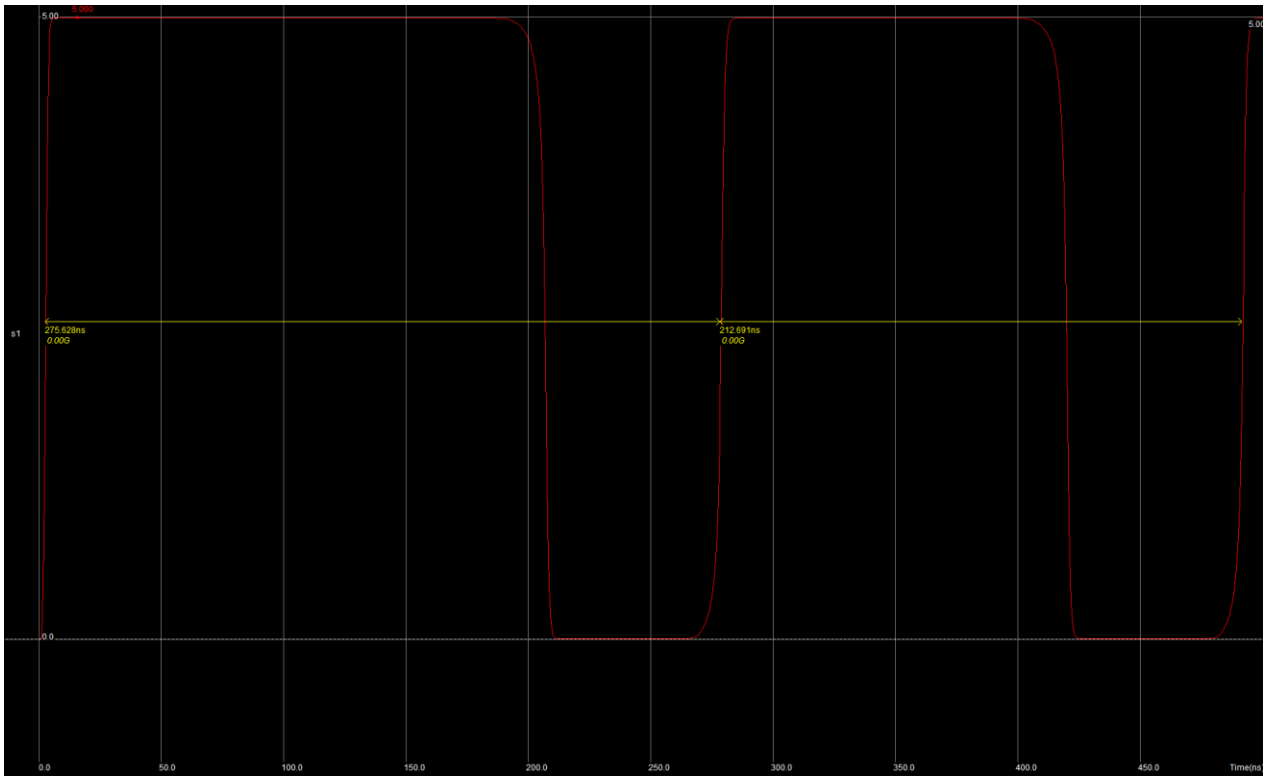

Figure 31: Oscillation for C = 50pF. Frequency is approximately 4.7MHz

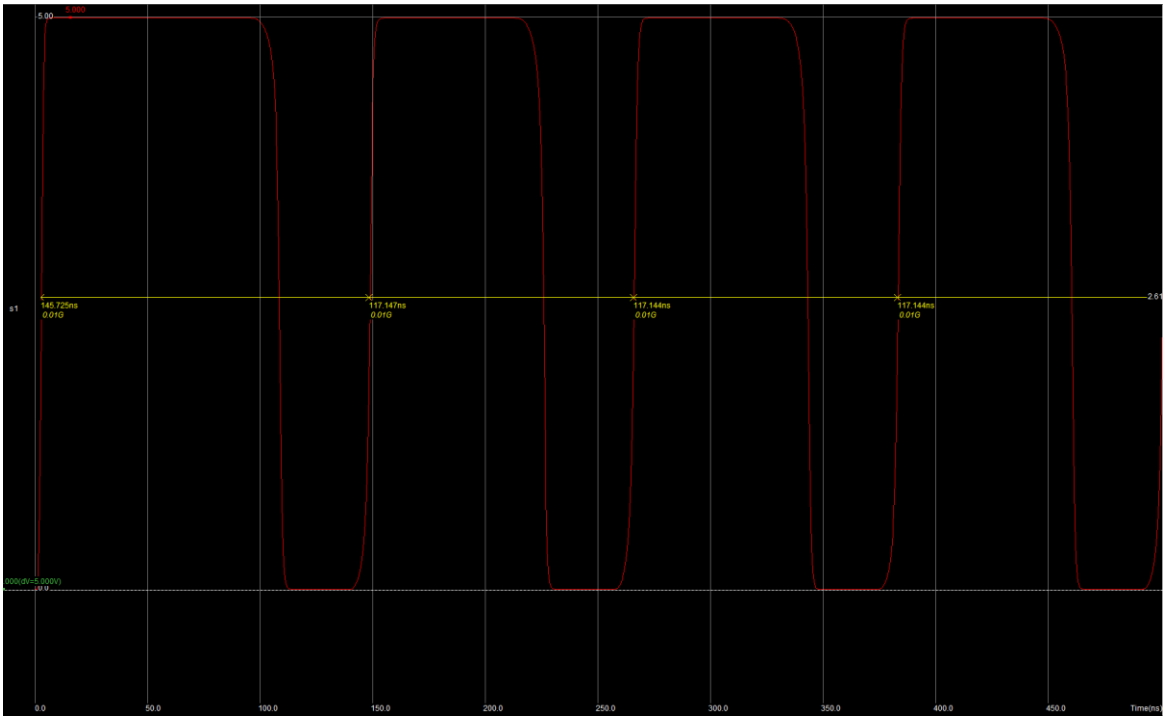

Figure 32: Oscillation for C = 20pF. Frequency is approximately 8.5MHz

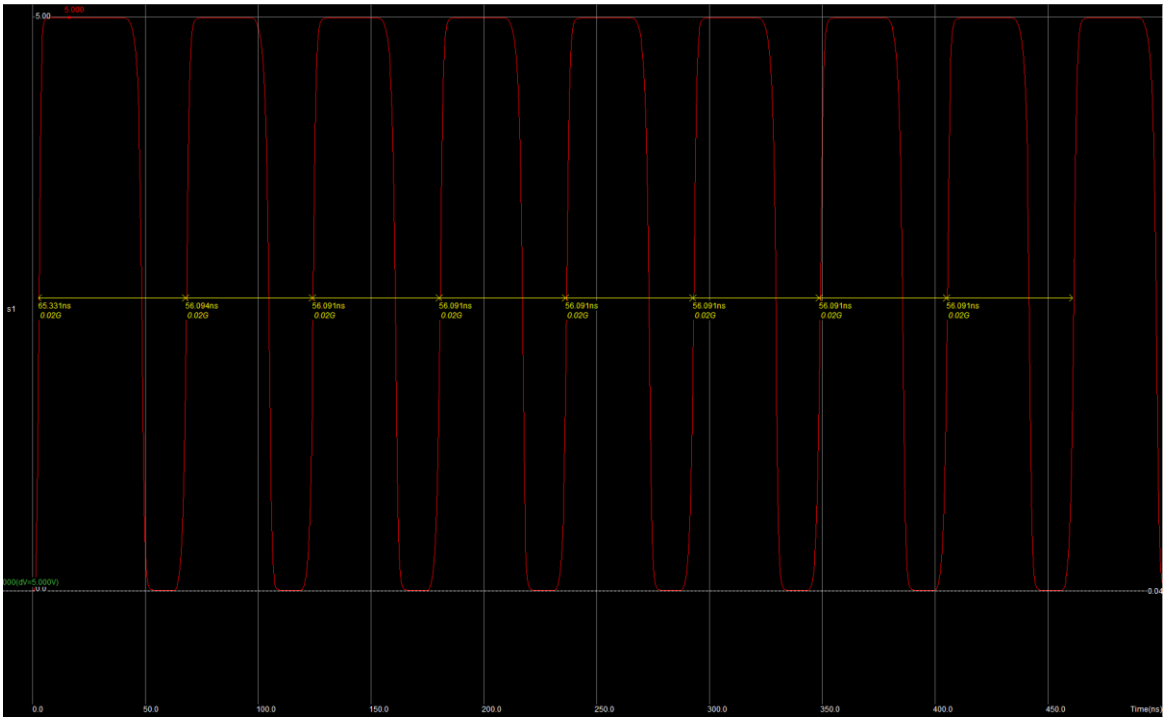

Figure 33: Oscillation for C = 10pF. Frequency is approximately 17.8MHz

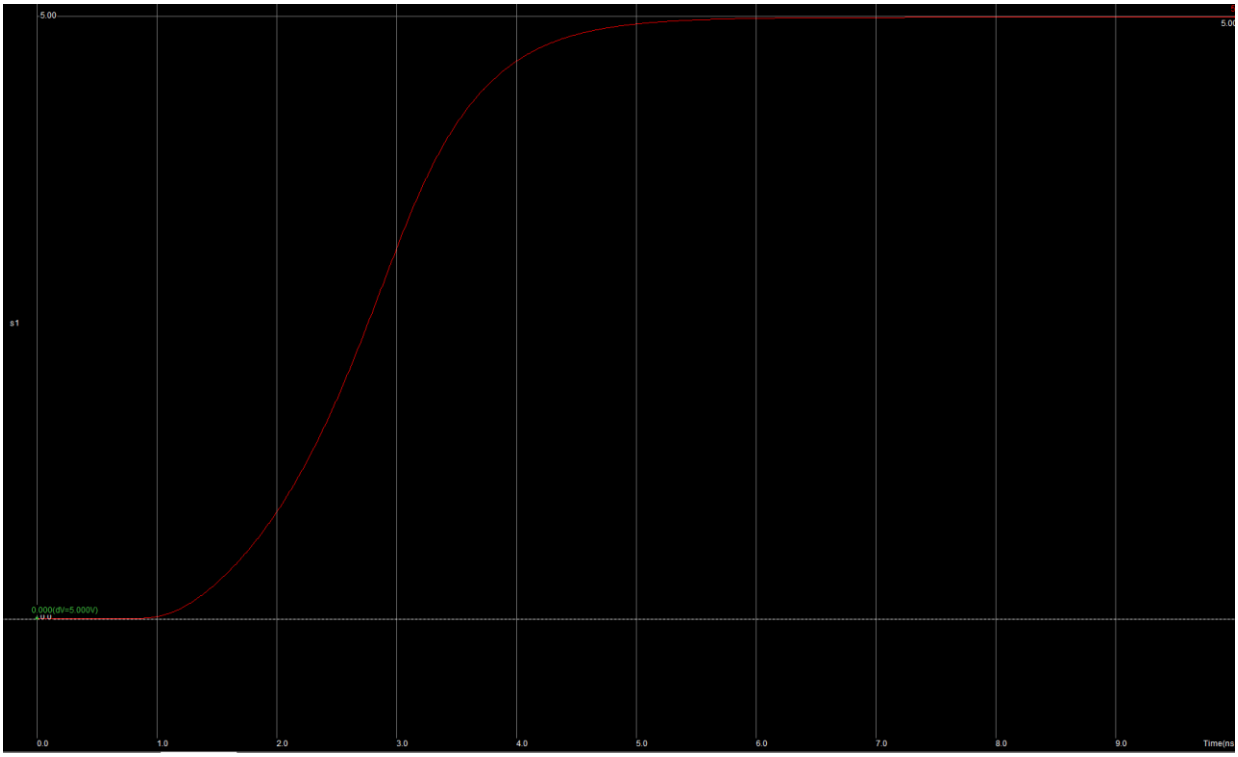

Figure 34: Rise time seen is approximately 3.6ns

Final oscillator implementation

The circuit was then optimized to occupy less area and to fix the problems discussed in the previous implementation. The final result is shown in Figure 35. The chosen capacitance was C = 2pF, due to the observed results. Figure 36 shows the oscillations obtained at the output for Vin = 3[V]. Figure 37 and Figure 38 show the oscillations for Vin = 5[V] and Vin = 1[V], respectively. It can be seen that the “asymmetry” effect on lowering Vin is also observed in this simulation. This highlights one of the mentioned aspects regarding the importance of simulating the circuit in SPICE

before making a mask diagram: the familiarity with the circuit. This effect does not come as a surprise and does not imply that a mistake was made in making the diagram.

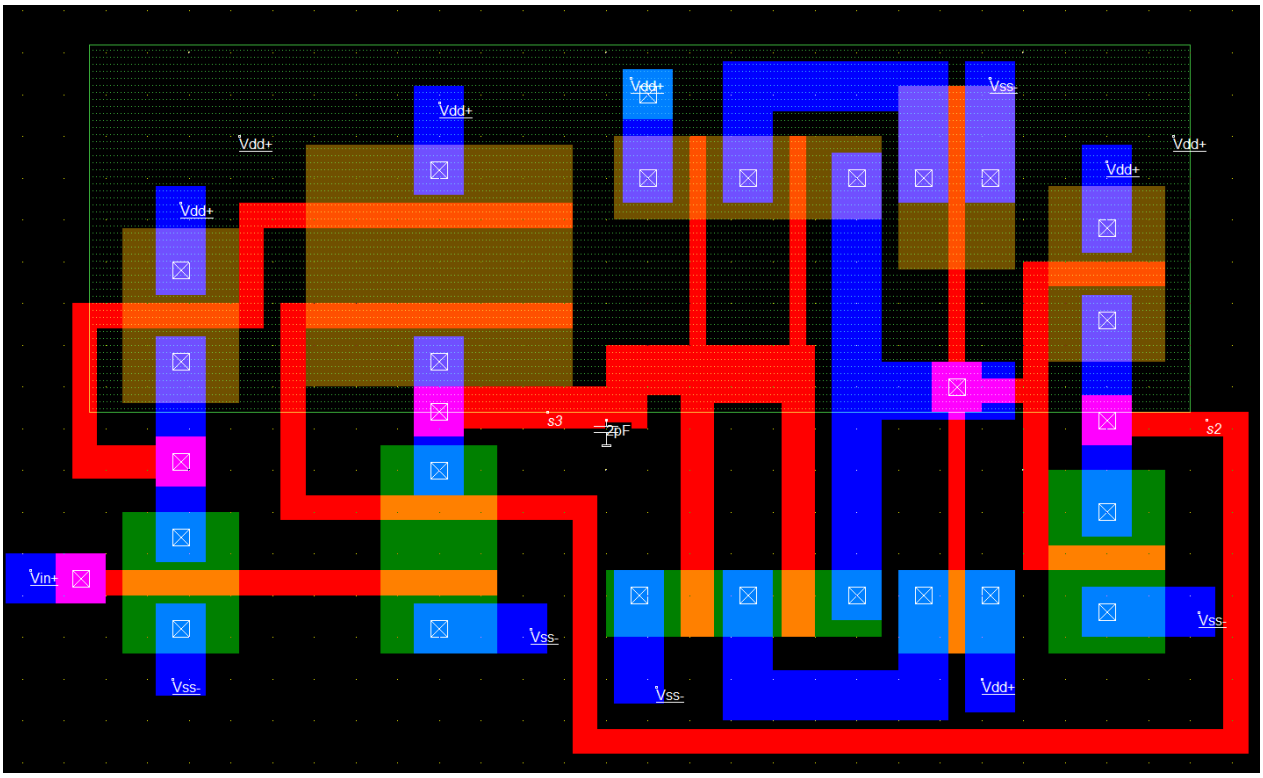

Figure 35: Final circuit mask diagram

Figure 39, Figure 40, Figure 41, and Figure 42 show that the timing requirements in Table 1: Clock signal quality specifications are met. These figures were obtained using Vin = 3[V], but it was observed that the timing requirements are also satisfied for Vin = 5[V].

Finally, Figure 43 shows the oscillation frequencies obtained by varying the input voltage. This is an interesting result, and can be used to estimate the voltage required for a given frequency value.

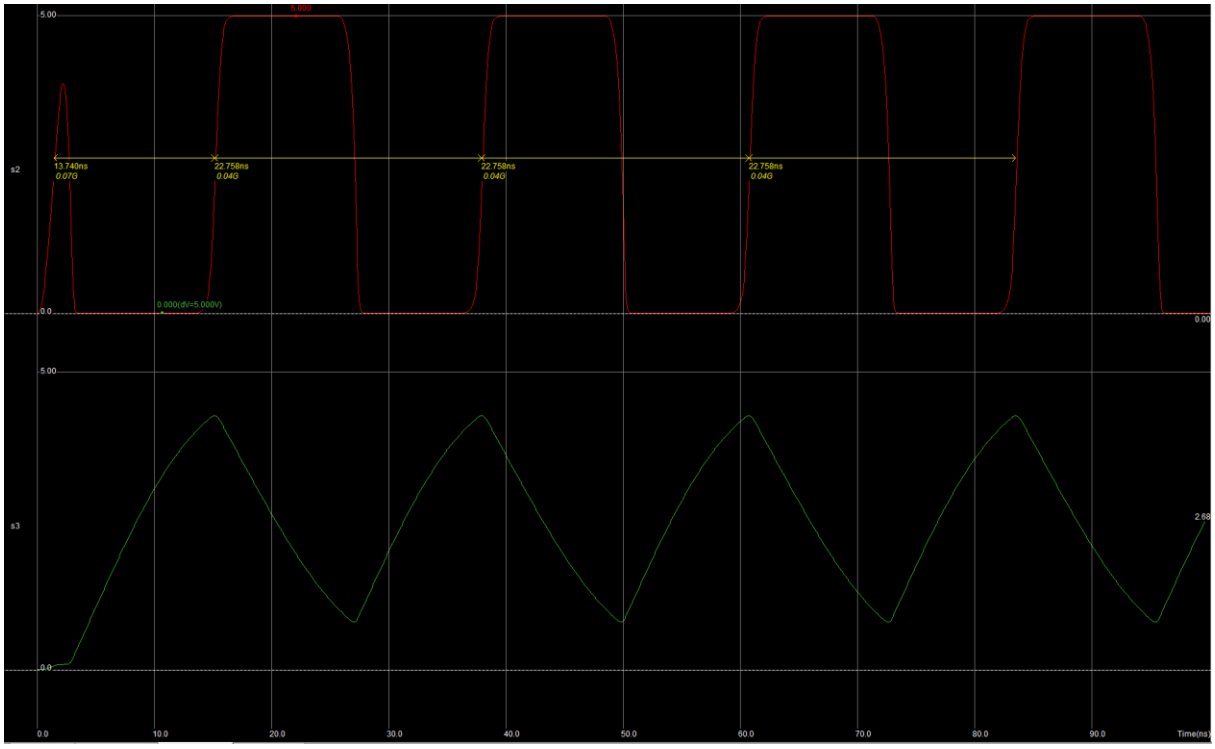

Figure 36: Oscillation frequency is 43.93 MHz for Vin = 3[V]

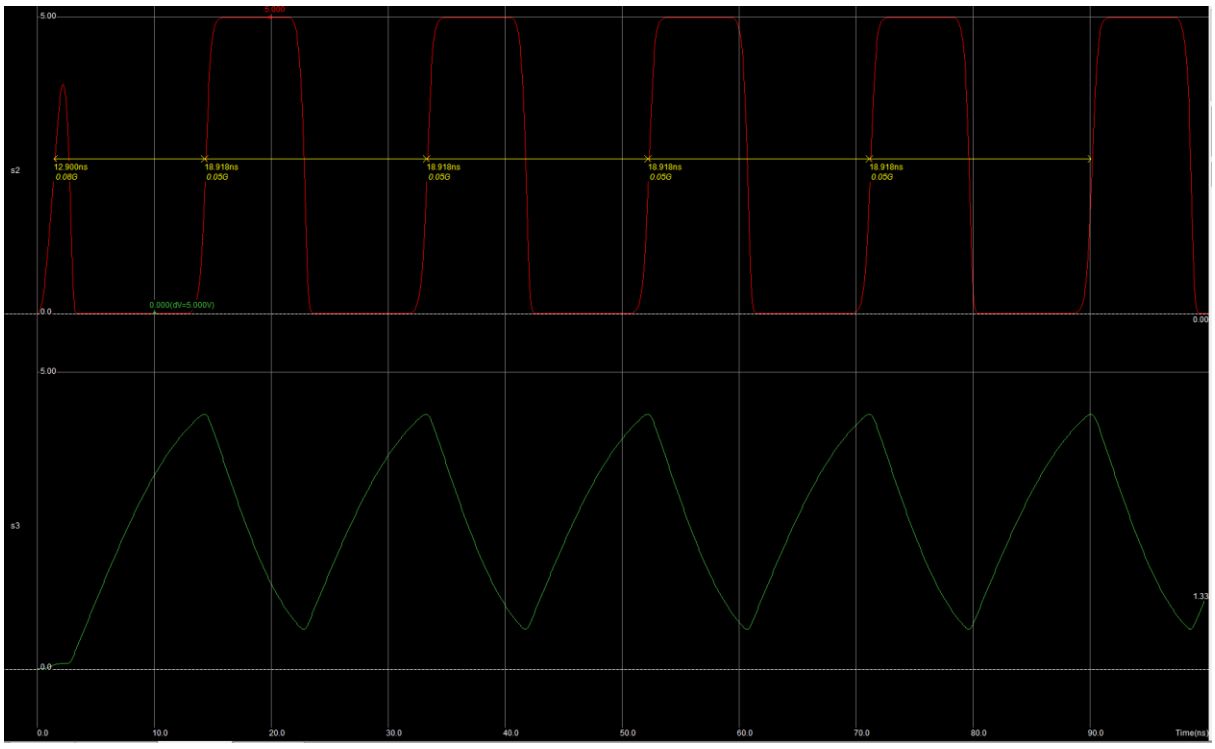

Figure 37: Oscillation frequency is approximately 52.9MHz for Vin = 5[V]

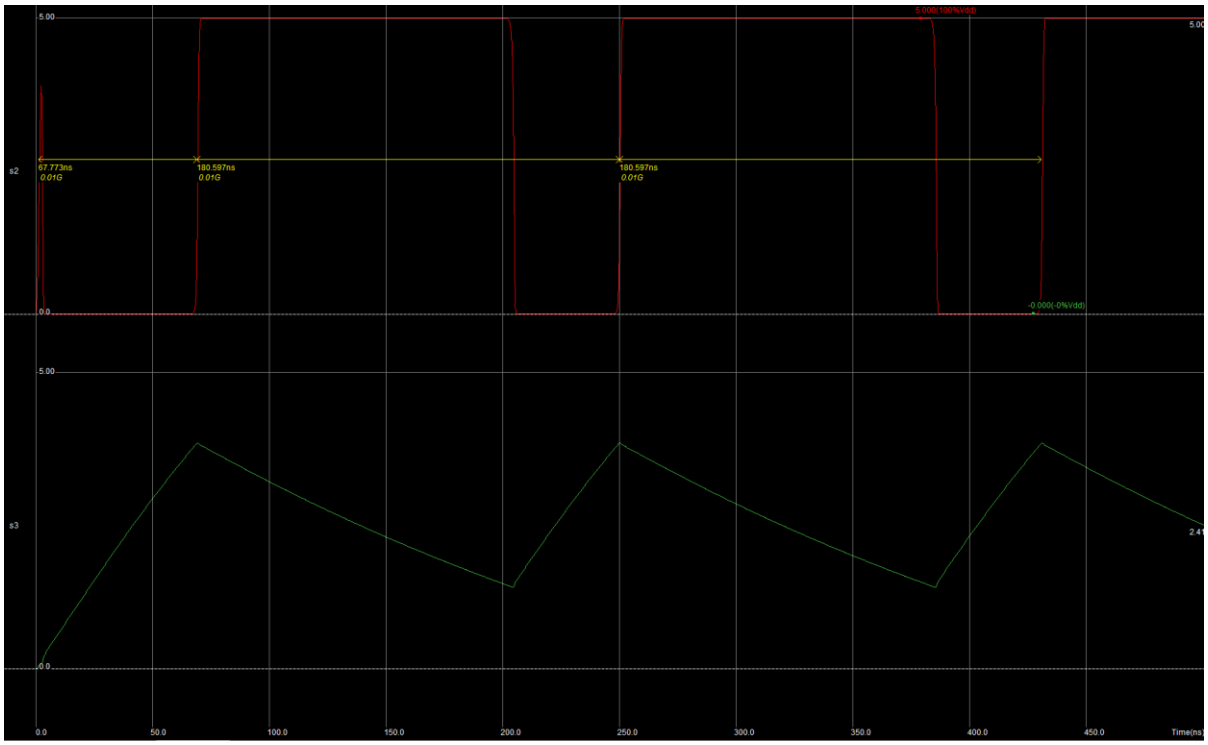

Figure 38:Oscillation frequency is approximately 5.5MHz for Vin = 1[V]

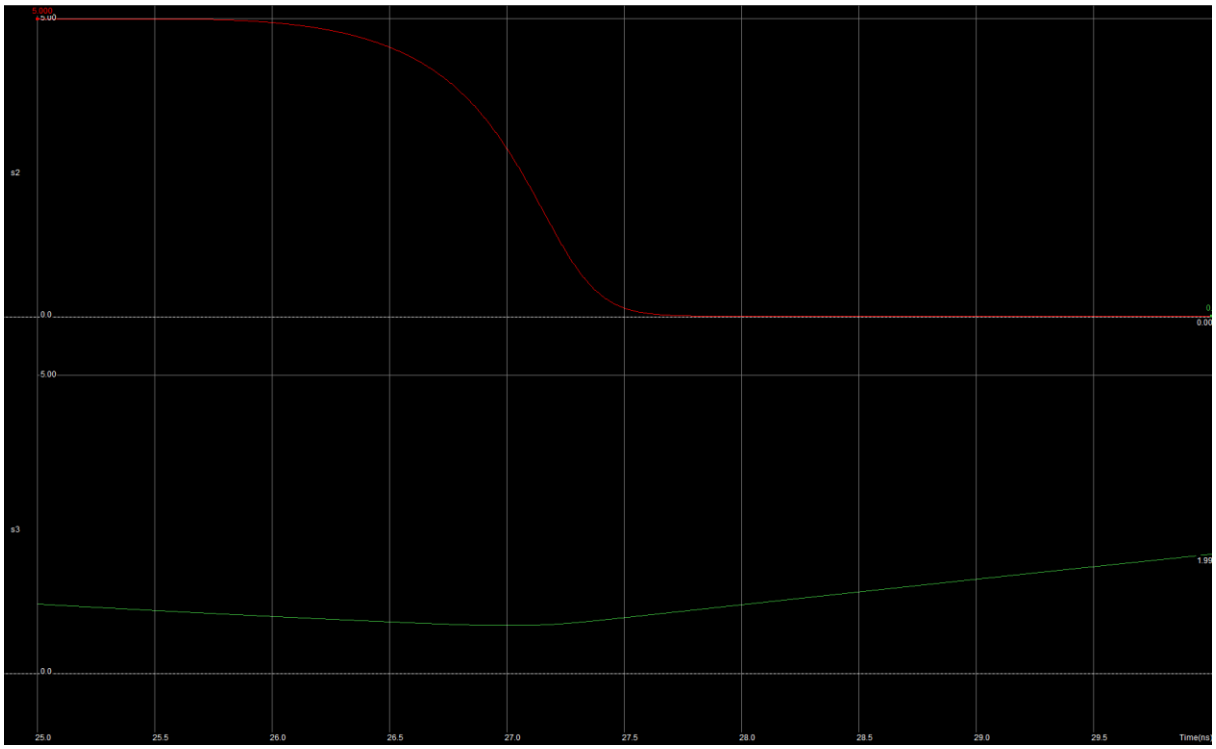

Figure 39: Final fall time is approximately 1.3ns

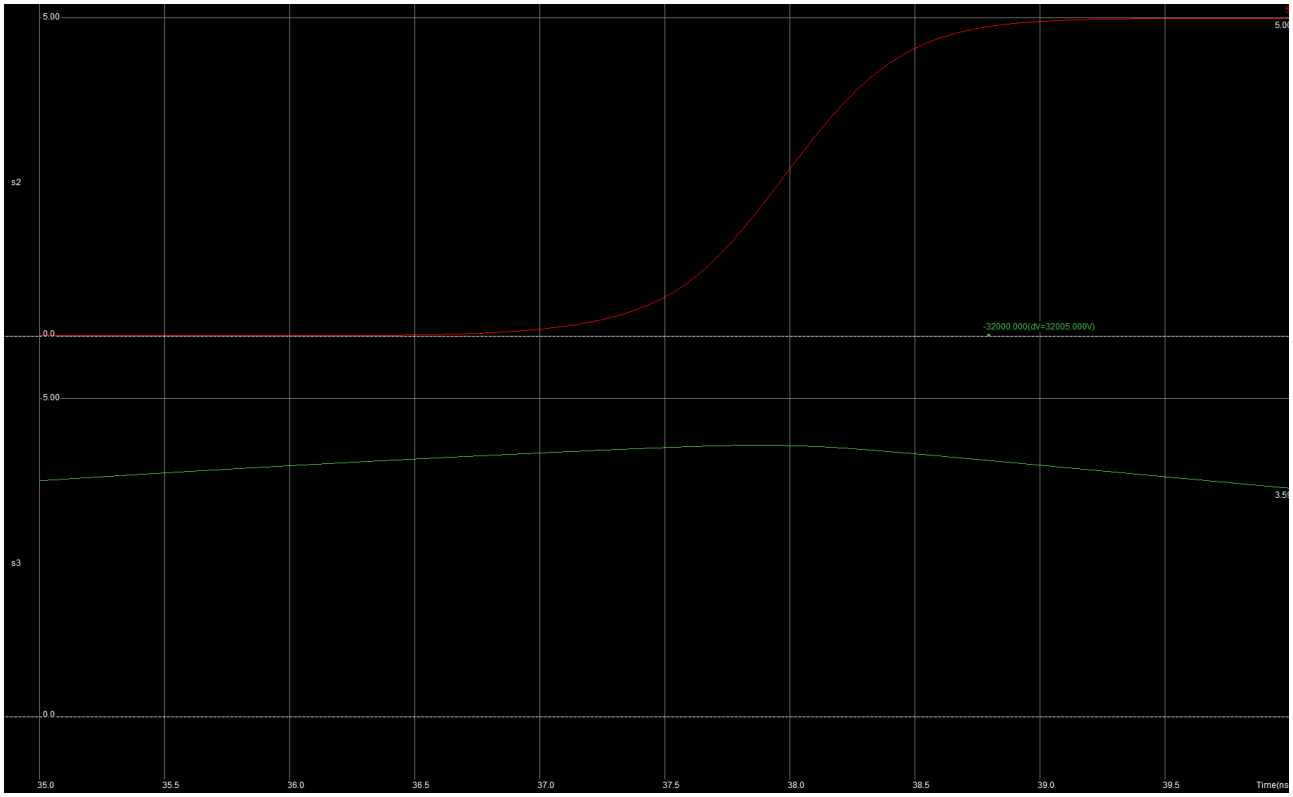

Figure 40: Final rise time is approximately 1ns

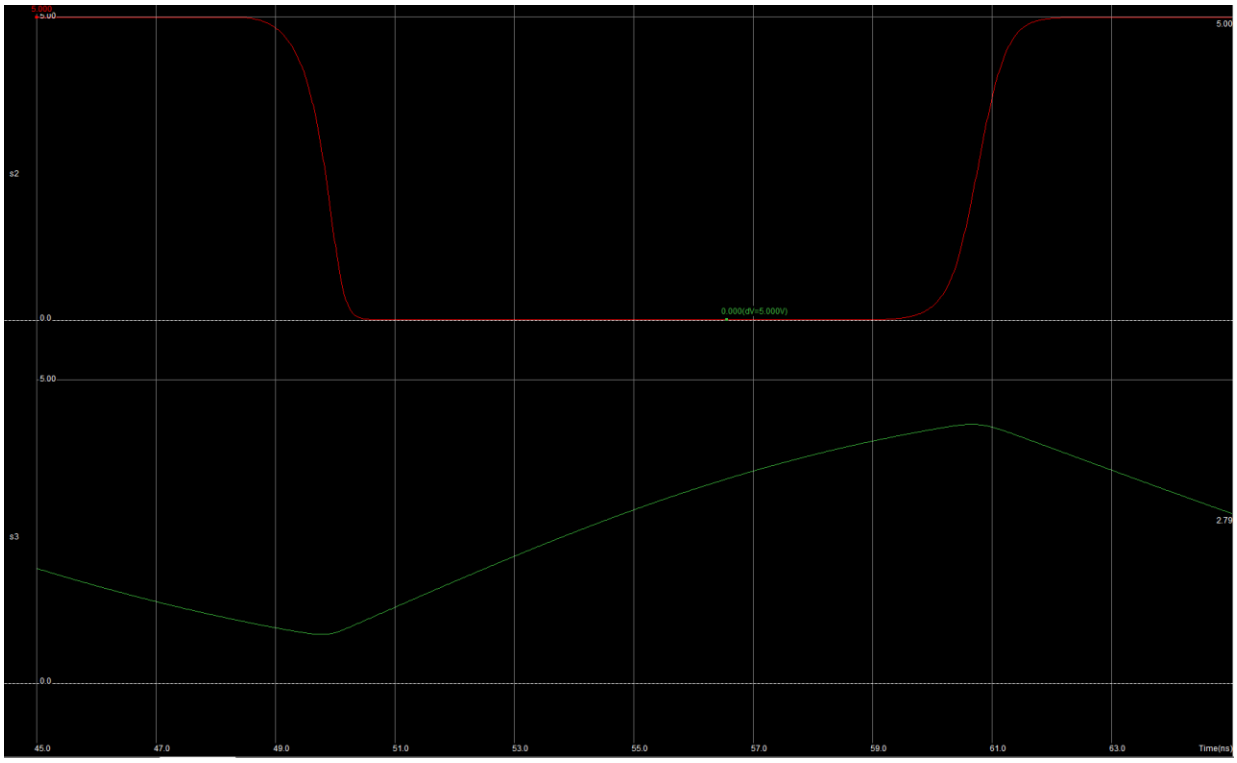

Figure 41: Low voltage dwell time is approximately 9ns

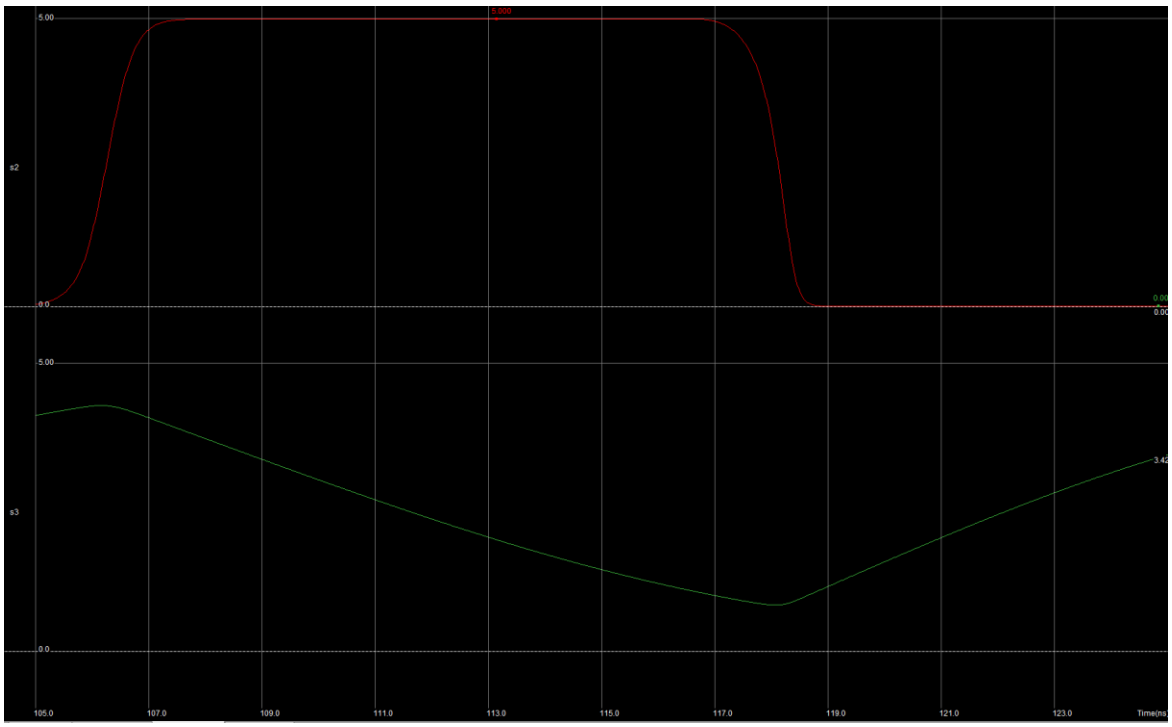

Figure 42: High voltage dwell time is approximately 10ns

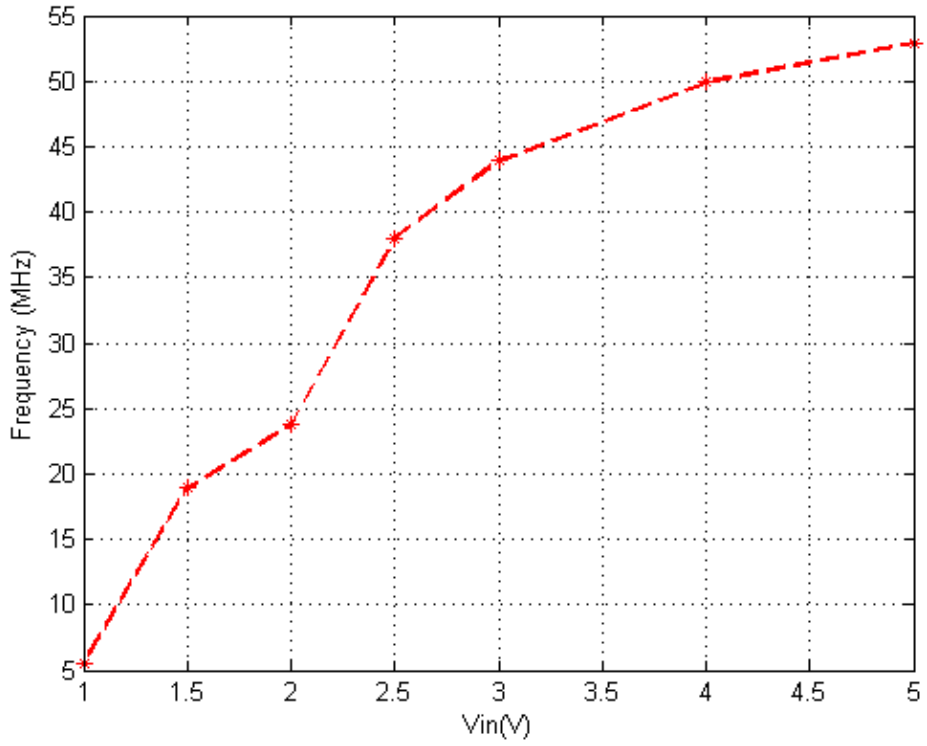

Figure 43: Oscillation frequency as a function of input voltage

Conclusion

This report specified the design, simulation, and mask diagram implementation process of a voltage controlled oscillator based. It also highlighted the design process of the Schmitt trigger, an essential component for the circuit. As a design check, the final VCO timing diagrams successfully achieved actual clock specifications from a major processor designer, indicating the validity of the design. Important considerations during the simulation process were also addressed.

References

[1] "Schmitt trigger," [Online]. Available: https://en.wikipedia.org/wiki/Schmitt_trigger.

[2] C. Cockrill, "Understanding Schmitt Triggers," Texas Instruments, 2011.

[3] Intel, "Pentium Processor Clock Design," November 1995. [Online]. Available: http://download.intel.com/design/pentium/applnots/24157402.pdf.