ROHM

BR6265

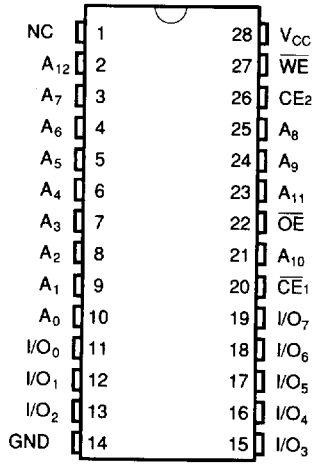
8K X 8 CMOS SRAM

FEATURES

- **Single +5V Power Supply**
- **Access Times 120ns (max.)**
- **Supply Current**
  — Very low power version:
  Operating: 40mA (max.)
  Standby: 50μA (max.)
- **Fully Static Operation - No Clock Or Refresh Cycles Required**
- **All Inputs And Outputs Directly TTL Compatible**
- **Common I/O Using Tri-State Output**
- **Output Enable And Two Chip Select Inputs For Easy Application**
- **Data Retention Voltage: 2V (min.)**
- **Available In 600 mil Plastic 28 Pin**

PIN CONFIGURATION

Plastic Dual-in-line Package



DESCRIPTION

The BR6265 is a low operating current 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates on a single 5V power supply. It is built using ROHM's high performance CMOS process.

Inputs and tri-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Two chip select inputs are provided for power down and device select, and an output enable input is included for easy interface.

Data retention is guaranteed at a power supply voltage as low as 2V.

PIN NAMES

A_0-A_{12}	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Select
I/O_0-I/O_7	Data Input/Output
V_{CC}	Power Supply (+5V)
GND	Ground

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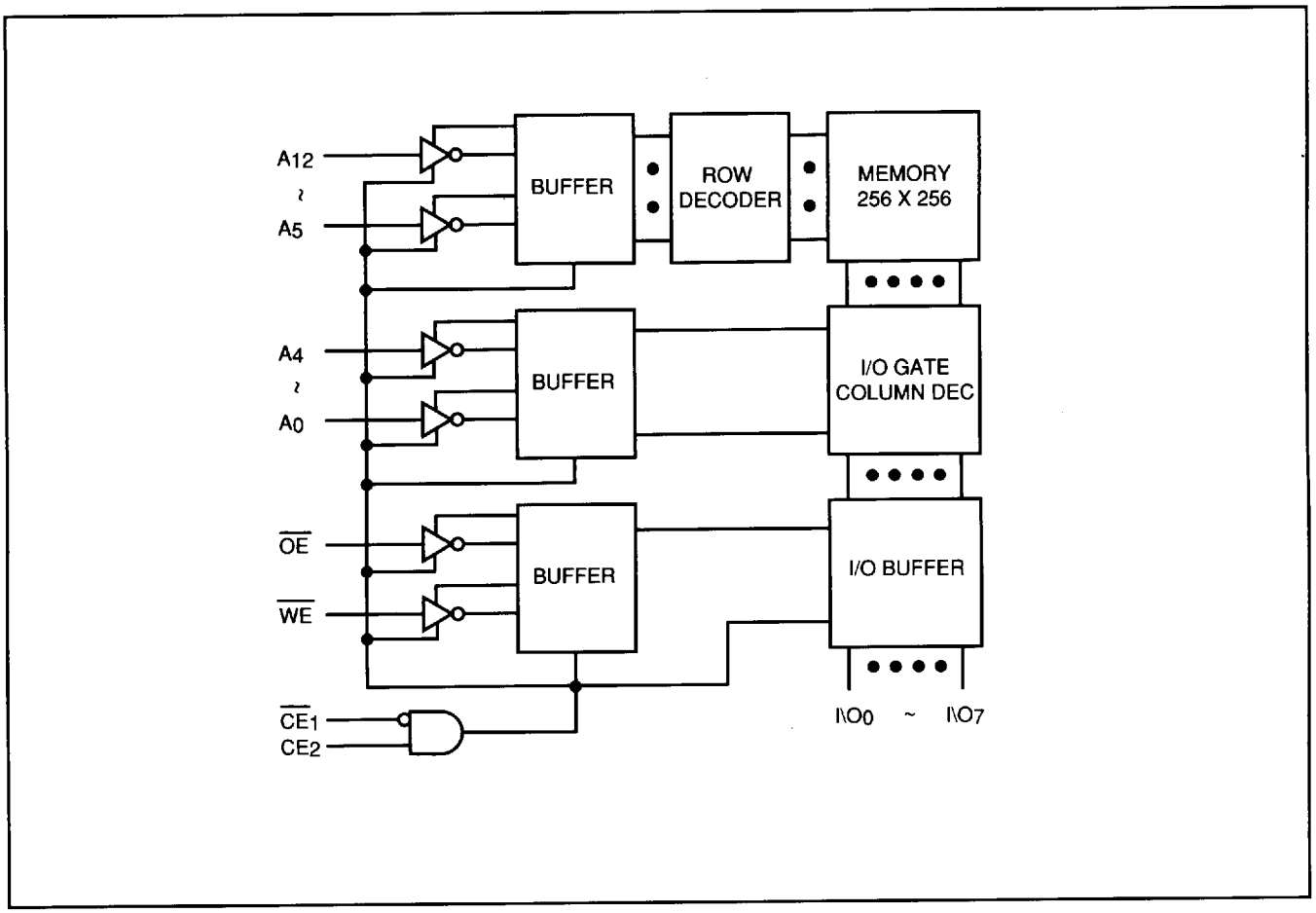
BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O Operation	V_{CC} Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disabled	L	H	H	H	High Z	I_{CCA1}, I_{CCA2}
Read	L	H	L	H	D_{OUT}	I_{CCA1}, I_{CCA2}
Write	L	H	X	L	D_{IN}	I_{CCA1}, I_{CCA2}

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to GND ..... -0.5V to +7.0V
IN, IN/OUT VOLT to GND ..... -0.5V to V_{CC}+0.5
Operating Temperature, T_{opr} ..... 0°C to +70°C
Storage Temperature, T_{stg} ..... -55°C to +125°C
Temperature Under Bias, T_{bias} ..... -10°C to +85°C
Power Dissipation, P_T 1.0W/SOP 0.7W
Soldering Temperature and Time ..... 260°C, 10 sec.

*NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	-0.3	—	+0.8	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, GND = 0V

Symbol	Parameter	BR6265-12LL		Unit	Test Conditions
		Min.	Max.		
I_{LI}	Input Leakage Current	—	1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	—	1	µA	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}
I_{CCA2}	Active Power Supply Current	—	10	mA	$\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}, $I_{I/O}$ = 0mA, f=1MHz
I_{CCA1}	Dynamic Operating Current	—	40	mA	Min. Cycle, Duty = 100% $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}, $I_{I/O}$ = 0mA
I_{SB}	Standby Power Supply Current	—	3	mA	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}
I_{SB1}		—	50	µA	$\overline{CE_1}$ ≥ V_{CC} - 0.2V, CE_2 ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V
I_{SB2}		—	50	µA	$\overline{CE_1}$ ≤ 0.2V, CE_2 ≤ 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH} = -1.0mA

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±10%

READ CYCLE①

Symbol	Parameter	BR6265-12LL		Unit
		Min.	Max.	
t_{RC}	Read Cycle Time	120	—	ns
t_{AA}	Address Access Time	—	120	ns
t_{CO1}	Chip Select Access Time ($\overline{CE}_1$)	—	120	ns
t_{CO2}	Chip Select Access Time (CE_2)	—	120	ns
t_{OE}	Output Enable to Output Valid	—	60	ns
t_{LZ1}②	Chip Selection to Output in Low Z ($\overline{CE}_1$)	10	—	ns
t_{LZ2}②	Chip Selection to Output in Low Z (CE_2)	10	—	ns
t_{OLZ}②	Output Enable to Output in Low Z	5	—	ns
t_{HZ1}②	Chip Deselection to Output in High Z ($\overline{CE}_1$)	0	40	ns
t_{HZ2}②	Chip Deselection to Output in High Z (CE_2)	0	40	ns
t_{OHZ}②	Output Disable to Output in High Z	0	40	ns
t_{OH}	Output Hold from Address Change	10	—	ns

① $\overline{WE}$ is always high all times for read cycles.
② Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE③

Symbol	Parameter	BR6265-12LL		Unit
		Min.	Max.	
t_{WC}	Write Cycle Time	120	—	ns
t_{CW}	Chip Selection to End of Write	85	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{AW}	Address Valid to End of Write	85	—	ns
t_{WP}④	Write Pulse Width	70	—	ns
t_{WR}⑤	Write Recovery Time	5	—	ns
t_{WHZ}⑦	Write to Output in High Z	0	40	ns
t_{DW}	Data to Write Time Overlap	50	—	ns
t_{DH}	Data Hold from Write Time	-10	—	ns
t_{OW}⑦	Output Active from End of Write	5	—	ns

③ If $\overline{OE}$ is high during write cycle, outputs are in high impedance state.
④ A write occures during the overlap (T_{WP}) of a low $\overline{CE}_1$ (or CE_2) and a low $\overline{WE}$.
⑤ t_{WR} is measured from $\overline{CE}_1$ (or CE_2) or $\overline{WE}$ going high to the end of a write cycle.
⑥ I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
⑦ Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.

CAPACITANCE

T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance	—	10	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	—	10	pF	$V_{I/O}$ = 0V

*This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	1TTL Gate and CL=100pF

DATA RETENTION CHARACTERISTICS

T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.①	Max.	Unit
V_{DR}	V_{CC} for Data Retention	2.0	—	5.5	V
I_{CCDR}	Data Retention Current	—	1.0	20③	µA
t_{CDR}	Chip Deselect to Data Retention Time	0	—	—	ns
t_R	Operation Recovery Time	t_{RC}②	—	—	ns

① V_{DR}=3.0V, T_A=25°C
② T_{RC}=Read Cycle Time
③ This characteristic is guaranteed to meet 3µA (max.) at T_A=0 to +40°C (V_{CC}=3.0V) and 1µA (max.) at T_A=0 to +25°C (V_{CC}=3.0V).

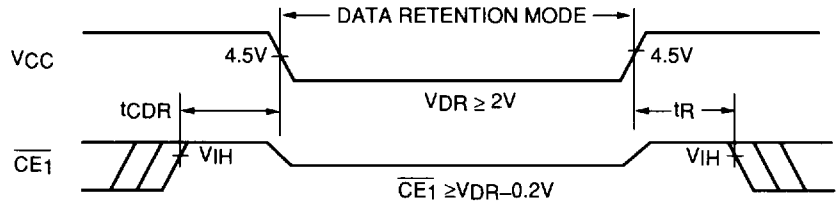


FIGURE 1. LOW V_{CC} DATA RETENTION WAVEFORM ($\overline{CE}_1$ CONTROLLED)

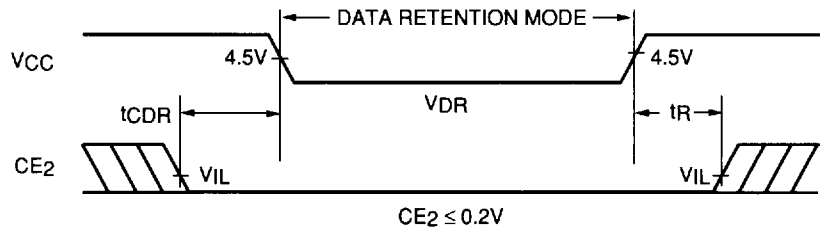


FIGURE 2. LOW V_{CC} DATA RETENTION WAVEFORM (CE_2 CONTROLLED)

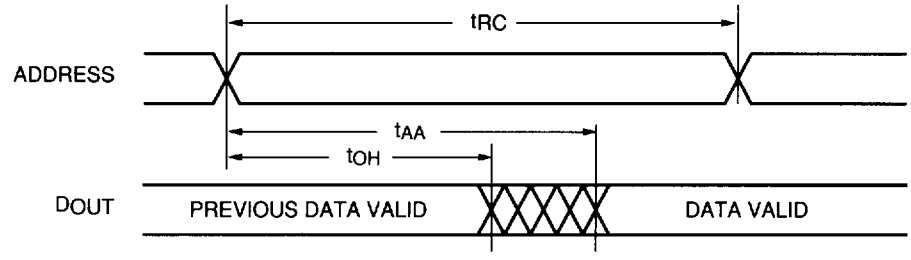


FIGURE 3. READ CYCLE TIMING NO. 1 ($\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})

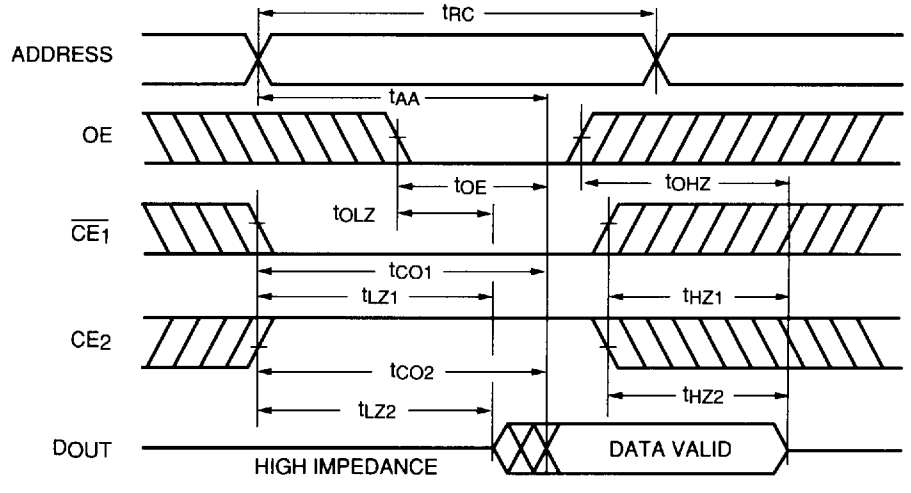


FIGURE 4. READ CYCLE TIMING NO. 2 ($\overline{WE}$=V_{IH})

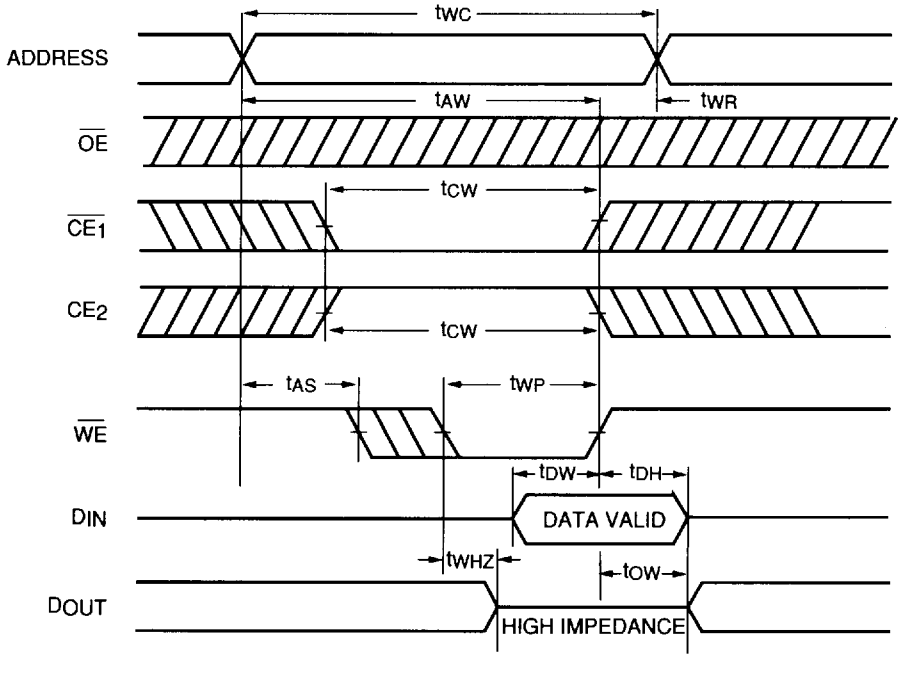


FIGURE 5. WRITE CYCLE TIMING NO. 1 ($\overline{WE}$ CONTROL)

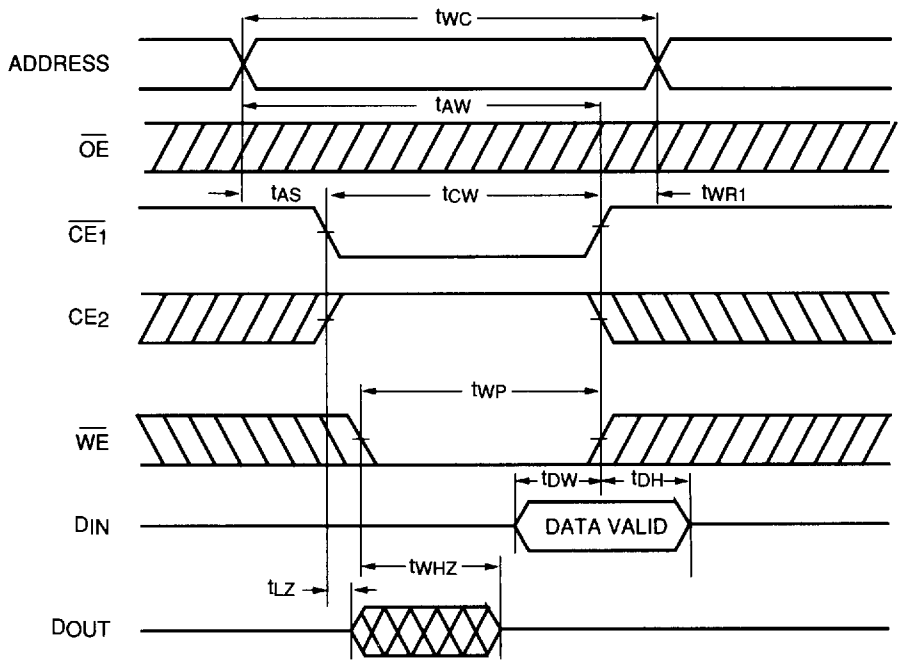


FIGURE 6. WRITE CYCLE TIMING NO. 2 ($\overline{CE}_1$ CONTROL)

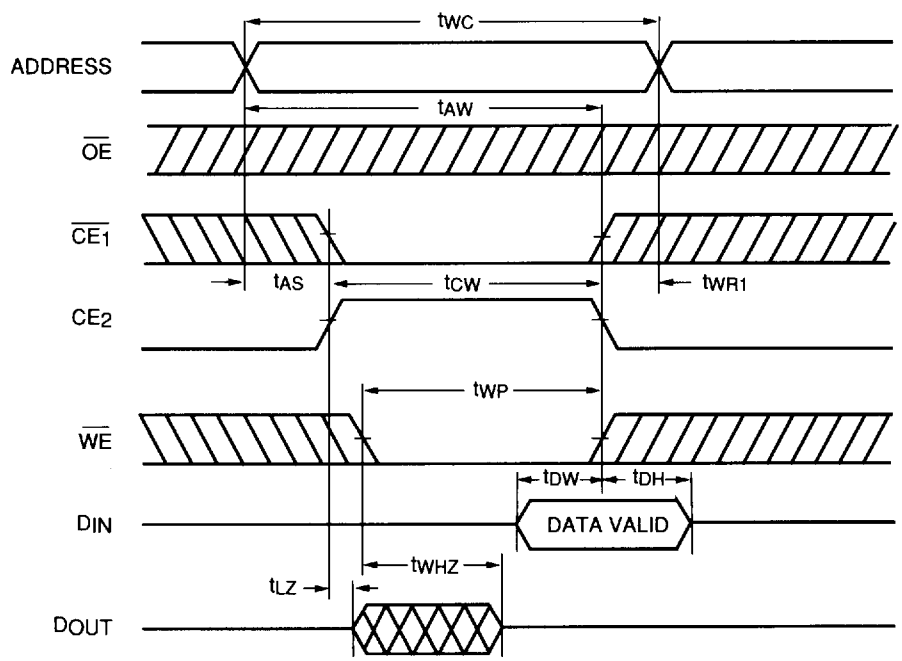
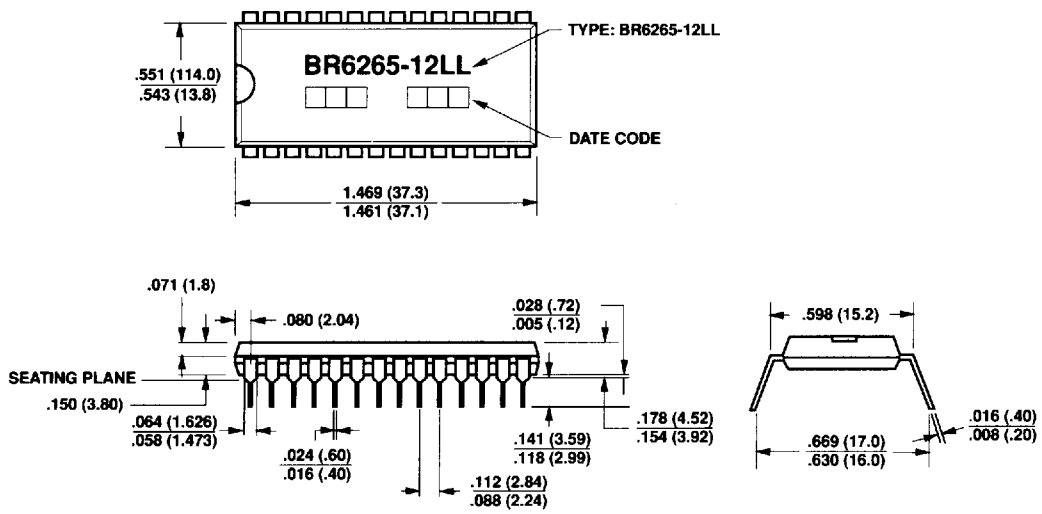


FIGURE 7. WRITE CYCLE TIMING NO. 3 (CE_2 CONTROL)

PACKAGE DIAGRAMS

Plastic Dual-in-line Package (PDIP)



ORDERING INFORMATION

Standard Configurations

Part Number	Access Time (ns)	Package
BR6265-12LL	120	600 MIL PLASTIC DIP28

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