

SRM20512LLMT_{85/10}

512K-Bit Static RAM

- Industrial Temperature Range
- Low Supply Current
- Access Time 85ns/100ns
- 65,536 Words×8-bit Asynchronous

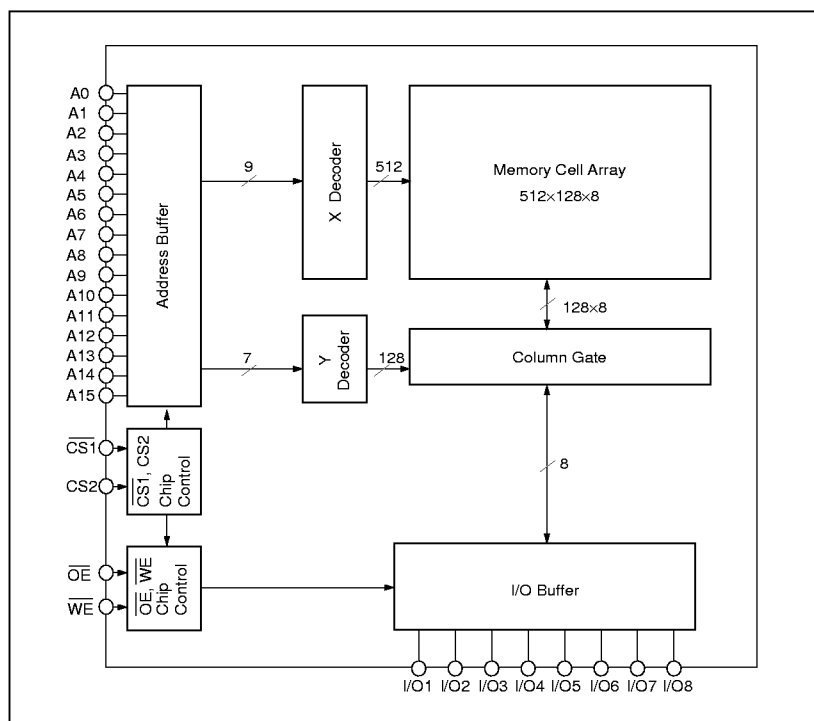
DESCRIPTION

The SRM20512LLMT_{85/10} is a 65,536 words×8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. And -40 to 85°C operating temperature range makes it ideal for industrial use. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and 3-state output allows easy expansion of memory capacity.

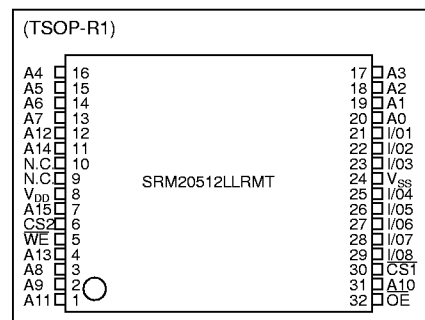
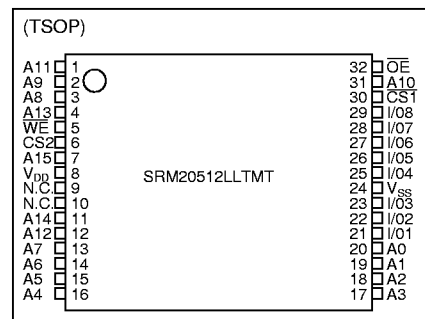
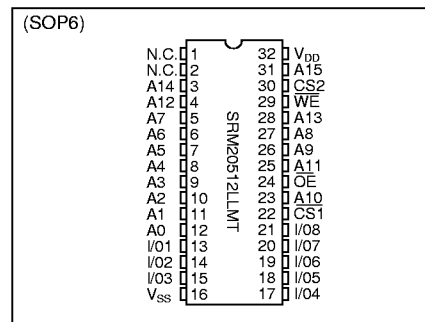
FEATURES

- Industrial temperature range -40 to 85°C
- Fast Access time SRM20512LLMT₈₅ 85ns (Max.)
SRM20512LLMT₁₀ 100ns (Max.)
- Low supply current standby: 1.5μA (Typ.)
operation: 15mA/MHz (Typ.)
- Completely static No clock required
- Single power supply 5V±10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package SRM20512LLMT_{85/10} SOP6-32pin(plastic)
SRM20512LLMT_{85/10} TSOP(I)-32pin(plastic)
SRM20512LLRMT_{85/10} TSOP(I)-32pin-R1(plastic)

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

| | |
|--------------|-------------------|
| A0 to A15 | Address Input |
| WE | Write Enable |
| OE | Output Enable |
| CS1, CS2 | Chip Select |
| I/O1 to I/O8 | Data I/O |
| VDD | Power Supply(+5V) |
| VSS | Power Supply(0V) |
| N. C. | No connection |

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

| Parameter | Symbol | Ratings | Unit |
|--------------------------------|------------------|-------------------------------|------|
| Supply voltage | V _{DD} | -0.5 to 7.0 | V |
| Input voltage | V _I | -0.5* to 7.0 | V |
| Input/Output voltage | V _{I/O} | -0.5* to V _{DD} +0.3 | V |
| Power dissipation | P _D | 1.0 | W |
| Operating temperature | T _{opr} | -40 to 85 | °C |
| Storage temperature | T _{stg} | -65 to 150 | °C |
| Soldering temperature and time | T _{sol} | 260°C, 10s(at lead) | - |

*V_I, V_{I/O}(Min.)= -3.0V (Pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, T_a=-40 to 85°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|----------------|-----------------|------------|-------|------|----------------------|------|
| Supply voltage | V _{DD} | - | 4.5 | 5.0 | 5.5 | V |
| | V _{SS} | - | 0 | 0 | 0 | V |
| Input voltage | V _{IH} | - | 2.2 | - | V _{DD} +0.3 | V |
| | V _{IL} | - | -0.3* | - | 0.8 | V |

*If pulse width is less than 50ns, it is - 3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, T_a=-40 to 85°C)

| Parameter | Symbol | Conditions | SRM20512LLMT85 | | | SRM20512LLMT10 | | | Unit |
|---------------------------|-------------------|---|----------------|-------|------|----------------|-------|------|------|
| | | | Min. | Typ.* | Max. | Min. | Typ.* | Max. | |
| Input leakage | I _{LI} | V _I =0 to V _{DD} | -1 | - | 1 | -1 | - | 1 | μA |
| Standby supply current | I _{DDS} | $\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ | - | 1.0 | 3.0 | - | 1.0 | 3.0 | mA |
| | I _{DDS1} | $\overline{CS1}=CS2 \geq V_{DD}-0.2V$ or $CS2 \leq 0.2V$ | - | 1.5 | 100 | - | 1.5 | 100 | μA |
| Average operating current | I _{DDA} | V _I =V _{IL} , V _{IH} I _{I/O} =0mA, t _{cyc} =Min. | - | 45 | 70 | - | 45 | 70 | mA |
| | I _{DDA1} | V _I =V _{IL} , V _{IH} I _{I/O} =0mA, t _{cyc} =1μs | - | 15 | 40 | - | 15 | 40 | mA |
| Operating supply current | I _{DDO} | V _I =V _{IL} , V _{IH} I _{I/O} =0mA | - | 15 | 40 | - | 15 | 40 | mA |
| Output leakage | I _{LO} | $\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, V _{I/O} =0 to V _{DD} | -1 | - | 1 | -1 | - | 1 | μA |
| High level output voltage | V _{OH} | I _{OH} =-1.0mA | 2.4 | - | - | 2.4 | - | - | V |
| Low level output voltage | V _{OL} | I _{OL} =2.1mA | - | - | 0.4 | - | - | 0.4 | V |

*Typical values are measured at T_a=25°C and V_{DD}=5.0V

● Terminal Capacitance

(f=1MHz, T_a=25°C)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|------------------|----------------------|------|------|------|------|
| Address Capacitance | C _{ADD} | V _{ADD} =0V | - | - | 9 | pF |
| Input Capacitance | C _I | V _I =0V | - | - | 10 | pF |
| I/O Capacitance | C _{I/O} | V _{I/O} =0V | - | - | 10 | pF |

SRM20512LLMT_{85/10}

●AC Electrical Characteristics

○Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, T_a=-40 to 85°C)

| Parameter | Symbol | Conditions | SRM20512LLMT ₈₅ | | SRM20512LLMT ₁₀ | | Unit |
|-------------------------------|-------------------|------------|----------------------------|------|----------------------------|------|------|
| | | | Min. | Max. | Min. | Max. | |
| Read cycle time | t _{RC} | *1 | 85 | - | 100 | - | ns |
| Address access time | t _{ACC} | | - | 85 | - | 100 | ns |
| Chip select 1 access time | t _{ACS1} | | - | 85 | - | 100 | ns |
| Chip select 2 access time | t _{ACS2} | | - | 85 | - | 100 | ns |
| Output enable access time | t _{OE} | | - | 45 | - | 50 | ns |
| Chip select 1 output set time | t _{CLZ1} | *2 | 10 | - | 10 | - | ns |
| Chip select 1 output floating | t _{CHZ1} | | - | 30 | - | 35 | ns |
| Chip select 2 output set time | t _{CLZ2} | | 10 | - | 10 | - | ns |
| Chip select 2 output floating | t _{CHZ2} | | - | 30 | - | 35 | ns |
| Output enable output set time | t _{OLZ} | | 0 | - | 0 | - | ns |
| Output enable output floating | t _{OHZ} | | - | 30 | - | 35 | ns |
| Output hold time | t _{OH} | *1 | 10 | - | 10 | - | ns |

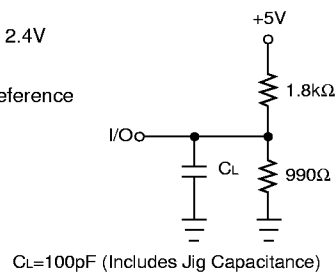
○Write Cycle

(V_{DD}=5V±10%, V_{SS}=0V, T_a=-40 to 85°C)

| Parameter | Symbol | Conditions | SRM20512LLMT ₈₅ | | SRM20512LLMT ₁₀ | | Unit |
|-----------------------|------------------|------------|----------------------------|------|----------------------------|------|------|
| | | | Min. | Max. | Min. | Max. | |
| Write cycle time | t _{WC} | *1 | 85 | - | 100 | - | ns |
| Chip select time 1 | t _{CW1} | | 70 | - | 80 | - | ns |
| Chip select time 2 | t _{CW2} | | 70 | - | 80 | - | ns |
| Address enable time | t _{AW} | | 70 | - | 80 | - | ns |
| Address setup time | t _{AS} | | 0 | - | 0 | - | ns |
| Write pulse width | t _{WP} | | 65 | - | 75 | - | ns |
| Address hold time | t _{WR} | | 0 | - | 0 | - | ns |
| Input data setup time | t _{DW} | | 35 | - | 40 | - | ns |
| Input data hold time | t _{DH} | | 0 | - | 0 | - | ns |
| WE Output floating | t _{WHZ} | *2 | - | 30 | - | 35 | ns |
| WE Output setup time | t _{OW} | | 5 | - | 5 | - | ns |

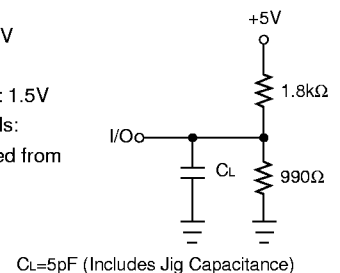
*1 Test Conditions

1. Input pulse level: 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L=100pF



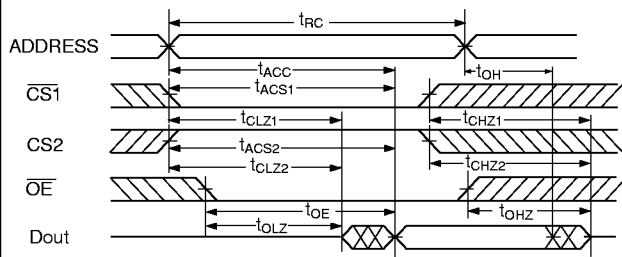
*2 Test Conditions

1. Input pulse level: 0.6V to 2.4V
2. t_r=t_f=5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load C_L=5pF

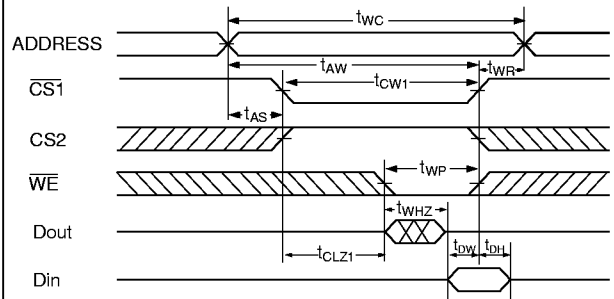


●Timing chart

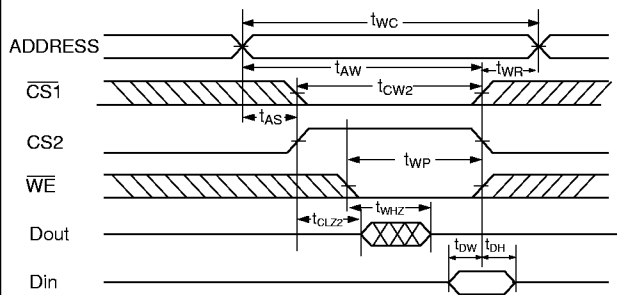
○Read Cycle*1



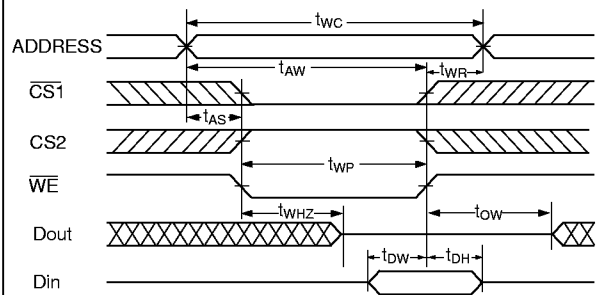
○Write Cycle(1)(CS1 Control)*2



○Write Cycle(2)(CS2 Control)*2



○Write Cycle(3)(WE Control)*3, *4



- Note: 1. During read cycle time, \overline{WE} is to be "H" level.
 2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state, whether \overline{OE} level is "H" or "L".
 3. During write cycle time that is controlled by \overline{WE} , Output Buffer is high impedance state if \overline{OE} is "H" level.
 4. When I/O terminals are output mode, be careful that do not give the opposite signals to the I/O terminals.

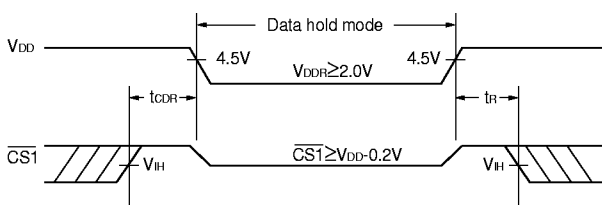
●DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

($V_{SS}=0V$, $T_a=-40$ to $85^\circ C$)

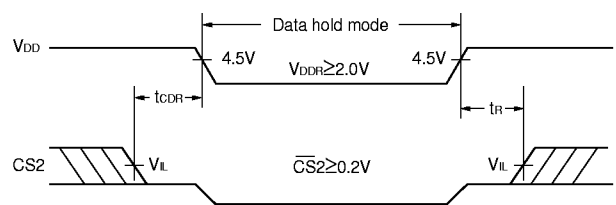
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|-----------|--|------|------|------|---------|
| Data retention Supply voltage | V_{DDR} | | 2.0 | - | 5.5 | V |
| Data retention current | I_{DDR} | $V_{DD}=3V$ $\overline{CS1}=CS2 \geq V_{DD}-0.2V$ or $CS2 \leq 0.2V$ | - | 1* | 50 | μA |
| Chip select data hold time | t_{CDR} | | 0 | - | - | ns |
| Operation recovery time | t_R | | 5.0 | - | - | ms |

* $T_a=25^\circ C$

Data retention timing (CS1 Control)



Data retention timing (CS2 Control)



When retaining data in standby mode, supply voltage can be lowered within a certain range. But read or write cycle cannot be performed while the supply voltage is low.

■ FUNCTIONS

● Truth Table

| $\overline{CS1}$ | CS2 | \overline{OE} | \overline{WE} | DATA I/O | Mode | I_{DD} |
|------------------|-----|-----------------|-----------------|-------------|----------------|---------------------|
| H | X | X | X | Hi-Z | Standby | I_{DDS}, I_{DDS1} |
| X | L | X | X | Hi-Z | Standby | I_{DDS}, I_{DDS1} |
| L | H | X | L | Input data | Write | I_{DDO} |
| L | H | L | H | Output data | Read | I_{DDO} |
| L | H | H | H | Hi-Z | Output disable | I_{DDO} |

X: "H" or "L"

● Reading data

Data is able to be read when the address is set while holding $\overline{CS1}$ = "L", CS2 = "H", \overline{OE} = "L" and \overline{WE} = "H". Since DATA I/O terminals are in high impedance state when \overline{OE} = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing data

There are the following four ways of writing data into the memory.

- (1) Hold CS2 = "H", \overline{WE} = "L", set addresses and give "L" pulse to $\overline{CS1}$.
- (2) Hold $\overline{CS1}$ = "L", \overline{WE} = "L", set addresses and give "H" pulse to CS2.
- (3) Hold $\overline{CS1}$ = "L", CS2 = "H", set addresses and give "L" pulse to \overline{WE} .
- (4) After setting addresses, give "L" pulse to $\overline{CS1}$, \overline{WE} and give "H" pulse to CS2.

Anyway, data on the Data I/O terminals are latched up into the SRM20512LLMT_{85/10} at the end of the period that $\overline{CS1}$, \overline{WE} are "H" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, \overline{OE} = "H", or CS2 = "L", the contention on the data bus can be avoided.

● Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM20512LLMT_{85/10} is in the standby mode which has retaning date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, \overline{WE} and data can be any "H" or "L". When CS1 and $\overline{CS2}$ level are in the range over $V_{DD}-0.2V$, CS2 level is in the range under 0.2V, in the SRM20512LLMT_{85/10} there is almost no current flow except through the high resistance parts of the memory.

Unit: mm
(inch)

Technical drawing of a rectangular structure with dimensions and a cross-section.

Dimensions (mm):

- Top width: $20^{+0.3}_{-0.2}$ (0.797 $^{+0.003}_{-0.002}$)
- Inner width: $18.4^{+0.2}_{-0.2}$ (0.724 $^{+0.008}_{-0.008}$)
- Right height: $32^{+0.2}_{-0.2}$ (0.315 $^{+0.007}_{-0.007}$)
- Bottom height: 16
- Left height: 1

Feature: INDEX (indicated by a circle and arrow pointing to the top-left corner).

Section view (right):

- Angle: 10°
- Dimension: 10°

Bottom view (left):

- Dimension: $0.6^{+0.1}_{-0.1}$ (0.02 $^{+0.005}_{-0.005}$)
- Dimension: $0.8^{+0.2}_{-0.2}$ (0.031 $^{+0.007}_{-0.007}$)

Bottom view (right):

- Dimension: $0.15^{+0.07}_{-0.07}$ (0.006 $^{+0.003}_{-0.003}$)
- Dimension: 0.5 (0.02)
- Dimension: $0.2^{+0.1}_{-0.1}$ (0.008 $^{+0.003}_{-0.003}$)
- Dimension: 0.030 (0.001)
- Dimension: $0.27^{+0.03}_{-0.03}$ (0.011 $^{+0.001}_{-0.001}$)

Unit: mm
(inch)

Technical drawing of a mechanical part, likely a bracket or support, showing dimensions and tolerances. The drawing includes a side view and a cross-sectional view.

Side View Dimensions:

- Overall width: $20^{+0.2}_{-0.3}$ (0.787 $^{+0.002}_{-0.003}$)
- Inner width: $18^{+0.2}_{-0.3}$ (0.724 $^{+0.002}_{-0.003}$)
- Left vertical dimension: 16
- Right vertical dimension: 17
- Bottom vertical dimension: 32
- Feature: INDEX (pointing to a hole)

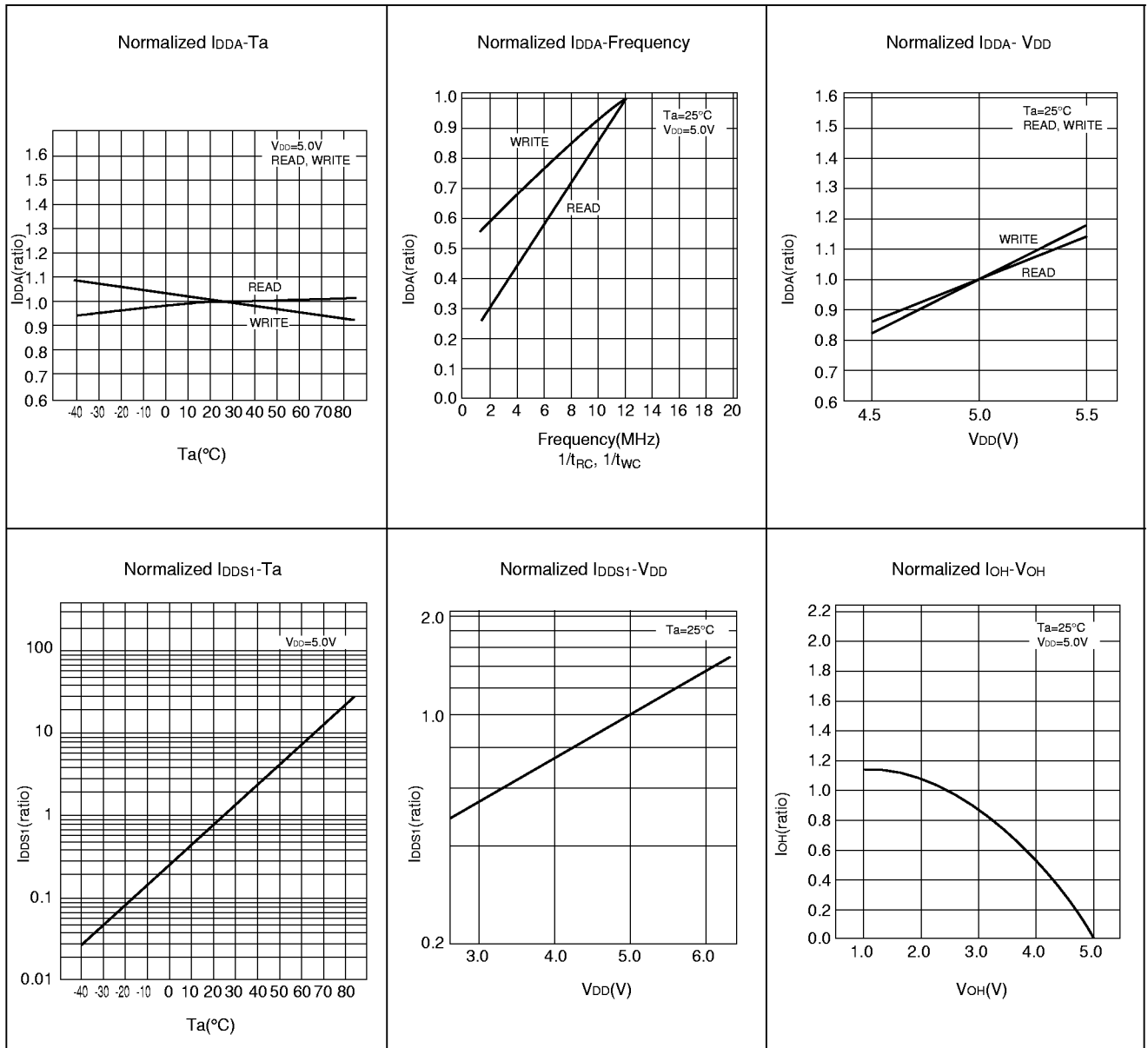
Cross-sectional View Dimensions:

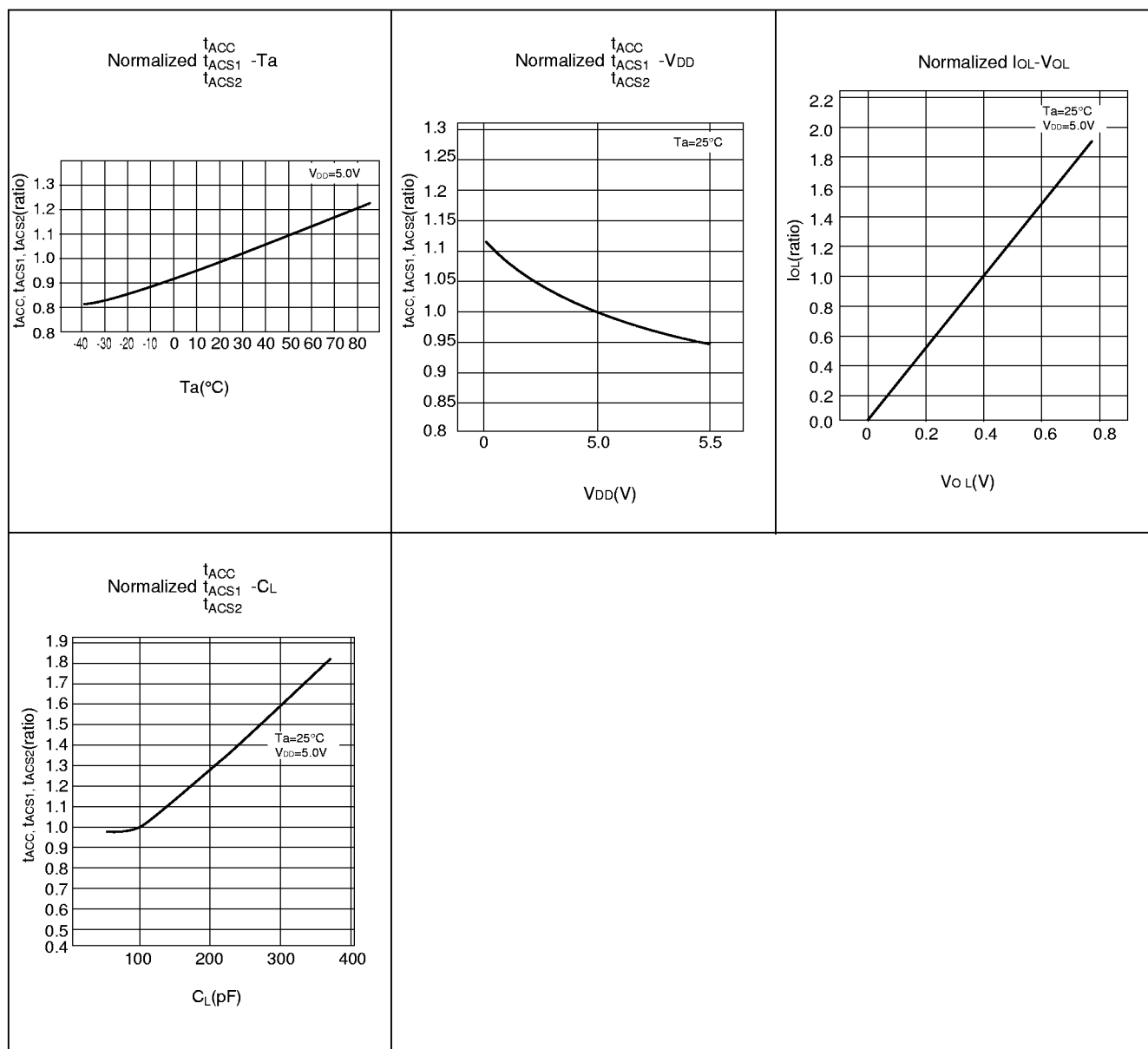
- Top horizontal dimension: $0.15^{+0.001}_{-0.002}$ (0.006 $^{+0.0001}_{-0.0002}$)
- Bottom horizontal dimension: $0.5^{+0.01}_{-0.02}$ (0.02)
- Right vertical dimension: $0.2^{+0.001}_{-0.002}$ (0.008 $^{+0.0001}_{-0.0002}$)
- Angle: 10°

Unit: mm
(inch)

*: The same characteristics as SRM20512LLMT_{85/10}.

■ CHARACTERISTICS CURVES





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SEIKO EPSON CORPORATION

ELECTRONIC DEVICE MARKETING DEPARTMENT

IC Marketing & Engineering Group
 421-8 Hino, Hino-shi, Tokyo 191, JAPAN
 Phone: 0425-87-5816 FAX: 0425-87-5624

International Marketing Derpartment I (Europe, U.S.A.)
 421-8 Hino, Hino-shi, Tokyo 191, JAPAN
 Phone: 0425-87-5812 FAX: 0425-87-5564

International Marketing Derpartment II (Asia)
 421-8 Hino, Hino-shi, Tokyo 191, JAPAN
 Phone: 0425-87-5814 FAX: 0425-87-5110

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