DD1_Practical_test_2

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4-bit 2's complement representation of a decimal number is 1000. The number is

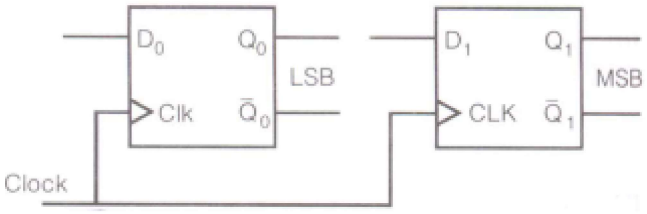
- 8
- 0
- -8
- -7

Clear selection

One multiplexer can take the place of

- several SSI logic gates
- several Ex-NOR gates
- several SSI logic gates or combinational logic circuits
- combinational logic circuits

Two D-flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following Q1Q0 sequence 00-> 01->11->10 ->00->... . The input D0 and D1 respectively should be connected as



- Q1'Q0' and Q1Q0
- Q1' and Q0
- Q0' and Q1
- Q1'Q0 and Q1'Q0

In the expression Y + ZX the total number of min-terms are _____

- 2
- 3
- 4
- 5

A 3x8 decoder with a enable line _____

- Can work as 1x8 de-multiplexer
- Can work as 8x3 encoder
- Can work as 8x1 multiplexer
- All the options

Digital Comparator is a

- gate
- combinational circuit
- sequential circuit
- complex circuit

How many flip-flops are in the 7474 IC?

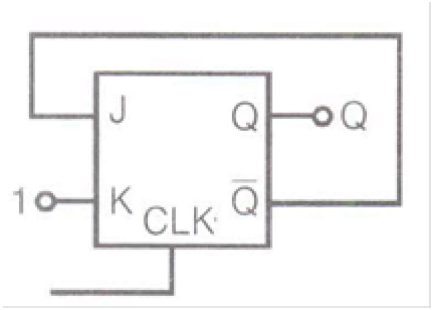
- 4
- 2
- 3
- 1

The output of a sequential circuit at any instant of time is dependent _____

- All the options
- on the present inputs
- past history of outputs
- past history of inputs

Clear selection

In a J-K flip-flop we have J=Q' and K=1 (see figure) Assuming the flip-flop was initially cleared an then clocked for 6 pulses, the sequence at the Q output will be



- 10010
- 11001
- 10000
- 10101

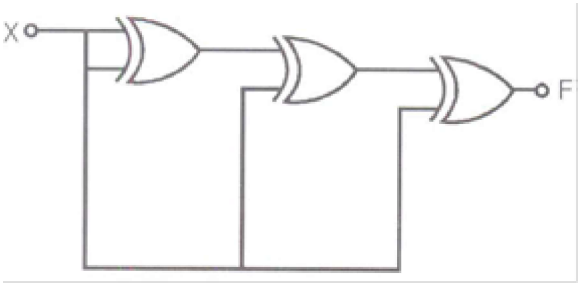
Clear selection

Which of the following statement is true about 8-bit barrel shifter

- It is a sequential circuit
- It takes 2 clock cycle to shift the 8-bit pattern towards right by 2 bit positions
- Both It takes 2 clock cycle to shift the 8-bit pattern towards right by 2 bit positions and It is a sequential circuit
- It is a combinational circuit

Clear selection

For the circuit shown below the output F is given by



- F=X'
- F=X
- F=0
- F=1

Clear selection

The number of product terms in the minimized sum-of-product expression obtained through the following K-map is (where, "d" denotes don't care states) *

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

- 4
- 3
- 5
- 2

The advantage of 2's complement system in digital design is

- (●) Only two arithmetic operation is required
- ( ) Only one arithmetic operation is required
- ( ) No arithmetic operation is required
- ( ) Different arithmetic operation is required

Clear selection

Consider the following two statements :- A:)- A 5-bit ring counter is known as mod 6 synchronous counters. B:)-. A 5-bit twisted ring counter has 10 stable states. Choose the best appropriate options

- ( ) Statement A is True; Statement B is True
- ( ) Statement A is false; Statement B is True
- ( ) Statement A is false; Statement B is false
- ( ) Statement A is True; Statement B is false

In standard TTL the 'totem pole' stage refers to

- ( ) The phase splitter
- ( ) The multi-emitter input stage
- (●) The output buffer
- ( ) Open collector output stage

Clear selection

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