/*

4357.(008) Embedded Firmware Essentials
Spring 2015

Toggle a GPIO Pin
File: toggle_gpio.c
Goal: write a code to toggle a GPIO pin as fast as possible.

1. Fast Read LPC178 schematics and data sheets
   http://developer.mbed.org/platforms/mbed-LPC1768/
   http://www.nxp.com/documents/user_manual/UM10360.pdf (Chapter 9: GPIO)
2. Read ARM Cortex-M3 Datasheet
   a. http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337h/CHDDIGAC.html
   b. https://ece.uwaterloo.ca/~ece222/ARM/ARM7-TDMI-manual-pt3.pdf
   c. http://infocenter.arm.com/help/topic/com.arm.doc.ddi0337h/DDI0337H_cortex_m3_r2p0_trm.pdf
3. write a C code to toggle a GPIO pin as fast as possible
4. study machine code output from objdump
5. write a page report to tell me the meaning of each bit of the machine code of the while loop body only.
   (you may ignore all machine code before and after the while loop.)

gcc commands:
$ arm-none-eabi-gcc -mcpu=cortex-m3 -mthumb -c hw01.c -o hw01.o
$ arm-none-eabi-gcc -mcpu=cortex-m3 -mthumb -O3 -c hw01.c -o hw01_O3.o
$ arm-none-eabi-gcc -mcpu=cortex-m3 -mthumb -Os -c hw01.c -o hw01_Os.o
$ arm-none-eabi-objdump -d hw01.o

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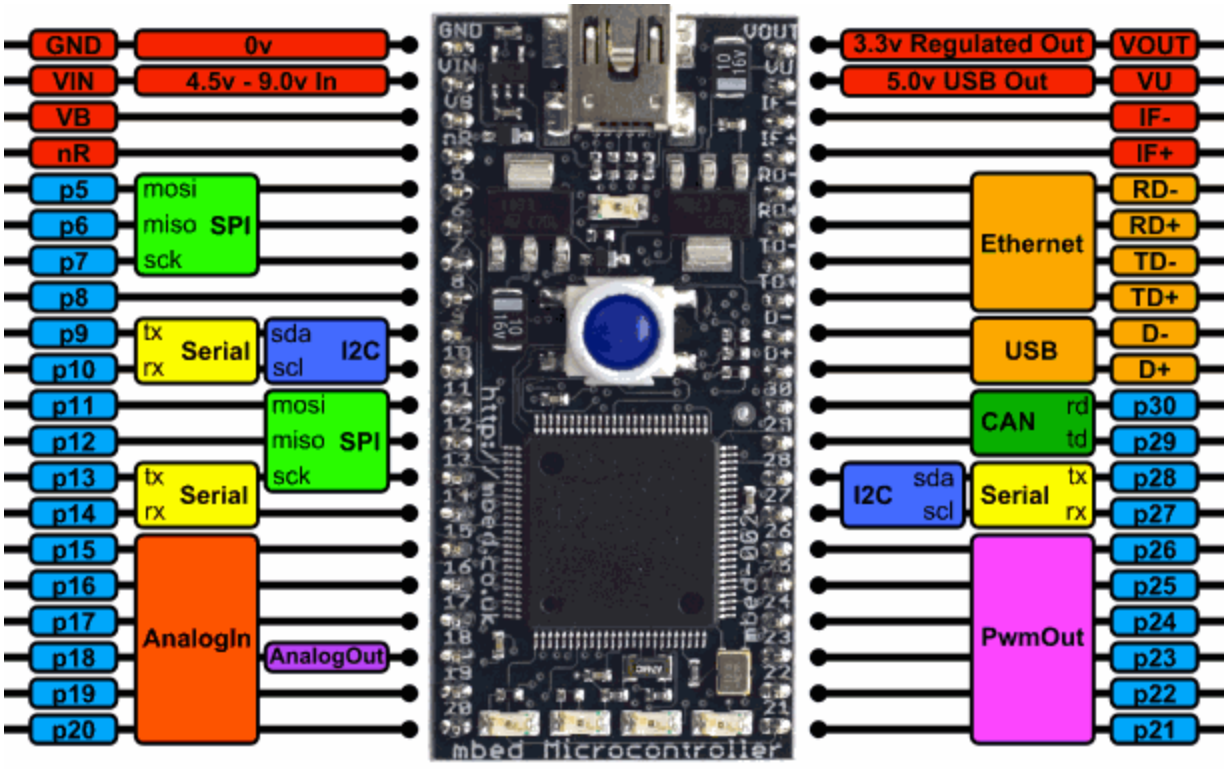
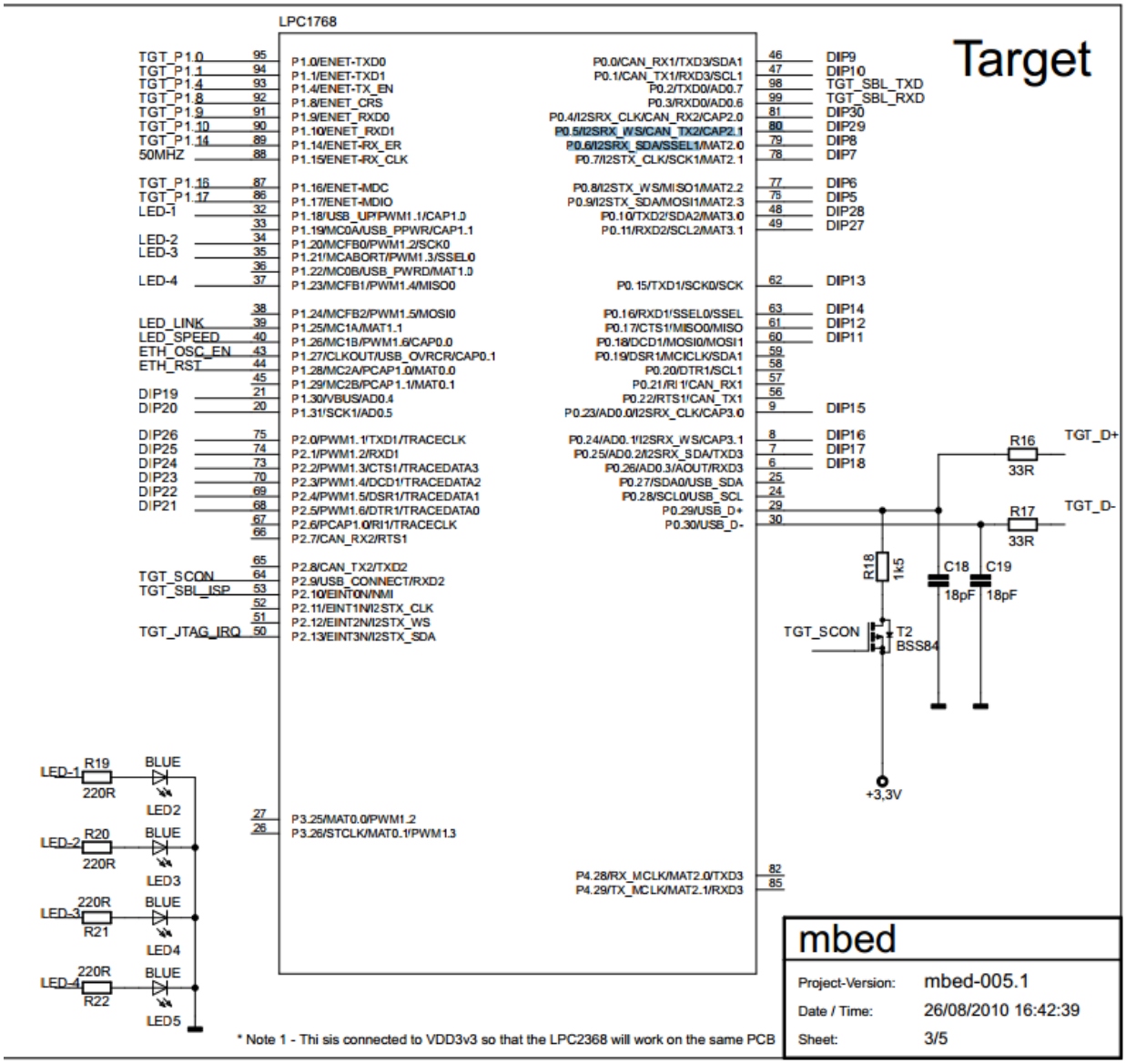
http://developer.mbed.org/handbook/mbed-NXP-LPC1768-Getting-Started



http://developer.mbed.org/media/uploads/chris/mbed-005.1.pdf


LPC1768
Target
TGT_P1.0
TGT_P1.1
TGT_P1.4
TGT_P1.8
TGT_P1.9
TGT_P1.10
TGT_P1.14
50MHZ
TGT_P1.16
TGT_P1.17
LED-1
LED-2
LED-3
LED-4
LED_LINK
LED_SPEED
ETH_OSC_EN
ETH_RST
DIP19
DIP20
DIP26
DIP25
DIP24
DIP23
DIP22
DIP21
TGT_SCON
TGT_SBL_ISP
TGT_JTAG_IRQ
P1.0/ENET-TXD0
P1.1/ENET-TXD1
P1.4/ENET-TX_EN
P1.8/ENET_CRS
P1.9/ENET_RXD0
P1.10/ENET_RXD1
P1.14/ENET-RX_ER
P1.15/ENET-RX_CLK
P1.16/ENET-MDC
P1.17/ENET-MDIO
P1.18/USB_UP/PWM1.1/CAP1.0
P1.19/MC0A/USB_PPWR/CAP1.1
P1.20/MCFB0/PWM1.2/SCK0
P1.21/MCABORT/PWM1.3/SSEL0
P1.22/MC0B/USB_PWRD/MAT1.0
P1.23/MCFB1/PWM1.4/MISO0
P1.24/MCFB2/PWM1.5/MOSI0
P1.25/MC1A/MAT1.1
P1.26/MC1B/PWM1.6/CAP0.0
P1.27/CLKOUT/USB_OVRCR/CAP0.1
P1.28/MC2A/PCAP1.0/MAT0.0
P1.29/MC2B/PCAP1.1/MAT0.1
P1.30/VBUS/AD0.4
P1.31/SCK1/AD0.5
P2.0/PWM1.1/TXD1/TRACECLK
P2.1/PWM1.2/RXD1
P2.2/PWM1.3/CTS1/TRACEDATA3
P2.3/PWM1.4/DCD1/TRACEDATA2
P2.4/PWM1.5/DSR1/TRACEDATA1
P2.5/PWM1.6/DTR1/TRACEDATA0
P2.6/PCAP1.0/RI1/TRACECLK
P2.7/CAN_RX2/RTS1
P2.8/CAN_TX2/TXD2
P2.9/USB_CONNECT/RXD2
P2.10/EINT0N/NMI
P2.11/EINT1N/I2STX_CLK
P2.12/EINT2N/I2STX_WS
P2.13/EINT3N/I2STX_SDA
P3.25/MAT0.0/PWM1.2
P3.26/STCLK/MAT0.1/PWM1.3
P0.0/CAN_RX1/TXD3/SDA1
P0.1/CAN_TX1/RXD3/SCL1
P0.2/TXD0/AD0.7
P0.3/RXD0/AD0.6
P0.4/I2SRX_CLK/CAN_RX2/CAP2.0
P0.5/I2SRX_WS/CAN_TX2/CAP2.1
P0.6/I2SRX_SDA/SSEL1/MAT2.0
P0.7/I2STX_CLK/SCK1/MAT2.1
P0.8/I2STX_WS/MISO1/MAT2.2
P0.9/I2STX_SDA/MOSI1/MAT2.3
P0.10/TXD2/SDA2/MAT3.0
P0.11/RXD2/SCL2/MAT3.1
P0.15/TXD1/SCK0/SCK
P0.16/RXD1/SSEL0/SSEL
P0.17/CTS1/MISO0/MISO
P0.18/DCD1/MOSI0/MOSI1
P0.19/DSR1/MCICLK/SDA1
P0.20/DTR1/SCL1
P0.21/RI1/CAN_RX1
P0.22/RTS1/CAN_TX1
P0.23/AD0.0/I2SRX_CLK/CAP3.0
P0.24/AD0.1/I2SRX_WS/CAP3.1
P0.25/AD0.2/I2SRX_SDA/TXD3
P0.26/AD0.3/AOUT/RXD3
P0.27/SDA0/USB_SDA
P0.28/SCL0/USB_SCL
P0.29/USB_D+
P0.30/USB_D-
P4.28/RX_MCLK/MAT2.0/TXD3
P4.29/TX_MCLK/MAT2.1/RXD3
DIP9
DIP10
TGT_SBL_TXD
TGT_SBL_RXD
DIP30
DIP29
DIP8
DIP7
DIP6
DIP5
DIP28
DIP27
DIP13
DIP14
DIP12
DIP11
DIP15
DIP16
DIP17
DIP18
R16
33R
TGT_D+
R17
33R
TGT_D-
R18
1k5
C18
18pF
C19
18pF
TGT_SCON
T2
BSS84
+3,3V
LED-1
R19
220R
BLUE
LED2
LED-2
R20
220R
BLUE
LED3
LED-3
220R
R21
BLUE
LED4
LED-4
220R
R22
BLUE
LED5
* Note 1 - Thi sis connected to VDD3v3 so that the LPC2368 will work on the same PCB
mbed
Project-Version: mbed-005.1
Date / Time: 26/08/2010 16:42:39
Sheet: 3/5

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9.2.1 Digital I/O ports

- Accelerated GPIO functions:
  - GPIO registers are located on a peripheral AHB bus for fast I/O timing.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte, half-word, and word addressable.
  - Entire port value can be written in one instruction.
  - GPIO registers are accessible by the GPDMA.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- All GPIO registers support Cortex-M3 bit-banding.
- GPIO registers are accessible by the GPDMA controller to allow DMA of data to or from GPIOs, synchronized to any DMA request.
- Direction control of individual port bits.
- All I/Os default to input with pullup after reset.

Table 102. GPIO register map (local bus accessible registers - enhanced GPIO features)

Generic Name	Description	Access	Reset value[1]	PORTn Register Name & Address
FIODIR	Fast GPIO Port Direction control register. This register individually controls the direction of each port pin.	R/W	0	FIO0DIR - 0x2009 C000 FIO1DIR - 0x2009 C020 FIO2DIR - 0x2009 C040 FIO3DIR - 0x2009 C060 FIO4DIR - 0x2009 C080
FIOMASK	Fast Mask register for port. Writes, sets, clears, and reads to port (done via writes to FIOPIN, FIOSET, and FIOCLR, and reads of FIOPIN) alter or return only the bits enabled by zeros in this register.	R/W	0	FIO0MASK - 0x2009 C010 FIO1MASK - 0x2009 C030 FIO2MASK - 0x2009 C050 FIO3MASK - 0x2009 C070 FIO4MASK - 0x2009 C090
FIOPIN	Fast Port Pin value register using FIOMASK. The current state of digital port pins can be read from this register, regardless of pin direction or alternate function selection (as long as pins are not configured as an input to ADC). The value read is masked by ANDing with inverted FIOMASK. Writing to this register places corresponding values in all bits enabled by zeros in FIOMASK. **Important:** if an FIOPIN register is read, its bit(s) masked with 1 in the FIOMASK register will be read as 0 regardless of the physical pin state.	R/W	0	FIO0PIN - 0x2009 C014 FIO1PIN - 0x2009 C034 FIO2PIN - 0x2009 C054 FIO3PIN - 0x2009 C074 FIO4PIN - 0x2009 C094
FIOSET	Fast Port Output Set register using FIOMASK. This register controls the state of output pins. Writing 1s produces highs at the corresponding port pins. Writing 0s has no effect. Reading this register returns the current contents of the port output register. Only bits enabled by 0 in FIOMASK can be altered.	R/W	0	FIO0SET - 0x2009 C018 FIO1SET - 0x2009 C038 FIO2SET - 0x2009 C058 FIO3SET - 0x2009 C078 FIO4SET - 0x2009 C098
FIOCLR	Fast Port Output Clear register using FIOMASK. This register controls the state of output pins. Writing 1s produces lows at the corresponding port pins. Writing 0s has no effect. Only bits enabled by 0 in FIOMASK can be altered.	WO	0	FIO0CLR - 0x2009 C01C FIO1CLR - 0x2009 C03C FIO2CLR - 0x2009 C05C FIO3CLR - 0x2009 C07C FIO4CLR - 0x2009 C09C

[1] Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 106. Fast GPIO port output Set register (FIO0SET to FIO4SET - addresses 0x2009 C018 to 0x2009 C098) bit description

Bit	Symbol	Value	Description	Reset value
31:0	FIO0SET FIO1SET FIO2SET FIO3SET FIO4SET		Fast GPIO output value Set bits. Bit 0 in FIOxSET controls pin Px.0, bit 31 in FIOxSET controls pin Px.31.	0x0
		0	Controlled pin output is unchanged.	
		1	Controlled pin output is set to HIGH.	

Aside from the 32-bit long and word only accessible FIOxSET register, every fast GPIO port can also be controlled via several byte and half-word accessible registers listed in Table 107, too. Next to providing the same functions as the FIOxSET register, these additional registers allow easier and faster access to the physical port pins.

Table 107. Fast GPIO port output Set byte and half-word accessible register description

Generic Register name	Description	Register length (bits) & access	Reset value	PORTn Register Address & Name
FIOxSET0	Fast GPIO Port x output Set register 0. Bit 0 in FIOxSET0 register corresponds to pin Px.0 … bit 7 to pin Px.7.	8 (byte) R/W	0x00	FIO0SET0 - 0x2009 C018 FIO1SET0 - 0x2009 C038 FIO2SET0 - 0x2009 C058 FIO3SET0 - 0x2009 C078 FIO4SET0 - 0x2009 C098
FIOxSET1	Fast GPIO Port x output Set register 1. Bit 0 in FIOxSET1 register corresponds to pin Px.8 … bit 7 to pin Px.15.	8 (byte) R/W	0x00	FIO0SET1 - 0x2009 C019 FIO1SET1 - 0x2009 C039 FIO2SET1 - 0x2009 C059 FIO3SET1 - 0x2009 C079 FIO4SET1 - 0x2009 C099
FIOxSET2	Fast GPIO Port x output Set register 2. Bit 0 in FIOxSET2 register corresponds to pin Px.16 … bit 7 to pin Px.23.	8 (byte) R/W	0x00	FIO0SET2 - 0x2009 C01A FIO1SET2 - 0x2009 C03A FIO2SET2 - 0x2009 C05A FIO3SET2 - 0x2009 C07A FIO4SET2 - 0x2009 C09A
FIOxSET3	Fast GPIO Port x output Set register 3. Bit 0 in FIOxSET3 register corresponds to pin Px.24 … bit 7 to pin Px.31.	8 (byte) R/W	0x00	FIO0SET3 - 0x2009 C01B FIO1SET3 - 0x2009 C03B FIO2SET3 - 0x2009 C05B FIO3SET3 - 0x2009 C07B FIO4SET3 - 0x2009 C09B
FIOxSETL	Fast GPIO Port x output Set Lower half-word register. Bit 0 in FIOxSETL register corresponds to pin Px.0 … bit 15 to pin Px.15.	16 (half-word) R/W	0x0000	FIO0SETL - 0x2009 C018 FIO1SETL - 0x2009 C038 FIO2SETL - 0x2009 C058 FIO3SETL - 0x2009 C078 FIO4SETL - 0x2009 C098
FIOxSETU	Fast GPIO Port x output Set Upper half-word register. Bit 0 in FIOxSETU register corresponds to Px.16 … bit 15 to Px.31.	16 (half-word) R/W	0x0000	FIO0SETU - 0x2009 C01A FIO1SETU - 0x2009 C03A FIO2SETU - 0x2009 C05A FIO3SETU - 0x2009 C07A FIO4SETU - 0x2009 C09A