Datos Personales

Nombres Pedro Antonio

Apellidos Coronel Mendoza

Fecha de 1-Oct-1982

Nacimiento

Lugar de Asunción

Nacimiento

Nacionalidad Paraguaya

Documento 3.711.332

de Identidad

Dirección Soldado Robustiano Quintana 1053

Email pcoron3l@gmail.com

Educación

1990-2001 Bachiller Técnico en Informatica, Colegio "Sgdo. Corazón de Jesús Salesianito".

2002-2008 Licenciado en Informática, Universidad Católica Ntra. Sra. de la Asunción, Carrera: Ingenieria en Informática.

2011- Maestría en Gestion de Sistemas, Universidad Autónoma de Asunción.

Actualidad

Otros Estudios

1997-1999 Ingles Avanzado, Anglo Paraguayo.

2000 Curso de Base de Datos en Telecel, Durante la Pasantía Laboral.

2008 SQL – Oracle, Universidad Católica.

2011 PMI -PMP Metodología en dirección de proyectos (PMBok), Centro de Calidad de Software.

2012 Curso Oracle in memory database – TimesTen, Exelsys.

2011 Curso de gestión de Calidad de Software – Software Testing – CMMI, Centro de Calidad de Software.

Seminarios y Conferencias

2008 ETYC - UNA, Universidad Nacional de Asunción.

2008 CLEI, Universidad Politecnica de Santa Fé, Santa Fé - Argentina.

2008 JIT CITA, Universidad Católica.

2008 Semana Cyt UCA, Universidad Católica.

2011 JIT CITA, Universidad Autonoma de Asuncion.

2012 Seminario de Gestión de Proyectos con Metodologías Agiles , Universidad Nacional de Asunción.

2012 Seminario de introducción a ITIL, Centro de Calidad de Software.

Experience

2010 IC Design Engineer, IMEC Netherlands, Eindhoven.

Working under minimum supervision; Understanding and learning of EDA tools; DSP group meetings, conference calls and technical reports.

2009 Teaching Assistant, University of Patras, Patras.

Set up of laboratory equipment and experiments; Guidance and supervision of undergraduate students.

2008 Intern student, Greek Public Power Corporation, Patras.

Assistance work within the department of physical network expansion.

Master Thesis

Title Optimized SIMD scheduling and architecture exploration and implementation for ultralow energy processor architectures

Supervisors Francky Catthoor, Constantinos Goutis

Description Project follows the complete flow of the implementation of an ASIP from high-level processor architecture design and Test Vector generation process to power dissipation measurements

Bachelor Thesis

Title Processor hardware implementation for Galois Counter Mode (GCM-AES) security encryption standard

Supervisors Constantinos Goutis

Description Project based on VHDL design language; Hardware architecture design of an encryption algorithm; Validation using C programming and implementation on a Xilinx FPGA

Other Projects

Master projects

VHDL Design and implementation of a multiply - add unit, Modeling using Octave, Testing in a Xilinx FPGA using a logic analyzer

VHDL Architectural exploration of a LMS filter, Optimization for power, area and performance

C Optimization of an edge - detection algorithm using compiler transformations

C Implementation of a compression algorithm to reduce testing data

UPPAAL Modeling and simulation of a Philips bus collision protocol

Bachelor Projects

VHDL Implementation of Booth multiplier and MESI protocol

Assembly Implementation of Virtual Mode for x86 processors

PSpice Implementation of parallel multiplier based on Wallace tree adders

C Development of a client management program implementing a hashing algorithm

Languages

Greek Native

English Fluent ECPE Proficiency in English, University of Michigan, 2005

French Basic DELF A1, Ministere Français de L'Education Nationale, 2000

Computer skills

Basic UML, HTML, C++, Tcl, System C

 $Intermediate \quad C, \, Matlab, \, Assembly (Intel \, x86)$

Expert VHDL, nML

 ${\it Tools} \quad {\it Cadence, Xilinx, Target, UPPAAL, Simplescalar}$