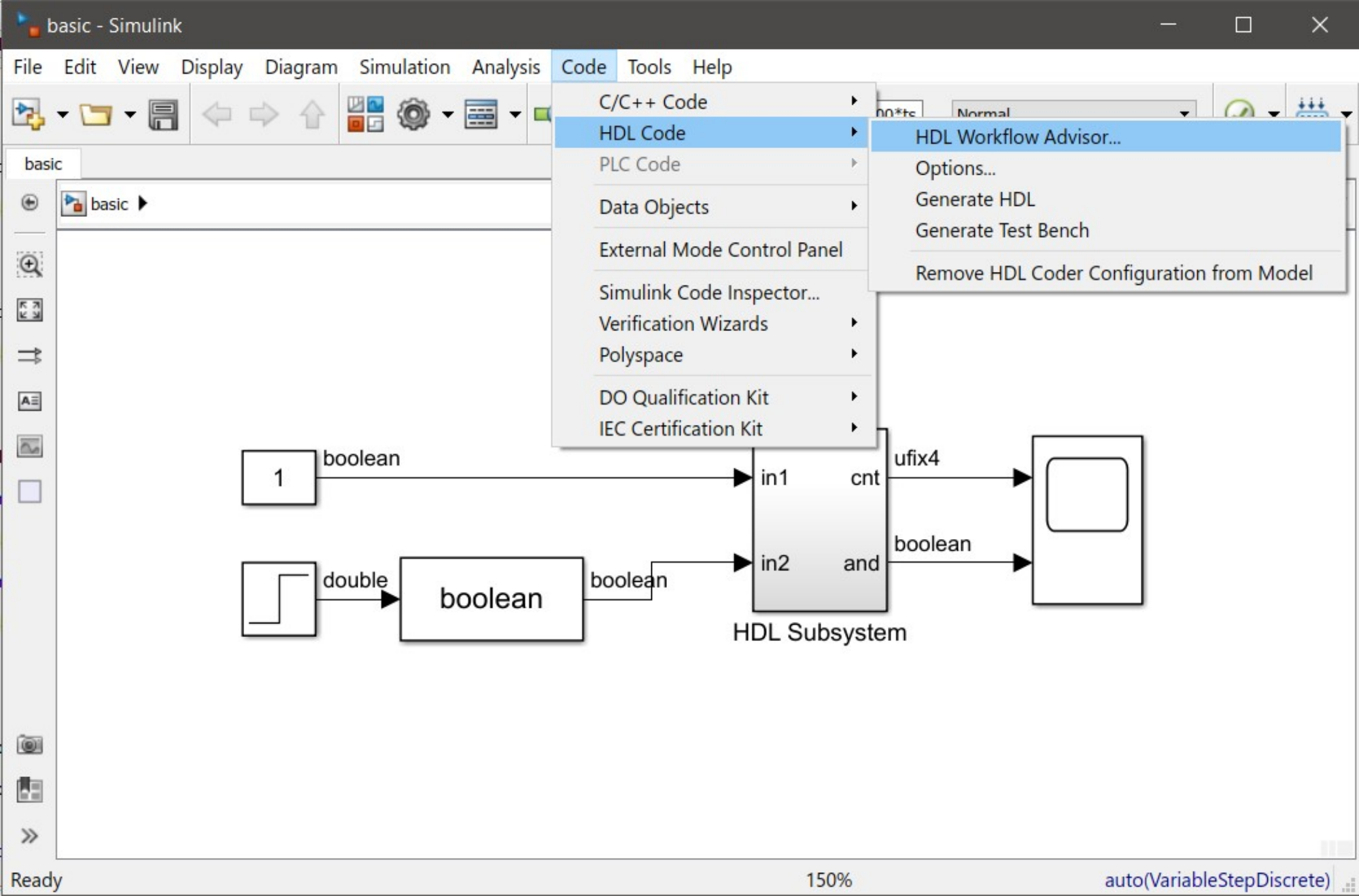
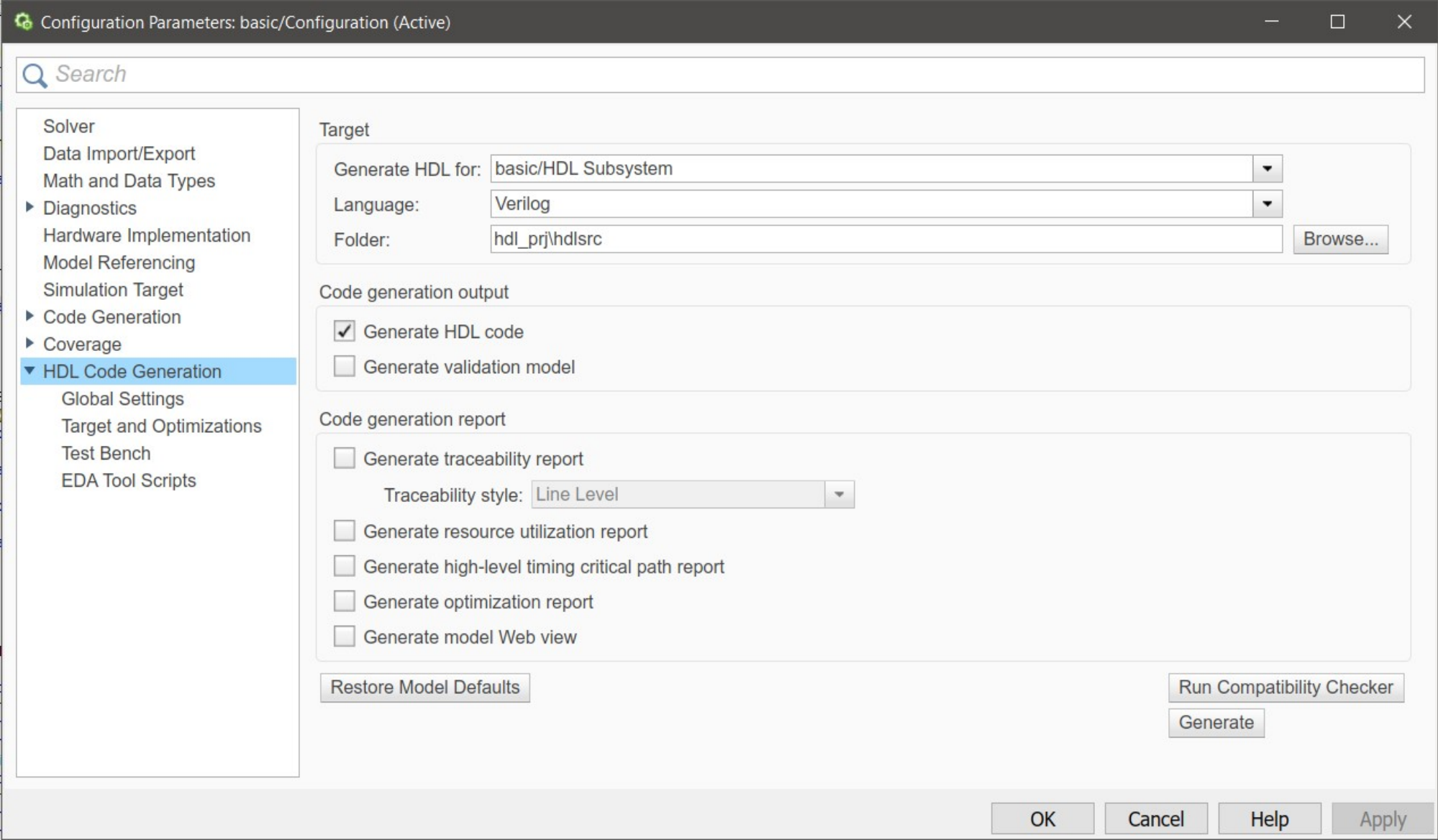

basic - Simulink
File
Edit
View
Display
Diagram
Simulation
Analysis
Code
Tools
Help
C/C++ Code
HDL Code
PLC Code
Data Objects
External Mode Control Panel
Simulink Code Inspector...
Verification Wizards
Polyspace
DO Qualification Kit
IEC Certification Kit
HDL Workflow Advisor...
Options...
Generate HDL
Generate Test Bench
Remove HDL Coder Configuration from Model
basic
1
boolean
in1
cnt
ufix4
in2
and
boolean
double
boolean
boolean
HDL Subsystem
Ready
150%
auto(VariableStepDiscrete)


Configuration Parameters: basic/Configuration (Active)
Search
Solver
Data Import/Export
Math and Data Types
Diagnostics
Hardware Implementation
Model Referencing
Simulation Target
Code Generation
Coverage
HDL Code Generation
Global Settings
Target and Optimizations
Test Bench
EDA Tool Scripts
Target
Generate HDL for: basic/HDL Subsystem
Language: Verilog
Folder: hdl_prj\hdlsrc
Browse...
Code generation output
Generate HDL code
Generate validation model
Code generation report
Generate traceability report
Traceability style: Line Level
Generate resource utilization report
Generate high-level timing critical path report
Generate optimization report
Generate model Web view
Restore Model Defaults
Run Compatibility Checker
Generate
OK
Cancel
Help
Apply

Configuration Parameters: basic/Configuration (Active)

Search

- Solver
- Data Import/Export
- Math and Data Types
- Diagnostics
- Hardware Implementation
- Model Referencing
- Simulation Target
- Code Generation
- Coverage
- HDL Code Generation
  - Global Settings
  - Target and Optimizations
  - Test Bench
  - EDA Tool Scripts

Clock settings

Reset type:	Asynchronous	Reset asserted level:	Active-high
Clock input port:	clk	Clock enable input port:	clk_enable
Reset input port:	reset	Clock inputs:	Single
Oversampling factor:	1	Clock edge:	Rising

Additional settings

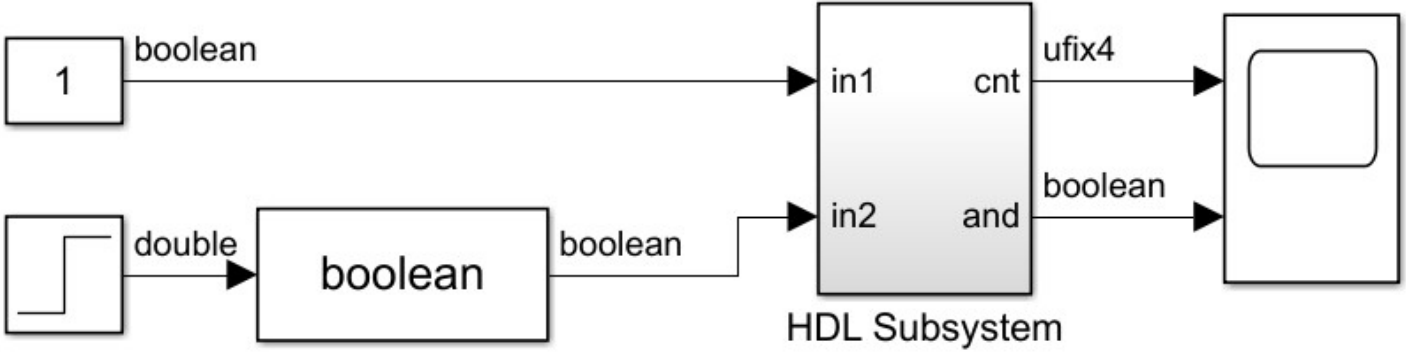
General | Ports | Coding style | Coding standards | Diagnostics | Floating Point Target

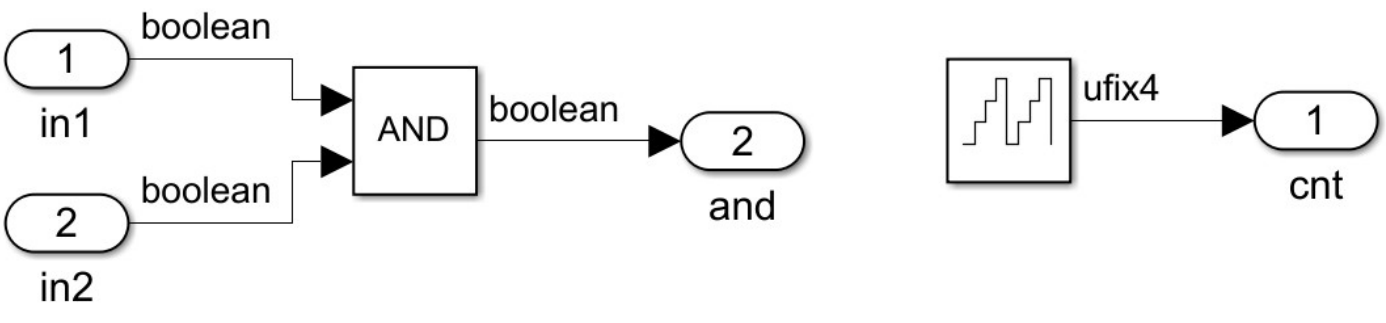
Comment in header:	<empty>		
Verilog file extension:	.v	VHDL file extension:	.vhd
Entity conflict postfix:	_block	Package postfix:	_pkg
Reserved word postfix:	_rsvd	Split entity file postfix:	_entity
Clocked process postfix:	_process	Split arch file postfix:	_arch
Complex real part postfix:	_re	Split entity and architecture	
Complex imaginary part postfix:	_im	VHDL architecture name:	rtl
		Module name prefix:	<empty>
Enable prefix:	enb	Timing controller postfix:	_tc
Pipeline postfix:	_pipe		
VHDL library name:	work		

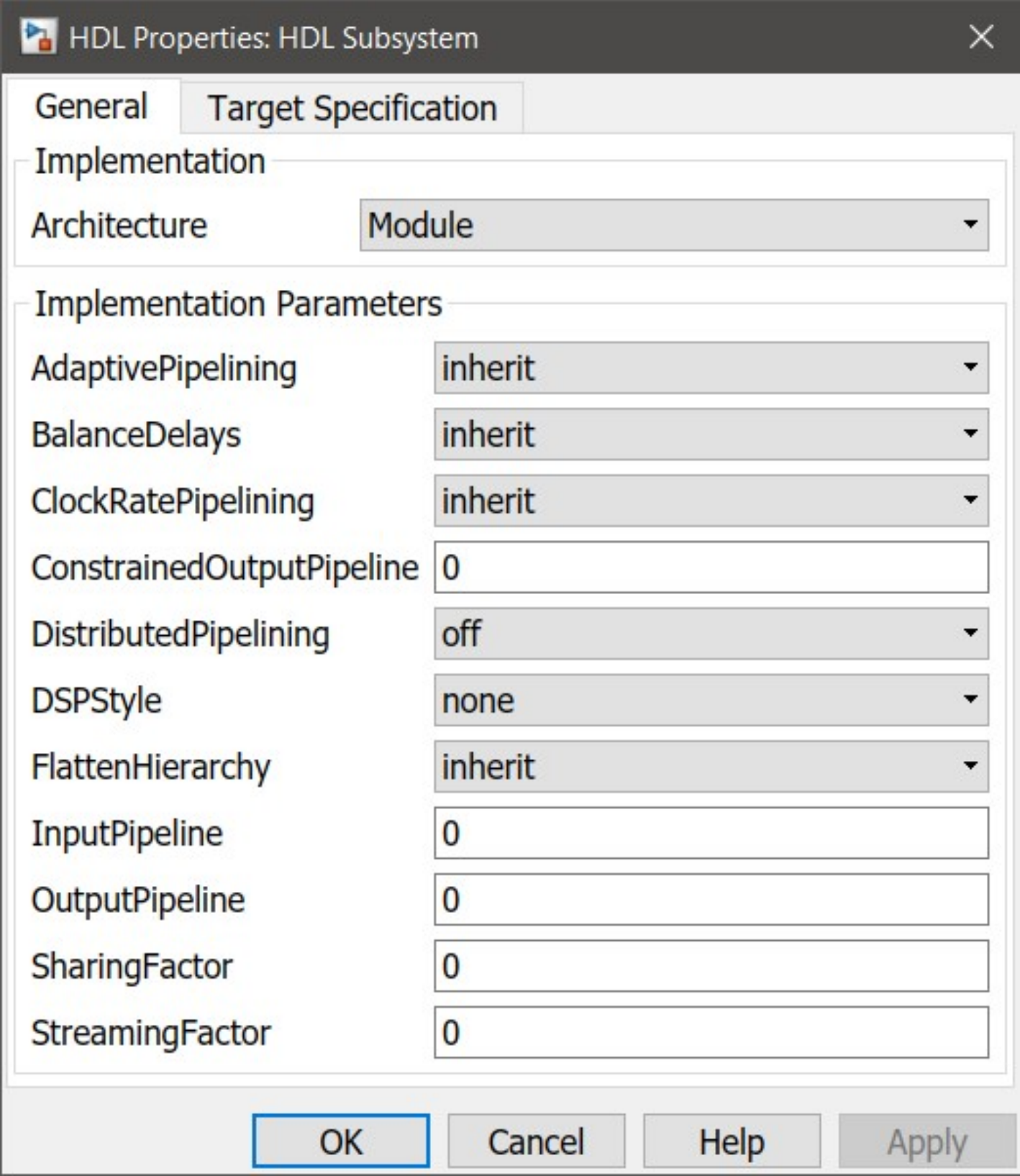
Generate VHDL code for model references into a single library

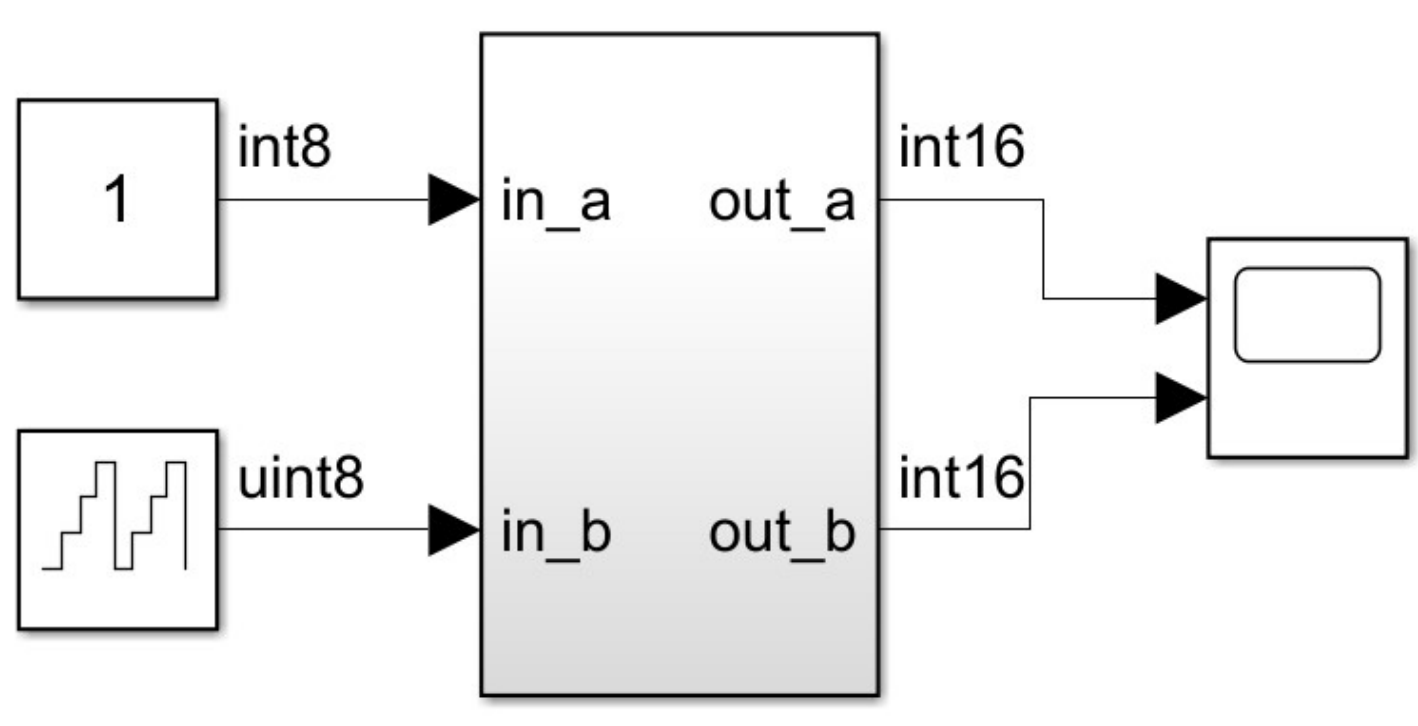
Block generate label:	_gen	Output generate label:	outputgen
Instance generate label:	_gen	Vector prefix:	vector_of_
Instance prefix:	u_	Instance postfix:	<empty>
Prefix for the generated model name:	gm_	Map file postfix :	_map.txt

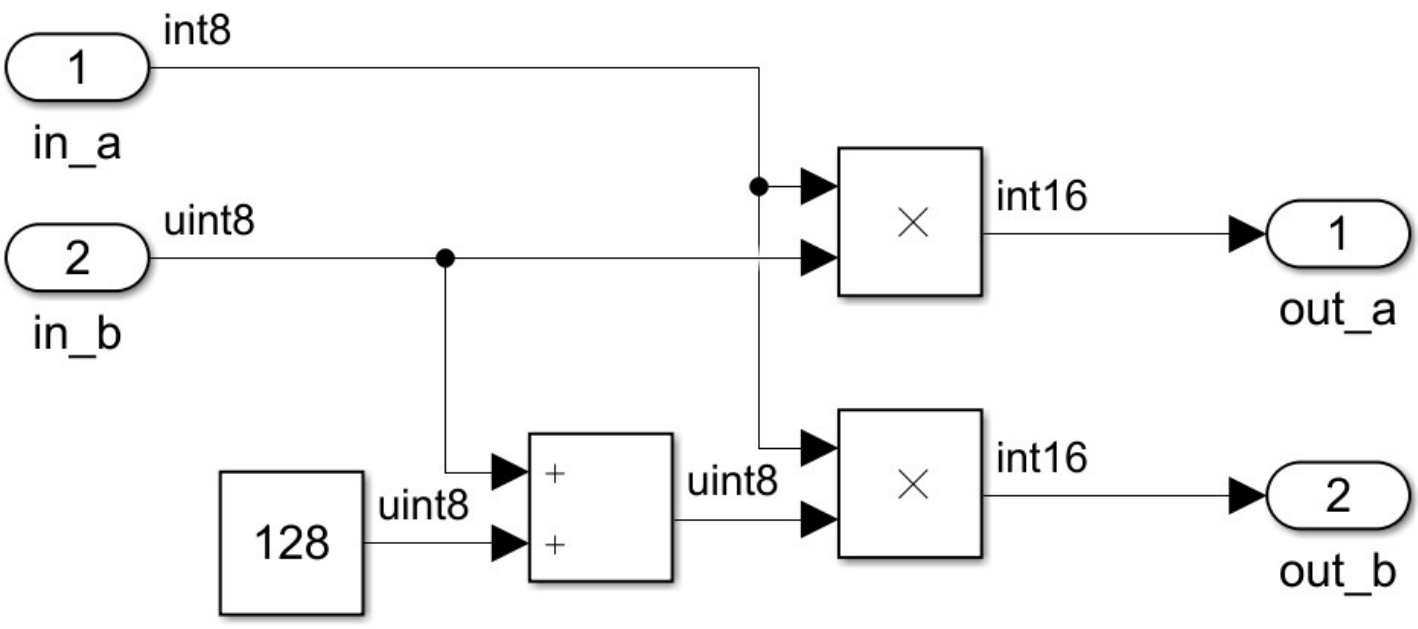
OK | Cancel | Help | Apply

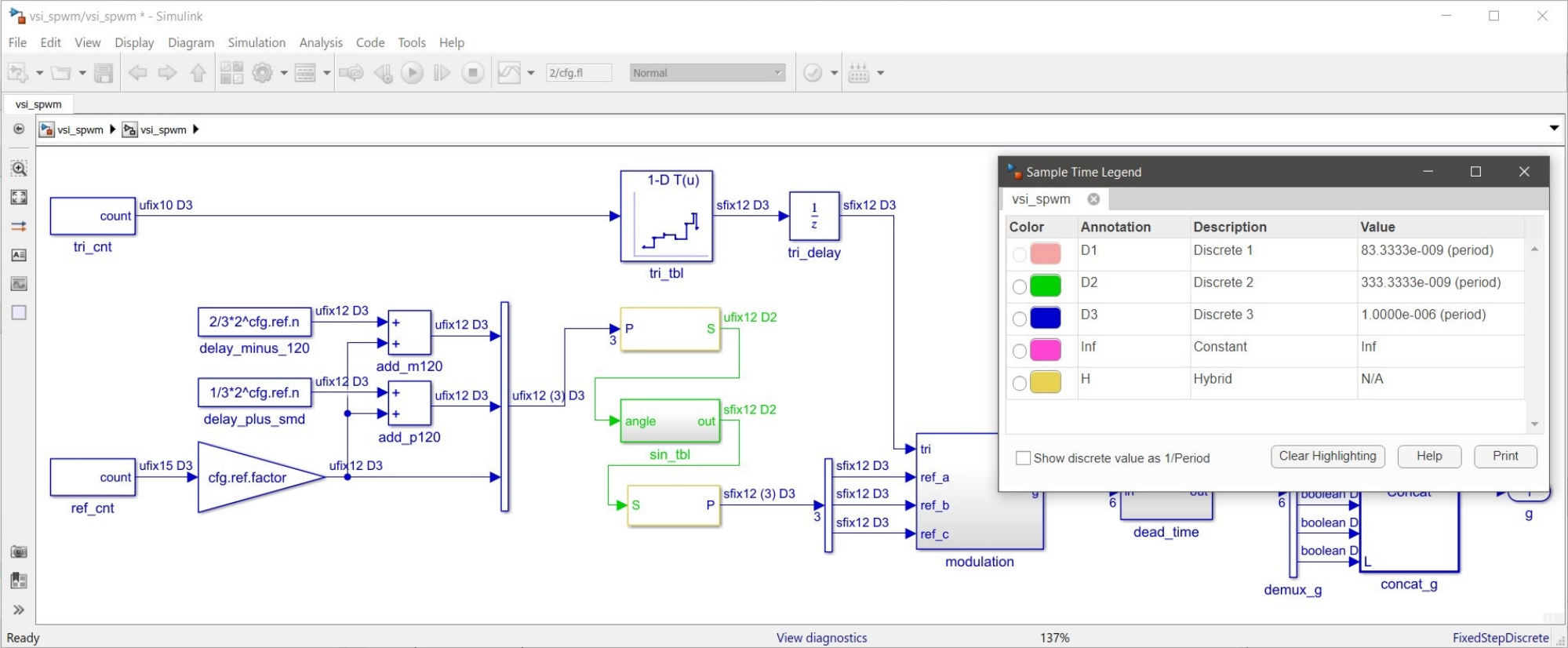

1
boolean
in1
cnt
ufix4
in2
and
boolean
double
boolean
boolean
HDL Subsystem


1
boolean
in1
2
boolean
in2
AND
boolean
2
and
ufix4
1
cnt


HDL Properties: HDL Subsystem
General
Target Specification
Implementation
Architecture
Module
Implementation Parameters
AdaptivePipelining
inherit
BalanceDelays
inherit
ClockRatePipelining
inherit
ConstrainedOutputPipeline
0
DistributedPipelining
off
DSPStyle
none
FlattenHierarchy
inherit
InputPipeline
0
OutputPipeline
0
SharingFactor
0
StreamingFactor
0
OK
Cancel
Help
Apply


1
int8
uint8
in_a
in_b
out_a
out_b
int16
int16


1
int8
in_a
2
uint8
in_b
128
uint8
+
+
uint8
int16
int16
1
out_a
2
out_b


vsi_spwm/vsi_spwm * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
vsi_spwm
count
ufix10 D3
tri_cnt
1-D T(u)
tri_tbl
sfix12 D3
1
z
tri_delay
2/3*2^cfg.ref.n
delay_minus_120
1/3*2^cfg.ref.n
delay_plus_smd
add_m120
add_p120
ufix12 D3
ufix12 (3) D3
P
S
sin_tbl
angle
out
sfix12 D2
count
ufix15 D3
ref_cnt
cfg.ref.factor
sfix12 (3) D3
tri
ref_a
ref_b
ref_c
modulation
dead_time
demux_g
concat_g
boolean D
g
Sample Time Legend
vsi_spwm
Color
Annotation
Description
Value
D1
Discrete 1
83.3333e-009 (period)
D2
Discrete 2
333.3333e-009 (period)
D3
Discrete 3
1.0000e-006 (period)
Inf
Constant
Inf
H
Hybrid
N/A
Show discrete value as 1/Period
Clear Highlighting
Help
Print
Ready
View diagnostics
137%
FixedStepDiscrete