Security HC meeting

March 31, 2022

Only RISC-V Members May Attend

- Non-members are asked to please leave except for Joint Working Groups (JWG).
- Members share IP protection by virtue of their common membership agreement. Non-members being present jeopardizes that protection. Joint working groups (JWG) agree that any IP discussed or worked on is fully open source and unencumbered as per the policy.
- It is easy to become a member. Check out riscv.org/membership
- If you need work done between non-members or or other orgs and RISC-V, please use a joint working group (JWG).
    - used to allow non-members in SIGs but the SIGs purpose has changed.
- Please put your name and company (in parens after your name) as your zoom name. If you are an individual member just use the word “individual” instead of company name.
- Non-member guests may present to the group but should only stay for the presentation. Guests should leave for any follow on discussions.

Antitrust Policy Notice

RISC-V International meetings involve participation by industry competitors, and it is the intention of RISC-V International to conduct all its activities in accordance with applicable antitrust and competition laws. It is therefore extremely important that attendees adhere to meeting agendas, and be aware of, and not participate in, any activities that are prohibited under applicable US state, federal or foreign antitrust and competition laws.

Examples of types of actions that are prohibited at RISC-V International meetings and in connection with RISC-V International activities are described in the RISC-V International Regulations Article 7 available here: https://riscv.org/regulations/

If you have questions about these matters, please contact your company counsel.

Collaborative & Welcoming Community

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/community/community-code-of-conduct/

RISC-V®

Conventions

- Unless it is a scheduled agenda topic, we don’t solve problems or detailed topics in most meetings unless specified in the agenda because we don’t often have enough time to do so and it is more efficient to do so offline and/or in email. We identify items and send folks off to do the work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unillaterly. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, …
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

Risc-V Security

Agenda

- SESIP (IoT certification methodology) presentation by Eve Atallah (NXP)
- Vice chair for the microarch side channel SIG
- Security Model TG charter

SESIP

- Over to Eve....

MicroArchitecture Side Channel SIG

- Congratulations to Allison Randal, new Vice Chair
- Joins Ronan Lashermes (Chair)

Security Model TG

- Acting Chair – Manuel Offenberg
- Draft Charter -

RVI is lacking documentation that defines platform-level security related recommendations, requirements, and guidance for RISC-V stakeholders.

This TG will create a specification that outlines the guiding principles (intrinsic security and zero trust), goals, a threat model, and security requirements & recommendations for RISC-V based implementations. The specification is expected to cover topics such as root-of-trust, platform secure boot, attestation, secure (credential) storage, recommended cryptographic algorithms, key length/strength, key lifecycles, entropy, unclonable unique identity, product life cycle (including RMA (return merchandise authorization) and debug) guidance, side-channel mitigations, platform firmware updates/resiliency, post-quantum readiness, tamper resistance, supply chain safety, and other security critical items.

The Security Model TG's scope of work:
To create a Platform Security Specification, which is a non-ISA spec;
To collect feedback and seek advice from pretty much all groups within RVI, but specifically from Security HC, Software HC, and SoC Infrastructure HC;
Will not define nor develop formal models or software-based artifacts;
To target a specification freeze by end of Q3 2022.

Any Other Status Updates

Open Action Items

Running list of open AI's