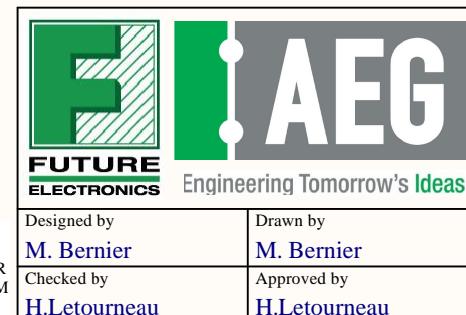
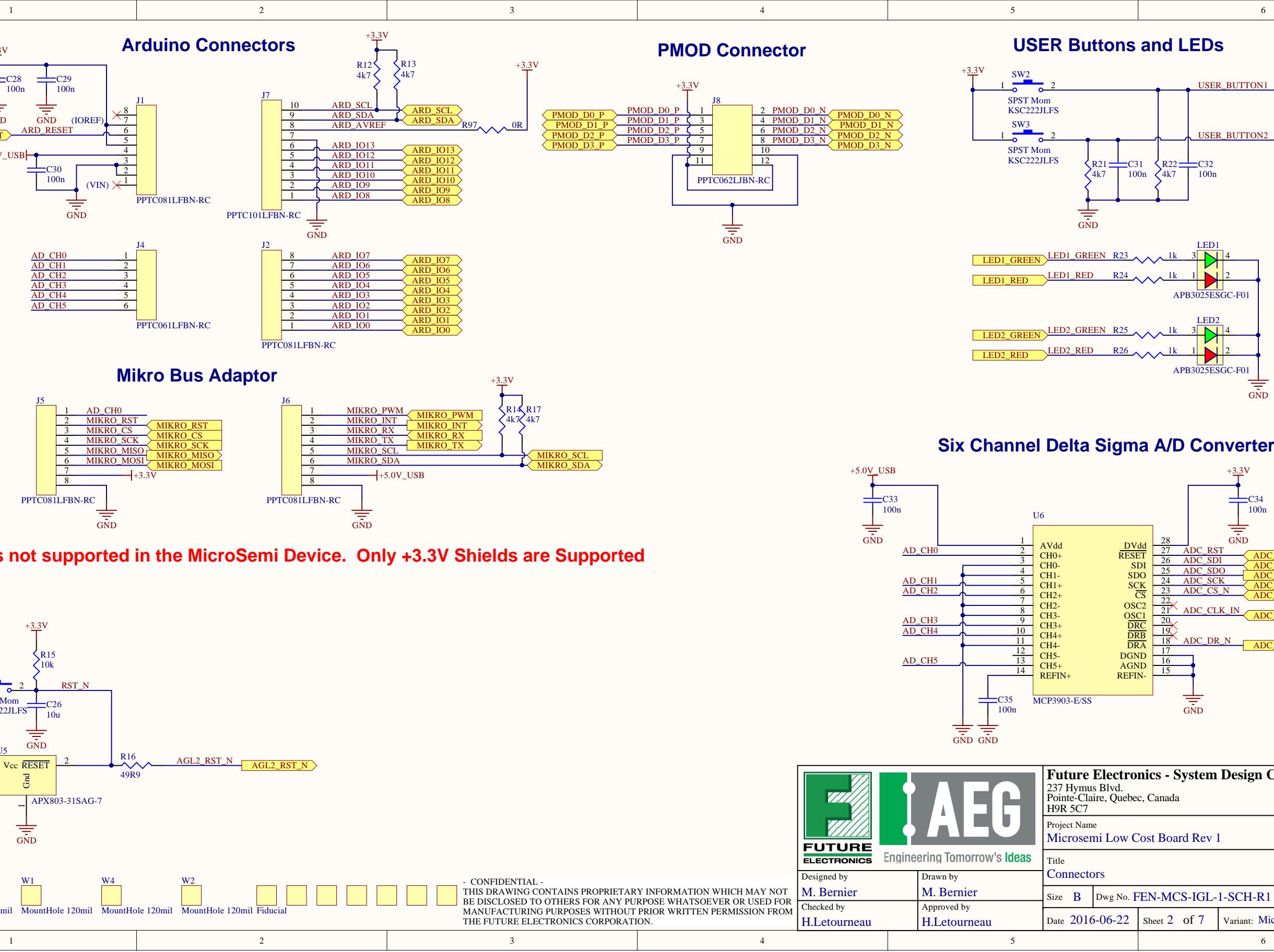


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237 Hymus Blvd. Pointe-Claire, Quebec, Canada H9R 5C7	
Project Name <b>Microsemi Low Cost Board Rev 1</b>	
Title <b>Block Diagram</b>	
Size <b>B</b> Dwg No. <b>FEN-MCS-IGL-1-SCH-R1</b> Rev <b>1</b>	
Designed by <b>M. Bernier</b> Drawn by <b>M. Bernier</b>	
Checked by <b>H.Letourneau</b> Approved by <b>H.Letourneau</b>	
Date <b>2016-06-22</b> Sheet <b>1</b> of <b>7</b> Variant: <b>Microsemi LoCostB_R1</b>	



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H9R 5C7

Project Name  
**Microsemi Low Cost Board Rev 1**

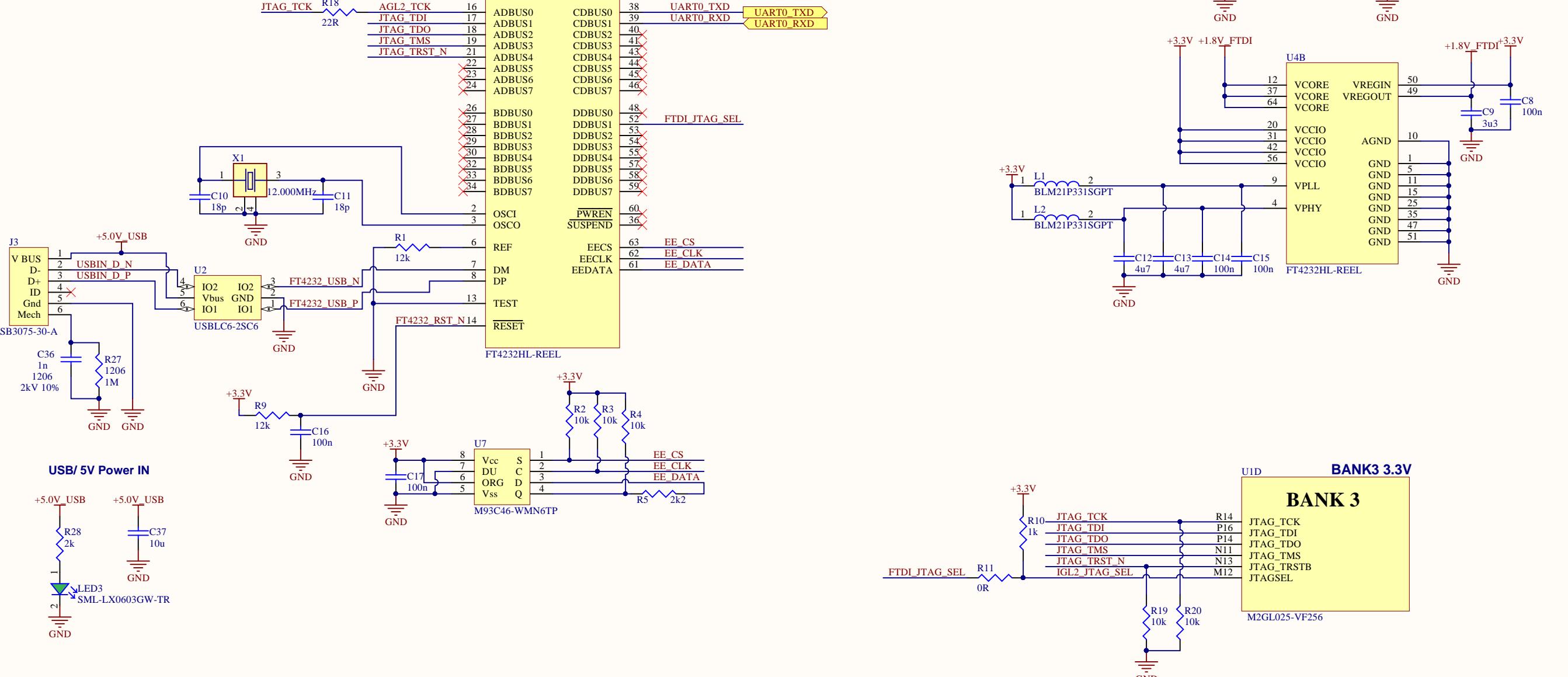
Title  
**Connectors**

Size **B** Dwg No. **FEN-MCS-IGL-1-SCH-R1** Rev **1**

Checked by **H.Letourneau** Approved by **H.Letourneau**

Date **2016-06-22** Sheet **2** of **7** Variant: **Microsemi LoCostB\_R1**

FTDI USB-JTAG



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Project Name  
Microsemi Low Cost Board Rev 1

title

TBYJAG - Page 1 of 1 - FEN-MCS-IGL-1-SGLD1

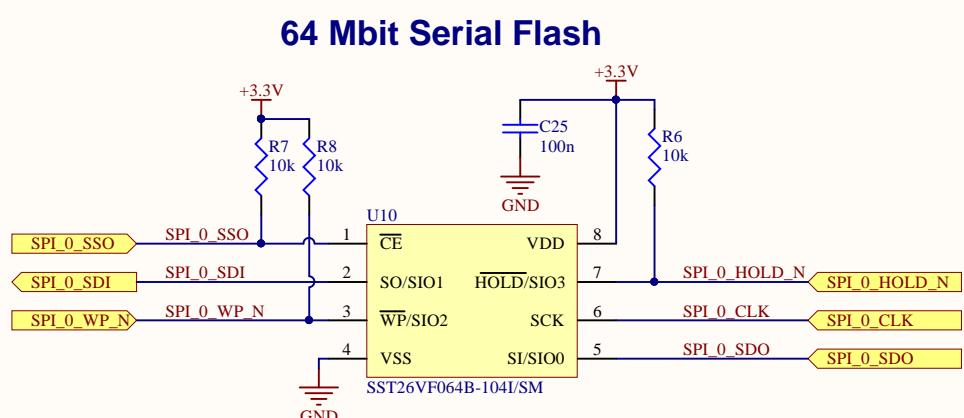
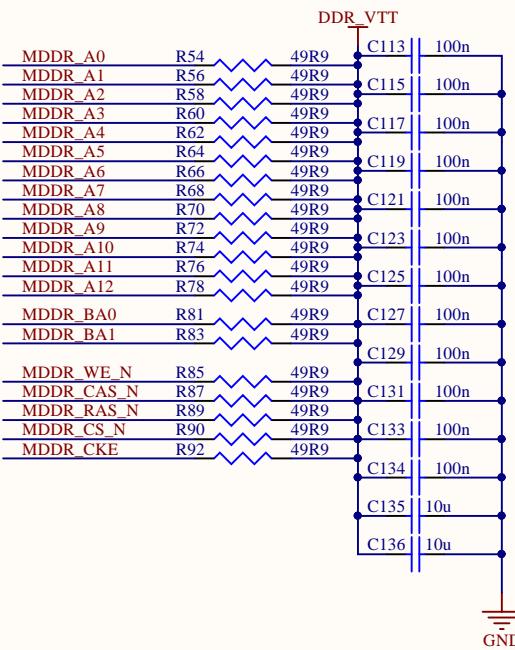
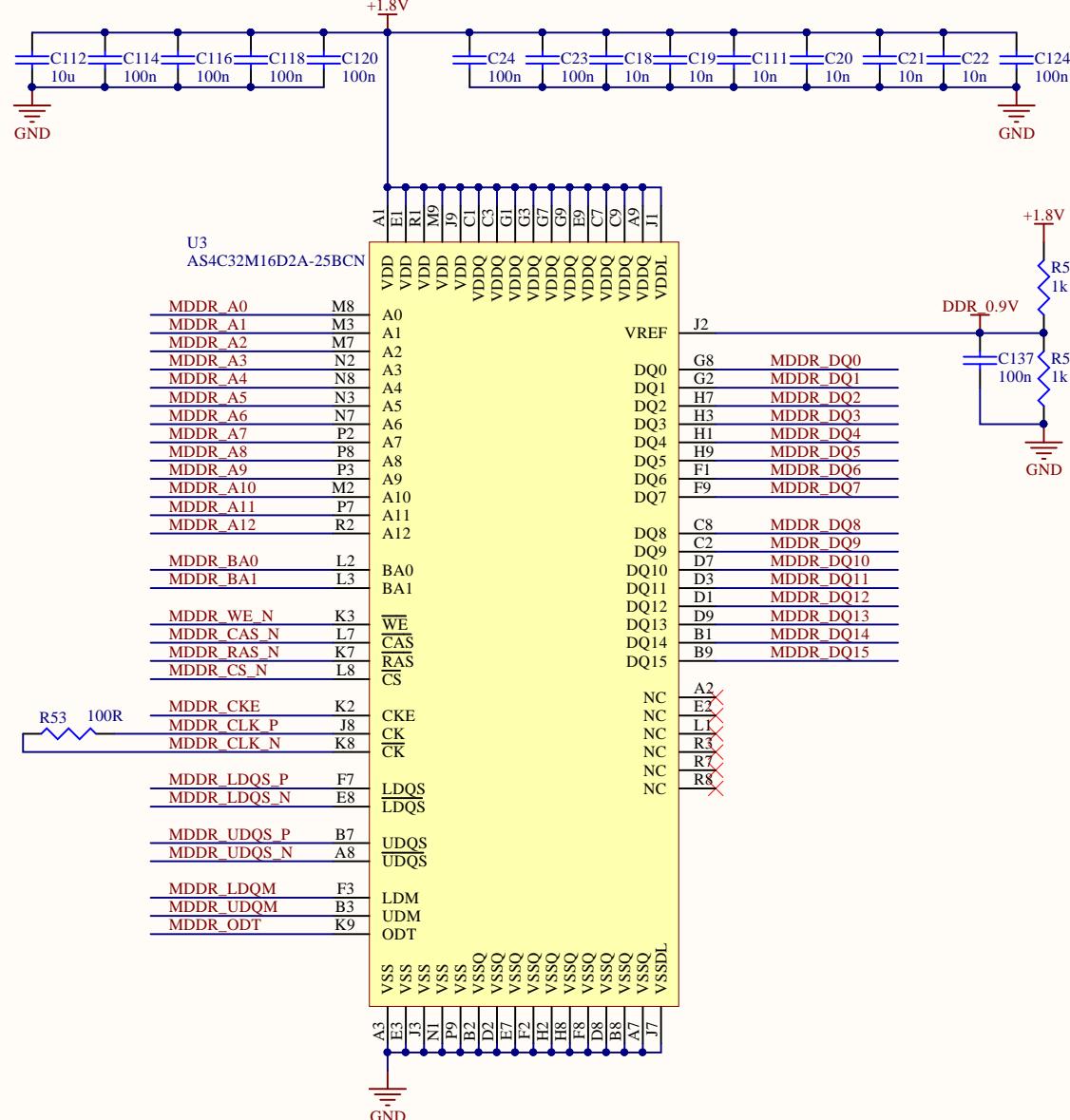
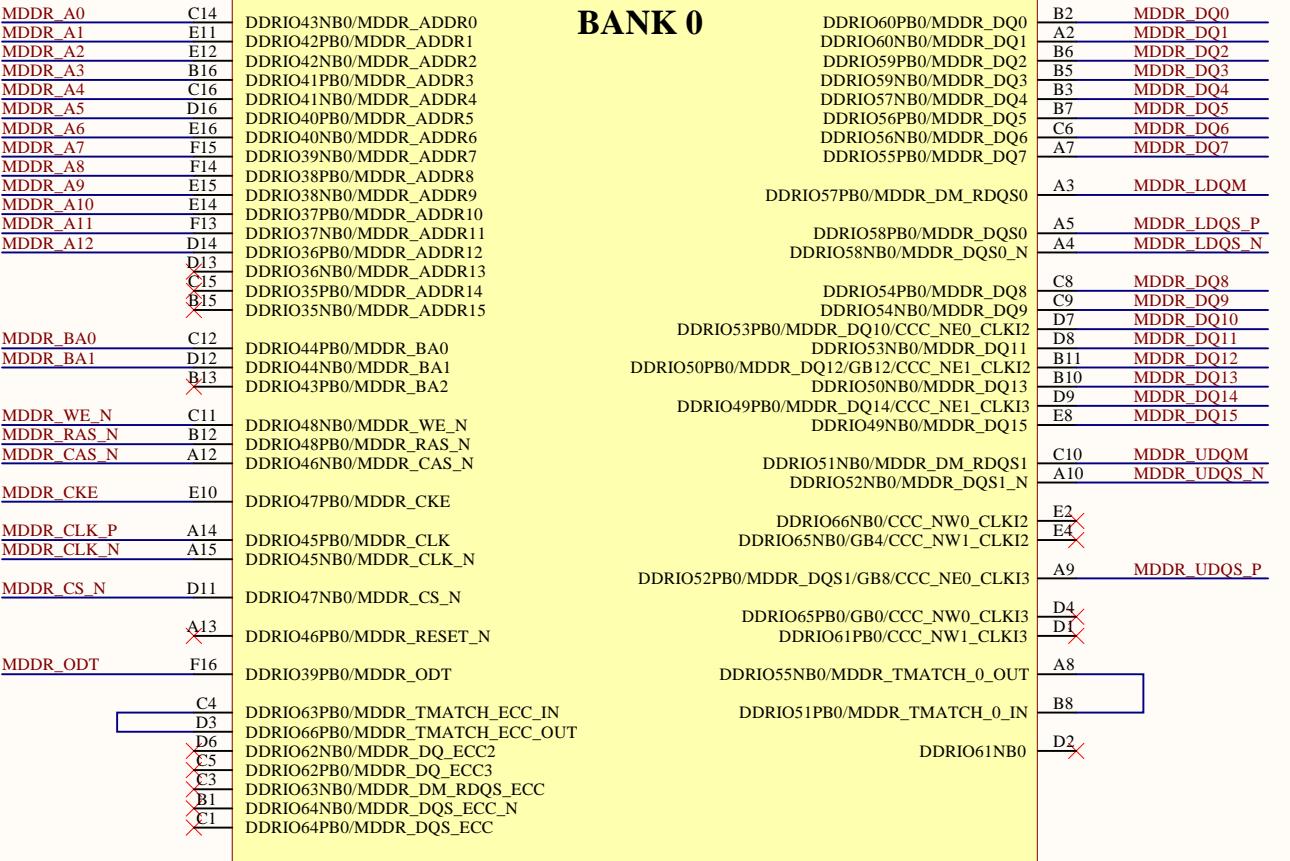
2016-06-22 2 of 7 Ueda - Microsoft Word - R1

Page 6 of 7 Variant: Microsemi LoCostB\_RT

# 32M x 16 bit DDR2 Synchronous DRAM (SDRAM)

U1A M2GL025-VF256

BANK0 1.8V

**BANK 0**

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Project Name  
Microsemi Low Cost Board Rev 1

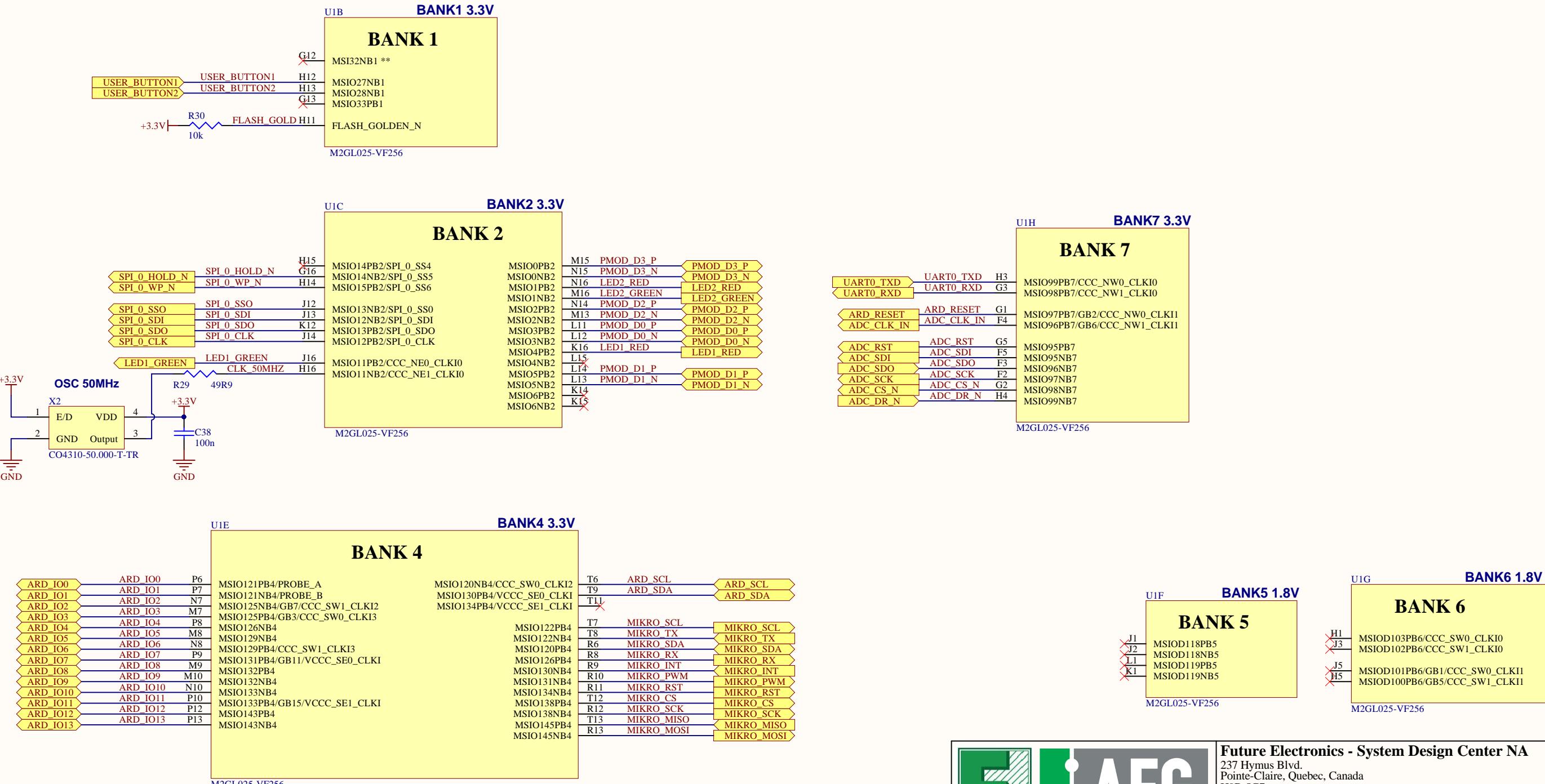
Title

DDR SDRAM

Size B Dwg No. FEN-MCS-IGL-1-SCH-R1 Rev 1

Checked by Approved by Date 2016-06-22 Sheet 4 of 7 Variant: Microsemi LoCostB\_R1

## GPIOs BANKs



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Designed by **M. Bernier** Drawn by **M. Bernier**  
Checked by **H.Letourneau** Approved by **H.Letourneau**  
Date **2016-06-22** Sheet **5** of **7** Variant: **Microsemi LoCostB\_R1**

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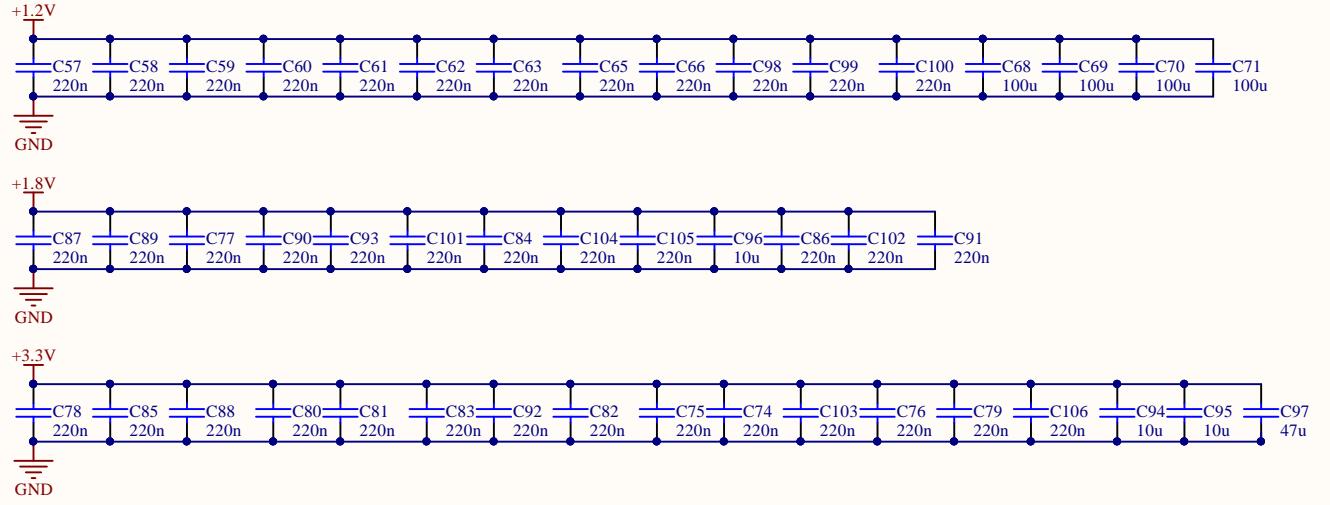
Project Name  
**Microsemi Low Cost Board Rev 1**

Title  
**FPGA IO**

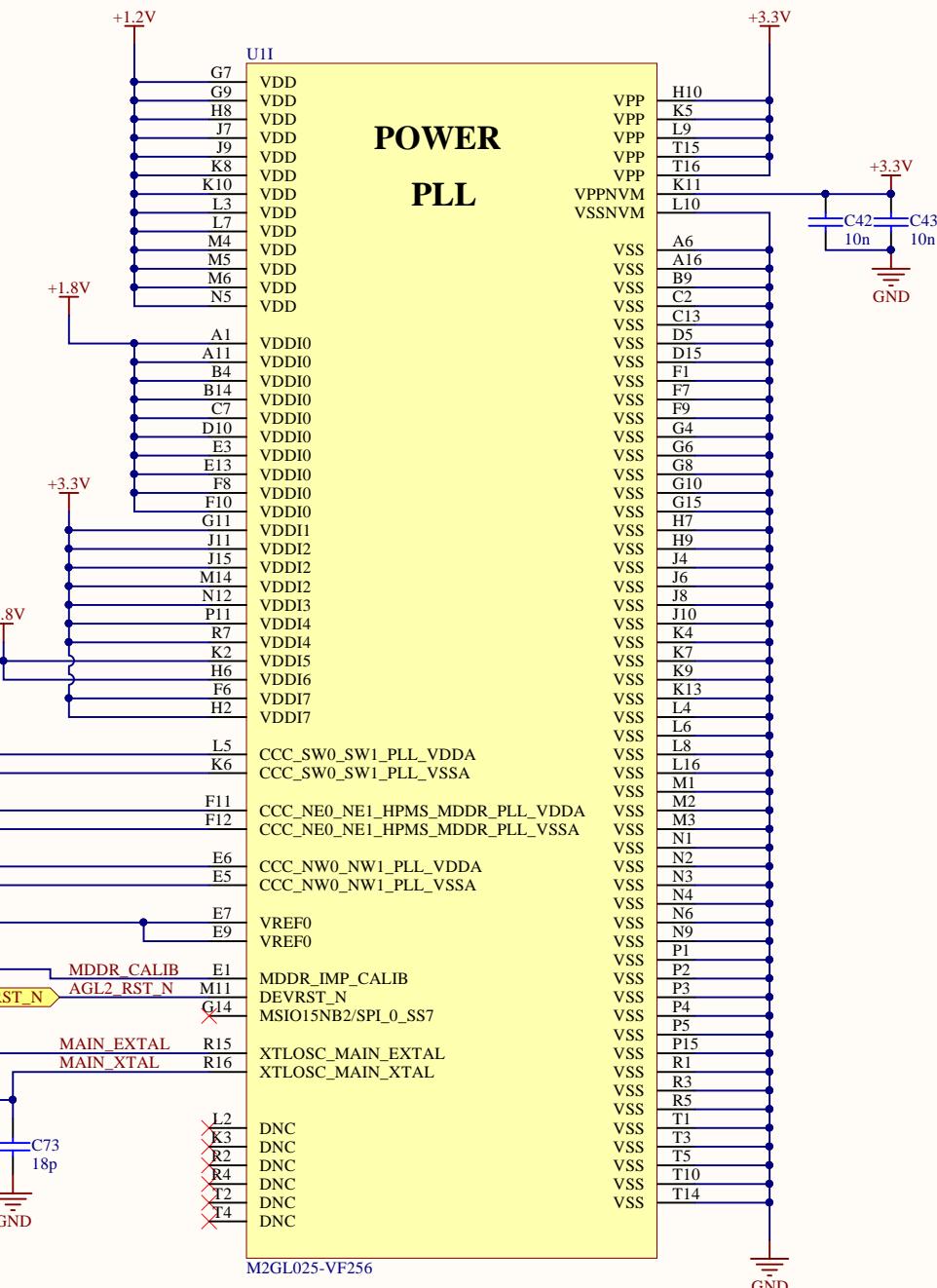
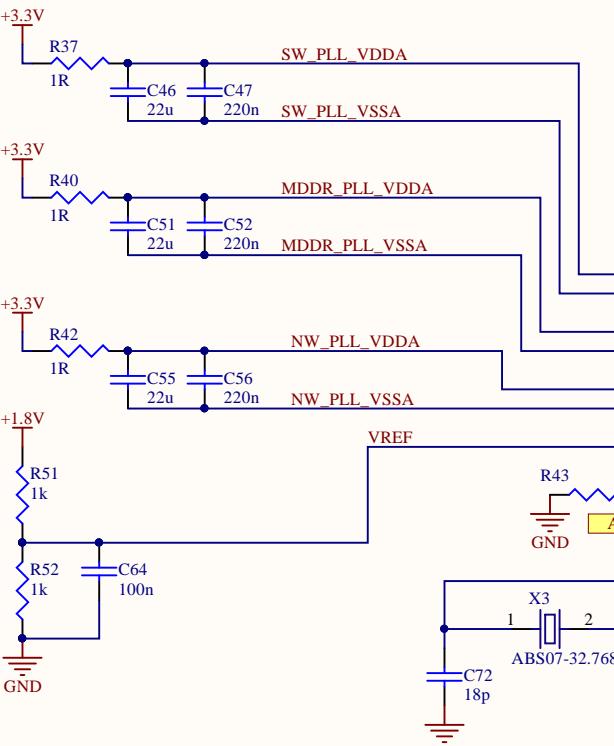
Size **B** Dwg No. **FEN-MCS-IGL-1-SCH-R1** Rev **1**

Date **2016-06-22** Sheet **5** of **7** Variant: **Microsemi LoCostB\_R1**

## POWER and DECOUPLING



See:  
microsemi\_smartfusion2\_and\_igloo2\_layout  
\_guidelines\_applicationnote\_ac394\_v5.pdf



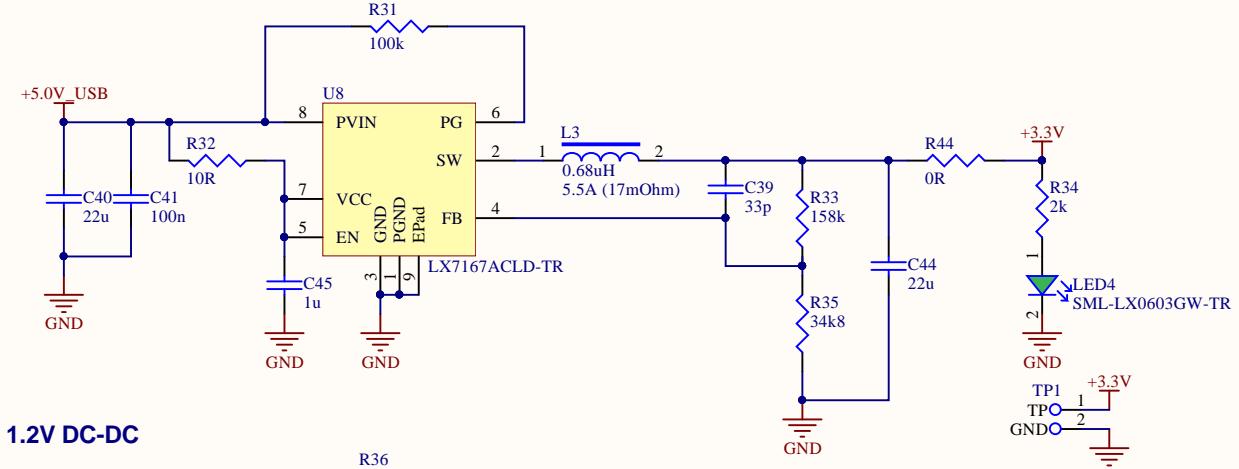
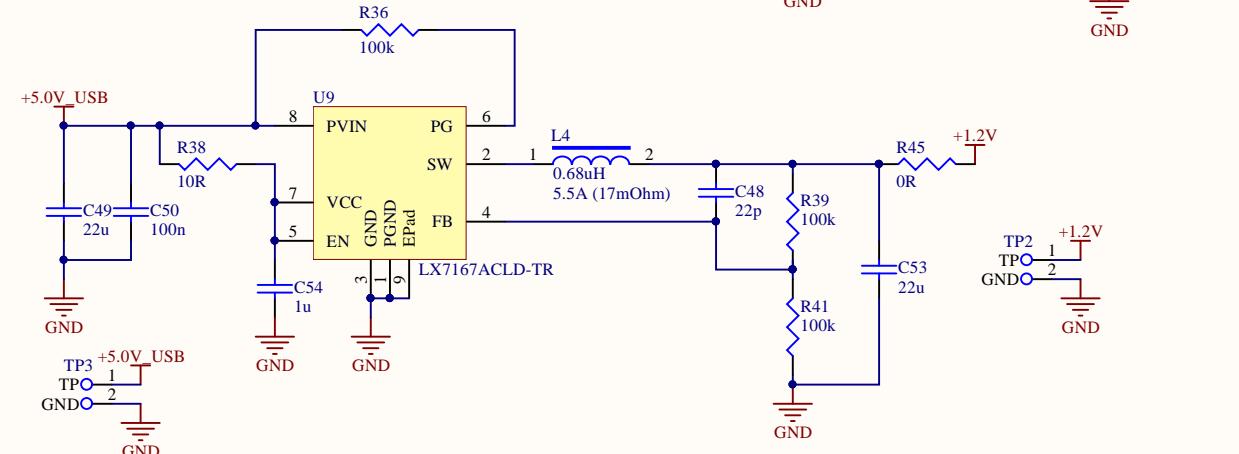
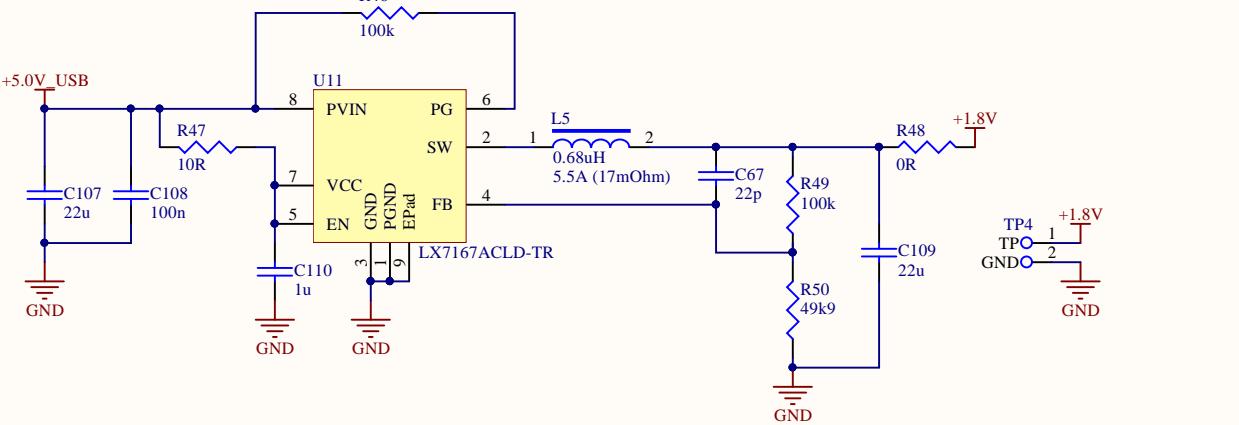
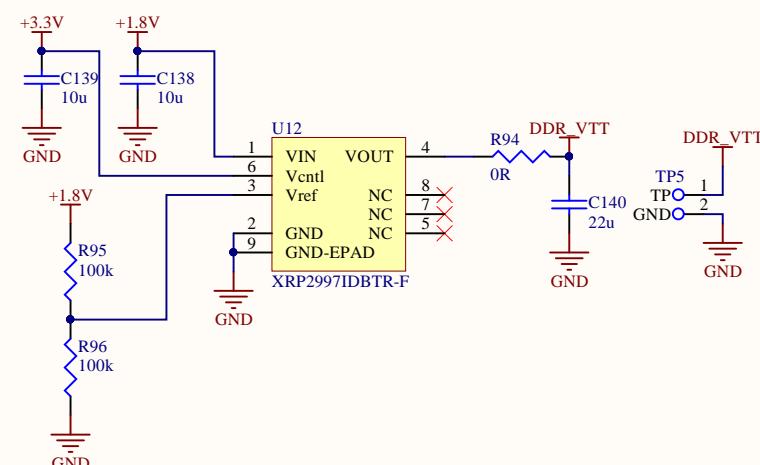
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237 Hymus Blvd.  
Pointe-Claire, Quebec, Canada  
H9R 5C7

Project Name  
**Microsemi Low Cost Board Rev 1**

Title  
**FPGA Power-PLL**  
Size **B** Dwg No. **FEN-MCS-IGL-1-SCH-R1** Rev **1**  
Designed by **M. Bernier** Drawn by **M. Bernier**  
Checked by **H.Letourneau** Approved by **H.Letourneau**  
Date **2016-06-22** Sheet **6** of **7** Variant: **Microsemi LoCostB\_R1**

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# POWER SUPPLY

**3.3V DC-DC**

**1.2V DC-DC**

**1.8V DC-DC**

**0.9V for DDR**


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 H9R 5C7

Project Name  
**Microsemi Low Cost Board Rev 1**

Title

**FPGA Power**

Size **B** Dwg No. **FEN-MCS-IGL-1-SCH-R1** Rev **1**

Checked by **H.Letourneau** Approved by **H.Letourneau**

Date **2016-06-22** Sheet **7** of **7** Variant: **Microsemi LoCostB\_R1**

Layers Top Layer (GTL)

## Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
Top Layer (GTL)	5mil	5mil	6mil			
	5mil	5mil	6mil			
	5mil	5mil	7mil			
	5mil	5mil	7mil			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer (GTL)	Copper	1.70mil		
4	Dielectric	FR-4 HTg	3.80mil	4.6	
5	GND (GPI)	Copper	0.70mil		
6	Dielectric	FR-4 HTg	5.00mil	4.6	
7	MidLayer_1 (G1)	Copper	0.70mil		
8	Dielectric	FR-4 HTg	37.50mil	4.6	
9	Mid-Layer_2 (G2)	Copper	0.70mil		
10	Dielectric	FR-4 HTg	5.00mil	4.6	
11	Power (GP2)	Copper	0.70mil		
12	Dielectric	FR-4 HTg	3.80mil	4.6	
13	Bottom Layer (GBL)	Copper	1.70mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

NOTES: &lt; UNLESS OTHERWISE SPECIFIED &gt;

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET  
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)2. BASE MATERIAL - FR4 High Tg  Metal Core  Other   
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL  
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

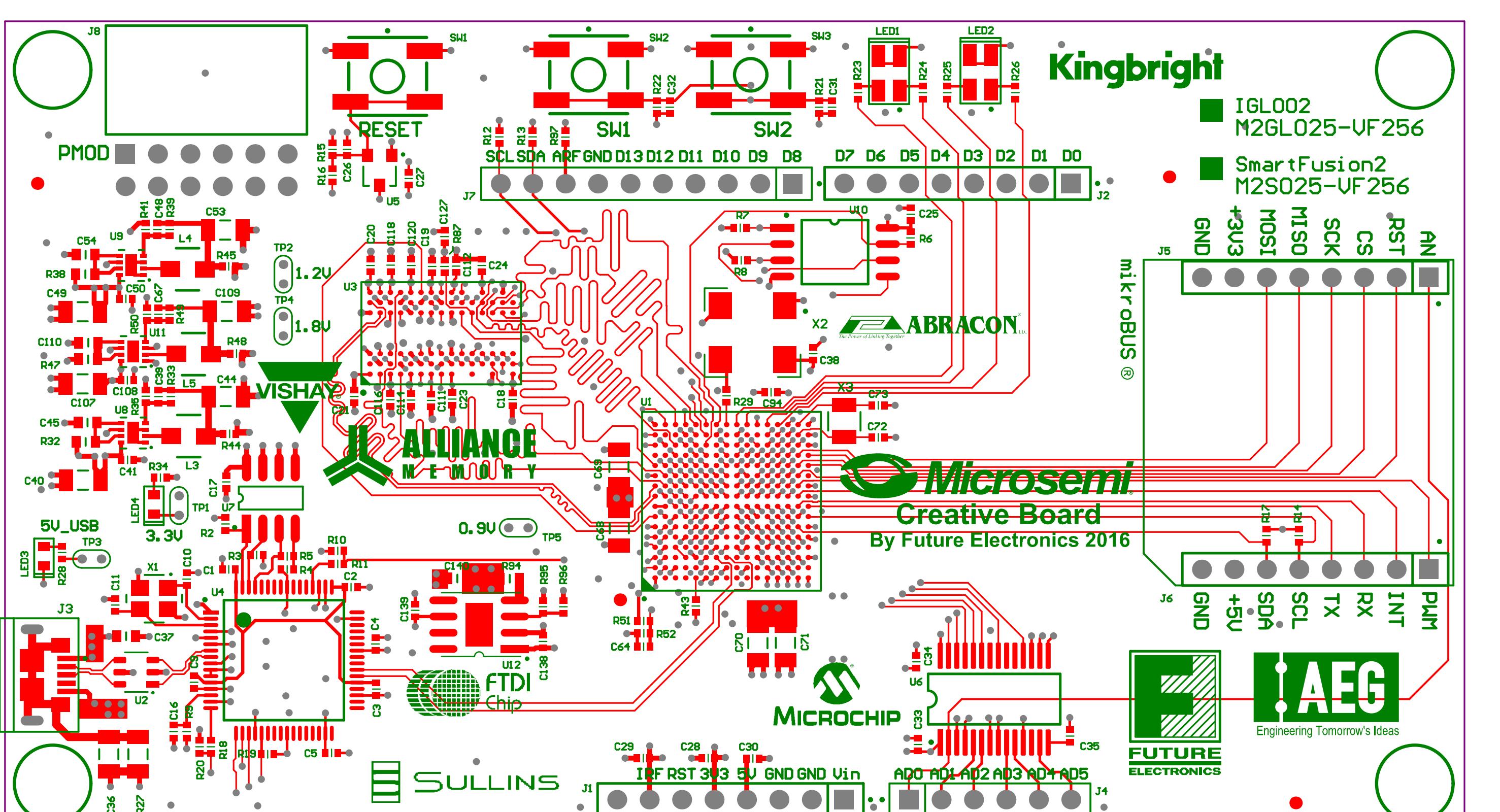
4. PLATING - 0.5oz  0.75oz  1oz  Other 5. FINISH - HASL RoHS  HASL  Immersion Silver  Immersion Tin  ENIG   
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER  
- GREEN  WHITE  BLUE  Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK  
- TOP/BOTTOM  TOP ONLY  BOTTOM ONLY  NONE   
- WHITE  BLACK  Other 8. IMPEDANCE CONTROL - NO  YES  SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

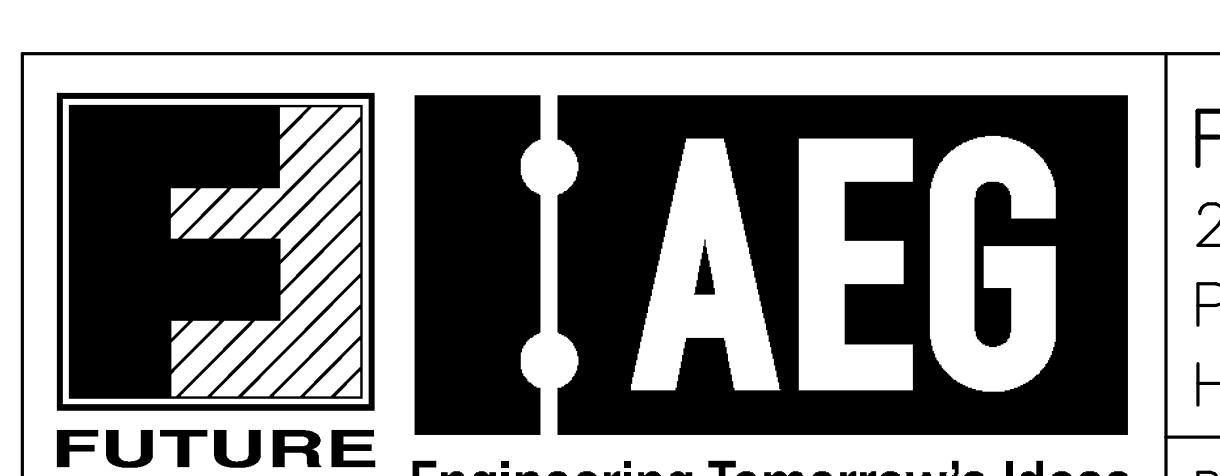
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237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7	
Project # Microsemi Low Cost Board	
Designed by: M. Bernier	Drawn by: M. Bernier
Checked by: H.Letourneau	Approved by: H.Letourneau
Date: 2016-06-22	Sheet 1 of 1

Layers

## Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
	5mil	5mil	6mil			
	5mil	5mil	6mil			
	5mil	5mil	7mil			
	5mil	5mil	7mil			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer (GTL)	Copper	1.70mil		
4	Dielectric	FR-4 HTg	3.80mil	4.6	
5	GND (GPI)	Copper	0.70mil		
6	Dielectric	FR-4 HTg	5.00mil	4.6	
7	MidLayer_1 (G1)	Copper	0.70mil		
8	Dielectric	FR-4 HTg	37.50mil	4.6	
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10	Dielectric	FR-4 HTg	5.00mil	4.6	
11	Power (GP2)	Copper	0.70mil		
12	Dielectric	FR-4 HTg	3.80mil	4.6	
13	Bottom Layer (GBL)	Copper	1.70mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

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3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

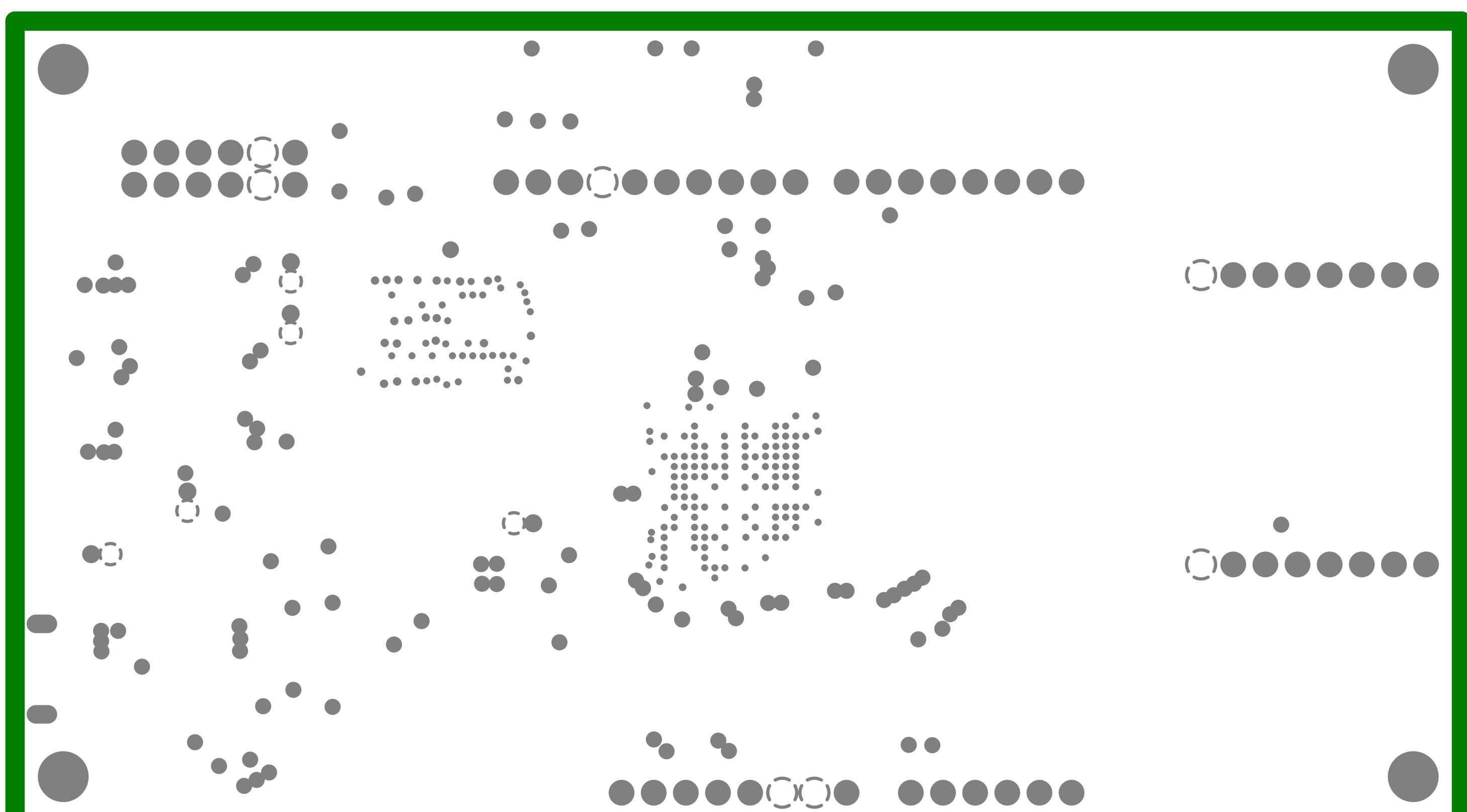
4. PLATING - 0.5oz  0.75oz  1oz  Other 5. FINISH - HASL RoHS  HASL  Immersion Silver  Immersion Tin  ENIG   
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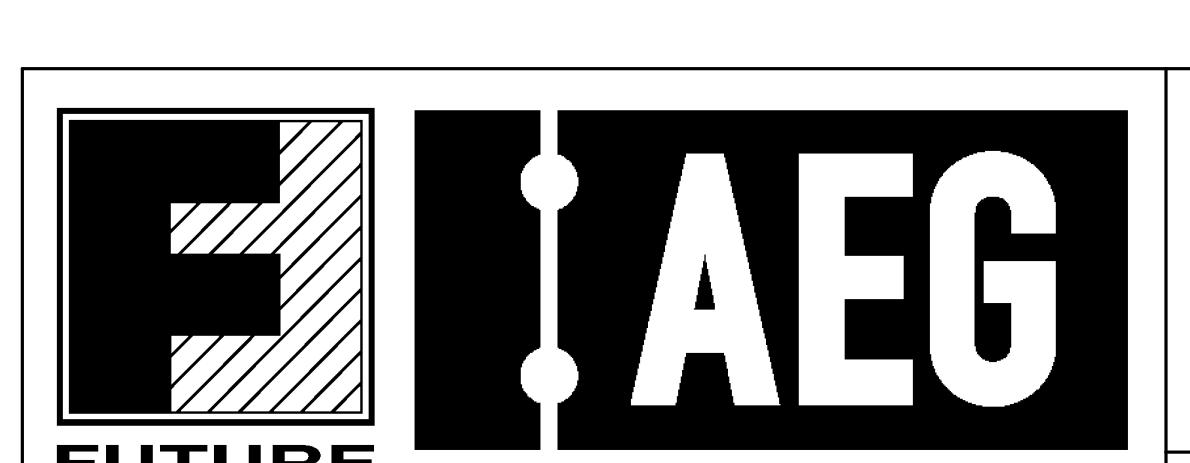
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H9R 5C7

Project #	Microsemi Low Cost Board
Title:	Microsemi Low Cost Board
Size: B	DWG NO: FEN-MCS-IGL-1-PCB-R1
Date:	2016-06-22
Sheet	1 of 1

Layers

MidLayer\_1 (G1)

## Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
	5mil	5mil	6mil			
	5mil	5mil	6mil			
MidLayer_1 (G1)	5mil	5mil	7mil			
	5mil	5mil	7mil			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer (GTL)	Copper	1.70mil		
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8	Dielectric	FR-4 HTg	37.50mil	4.6	
9	Mid-Layer_2 (G2)	Copper	0.70mil		
10	Dielectric	FR-4 HTg	5.00mil	4.6	
11	Power (GP2)	Copper	0.70mil		
12	Dielectric	FR-4 HTg	3.80mil	4.6	
13	Bottom Layer (GBL)	Copper	1.70mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

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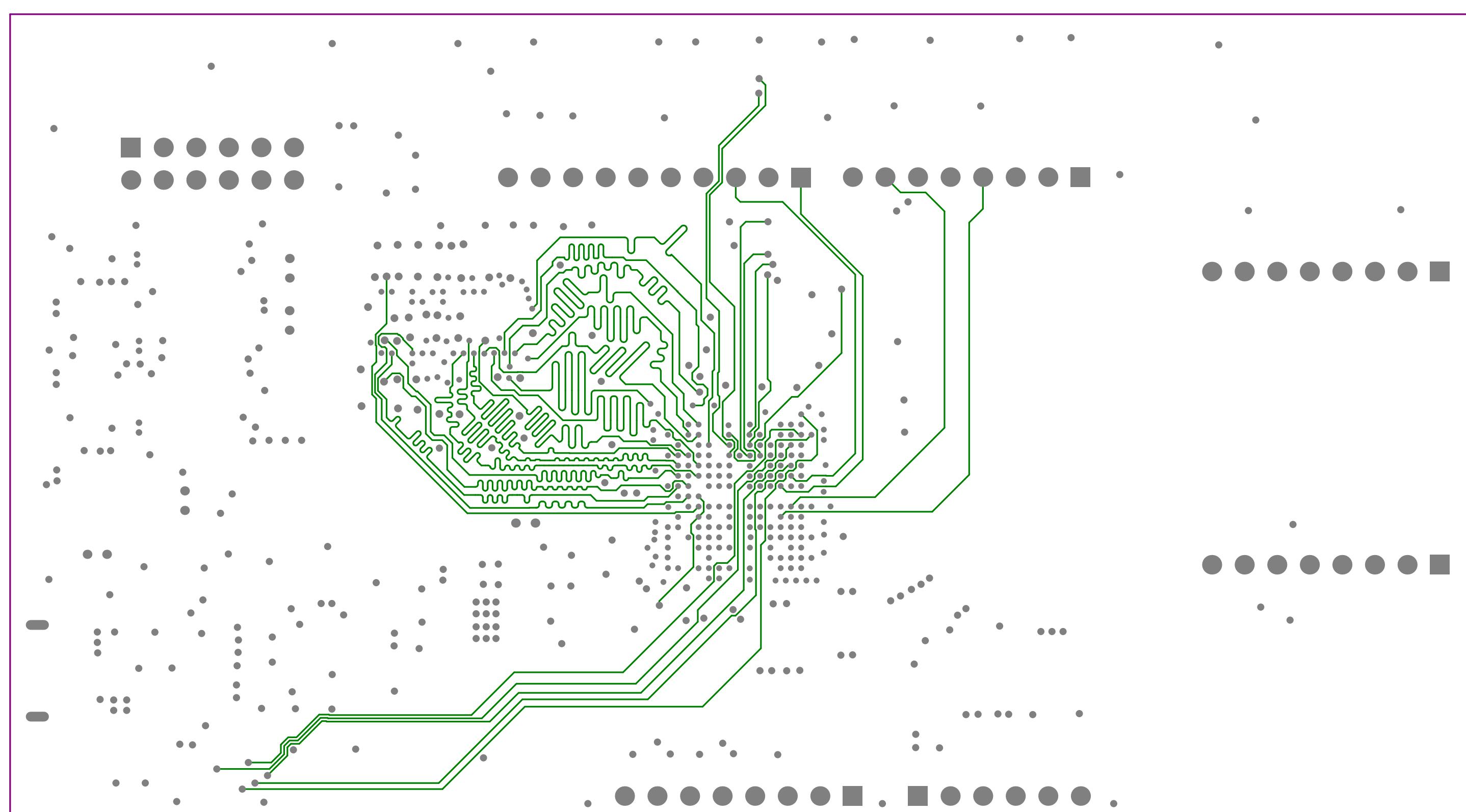
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- TOP/BOTTOM  TOP ONLY  BOTTOM ONLY  NONE   
- WHITE  BLACK  Other 8. IMPEDANCE CONTROL - NO  YES  SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

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Pointe-Claire, Quebec, Canada  
H9R 5C7

Project #	Microsemi Low Cost Board
Title:	Microsemi Low Cost Board
Size:	B
DWG NO:	FEN-MCS-IGL-1-PCB-R1
REV:	1
Date:	2016-06-22
Sheet	1 of 1

Layers

Mid-Layer\_2 (G2)

## Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
1	5mil	5mil	6mil			
2	5mil	5mil	6mil			
3	5mil	5mil	7mil			
Mid-Layer_2 (G2)	5mil	5mil	7mil			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer (GTL)	Copper	1.70mil		
4	Dielectric	FR-4 HTg	3.80mil	4.6	
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11	Power (GP2)	Copper	0.70mil		
12	Dielectric	FR-4 HTg	3.80mil	4.6	
13	Bottom Layer (GBL)	Copper	1.70mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

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H9R 5C7

Project # Microsemi Low Cost Board

Title: Microsemi Low Cost Board

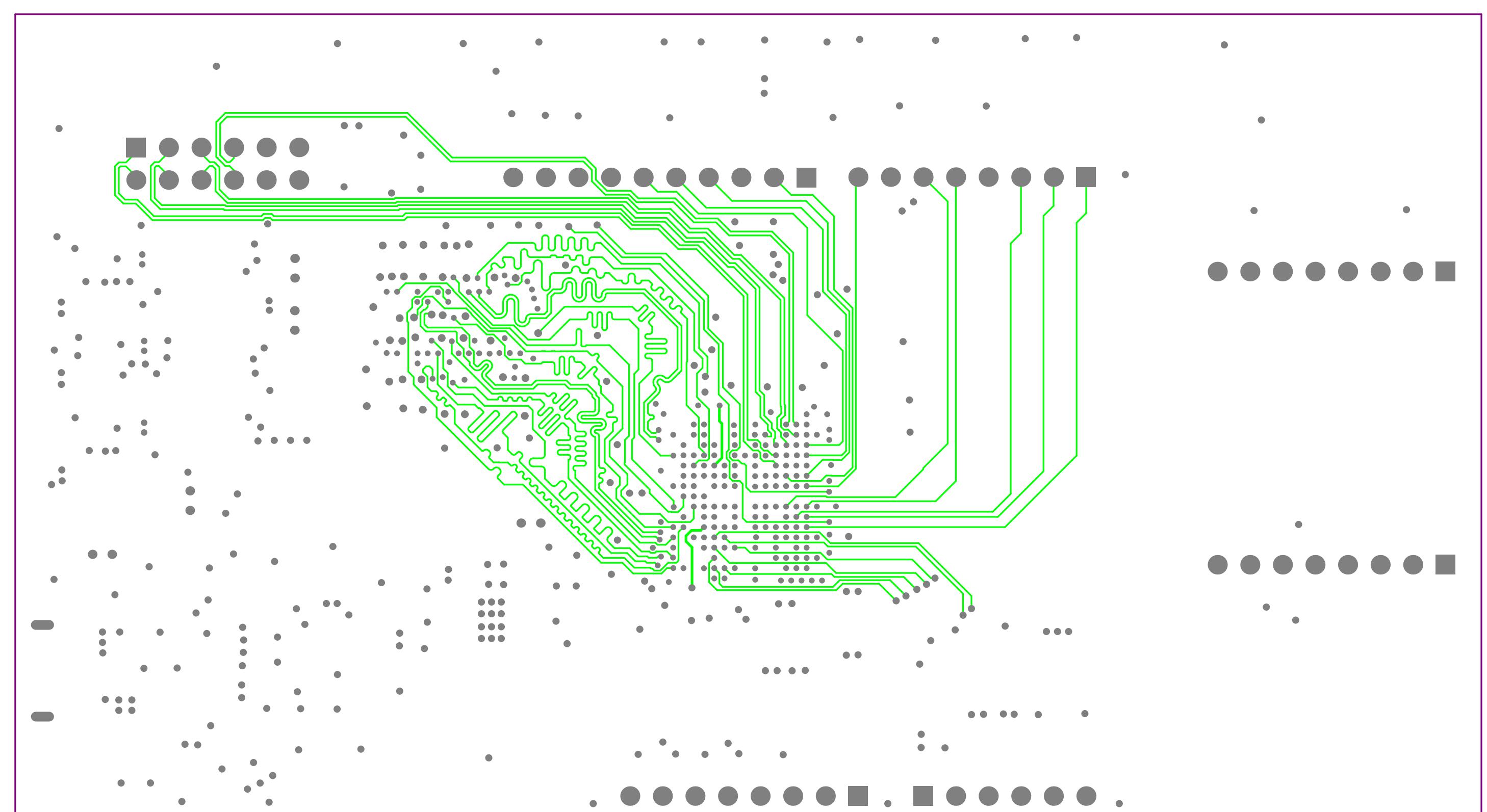
Size: B DWG NO: FEN-MCS-IGL-1-PCB-R1

REV: 1

Date: 2016-06-22

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Layers

## Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
	5mil	5mil	6mil			
	5mil	5mil	6mil			
	5mil	5mil	7mil			
	5mil	5mil	7mil			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer (GTL)	Copper	1.70mil		
4	Dielectric	FR-4 HTg	3.80mil	4.6	
5	GND (GPI)	Copper	0.70mil		
6	Dielectric	FR-4 HTg	5.00mil	4.6	
7	MidLayer_1 (G1)	Copper	0.70mil		
8	Dielectric	FR-4 HTg	37.50mil	4.6	
9	Mid-Layer_2 (G2)	Copper	0.70mil		
10	Dielectric	FR-4 HTg	5.00mil	4.6	
11	Power (GP2)	Copper	0.70mil		
12	Dielectric	FR-4 HTg	3.80mil	4.6	
13	Bottom Layer (GBL)	Copper	1.70mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

NOTES: &lt; UNLESS OTHERWISE SPECIFIED &gt;

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET  
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg  Metal Core  Other   
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL  
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR STACK-UP DETAIL

4. PLATING - 0.5oz  0.75oz  1oz  Other

5. FINISH - HASL RoHS  HASL  Immersion Silver  Immersion Tin  ENIG   
Other

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER  
- GREEN  WHITE  BLUE  Other

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK  
- TOP/BOTTOM  TOP ONLY  BOTTOM ONLY  NONE   
- WHITE  BLACK  Other

8. IMPEDANCE CONTROL - NO  YES  SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

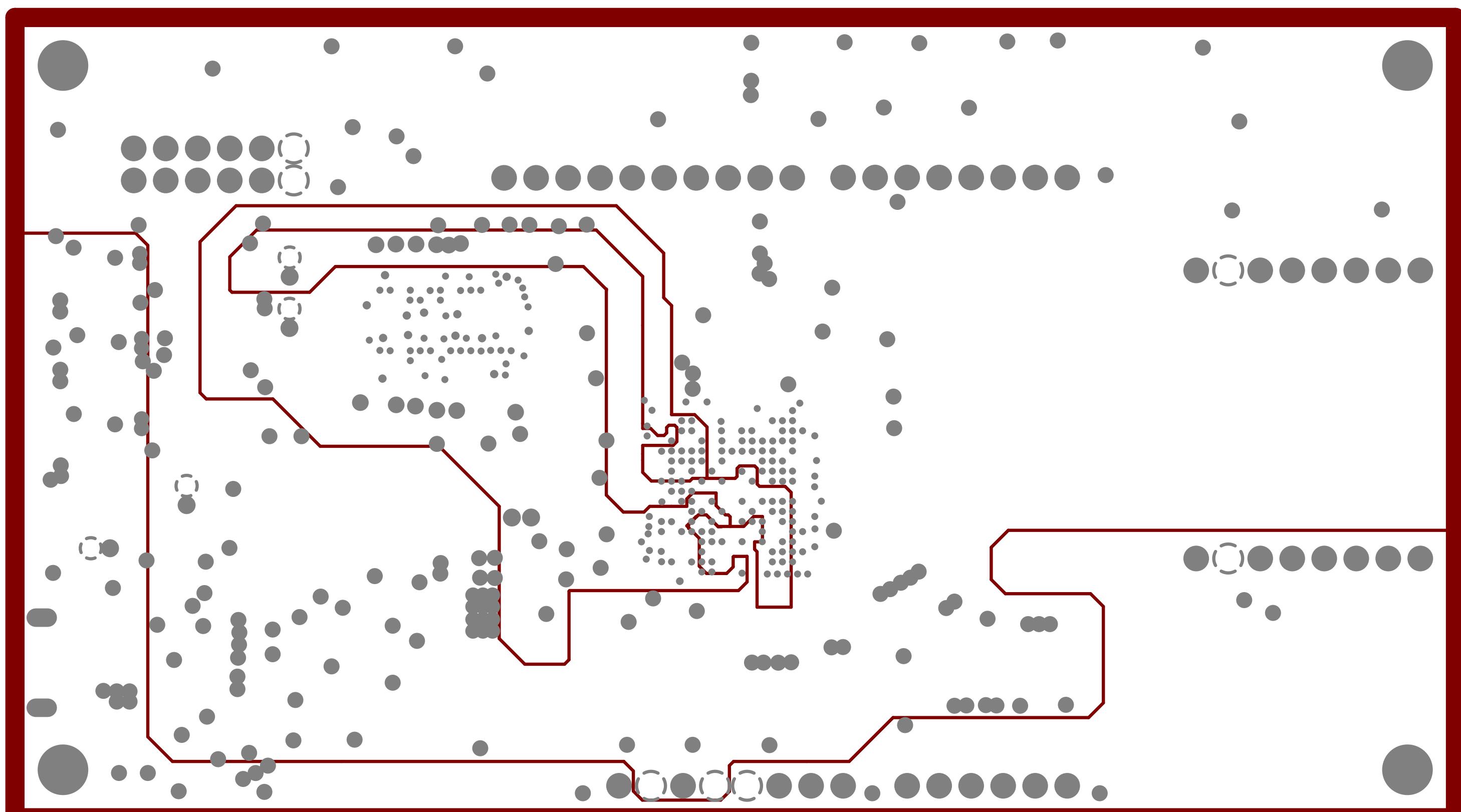
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP  
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

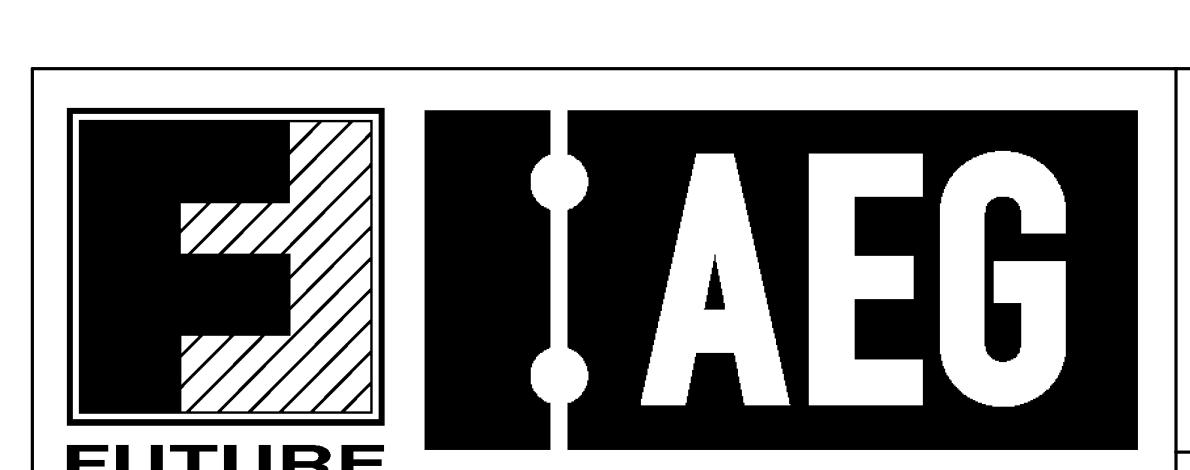
12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED  
IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD  
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Future Electronics – System Design Center NA  
237 Hymus Blvd  
Pointe-Claire, Quebec, Canada  
H9R 5C7

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Layers

Bottom Layer (GBL)

## Impedance Requirements

Layer	Impedance 50 Ohms		Impedance 90 Ohms (Diff)		Impedance 100 Ohms (Diff)	
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)	
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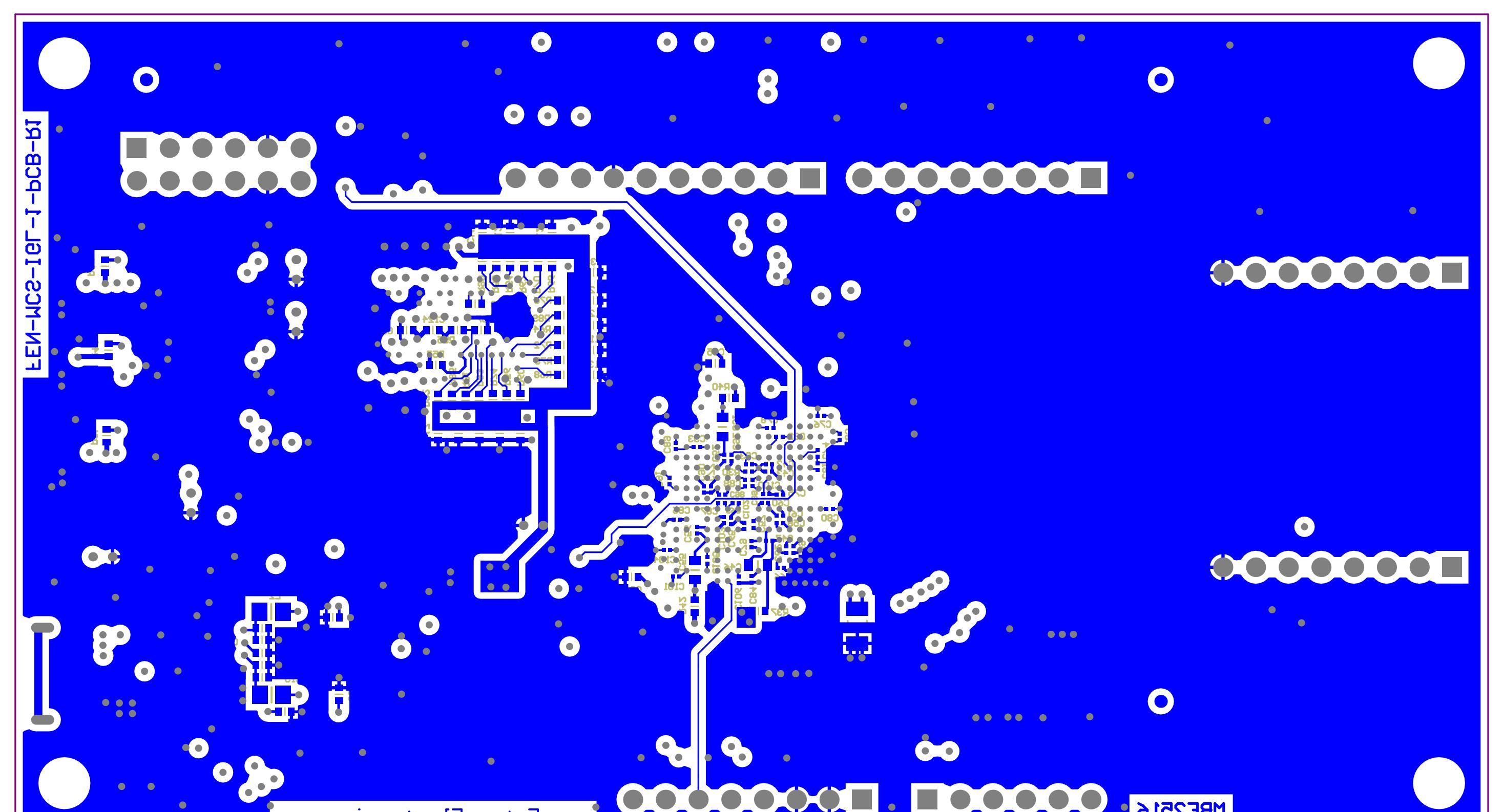
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Layers Top Layer (GTL) Bottom Layer (GBL)

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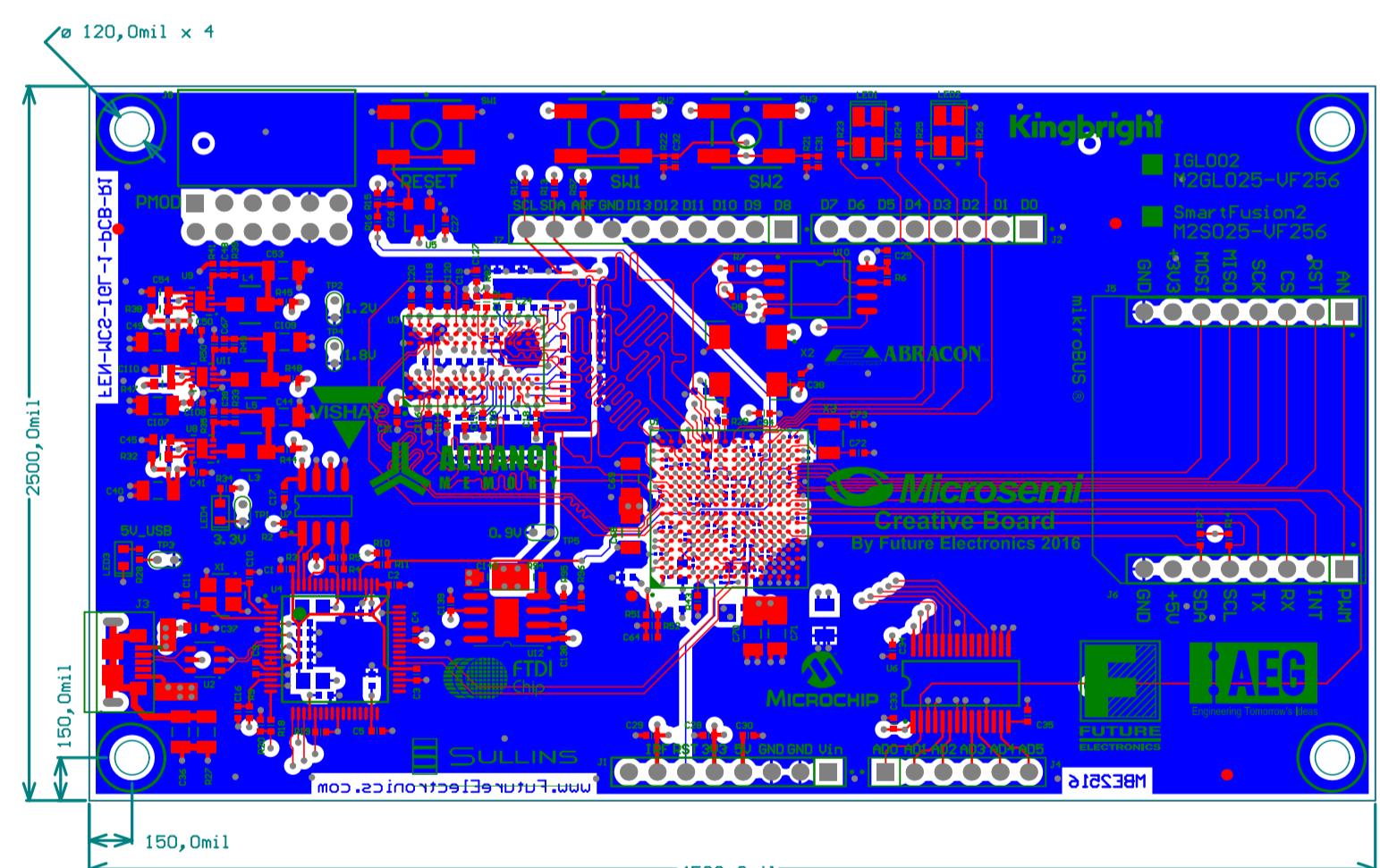
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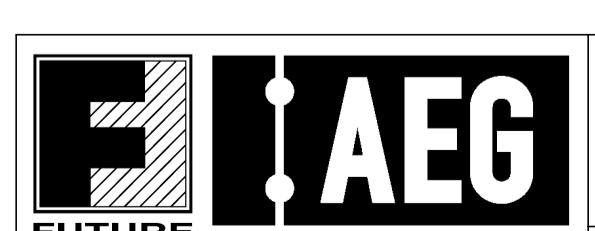
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Project # Microsemi Low Cost Board	
Designed by: M. Bernier	Drawn by: M. Bernier
Checked by: H.Letourneau	Approved by: H.Letourneau
Date: 2016-06-22	Sheet 1 of 1