14 Analog-to-digital converter (ADC)

This section applies to low-density STM8L05xx/STM8L15xx devices, medium-density STM8L05xx/STM8L15xx devices, medium+ density STM8L05xx/STM8L15xx devices and high-density STM8L05xx/STM8L15xx/STM8L16xx devices, unless otherwise specified.

14.1 ADC introduction

The analog-to-digital converter is used to convert the analog voltage signals to digital values. Up to 28 analog channels are available. A/D conversion can be performed in single or continuous mode.

14.2 ADC main features

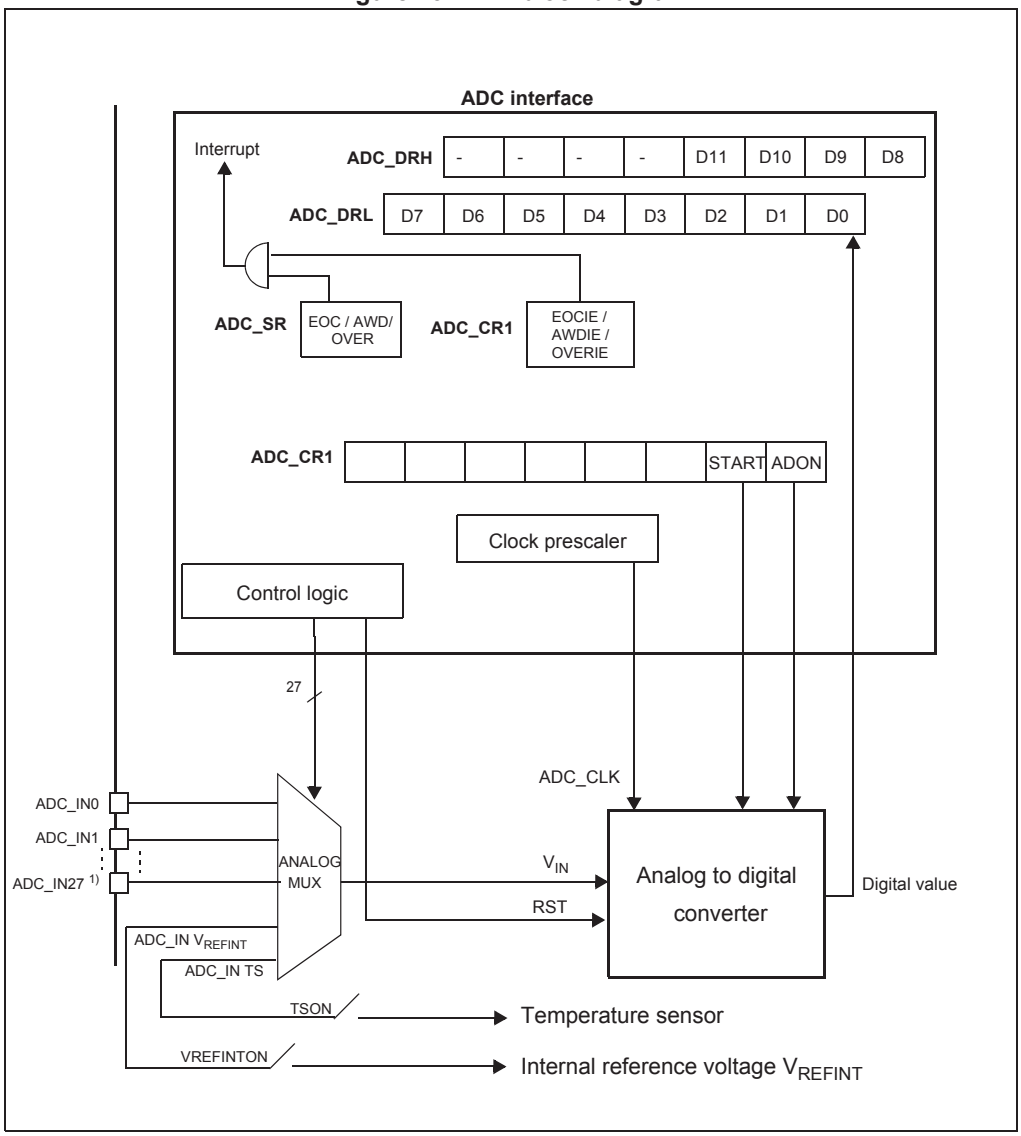
- Configurable resolution (up to 12-bit data width)
- Number of analog channels:
  - Medium-density devices:
    25 analog channels : 1 fast channel (1 µs) + 24 slow channels
  - Low, medium+ and high-density devices:
    28 analog channels : 4 fast channels (1 µs) + 24 slow channels
- 2 internal channels connected to temperature sensor and internal reference voltage
- Configurable single or continuous conversion
- Prescalable ADC clock
- Analog watchdog
- Separate interrupt generation at end of conversion, watchdog or overrun event
- Multiple channel conversion (scan mode)
- Data integrity mechanism
- DMA capability
- Programmable sampling time
- Schmitt trigger disabling capability
- Conversion time which can be up to 1 µs when SYSCLK = 16 MHz
- Voltage range: 1.8 V to 3.6 V
  - Maximum conversion rate obtained from 2.4 V to 3.6 V
  - ADC at a lower speed between 1.8 V and 2.4 V
  - ADC functionality not guaranteed below 1.8 V

14.3 ADC functional description

14.3.1 General description

Figure 43 shows the block diagram of the complete system ADC interface.

Figure 43. ADC block diagram



1. ADC_IN27 for medium+ and high-density devices.
   ADC_IN24 for medium-density devices.
2. Only basic features are shown in this diagram

14.3.2 Number of analog channels

Up to 30 analog input channels are available in the STM8L05xx/STM8L15xx devices:

- Up to 27 analog input channels in the medium-density devices.
- Up to 28 analog input channels in the low-density devices.
- Up to 30 analog input channels in the medium+ and high-density devices.

They can be classified into three groups:

- Slow channels: channels 0 to 23 with a sampling time selected through the SMP1 bits in the ADC_CR2 register
- Fast channels: channel 24 (medium-density devices) or channels 24 to 27 (medium+ and high-density devices) with a sampling time selected through the SMP2 bits in the ADC_CR3 register
- Fast internal channels: channels V_{REFINT} and TS with a sampling time selected through the SMP2 bits in the ADC_CR3 register.

14.3.3 ADC on-off control

The ADC can be powered-on by setting the ADON bit in the ADC_CR1 register. When the ADON bit is set, it wakes up the ADC from Power-down mode. Conversion should be started only when the ADC power-up time (t_{WKUP}) has elapsed and before the ADC maximum idle delay (t_{IDLE}) has elapsed. The software can stop conversion and put the ADC in Power-down mode by resetting the ADON bit.

14.3.4 Single conversion mode

In this mode, only one input channel must be selected in the ADC_SQRx registers (if more channels are selected, the highest selected channel is measured). In addition, the DMAOFF bit must be set in the ADC_SQR1 register (to disable DMA transfer). The input channel is then converted and the ADC conversion stops (one simple conversion). The converted value is stored into the ADC_DR data register. An interrupt (EOC) can be generated after the end of conversion. The time between 2 conversions must be lower than the ADC maximum idle delay (t_{IDLE}). In case the time between 2 conversions is greater than t_{IDLE}, the ADC must be powered-off between the 2 conversions (by clearing the ADON bit).

Another possiblity is to discard the first conversion (occuring in a time greater than tidle after previous one) and keep the next one

Note: If the DMAOFF bit in the ADC_SQR1 register is reset (and if DMA is properly programmed) the conversion is then performed in single scan mode.

In the single conversion mode, the ADC does one conversion. The conversion can be started in two different ways:

- by software: conversion is performed by setting the START bit in the ADC_CR1 register. The START bit is then reset by hardware.

Note: The channel selection is performed using the ADC_SQRx registers.
Before starting a conversion, the software should wait for the stabilization time (t_{WKUP}).

- by hardware: three external triggers can start a conversion (ADC_TRIGR1, ADC_TRIGR2 or ADC_TRIGR3). The selection of one of these three triggers is made through the EXTSEL[1:0] bits in the ADC_CR2 register. The conversion can be triggered either on the rising edge, on the falling edge or on both edges of the signal, depending on the TRIG_EDGE[1:0] bits in the ADC_CR2 register.

Note: Any start event occurring during the conversion will be ignored.

Once the conversion is complete:

- the EOC flag is set
- and an interrupt is produced if the EOCIE bit is set in the ADC_CR1 register.

The EOC flag can be reset by software or by reading the LSB of the converted data.

Further single conversions can be initiated by simply setting the START bit or by rising an external trigger.

Note: 1 The channel must not be changed during a conversion.

2 The user must avoid generating triggers before the end of an ongoing conversion.

3 The trigger edge configuration must be set before enabling the triggers

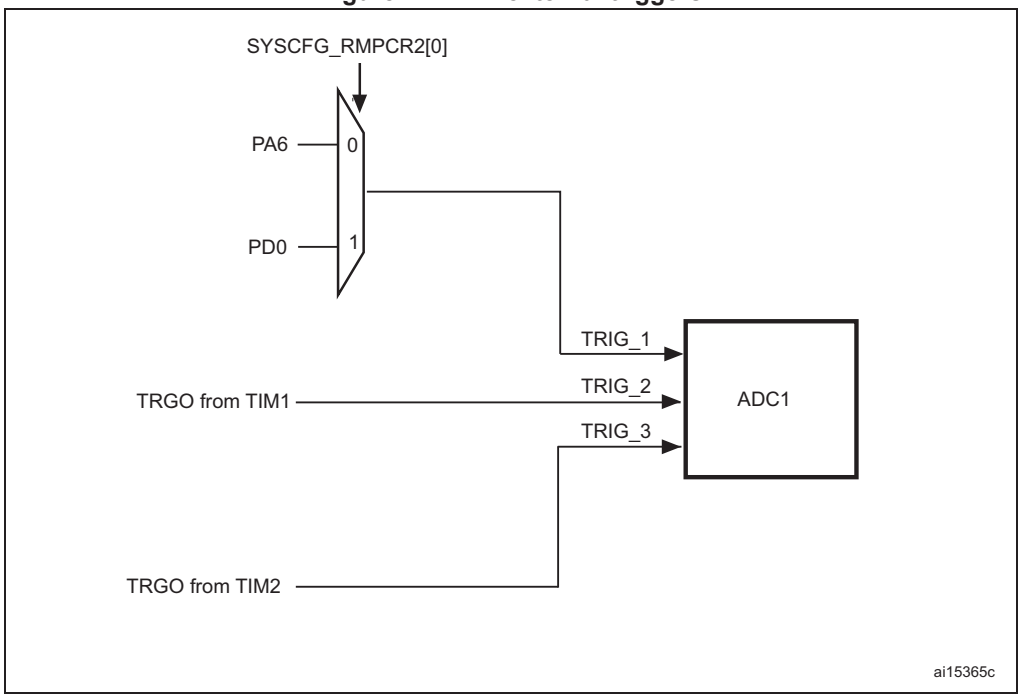
4 Even if no channel is programmed, a conversion can be started and the EOC flag will be set.

ADC external triggers

Three external trigger sources can be selected:

- ADC trigger 1.
  The trigger can be performed
  - either from PA6 *(if the ADC_TRIG bit in the SYSCFG_RMPCR2 register is reset; refer to Alternate function remapping section in the datasheet)*
  - or directly from PD0 *(if ADC_TRIG bit in the SYSCFG_RMPCR2 register is set; refer to Alternate function remapping section in the datasheet)*
- ADC trigger 2.
  The trigger is performed directly from Timer 1 trigger output (TIM1_TRGO)
- ADC trigger 3.
  The trigger is performed directly from Timer 2 trigger output (TIM2_TRGO)

Figure 44. ADC external triggers



14.3.5 Continuous conversion mode

In this mode , the ADC does not stop after conversion but continues to the next channel in the selected channel sequence. Conversions continue until the CONT bit and the ADON bits are set and the converted values are transferred through the DMA to the RAM or EEPROM memory buffer.

As the EOC interrupt is generated only after the end of the conversion of the selected channel sequence, the result of each channel conversion cannot be read from the ADC_DR register.

To save the conversion of each channel in a memory (RAM or EEPROM), the DMA must be used in peripheral to memory mode. If the CONT bit is reset during a conversion, the current selected channel sequence conversions end with the last selected channel) and then the ADC stops.

Note: The CONT bit must not be set again during a conversion.

14.3.6 ADC clock

The ADC clock provided by the clock controller can be either the ADC system clock (CK) or the ADC system clock divided by 2. The selection of the frequency feeding the clock (f_{ADC_CLK}= CK or f_{ADC_CLK}= CK/2) is done through the PRESC bit in the ADC_CR2 register.

14.3.7 Analog watchdog

The analog watchdog status bit (AWD) in the ADC_SR register is set when the analog voltage converted by the ADC is above or below a reference voltage threshold defined by

the higher/lower thresholds programmed into the ADC_HTRH/L and ADC_LTRH/L registers.

In scan mode, the channel where the analog watchdog is enabled is the one selected through the CHSEL[4:0] bits in the ADC_CR3 register.

Note: The threshold values must be set/changed before starting the conversion.
In scan mode a watchdog flag rise occurring during a conversion does not stop the next conversions of the sequence. This avoids having to start the ADC again every time an analog watchdog is enabled.
The action related to the analog watchdog is not necessarily linked to the other tasks using the other ADC channels.

14.3.8 Interrupts

An interrupt can be generated when an EOC event occurs (end of conversion in single mode or end of last scan conversion in scan mode) when the analog watchdog status bit (AWD) is set in the ADC_SR register or, in scan mode, when a DMA request is not serviced and a new conversion is completed.

Individual interrupt lines are available as well as a common interrupt line. The following table summarizes the possible flag/interrupt configuration.

Table 44. Flag/interrupt configuration

Flag	Description	Interrupt generation
OVER	Rises when a new converted data is ready and the previous one is not yet read by the DMA (scan mode)	yes
AWD	Rises when the converted data is outside the reference voltage threshold	yes
EOC	Rises when an end of conversion occurs (single mode) Rises when the end of conversion of last channel of the sequence occurs (scan mode)	yes

14.3.9 Channel selection (Scan mode)

This mode works automatically in continuous mode. It can also be used in single mode by resetting the DMAOFF bit in the ADC_SQR1 register.

In scan mode, the selected channel sequence is taken into account (like in single mode) and the selected channels are converted and transferred through DMA to memory (DMA should be properly programmed).

If the single mode is selected, the ADC converts the selected channel sequence and it is stopped after the last channel conversion. For the next selected channel sequence, a scan conversion is necessary to restart the ADC. An interrupt (EOC) can be generated after the end of the channel sequence conversion.

Three registers are available to select the channel or the sequence of channels used for conversion in Scan mode: ADC_SQR1, ADC_SQR2 and ADC_SQR3.

Note: This feature must be used in conjunction with the DMA controller.

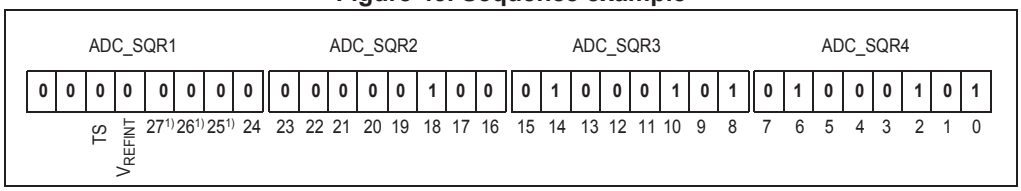
The channel selection must be performed after enabling the ADC peripheral (by setting the ADON bit in the ADC_CR1 register).

A single conversion is initiated on each channel of a sequence. After the end of conversion, the next channel of the sequence is automatically converted.

The channel selection is performed using the ADC_SQRx registers. A logic 1 in the position 'n' of these registers means that channel 'n' is in the list of channels to be converted.

For example, *Figure 45* below shows how to select the sequence: 0; 2; 6; 8; 10; 14; 18.

Figure 45. Sequence example



1. Available on medium+ and high-density devices only.

If the CONT bit in the ADC_CR1 register is set (continuous mode selected), the conversion does not stop at channel 'n' but restarts from the first channel of the sequence. After each conversion, a DMA ADC request is sent and the DMA controller is used to transfer the converted data to the RAM.

Note: The ADC_SQRx registers must not be changed during a conversion.

14.3.10 Data integrity

An 8-bit shadow register is used to store the LSB data when the MSB is read. The LSB data is read from the shadow register.

This guarantees the data consistency if a new data from the ADC is coming between the MSB and LSB data read. Consequently, the software must read the MSB before reading the LSB to be sure that both LSB and MSB are related to the same data.

Note: An MSB read operation must always be followed by an LSB read operation.

14.3.11 DMA transfer

When a scan conversion is performed, a DMA ADC request is sent as soon as an end of conversion is detected, to signal that a data is ready to be transferred.

If a new conversion is complete and the DMA has not completed the transfer of previous conversion data, the overrun flag is risen and an interrupt is generated (if enabled).

The DMA transfer can be disabled by setting the DMAOFF bit in the ADC_SQR1 register.

Caution: In scan mode, DMA transfer shall be disabled only when the ADC scan sequence is finalized.

14.3.12 Configurable resolution

It is possible to reduce the conversion time by reducing the ADC resolution.

The RES[1:0] bits in the ADC_CR1 register are used to configure the resolution to 6, 8, 10 or 12 bits. The converted data is received from the ADC through its serial output.

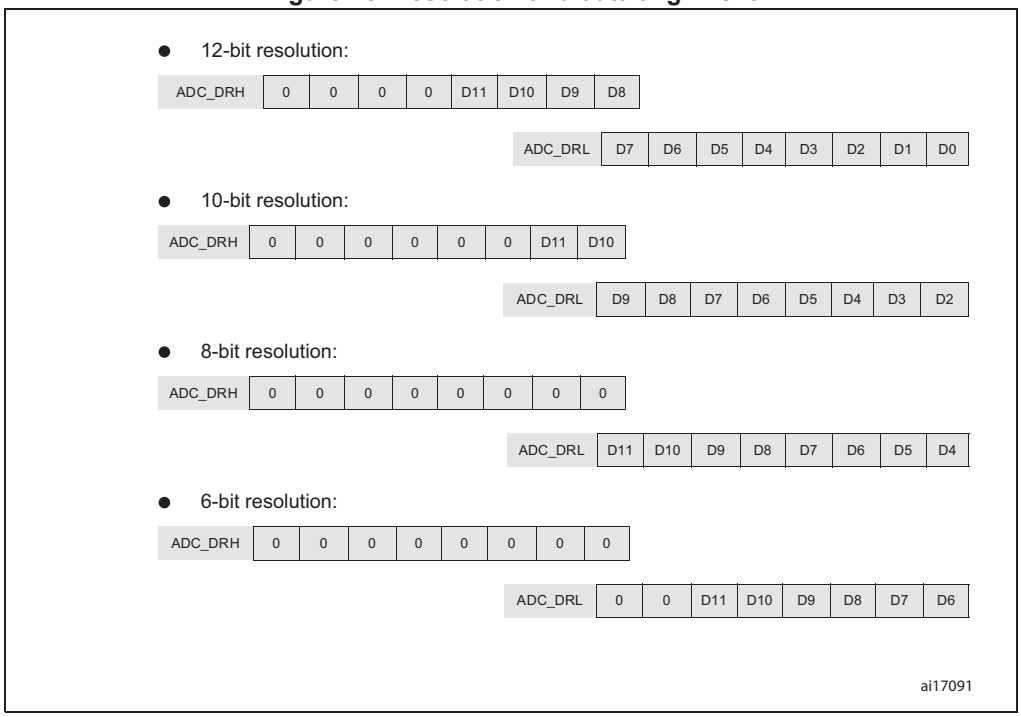
When the desired number of bits is achieved, a new conversion can start immediately.

Note: The resolution bits can be changed only when no ADC conversion is ongoing.

14.3.13 Data alignment

The converted data stored after conversion are right aligned and their configuration depends on the selected resolution, as shown in the following figure:

Figure 46. Resolution and data alignment



14.3.14 Programmable sampling time

The ADC input voltage is sampled during a number of cycles which is selected using:

- the SMP1[2:0] bits in the ADC_CR2 register for the first 24 channels
- and the SMP2[2:0] bits in the ADC_CR3 register for channels 24 to 27 (or channel 24 in medium-density devices), V_{REFINT} and TS.

The following table shows the allowed values of sampling cycles.

Table 45. Authorized sampling cycles

Bit configuration		Sampling cycles
SMP1[2:0] for channels 0 to 23 & SMP2[2:0] for channels 24 to 27 (or for channel 24 in medium-density devices) V_{REFINT} and TS	000	4
	001	9
	010	16
	011	24
	100	48
	101	96
	110	192
	111	384

Note: A different sampling time can be selected for slow channels and for fast channels.

The sampling time must not be changed during a conversion.

14.3.15 Schmitt trigger disabling

The Schmitt trigger can be disabled to reduce the consumption on some pins used as analog inputs.

As there are 2 internal channels, only 25 Schmitt triggers can be disabled on medium-density devices and 28 Schmitt triggers on medium+ and high-density devices.

Note: In order to disable the Schmitt trigger on the ADC channels which are shared with the comparators inputs, it is also required to disable the Schmitt trigger through the COMP_CSR4 and/or COMP_CSR5 registers.

If the control of the I/O using the Routing interface is enabled (with the corresponding bit set in the RI_IOCMRn register), the setting of the STE bit in the COMP_CSR1 register takes priority over the setting of the ADC_TRIGRn registers.

14.3.16 Temperature sensor

The temperature sensor is not available on STM8L05xx value line devices.

The temperature sensor can be used to measure the internal temperature of the device. It is internally connected to the ADC TS (temperature sensor) input channel that is used to convert the sensor output voltage into a digital value.

Note: When it is not used, this sensor can be put in power-down mode.

The TSON bit in the ADC_TRIGR1 register must be set to enable the internal ADC TS channel connection. This connection must be enabled only if the temperature sensor conversion is required.

The internal temperature sensor can also be used to detect temperature variations. The output voltage of the temperature sensor is factory measured at high temperature and the result of the ADC conversion is stored in a specific data address: the TS_Factory_CONV_V90 byte represents the LSB of the V90 12-bit ADC conversion result while the MSB have a fixed value: 0x3.

To reduce the temperature sensor error, the user can measure it at ambient temperature (25°C) to redefine more accurately the average slope (avg_slope) and the offset.

How to read the temperature

To read the temperature from the sensor, use the following procedure:

1. Select the ADC1 TS (temperature sensor) input channel.
2. Select a sample time of 10 µs.
3. Set the TSON bit in the ADC_TRIGR1 register to wake up the temperature sensor from power-down mode.
4. Start the ADC conversion.
5. Read the resulting V_{SENSE} data in the ADC data register (ADC_DRx).
6. Calculate the temperature using the following formulae:

$$T[°K] = \frac{V_{SENSE}}{AvgSlope}$$

$$T[°C] = \frac{V_{SENSE}}{AvgSlope} - 273.15$$

Where

Avg_Slope = estimation of the average slope of the “Temperature vs. V_{SENSE}” curve (given in V/°K).

Refer to the Electrical characteristics section for the Avg_Slope value.

Note: When the sensor wakes up from power-down mode, a stabilization time is required before a correct voltage can be output.

After power-on, the ADC also needs a stabilization time. To minimize this delay, the ADON and TSON bits should be set at the same time.

14.3.17 Internal reference voltage conversion

The internal reference voltage is internally connected to the V_{REFINT} channel. This analog input channel is used to convert the internal reference voltage into a digital value.

The VREFINTON bit in the ADC_TRIGR1 register must be set to enable the internal reference voltage. This reference voltage must be enabled only if its conversion is required.

The internal reference voltage is factory measured and the result of the ADC conversion is stored in a specific data address: the VREFINT_Factory_CONV byte represents the LSB of the VREFINT 12-bit ADC conversion result while the MSB have a fixed value: 0x6.

14.4 ADC low power modes

Table 46. Behavior in low power modes

Mode	Description
Wait/ Low power wait	ADC interface is active. Interrupt events cause the device to exit from Wait or Low power wait mode.
Halt/ Active-halt	ADC interface is not active.

14.5 ADC interrupts

Table 47. Interrupt requests

Interrupt event	Event flag	Enable control bit	Exit from Wait / Low power wait	Exit from Halt / Active-halt
End of conversion flag	EOC	EOCIE	Yes	No
Analog watchdog flag	AWD	AWDIE	Yes	No
Overrun flag	OVER	OVERIE	Yes	No

14.6 ADC registers

14.6.1 ADC configuration register 1 (ADC_CR1)

Address offset: 0x00

Reset value: 0x00

7	6	5	4	3	2	1	0
OVERIE	RES[1:0]		AWDIE	EOCIE	CONT	START	ADON
rw	rw		rw	rw	rw	rw	rw

Bit 7 **OVERIE**: Overrun interrupt enable
This bit is set and cleared by software. If set it enables the interrupt generated by an overrun event.
0: Overrun interrupt disabled
1: Overrun interrupt enabled

Bits 6:5 **RES[1:0]**: Configurable resolution
These bits are set and cleared by software. These bits are used to configure the ADC resolution.
00: 12-bit resolution
01: 10-bit resolution
10: 8-bit resolution
11: 6-bit resolution

Bit 4 **AWDIE**: Analog watchdog interrupt enable
This bit is set and cleared by software. If set it enables the interrupt generated by the analog watchdog.
0: Analog watchdog interrupts disabled
1: Analog watchdog interrupts enabled

Bit 3 **EOCIE**: Interrupt enable for EOC
This bit is set and cleared by software. It enables the interrupt at the end of conversion.
0: EOC interrupt disabled
1: EOC interrupt enabled

Bit 2 **CONT**: Continuous conversion

This bit is set and cleared by software. If set, conversion takes place continuously till this bit is reset.

0: Single conversion mode

1: Continuous conversion mode

Bit1 **START**: Conversion start

This bit is set by software and cleared by hardware.

If set, it starts a conversion (if enabled). It is automatically reset by hardware after one ADC clock cycle.

Note: If this bit is set during a conversion, it will not be considered.

Bit 0 **ADON**: A/D converter ON / OFF

This bit is set and reset by software. It wakes up the ADC from Power down mode.

0: ADC disabled (Power-down mode)

1: ADC enabled (wakeup from Power-down mode)

14.6.2 ADC configuration register 2 (ADC_CR2)

Address offset: 0x01

Reset value: 0x00

7	6	5	4	3	2	1	0
PRESC	TRIG_EDGE1	TRIG_EDGE0	EXTSEL1	EXTSEL0	SMTP1[2:0]		
rw	rw	rw	rw	r	rw	rw	rw

Bit 7 **PRESC**: Clock prescaler

This bit is set and cleared by software. If set, it divides the ADC clock frequency by 2.

0: $f_{(ADC\_CLK)}$ = CK
1: $f_{(ADC\_CLK)}$ = CK/2

Bits 6:5 **TRIG_EDGE[1:0]**: Active edge for external triggers

These bits are set and cleared by software. They select the active edges for external triggers.

00: Reserved
01: Rising edge sensitive
10: Falling edge sensitive
11: Both rising and falling edge sensitive

Bits 4:3 **EXTSEL[1:0]**: External event selection

These two bits select the software start or one of 3 external events that can trigger a conversion.

00: Triggers disabled, software start enabled.
01: Trigger 1 enabled
10: Trigger 2 enabled
11: Trigger 3 enabled

Bits 2:0 **SMTP1[2:0]**: Sampling time selection

These bits are set/reset by software. They are used to select one of the following sampling times for the first 24 channels.

000: 4 ADC clock cycles
001: 9 ADC clock cycles
010: 16 ADC clock cycles
011: 24 ADC clock cycles
100: 48 ADC clock cycles
101: 96 ADC clock cycles
110: 192 ADC clock cycles
111: 384 ADC clock cycles

14.6.3 ADC configuration register 3 (ADC_CR3)

Address offset: 0x02

Reset value: 0x1F

7	6	5	4	3	2	1	0
SMTP2[2:0]			CHSEL[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw

Bit 7:5 **SMTP2[2:0]**: Sampling time selection

These bits are set/reset by software. They are used to select one of the following sampling times for channels 24, V_{REFINT} and TS.

000: 4 ADC clock cycles
001: 9 ADC clock cycles
010: 16 ADC clock cycles
011: 24 ADC clock cycles
100: 48 ADC clock cycles
101: 96 ADC clock cycles
110: 192 ADC clock cycles
111: 384 ADC clock cycles

Bit 4:0 **CHSEL[4:0]**: Channel selection

These bits are set and cleared by software. They are used to select the channel to be checked by the analog watchdog.

00000: ADC channel 0 is selected
00001: ADC channel 1 is selected
...
10111: ADC channel 23 is selected
11000: ADC channel 24 is selected
11001: ADC channel 25 is selected (1)
11010: ADC channel 26 is selected (1)
11011: ADC channel 27 is selected (1)
11100: ADC channel V_{REFINT} is selected
11101: ADC channel TS is selected(2)

1. This configuration is “reserved” in medium-density devices.
2. This configuration is “reserved” in STM8L05xx value line devices.

14.6.4 ADC status register (ADC_SR)

Address offset: 0x03

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved					OVER	AWD	EOC
					rw_0	rw_0	rw_0

Bits 7:3 Reserved, forced by hardware to 0.

Bit 2 **OVER**: Overrun flag

This bit is reset by software writing 0 to it or by hardware when the ADC is put in power-down mode. It is set by hardware when, after a conversion, a second conversion has completed and the DMA has not read the first conversion value.

It cannot be set by software.

0: No overrun occurred

1: Overrun occurred

Bit 1 **AWD**: Analog watchdog flag

This bit is reset by software writing 0 to it or by hardware when the ADC is in power-down mode. It is set when the analog voltage converted by the ADC is above or below the reference voltage thresholds defined by the lower/higher thresholds in the ADC_xTRx registers.

It cannot be set by software.

0: No analog watchdog event occurred

1: Analog watchdog event occurred

Bit 0 **EOC**: End of conversion

This bit is set by hardware at the end of conversion. It is cleared by software by writing ‘0’ to it or by reading the LSB of the converted data or when the ADC is put in power-down mode.

In case of scan conversion, this bit is set at the end of conversion of the last channel of the sequence.

It cannot be set by software.

0: Conversion not complete

1: Conversion complete

14.6.5 ADC data register high (ADC_DRH)

Address offset: 0x04

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved				CONV_DATA[11:8]			
				r	r	r	r

Bits 7:4 Reserved, forced by hardware to 0.

Bits 3:0 **CONV_DATA[11:8]**: Data bits high

These bits are set/reset by hardware and are read only. They contain the 4 MS bits of the converted data. The converted voltage data bits are right aligned and their configuration depends on the programmed resolution, as described below:

12-bit resolution: bits 3:0 = CONV_DATA[11:8]

10-bit resolution: bits 3:2 = reserved; Bits1:0 : CONV_DATA[9:8]

8-bit resolution: bits 3:0 = reserved

6-bit resolution: bits 3:0 = reserved

14.6.6 ADC data register low (ADC_DRL)

Address offset: 0x05

Reset value: 0x00

7	6	5	4	3	2	1	0
CONV_DATA[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **Data[7:0]**: Data bits low

These bits are set/reset by hardware and are read only. They contain the 8 LS bits of the converted data. The converted voltage data bits are right aligned and their configuration depends on the programmed resolution, as described below:

12-bit resolution: Bits 7:0 = CONV_DATA[7:0]

10-bit resolution: Bits 7:0 = CONV_DATA[7:0]

8-bit resolution: Bits 7:0 = CONV_DATA[7:0]

6-bit resolution: Bits 7:6 = reserved; bits 5: 0 = CONV_DATA[5:0]

14.6.7 ADC high threshold register high (ADC_HTRH)

Address offset: 0x06

Reset value: 0x0F

7	6	5	4	3	2	1	0
Reserved				HT[11:8]			
				rw	rw	rw	rw

Bits 7:4 Reserved, forced by hardware to 0.

Bits 3:0 **HT[11: 8]**: Analog watchdog higher threshold high
These bits are set/reset by software. They define the MSB of the higher threshold for the analog watchdog.

14.6.8 ADC high threshold register low (ADC_HTRL)

Address offset: 0x07

Reset value: 0xFF

7	6	5	4	3	2	1	0
HT[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **HT[7:0]**: Analog watchdog higher threshold low
These bits are set/reset by software. They define the LSB of the higher threshold for the analog watchdog.

14.6.9 ADC low threshold register high (ADC_LTRH)

Address offset: 0x08

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved				LT[11:8]			
				rw	rw	rw	rw

Bits 7:4 Reserved, forced by hardware to 0.

Bits 3:0 **LT[11: 8]**: Analog watchdog lower threshold high
These bits are set/reset by software. They define the MSB of the lower threshold for the analog watchdog.

14.6.10 ADC low threshold register low (ADC_LTRL)

Address offset: 0x09

Reset value: 0x00

7	6	5	4	3	2	1	0
LT[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **LT[7:0]** Analog watchdog lower threshold low
These bits are set/reset by software. They define the LSB of the lower threshold for analog watchdog.

Note: The reference voltage threshold data bits are right aligned and their configuration depends on the programmed resolution, as described below:

12-bit resolution

ADC_HTRH & ADC_LTRH Bits 7:4 = reserved ; Bits 3:0 = HT[11:8] or LT[11:8]

ADC_HTRL & ADC_LTRL Bits 7:0 = HT[7:0] or LT[7:0]

10-bit resolution

ADC_HTRH & ADC_LTRH Bits 7:2 = reserved ; Bits 1:0 = HT[9:8] or LT[9:8]

ADC_HTRL & ADC_LTRL Bits 7:0 = HT[7:0] or LT[7:0]

8-bit resolution

ADC_HTRH & ADC_LTRH Bits 7:0 = reserved

ADC_HTRL & ADC_LTRL Bits 7:0 = HT[7:0] or LT[7:0]

6-bit resolution

ADC_HTRH & ADC_LTRH Bits 7:0 = reserved

ADC_HTRL & ADC_LTRL Bits 7:6 = reserved ; Bits 5:0 = HT[5:0] or LT[5:0]

14.6.11 ADC channel sequence 1 register (ADC_SQR1)

Address offset: 0x0A

Reset value: 0x00

7	6	5	4	3	2	1	0
DMAOFF	Reserved	CHSEL_STS(?)	CHSEL_ SVREFINT	CHSEL_S[27:24] (1)			
rw	-	rw	rw	rw	rw	rw	rw

Bits 7 **DMAOFF**: DMA disable for a single conversion
0: DMA Enabled
1: DMA Disabled

Bit 6 Reserved, forced by hardware to 0.

Bit 5 **CHSEL_STS**: Selection of channel TS for scan
These bits are set/reset by software. Channel TS must be kept reset.
A value ‘1’ in the CHSEL_Sx bit means that channel x is assigned in the scan sequence.

Bit 4 **CHSEL_SVREFINT**: Selection of channel V_{REFINT} for scan
These bits are set/reset by software. Channels V_{REFINT} must be kept reset.
A value ‘1’ in the CHSEL_Sx bit means that channel x is assigned in the scan sequence.

Bits 3:0(1) **CHSEL_S[27:24]**: Selection of channels 24 to 27 for scan (1)
These bits are set/reset by software.
A value ‘1’ in the CHSEL_Sx bit means that channel x is assigned in the scan sequence.

1. On medium-density devices, bits 3:1 are reserved and bit 0 is the CHSEL_S24 bit (selection of channel 24 for scan).

On STM8L05xx value line devices, bit 5 is reserved and must be kept cleared.

Note: This register must be modified after ADC is enabled by ADON bit in ADC_CR1 register.

14.6.12 ADC channel sequence register 2 (ADC_SQR2)

Address offset: 0x0B

Reset value: 0x00

7	6	5	4	3	2	1	0
CHSEL_S[23:16]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **CHSEL_S[23:16]**: Selection of channels 16 to 23 for scan
These bits are set/reset by software.
A value ‘1’ in the CHSEL_Sx bit means that channel x is assigned in the scan sequence.

Note: This register must be modified after ADC is enabled by ADON bit in ADC_CR1 register.

14.6.13 ADC channel select scan 3 (ADC_SQR3)

Address offset: 0x0C

Reset value: 0x00

7	6	5	4	3	2	1	0
CHSEL_S[15:8]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **CHSEL_S[15:8]**: Selection of channels 8 to 15 for scan
These bits are set/reset by software.
A value ‘1’ in the CHSEL_Sx bit means that channel x is assigned in the scan sequence.

Note: This register must be modified after ADC is enabled by ADON bit in ADC_CR1 register.

14.6.14 ADC channel select scan 4 (ADC_SQR4)

Address offset: 0x0D

Reset value: 0x00

7	6	5	4	3	2	1	0
CHSEL_S[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **CHSEL_S[7:0]**: Selection of channels 0 to 7 for scan
These bits are set/reset by software.
A value ‘1’ in the CHSEL_Sx bit means that channel x is assigned in the scan sequence.

Note: This register must be modified after ADC is enabled by ADON bit in ADC_CR1 register.

14.6.15 ADC trigger disable 1 (ADC_TRIGR1)

Address offset: 0x0E

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved		TSON(1)	VREFINTON	TRIG[27:24]			
		rw	rw	rw	rw	rw	rw

Bits 7:6 Reserved, forced by hardware to 0.

Bit 5 **TSON**: Temperature sensor internal reference voltage enable
This bit is set/reset by software.
0: Temperature sensor internal reference voltage disabled
1: Temperature sensor internal reference voltage enabled

Bit 4 **VREFINTON**: Internal reference voltage enable
This bit is set/reset by software.
0: Internal reference voltage disabled
1: Internal reference voltage enabled

Bits 3:0(1) **TRIG[27:24]**: Channels 24 to 27 schmitt trigger disable
These bits are set/reset by software.
A value ‘1’ in the TRIGx bit means that the Schmitt trigger corresponding to channel x is disabled.

1. On medium-density devices, bits 3:1 are reserved and bit 0 is the TRIG24 bit (channel 24 schmitt trigger disabled). On STM8L05xx value line devices, bit 5 is reserved and must be kept cleared.

14.6.16 ADC trigger disable 2 (ADC_TRIGR2)

Address offset: 0x0F

Reset value: 0x00

7	6	5	4	3	2	1	0
TRIG[23:16]							
				rw	rw	rw	rw

Bits 7:0 **TRIG[23:16]**: Channels 16 to 23 schmitt trigger disable
These bits are set/reset by software.
A value ‘1’ in the TRIGx bit means that the Schmitt trigger corresponding to channel x is disabled.

14.6.17 ADC trigger disable 3 (ADC_TRIGR3)

Address offset: 0x10

Reset value: 0x00

7	6	5	4	3	2	1	0
TRIG[15:8]							
				rw	rw	rw	rw

Bits 7:0 **TRIG[15:8]**: Channels 8 to 15 schmitt trigger disable
These bits are set/reset by software.
A value ‘1’ in the TRIGx bit means that the Schmitt trigger corresponding to channel x is disabled.

14.6.18 ADC trigger disable 4 (ADC_TRIGR4)

Address offset: 0x11

Reset value: 0x00

7	6	5	4	3	2	1	0
TRIG(7:0)							
				rw	rw	rw	rw

Bits 7:0 **TRIG[7:0]**: Channels 0 to 7 schmitt trigger disable
These bits are set/reset by software.
A value ‘1’ in the TRIGx bit means that the schmitt trigger corresponding to channel x is disabled

14.6.19 ADC register map and reset values

Table 48. Register map

Address offset	Register name	7	6	5	4	3	2	1	0
0x00	ADC_CR1 Reset value	OVERIE 0	RES[1:0] 00		AWDIE 0	EOCIE 0	CONT 0	START 0	ADON 0
0x01	ADC_CR2 Reset value	PRESC 0	TRIG_EDGE1 0	TRIG_EDGE0 0	EXTSEL1 0	EXTSEL0 0	SMPT1_2 0	SMTP1_1 0	SMTP1_0 0
0x02	ADC_CR3 Reset value	SMTP2_2 0	SMTP2_1 0	SMTP2_0 0	CHSEL4 1	CHSEL3 1	CHSEL2 1	CHSEL1 1	CHSEL0 1
0x03	ADC_SR Reset value	-	-	-	-	-	OVER 0	AWD 0	EOC 0
0x04	ADC_DRH Reset value	-	-	-	-	CONV_DATA[11:8] 0			
0x05	ADC_DRL Reset value	CONV_DATA[7:0] 0							
0x06	ADC_HTRH Reset value	-	-	-	-	HT11 1	HT10 1	HT9 1	HT8 1
0x07	ADC_HTRL Reset value	HT7 1	HT6 1	HT5 1	HT4 1	HT3 1	HT2 1	HT1 1	HT0 1
0x08	ADC_LTRH Reset value	-	-	-	-	LT11 0	LT10 0	LT9 0	LT8 0
0x09	ADC_LTRL Reset value	LT7 0	LT6 0	LT5 0	LT4 0	LT3 0	LT2 0	LT1 0	LT0 0
0x0A	ADC_SQR1 Reset value	DMAOFF 0	-	CHSEL_STS(1) 0	CHSEL_SVREFINT 0	CHSEL_S27(2) 0	CHSEL_S26(2) 0	CHSEL_S25(2) 0	CHSEL_S24 0
0x0B	ADC_SQR2 Reset value	CHSEL_S[23:16] 0							
0x0C	ADC_SQR3 Reset value	CHSEL_S[15:8] 0							
0x0D	ADC_SQR4 Reset value	CHSEL_S[7:0] 0							
0x0E	ADC_TRIGR1 Reset value	-	-	TSON(1) 0	VREFINTON 0	-TRIG27(2) 0	-TRIG26(2) 0	TRIG25(2) 0	TRIG24 0
0x0F	ADC_TRIGR2 Reset value	TRIG23 0	TRIG22 0	TRIG21 0	TRIG20 0	TRIG19 0	TRIG18 0	TRIG17 0	TRIG16 0
0x10	ADC_TRIGR3 Reset value	TRIG15 0	TRIG14 0	TRIG13 0	TRIG12 0	TRIG11 0	TRIG10 0	TRIG9 0	TRIG8 0
0x11	ADC_TRIGR4 Reset value	TRIG7 0	TRIG6 0	TRIG5 0	TRIG4 0	TRIG3 0	TRIG2 0	TRIG1 0	TRIG0 0

1. This bit is reserved in STM8L05xx value line devices.
2. This bit is reserved in medium-density devices.