COMPUTER BASICS
U4 EXERCISES: Sequential Systems

U4.1. Consider a Jhonson counter or queue switch consisting of four FF-D (D0 = / Q3), being one of the valid states Q3Q2Q1Q0 = 0000. Suppose that due to some noise of electromagnetic origin, the counter is not in any of the states of the expected sequence. Demonstrate that in this case, the counter will continue with a new sequence, without reaching the expected sequence. **b)** Modify the counter by replacing the FF0 with a FF-JK. The entry J0 = / Q2. / Q3 and K0 = Q3. Show that in this case the counter will autocorrect to the expected sequence.

Solution: a)

	Expected Sequence			
	Q_3	Q_2	Q_1	Q_0
S_0	0	0	0	0
S_1	0	0	0	1
S_2	0	0	1	1
S_3	0	1	1	1
S_4	1	1	1	1
S_5	1	1	1	0
S_6	1	1	0	0
S_7	1	0	0	0
S_0	0	0	0	0

Erroneous Sequence			
Q_3	Q_2	Q_1	Q_0
0	1	1	0
1	1	0	1
1	0	1	0
0	1	0	0
1	0	0	1
0	0	1	0
0	1	0	1
1	0	1	1
0	1	1	0

b) The state equation for FF_0 will be $\overline{D}$ after the modification

$$Q_0^{n+1} = J_0^n \overline{Q_0^n} + \overline{K_0^n} Q_0^n = \overline{Q_3^n}\ \overline{Q_2^n}\ \overline{Q_0^n} + \overline{Q_3^n} Q_0^n = \overline{Q_3^n}\ (\overline{Q_2^n} + Q_0^n)$$

For example, an erroneous initial sequence such as 0110 will evolve to a valid statec such as 1100 (S_6).

U4.2. Design a module-4 synchronous counter, using: a) FF-JK; b) FF-D and c) FF-T.

Solution:

	Current state		Next state	
	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}
S_0	0	0	0	1
S_1	0	1	1	0
S_2	1	0	1	1
S_3	1	1	0	0

a) $J_0 = 1$; $K_0 = 1$ $\quad J_1 = Q_0$; $K_1 = Q_0$

b) $D_0 = \overline{Q_0}$ $\quad D_1 = Q_1 \overline{Q_0} + \overline{Q_1} Q_0$

c) $T_0 = 1$ $\quad T_1 = Q_0$

U4.3. Design a module-7 counter using FF-T. The counter traces the states in increasing order except for S3. Design a protection mechanism so that the counter goes to the S0 state if it accidentally reaches the S3 state.

Solution:

Assigning the corresponding binary value to each state of the counter, the transition table will be:

	Current state			Next State		
	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
S_0	0	0	0	0	0	1
S_1	0	0	1	0	1	0
S_2	0	1	0	1	0	0
S_3	0	1	1	0	0	0
S_4	1	0	0	1	0	1
S_5	1	0	1	1	1	0
S_6	1	1	0	1	1	1
S_7	1	1	1	0	0	0

The following expressions are obtained:

$$T_0 = Q_2 + \overline{Q_1} + Q_0\ ; \qquad T_1 = Q_0 + \overline{Q_2}\ Q_1\ ; \qquad T_2 = \overline{Q_2}\ Q_1\ \overline{Q_0} + Q_2 Q_1 Q_0$$

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U4.4. Using three FF-JK, perform a synchronous circuit that counts only the four possible even states. To avoid any blocking problem, design a mechanism so that if the counter accidentally goes into an odd state, go to the state defined as Q2Q1Q0 = 000.

Solution:

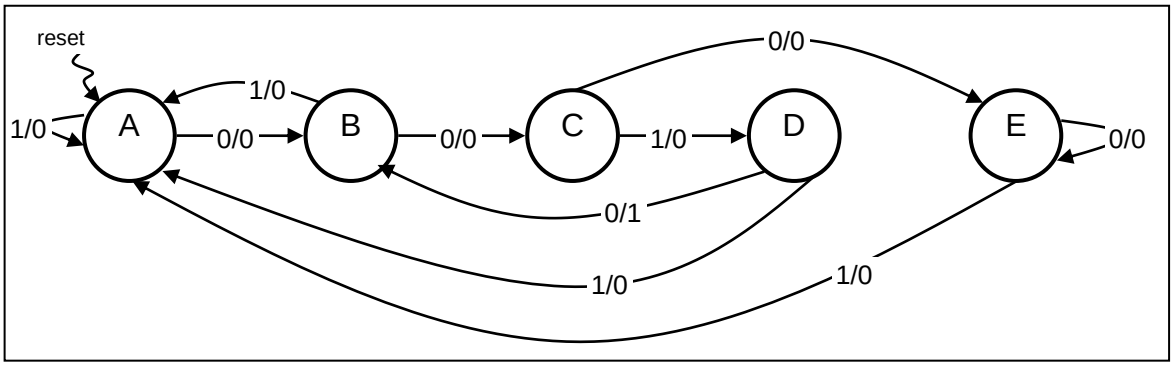
	Current state			Next State		
	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
S_0	0	0	0	0	1	0
S_1	0	0	1	0	0	0
S_2	0	1	0	1	0	0
S_3	0	1	1	0	0	0
S_4	1	0	0	1	1	0
S_5	1	0	1	0	0	0
S_6	1	1	0	0	0	0
S_7	1	1	1	0	0	0

By assigning the corresponding binary value to each state of the counter, the following equations are obtained:

$J_0 = 0$; $K_0 = 1$ $\quad J_1 = \overline{Q_0}$; $K_1 = 1$ $\quad J_2 = Q_1 \overline{Q_0}$; $K_2 = Q_1 + Q_0$

U4.5. Given the attached state table, calculate the state equations if FF-JK is used to implement the circuit. Draw the logic diagram for the sequence detector.

Current state	Next State	
	X=0	X=1
A	B/0	A/0
B	C/0	A/0
C	E/0	D/0
D	B/1	A/0
E	E/0	A/0



Solution:

For the assigned states. A (000), B (001), C (010), D (011) y E (101), the state equations will be:

$J_0 = Q_1 + \overline{X}$ $\quad K_0 = \overline{Q_2}\ \overline{Q_1} + X$

$J_1 = \overline{Q_2}\ Q_0\ \overline{X}$ $\quad K_1 = Q_0 + \overline{X}$

$J_2 = Q_1\ \overline{Q_0}\ \overline{X}$ $\quad K_2 = X$

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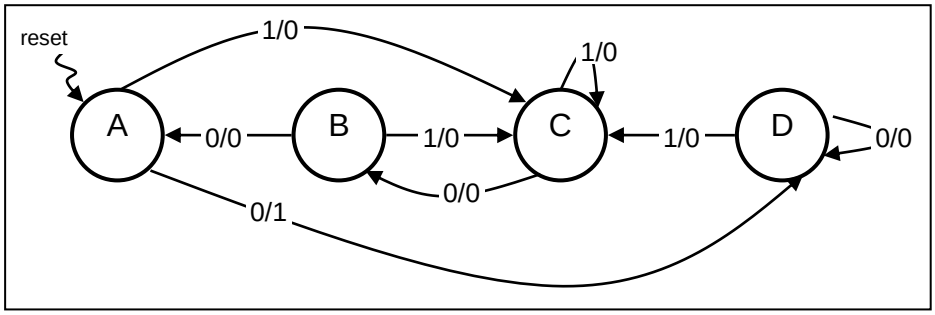
U4.6. A four state sequential circuit is characterized by the attached state table. Calculate the excitation equations of the flip-flops (state equations) and draw the logic diagram for a) FF-D, b) FF-JK and c) FF-T.

Current state	Next State	
	X=0	X=1
A	D/1	C/0
B	A/0	C/0
C	B/0	C/0
D	D/0	C/0

Solution:



For the assigned states. A (00), B (01), C (11) y D (10), the state equations Will be:

a) $D_0 = Q_1Q_0 + X$ $D_1 = \overline{Q_0} + X$

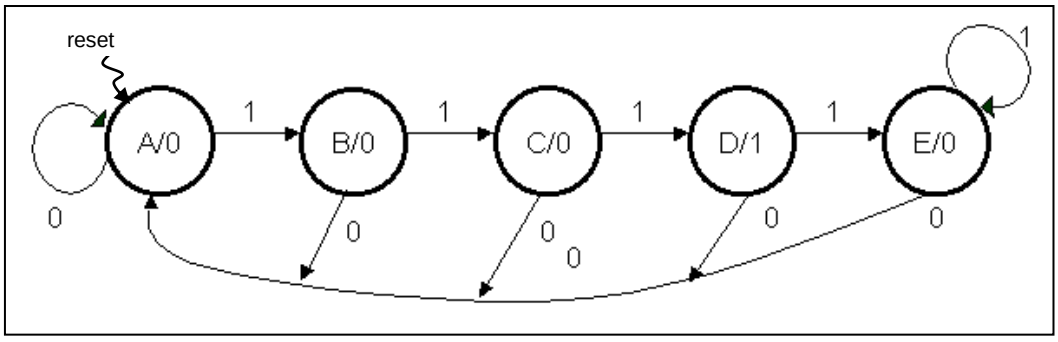
b) $J_0 = X$ $K_0 = \overline{Q_1}\ \overline{X}$

$J_1 = \overline{Q_0} + X$ $K_1 = Q_0\overline{X}$

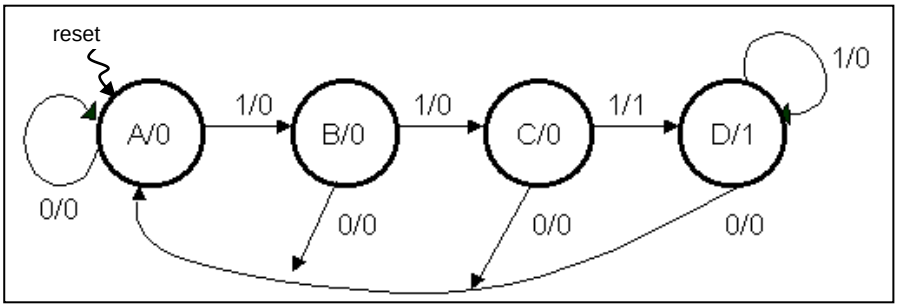
c) $T_0 = \overline{Q_0}X + \overline{Q_1}Q_0\overline{X}$ $T_1 = \overline{Q_1}\ \overline{Q_0} + \overline{Q_1}X + Q_1Q_0\overline{X}$

U4.7. Design only the state diagram for a MOORE circuit that has an output Z = 1 during a clock cycle, when exactly three 1 have been supplied through the input line during the three preceding clock intervals. If during 4 or more cycles are 1, the output should be Z = 0. Repeat the problem for a MEALY circuit, that is, the determination that exactly three 1 have appeared is done during the moment of occurrence of the third 1.

Solution: a) MOORE



a) MEALY



FUNDAMENTOS DE COMPUTADORES
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U4.8. You are asked to control a beverage vending machine. The inputs to the circuit are signals that come from the input of coins. The Outputs are signals that must be sent to dispense the (unique) drink and activate the return of the change when necessary. The price of the drink is € 1.5 and the system only accepts coins of 50 cents, € 1 and € 2 that are detected one in one independently in a cycle of the system.

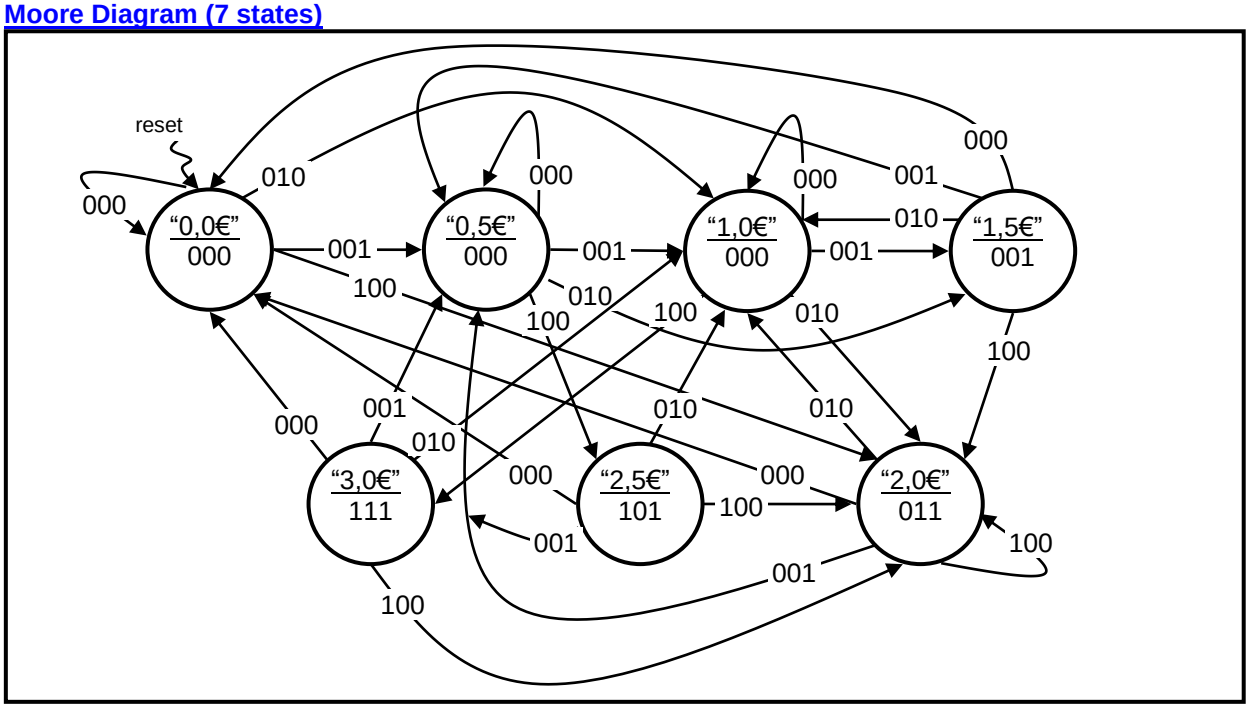
Solution:

Input assignment: X_2, X_1,X_0, are equivalent to entering a 2 €, 1 € and 0,5 € coin, respectively.

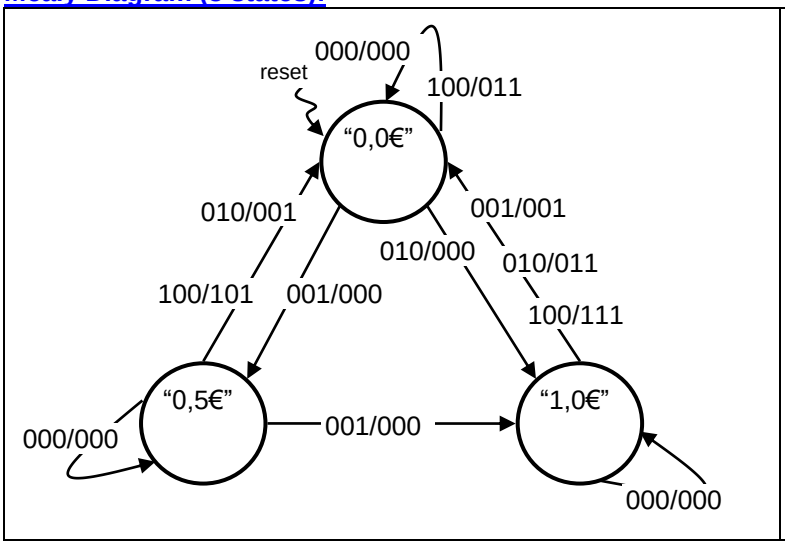
Any combination that means receiving more than one coin at a time will not be considered.

Output assignment: Z_2, Z_1, Z_0, are equivalent to, returning 1 €, returning 0,5 €, and dispense a drink, respectively.

Moore Diagram (7 states)



Mealy Diagram (3 states):



Assignment of states:

Q_1Q_0 = 00 - 0 € Returned

Q_1Q_0 = 01 - 0,5 € Returned

Q_1Q_0 = 10 - 1 € Returned

Output expression: $Z_0=X_2+Q_0X_1+Q_1X_1+Q_1X_0$; $Z_1=Q_1X_1+\overline{Q_0}\,X_2$; $Z_2=Q_1X_2+Q_0X_2$

State expression: $D_0=\overline{Q_1}\;\overline{Q_0}\;X_0+Q_0\;\overline{X_2}\;\overline{X_1}\;X_0$; $D_1=Q_0X_0+\overline{Q_1}\;\overline{Q_0}\;X_1+Q_1\;\overline{X_2}\;\overline{X_1}\;\overline{X_0}$

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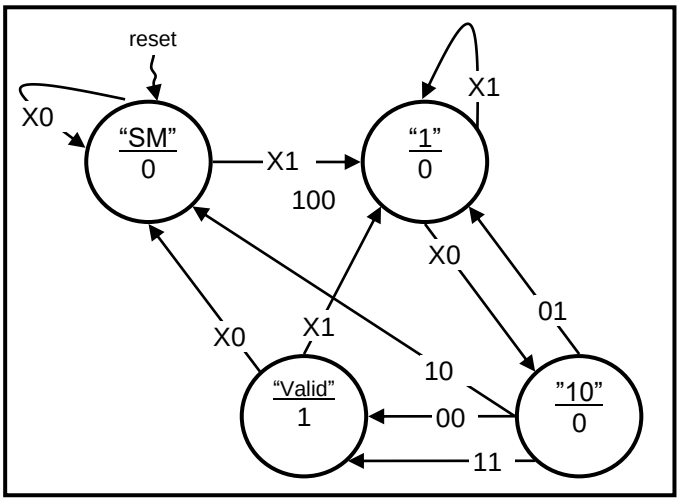
U4.9. Design a MOORE circuit which detects a complete sequence of three consecutive bits as a function of a control signal S (if S = 0 : sequence is100, if S = 1:sequence is 101). When a valid sequence is detected, you should start searching for a new one without taking into account the previous sequence. If, in the middle of searching for a valid sequence, the control signal is changed, the circuit must respond on the next clock edge to the new signal. Design the state diagram, state table, state excitation equations and Outputs and draw the circuit. An example of the sequence can be:

S	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	0	1	X
X	1	1	0	1	0	1	0	0	1	0	0	1	0	0	1	0	1	X
Z	0	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0	1

Solution:



Assignment of states in the detection order for a valid sequence: SM (00), "1" (01), "10" (10) and "Valid Sequence" (11).

The system inputs are S and X. The output Will be 1 for the 11 state.

The excitation and output expressions are:

$$D_0 = X + Q_1 \overline{Q_0}\ \overline{S}$$

$$D_1 = \overline{Q_1}\ Q_0\ \overline{X} + Q_1\ \overline{Q_0}\ SX + Q_1\ \overline{Q_0}\ \overline{S}\ \overline{X}$$

$$Z = Q_1 Q_0$$

FUNDAMENTOS DE COMPUTADORES
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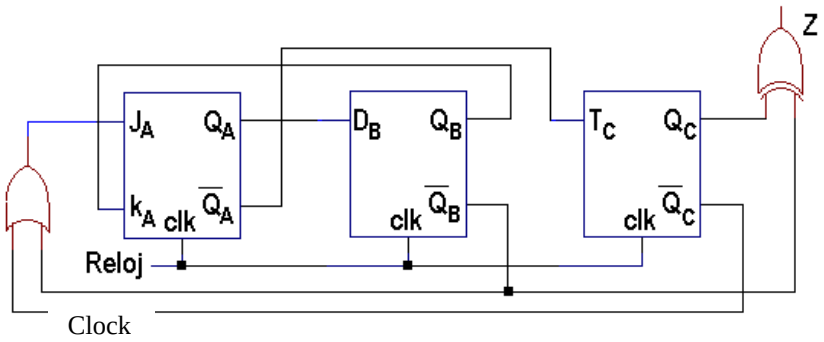
U4.10. The circuit in the figure performs the operation of a certain MOORE automaton:

a) Build the transition table of circuit states, indicating for each state the corresponding value of the output Z.

b) Write the sequence of System Outputs if the initial state is:

$Q_C = 0$, $Q_B = 0$ y $Q_A = 1$.



Solution:

a)

Current State			Output	Next State		
Q_C^n	Q_B^n	Q_A^n	Z	Q_C^{n+1}	Q_B^{n+1}	Q_A^{n+1}
0	0	0	1	1	0	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	1	0	0	1	0
1	0	0	0	0	0	1
1	0	1	0	1	1	1
1	1	0	1	0	0	0
1	1	1	1	1	1	0

b)

Time:	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12
State:	1	3	2	5	7	6	0	5	7	6	0	...
Output:	1	0	0	0	1	1	1	0	1	1	1	

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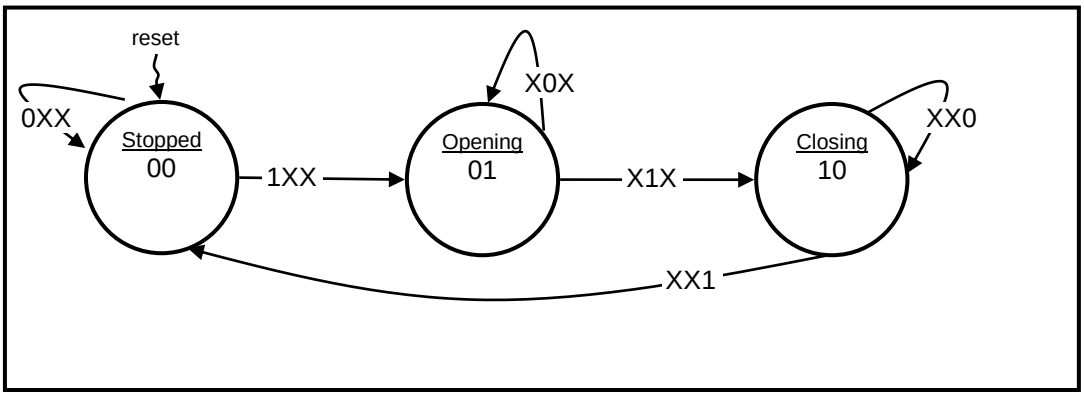
U4.11. You want to control a sliding door, which can move from left to right and vice versa. Its route is limited by two limit switches, one on the left (B) that will activate when the door is fully open and another on the right (C) that will indicate that it is completely closed. When the door is closed, acting on a button (A), an opening cycle begins, moving to the left, until the door reaches the end of the stroke, at which time the door will reverse its movement, moving to the right until it is completely closed. If for any reason A is pressed during the movement of the door, it must not stop. The Outputs of the circuit must activate in each case the movement of the motors to open and close the door. Using J-K type flip-flops, perform the control circuit that is needed. Indicate the state diagram and the state and output equations.

Solution:



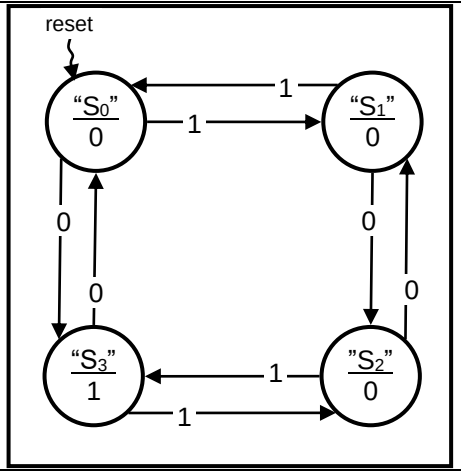
The three system states are:
Door stopped. Bits assignment Q_1Q_0 (00). Output assigned to the motors to open Ma=0 and close Mc=0.
Door moving, opening. Bits assignment (01). Mc = 0 and Ma = 1
Door moving, closing. Bits assignment (10). Mc = 1 and Ma = 0
The system inputs are variables A, B, and C defined above.

Excitation expression: $J_0 = \overline{Q_1}\,A$ $K_0 = B$ $J_1 = Q_0B$ $K_1 = C$

Output expression: $Ma = Q_0$ $Mc = Q_1$

U4.12. Perform a sequential Moore circuit that analyzes a string of n bits that are transmitted in series synchronized with a clock signal. Using type D flip-flops, the output of which must be "1" each time the string has an even number of "1" and an odd number of "0". Suppose that an asynchronous reset signal puts the circuit in the initial state So. NOTE: no "0" or no "1" is considered even. Indicate the state diagram, as well as the excitation (state) and output equations.

Solution:



The four possible states for the system are:

S_0: Even number of "0" and even number of "1". Assignment of bits $Q_1Q_0 = 00$

S_1: Even number of "0" and an odd number of "1". Assignment of bits $Q_1Q_0 = 01$

S_2: Odd number of "0" and an odd number of "1". Assignment $Q_1Q_0 = 10$

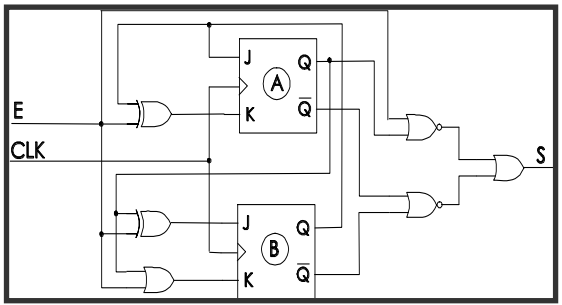
S_3: Odd number of "0" and an even number of "1". Assignment of bits $Q_1Q_0 = 11$)

The excitation and output expressions:

$D_0 = \overline{Q_0}$; $D_1 = \overline{Q_1}\,\overline{X} + Q_1X$;

$Z = Q_1Q_0$

U4.13. Supposing that the circuit, initially is E=QB=QA=0:



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

a) Explain the machine type (Moore o de Mealy) and justify your answer.

b) Obtain the state diagram.

c) Find the transition table and the output that defines it.

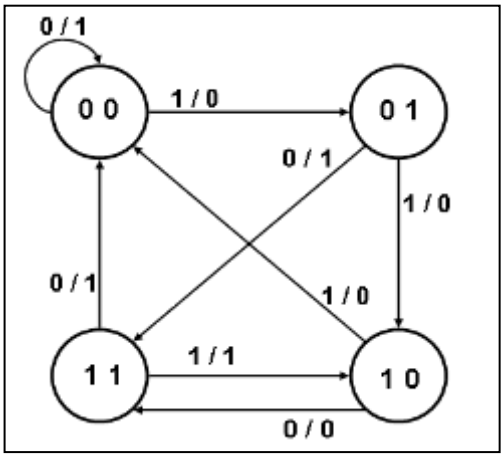
Solution:

a) It's a Mealy circuit since the output is a function of the input: $S = \overline{Q_A + E} + \overline{\overline{Q_A} + \overline{Q_B}}$

b) The state diagram is shown in the figure

c) The transition and output tables are:

Q_A^n	Q_B^n	E	J_A	K_A	J_B	K_B	Q_A^{n+1}	Q_B^{n+1}	S
0	0	0	0	0	0	0	0	0	1
0	0	1	0	1	1	1	0	1	0
0	1	0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	1	0	0
1	0	0	0	0	1	1	1	1	0
1	0	1	0	1	0	1	0	0	0
1	1	0	1	1	1	1	0	0	1
1	1	1	1	0	0	1	1	0	1



U4.14. A Mealy machine has a synchronized input with a clock signal and a Z output. The circuit sets Z = 1 when it detects a sequence at input 110 and only returns Z = 0 when it detects sequence 010. For example:

T	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
X	0	0	1	1	1	0	1	0	1	1	0	1	1	1	0	0	1	0	0	1
Z	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0

Draw the state diagram using a maximum of 6 states, knowing that the state at the start of the output is Z = 0.

Solution:

The system will need memory from the last active sequence.

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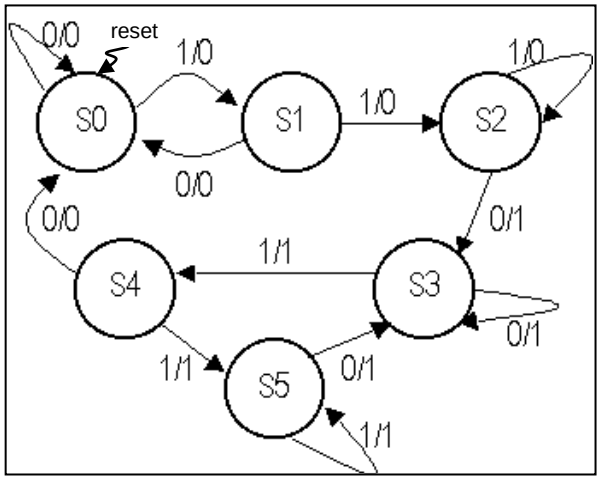

State description:

S0: Reset state without memory, or after "010"

S1: Valid sequence, "1" from reset to set

S2: Valid sequence "11" from reset to set

S3: Requested sequence "110" from reset to set

S4: Valid sequence "01" from set to reset

S5: Set state without memory, or after "011"

FUNDAMENTOS DE COMPUTADORES
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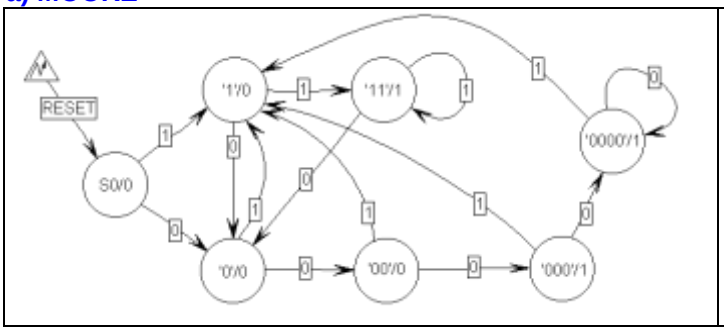
U4.15. A circuit receives serial data synchronized with a clock signal via an input X. Starting from an initial state without memory and with output Z = 0, the circuit must switch the output Z to 1 each time it detects that 2 or more successive "1" s have been received, or 4 or more successive "0"s. **a)** Design a Moore machine indicating the state diagram, the transition table and the gate scheme (transition and output equations), use type D FF. **b)** Draw the state Diagram for a Mealy machine.

Solution:

a) MOORE



State assignment
$Q_2Q_1Q_0$:
S0 : 0 0 0
“0” : 0 0 1
”00” : 0 1 0
“000” : 0 1 1
“0000” : 1 0 0
“1” : 1 0 1
“11” : 1 1 0

The transition and output expressions are:

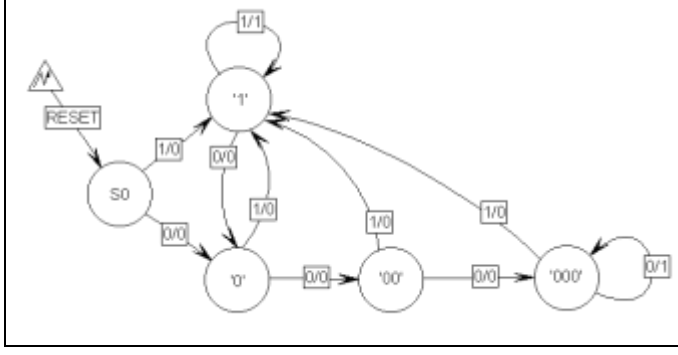
$$D_0 = \overline{Q_2}\ \overline{Q_0} + \overline{Q_1}\ X + \overline{Q_1}\ \overline{Q_0}\ X + Q_1\ \overline{Q_0}\ X + Q_2Q_0\ \overline{X}$$

$$D_1 = \overline{Q_2}\ \overline{Q_1}\ Q_0\ \overline{X} + \overline{Q_2}\ Q_1\ \overline{Q_0}\ X + Q_2Q_1X + Q_2Q_0X$$

$$D_2 = Q_2\ \overline{Q_1}\ \overline{Q_0} + Q_1Q_0 + X$$

$$Z = Q_2\ \overline{Q_0}$$

b) MEALY:



State assignment
$Q_2Q_1Q_0$
S0 : 0 0 0
“0” : 0 0 1
”00” : 0 1 0
“000” : 0 1 1
“1” : 1 0 0

The transition and output expressions are:

$$D_0 = Q_1\ \overline{X} + \overline{Q_0}\ \overline{X} \qquad D_1 = Q_1\ \overline{X} + Q_0\ \overline{X} \qquad D_2 = X$$

$$Z = Q_2X + Q_1Q_0\ \overline{X}$$

FUNDAMENTOS DE COMPUTADORES
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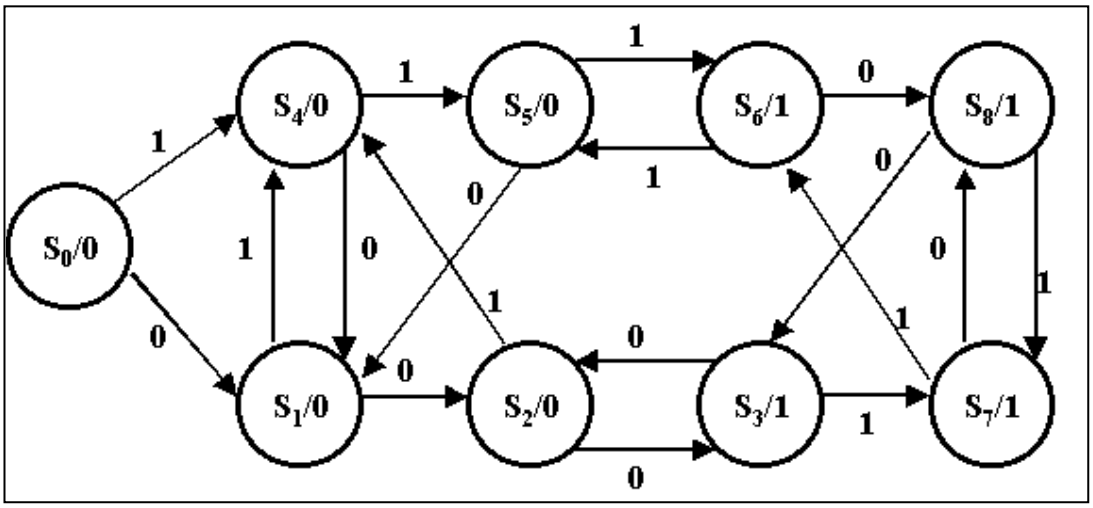
U4.16. A sequential circuit has an X input synchronized with a CLK clock and a serial data Z output. Starting from an initial state without memory with Z = 0, the Z output should only change when it detects that 3 consecutive bits of input have the same value. For example:

CYCLE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	1	0	1	0	1	1	1	1	1	0	0	0	0	0	1	--
Z	--	0	0	0	0	0	0	1	0	1	1	1	0	1	0	0

Draw the corresponding state diagram for a Moore machine and indicate the minimum number of FFs needed to build the circuit.

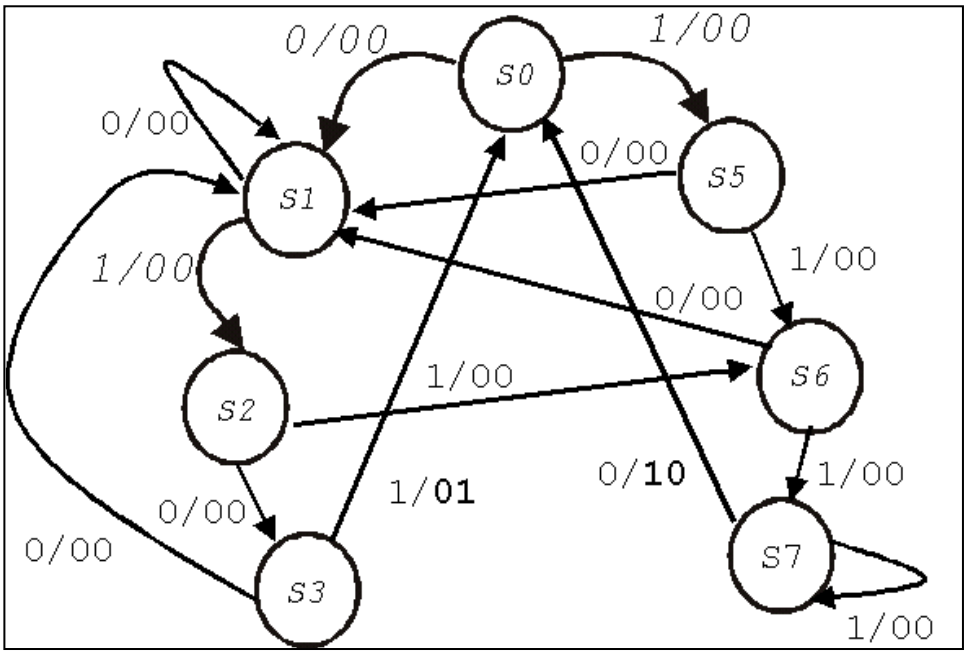
Solution:



By having 9 states, you need a minimum of 4 FF

U4.17. A sequential Mealy-type circuit has a one-bit serial data input X synchronized with a clock signal CLK. The Z output of the circuit has two bits Z1 Z0. The circuit is normally maintained with Z1 Z0 = 00 but passes to Z1 Z0 = 01 when the sequence 0101 is detected. Similarly, it goes to Z1 Z0 = 10 when it detects sequence 1110. Each time it detects a correct sequence the circuit returns to its initial state (ie, there is no overlap, for example, 010101 does not activate output twice). Design said circuit.

Solution:



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.18. From the following table of states of a Mealy machine, find the value of the output function Z. The machine has three inputs A2 A1 A0 and a single output.

	$Q^{n+1}{}_1Q^{n+1}{}_0$ / Z					
$Q^n{}_1Q^n{}_0$	$A_2A_1A_0$=000	$A_2A_1A_0$=0X1	$A_2A_1A_0$=010	$A_2A_1A_0$=1X0	$A_2A_1A_0$=101	$A_2A_1A_0$=111
00	00/0	00/1	01/0	00/0	00/0	00/1
01	01/0	01/1	00/0	01/0	00/0	01/1
10	00/0	10/1	01/0	00/1	00/0	01/0
11	11/1	11/0	11/0	11/1	11/0	11/0

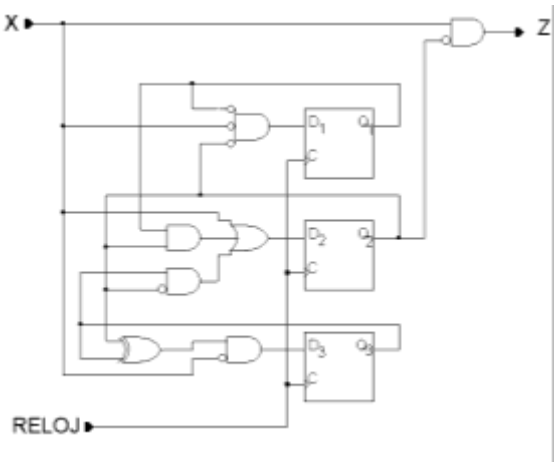
Solution:

$$Z = \overline{A_2}\, A_0\, \overline{Q_1} + A_1\, A_0\, \overline{Q_1} + \overline{A_2}\, A_0\, \overline{Q_0} + A_2\, \overline{A_0}\, Q_1 + \overline{A_1}\, \overline{A_0}\, Q_1\, Q_0$$

U4.19. Given the circuit in the figure:

a) Explain what type of machine it is (Moore or de Mealy) and indicate why.

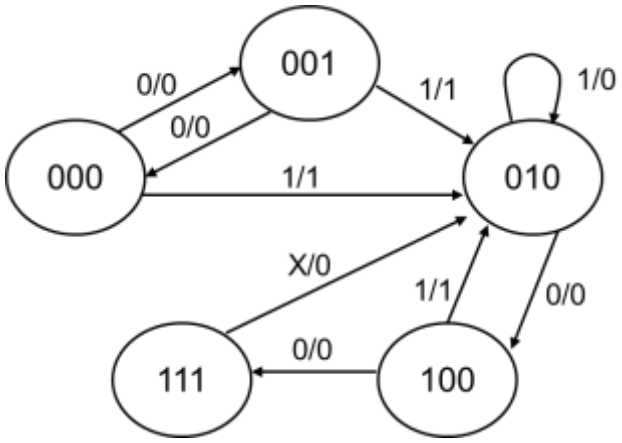
b) Starting from a state of Q3 = Q2 = Q1 = 0, obtain the state diagram.



Solution:

a) It is a Mealy FSM, because the output is a function of the input. $Z = \overline{Q_2}\, X$

b)



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.20. Given the following state table: **a)** Indicate, justifying the answer, if the machine it represents is Moore or Mealy. **b)** Using FF-JK, calculate the state equations. **c)** Calculate the equation of the output and d**)** draw the state diagram.

Current state $Q_1^n\ Q_0^n$	Next State/output $(Q_1^{n+1}\ Q_0^{n+1}/Z)$			
	$X_1X_o = 00$	$X_1X_o = 01$	$X_1X_o = 10$	$X_1X_o = 11$
00	01/0	00/0	01/0	00/0
01	10/0	00/0	10/0	00/0
10	10/0	11/0	10/0	11/0
11	01/0	00/1	00/1	00/0

Solution:

a) It is a Mealy machine since the output depends on the inputs of the system.

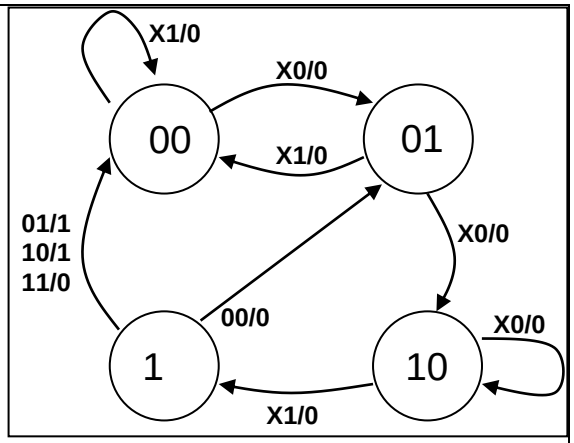
b)

$J_1 = \overline{X_0}\ Q_0$; $K_1 = Q_0$

$J_0 = \overline{X_0}\ \overline{Q_1} + X_0\ Q_1$; $K_0 = \overline{Q_1} + X_0 + X_1$

c)

$Z = X_1\ X_0\ \overline{Q_1}\ Q_0 + X_1\ X_0\ Q_1\ \overline{Q_0}$



d) The state machine detects the sequence 0010 without overlap if X_1=1 and the sequence without overlap 0011 if X_1=0

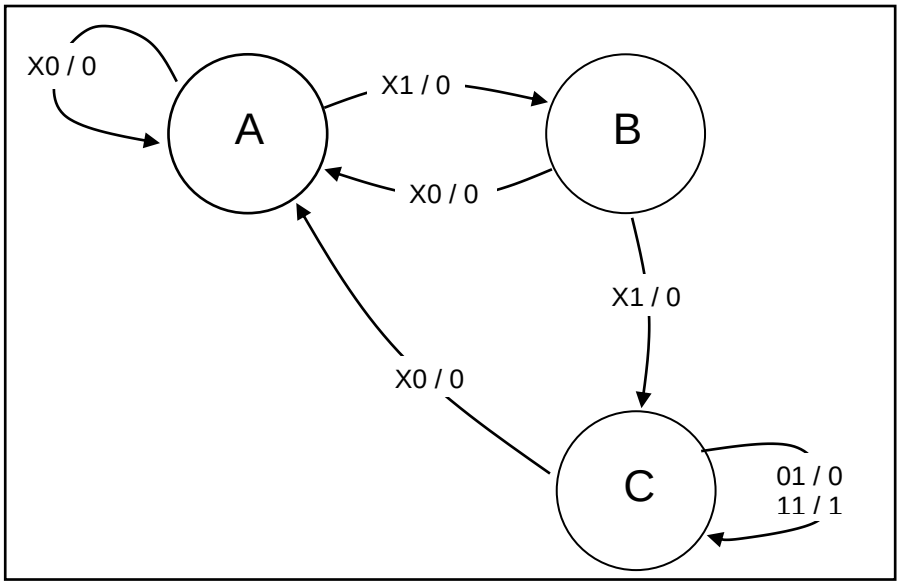
FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.21. In order to minimize the risk of falling while in a curve of Moto GP driver Dani Pedrosa (there is a serious risk when the speed is low and the inclination of the bike very large), the Repsol-Honda team has decided to place a sensor in each lateral of the pilot's knees (these are the sides that approach the ground when taking the curves) to detect how close it is to the ground, and another sensor connected to the speed counter of the motorcycle. If after detecting that, for a certain time, the speed of the motorcycle falls below a threshold value and the sensor installed in one of the two knees is activated because the pilot is very close to the ground, a warning light on the motorcycle is lit, indicating Pedrosa that there is a risk of falling and that the bike should be straightened. Help the Repsol-Honda engineers in their project, designing a Mealy state machine that controls the sensors. Let X_1, X_0 be the input sensors (inputs of the Mealy PLC). X_1=1, when one of the two sensors installed in the knees is activated because the knee is very close to the ground and X_0=1, warns if the speed of the motorcycle is below a certain threshold.

The unique output signal will be Z_0 (set to "1" when there is a risk of falling) and this occurs if in three consecutive clock cycles in which X_0=1 the sensor placed on some knee is activated (it is set to value "1"):

a) Make the state diagram of the automaton, using the necessary states of the attached diagram, adding more if necessary or leaving blank those that are not needed.
b) Write the table of states for the automaton.
c) For FF-JK, write the excitation (state) and output equations.

Solution:



The transition table will be:

	Next State / Current output (Q^+_1 Q^+_0 / Z_0)			
Current state (Q_1 Q_0)	X_1 X_0 = 0 0	X_1 X_0 = 0 1	X_1 X_0 = 1 0	X_1 X_0 = 11
0 0	**0 0 / 0**	**0 1 / 0**	**0 0 / 0**	**0 1 / 0**
0 1	**0 0 / 0**	**1 0 / 0**	**0 0 / 0**	**1 0 / 0**
1 0	**0 0 / 0**	**1 0 / 0**	**0 0 / 0**	**1 0 / 1**
1 1	**X X / X**	**X X / X**	**X X / X**	**X X / X**

Las excitation and output states, using FF-JK:

$J_1 = X_0\, Q_0$; $K_1 = \overline{X_0}$; $J_0 = X_0\, \overline{Q_1}$; $K_0 = 1$

$Z_0 = X_1\, X_0\, Q_1$

FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.22. We want to control the level of emission in a mobile phone. To do this, a state machine is designed with two inputs, E1 and E0, which estimate the emission level. The behavior of the same is the following: if both signals are at 0 ("00") is that the estimate is not valid. In other cases, the estimate is valid and its meaning is as follows:

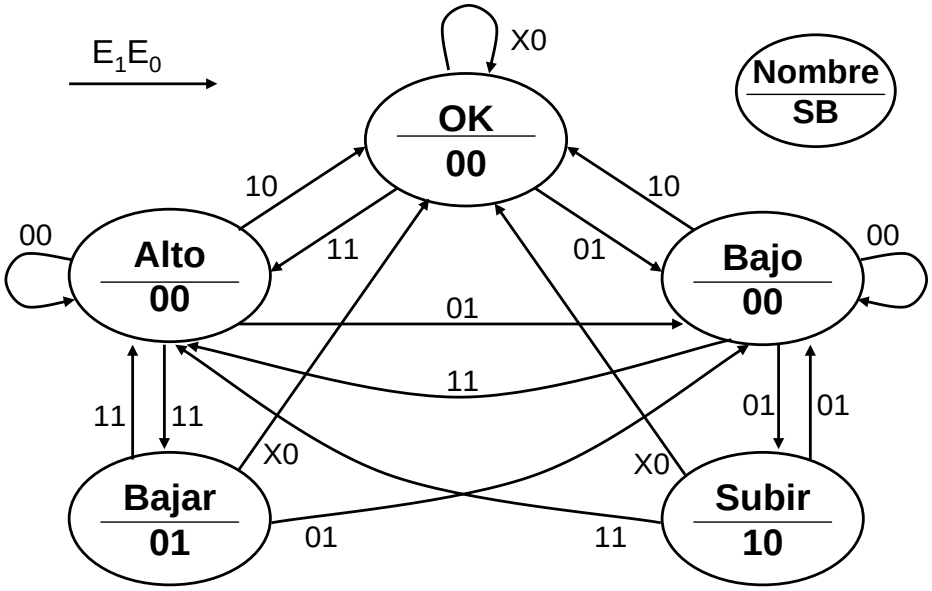
- "01" if it is estimated that the emission level is too low,
- "10" if the emission level is estimated to be adequate,
- "11" if it is estimated that the emission level is too high.

The emission level will be raised only if the last two valid estimates have been too low. Similarly, the emission level will be lowered if the last two valid estimates have been too high. Once the emission level changes, the estimates prior to the change will not be taken into account (there is no overlap).

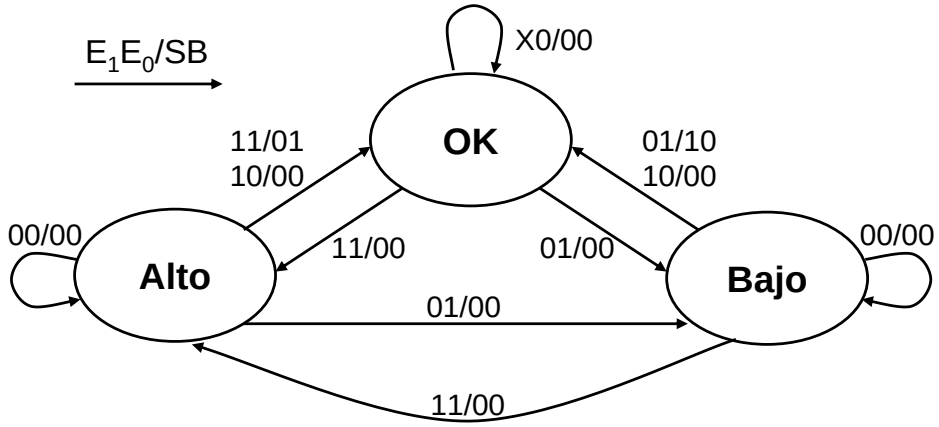
The Outputs of the circuit are two: S (up) and B (down). Both are activated by high level and during a single clock cycle each time they must act.

a) Draw the state diagram if the state machine is of the Moore type.

Solution



b) Draw the state diagram if the state machine is of the Mealy type.



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.23. The transition table between states of a given finite state machine (FSM) and its corresponding output table is provided.

State Transition table							
Current State			Input		Next State		
Q_2^n	Q_1^n	Q_0^n	X		Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	0	0	0		0	1	0
0	0	0	1		0	1	0
0	0	1	0		0	0	0
0	0	1	1		0	1	0
0	1	0	0		0	0	1
0	1	0	1		1	0	1
0	1	1	0		1	0	0
0	1	1	1		0	0	0
1	0	0	0		0	0	0
1	0	0	1		1	0	1
1	0	1	0		0	0	1
1	0	1	1		0	1	0
1	1	0	0		0	0	0
1	1	0	1		0	0	0
1	1	1	0		0	0	1
1	1	1	1		0	0	1

a) Assuming that flip-flop FF2 is of type JK, it is requested, using the corresponding Karnaugh diagrams provided, to minimize the state equations for this flip-flop.

Solution

Q_0X / Q_2Q_1	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	X	X	X	X

Q_0X / Q_2Q_1	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	1	1	1

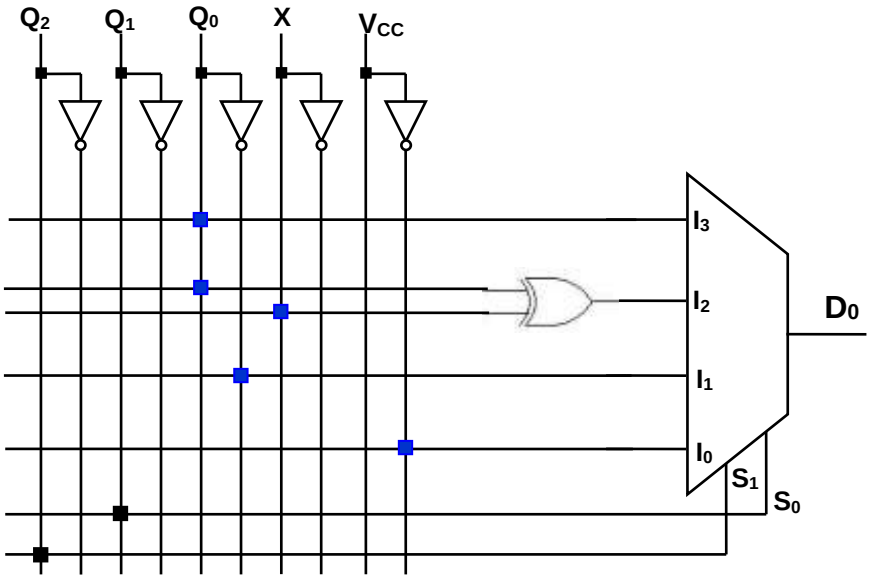
FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

10	X	X	X	X	**10**	1	0	1	1

$J_2 = Q_1 \overline{Q_0}\, X + Q_1 Q_0 \overline{X}$

$K_2 = Q_1 + Q_0 + \overline{X}$

b) Use the diagram of the attached figure and the minimum number of additional logical gates to implement the state equation for flip-flop FF0 assuming that it is of type D.



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EJERCICIOS U4: Circuitos Secuenciales

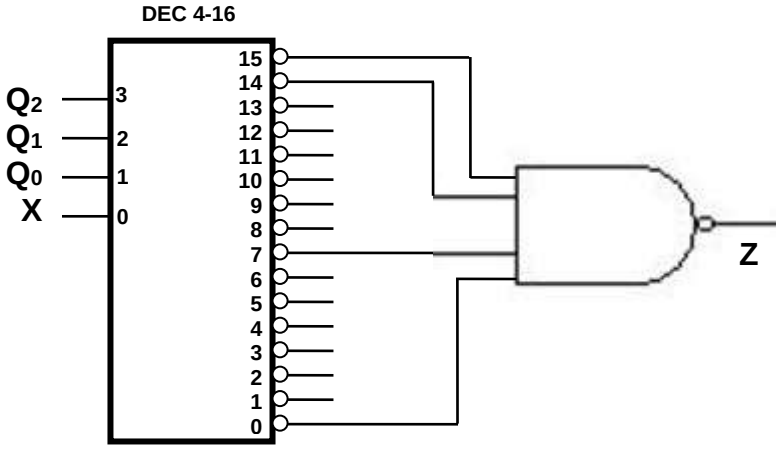
c) Use the diagram in the figure below with the decoder 4-16 with Outputs ACTIVATES LOW and the minimum number of additional logic gates to implement the output equation.

NOTE: All inputs must have a connected signal.

Output Table					
Current State			Input		Output
Q_2^n	Q_1^n	Q_0^n	X		Z
0	0	0	0		1
0	0	0	1		0
0	0	1	0		0
0	0	1	1		0
0	1	0	0		0
0	1	0	1		0
0	1	1	0		0
0	1	1	1		1
1	0	0	0		0
1	0	0	1		0
1	0	1	0		0
1	0	1	1		0
1	1	0	0		0
1	1	0	1		0
1	1	1	0		1
1	1	1	1		1

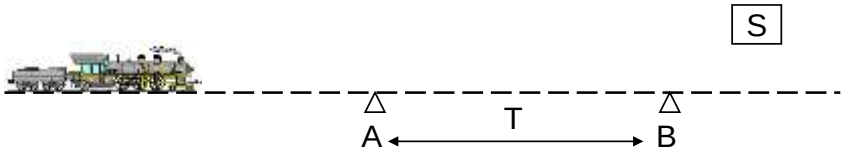
Indicate if it is a Moore or Mealy type WSF. Briefly justify the answer.

It is a Mealy machine, the Z output depends not only on the state but also on the X input, as shown in the table for the states Q2Q1Q0 = 000 and Q2Q1Q0 = 011.



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

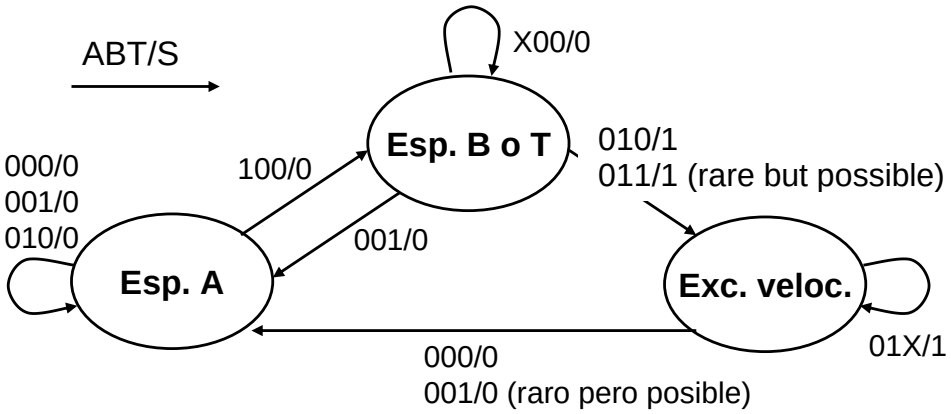
U4.24. We want to design a circuit that warns trains approaching a station with excessive speed. For this, there are three entries. There are two presence sensors, "A" and "B", which indicate by a '1' if there is a train on top of them (the sensors give their output with no bounces). There is also a timer circuit that is automatically activated when the train passes through "A" and activates "T" (input to the circuit to be designed) during a single clock cycle after a fixed time. This time is equal to the distance (B-A) divided by the maximum speed allowed.



The operation of the circuit must be as follows. The train always goes through "A" first. Once the train is detected, if "T" arrives before "B", the speed is correct and nothing is indicated. If "B" arrives before or at the same time as "T", there is an excess of speed. This is indicated by activating the only output, "S", which must remain active while the train passes through "B".
Note: The "A" and "B" inputs always remain active for more than one clock cycle at a time, but "T" is only activated during one cycle. It can be assumed that before the next train arrives, "B" and "T" will already have been activated, that the pair of variables "A" and "T" and "A" and "B" can never be active at the time:

a) Design the Mealy state diagram for the circuit.

Solution:



b) Make the assignment of states and write the table of states and output (only the table, without minimizing equations)

STATE	Q_1	Q_0		Q_1^n	Q_0^n	A	B	T		Q_1^{n+1}	Q_0^{n+1}		S
Wait A	0	0		0	0	0	0	0		0	0		0
Wait B or T	0	1		0	0	0	0	1		0	0		0
Exc. veloc.	1	0		0	0	0	1	0		0	0		0
				0	0	1	0	0		0	1		0
				0	1	0	0	0		0	1		0
				0	1	0	0	1		0	0		0
				0	1	0	1	0		1	0		X
				0	1	0	1	1		1	0		X
				0	1	1	0	0		0	1		0
				1	0	0	0	0		0	0		X
				1	0	0	0	1		0	0		X
				1	0	0	1	0		1	0		1
				1	0	0	1	1		1	0		1

FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.25. An interactive banking terminal offers the client two possibilities: Show on screen the latest movements associated with an account and show the balance of said account on the screen. Prior to the selection of any of the options, it is necessary to press a button that indicates "Start of a new operation", after which a menu with the two options described above will appear on the screen, each of them associated with a different button. Only one button can be pressed at a time, so operations cannot be selected simultaneously. If the button "Show last movements" is pressed, after two active flanks of the clock, the terminal will show on the screen the message "These are the last movements requested". If the "Show end balance" button is pressed, after an active clock edge, the terminal will display the message "This is the requested final balance". Once either of the two operations is started, you can only go to the beginning of a new operation in the first clock cycle of its execution by pressing the "Start a new operation" button, and it cannot be interrupted in the remaining execution clock cycles. Once the selected option is finished, the terminal will wait for the "Start a new operation" button to be pressed.

Draw the state diagram of a Mealy circuit that controls the operation of the terminal. The three operation buttons will be the circuit inputs:

Start of a new operation: X_2

Show latest movements: X_1

Update notepad: X_0

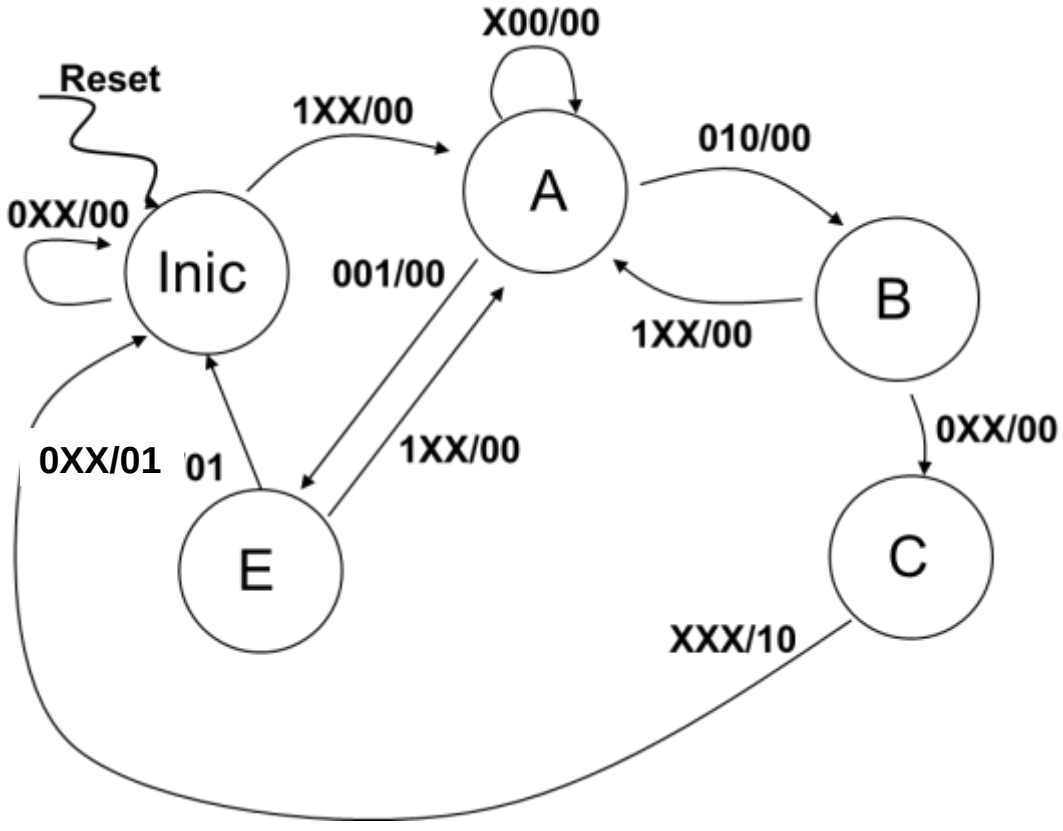
The end of operation messages will be activated by the Outputs of the circuit:

These are the last requested operations: Z_1

This is the requested final balance: Z_0

The nomenclature to follow is shown. Use the states in the attached diagram, adding more if necessary or leaving blank those that are not needed.

Solution:



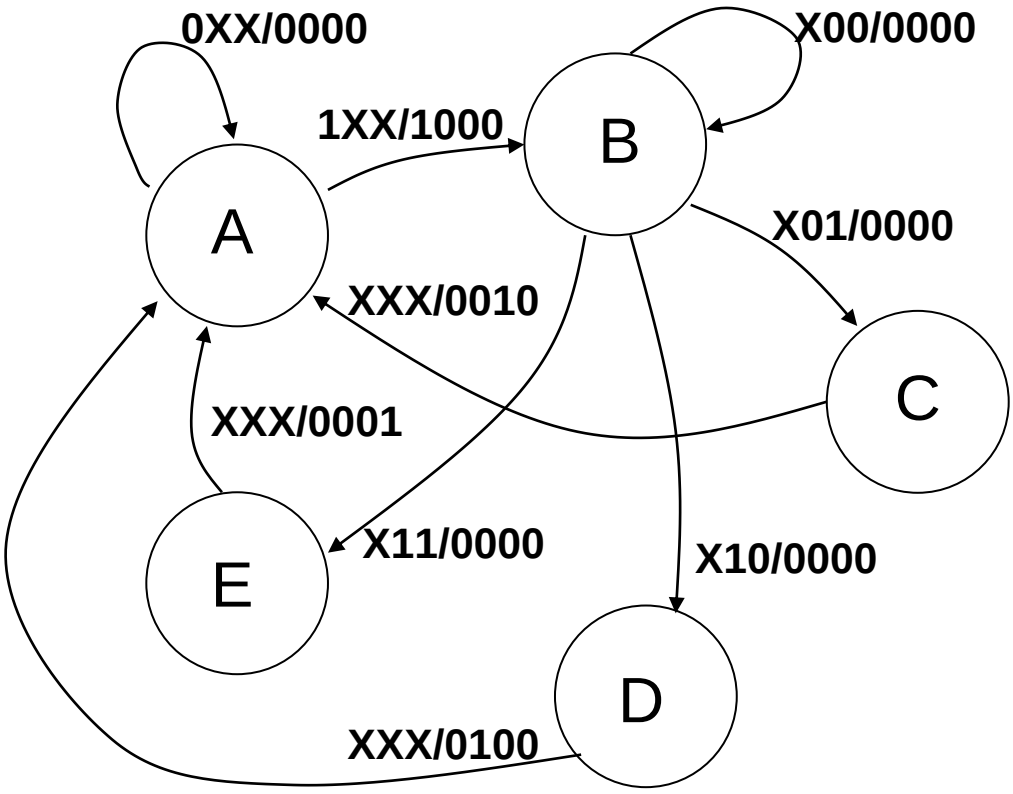
FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.26. Make a Mealy machine that controls the operation of an ice cream vending machine. The entries will be denoted with Xi and the Outputs with Zi. The machine, after inserting a coin of the unique value (X1), ejects a cone (Z1). After that, it gives the user the possibility to choose a strawberry (Z2), chocolate (Z3) or strawberry and chocolate (Z4) ice cream. For this the customer must press the button corresponding to "strawberry flavor" (X2), "chocolate flavor" (X3), or both buttons if you want the mixed flavor ice cream. Once the flavor has been chosen, and after a waiting watch cycle (delay) to allow the user time to prepare, the ice cream is obtained by placing the cone under the dispenser.
In the same clock cycle that the ice cream dispenses, the system returns to the initial state and awaits a new client.

In a Mealy FSM, counting a clock cycle is equivalent to counting an additional active edge.

The nomenclature to follow is shown. Use the states in the attached diagram, adding more if necessary or leaving blank those that are not needed.

Solution:



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.27. The following table represents the state and output equations of a state machine. The state is defined by Q_2, Q_1 y Q_0, where A is the only input apart from the clock and the reset. The Outputs are X and Y:

a) Determine if the machine is Mealy or Moore, justifying the answer (there will be no qualification without justification).

b) Draw the state diagram using the states of the attached diagram, adding more if necessary or leaving blank those that are not needed.

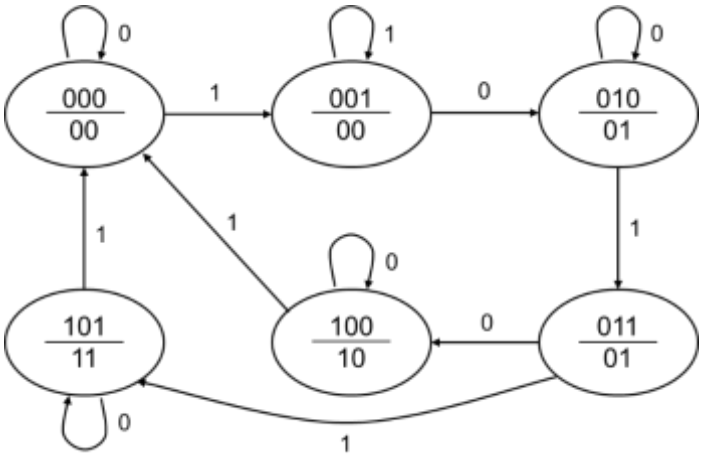
c) Q_0 is implemented with a T-type flip-flop. The minimized expression is requested as the sum of T0 and Y products.

PREVIOUS STATE (n)				NEXT STATE (n+1)				
Q_2	Q_1	Q_0	A	Q'_2	Q'_1	Q'_0	X	Y
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0	0
0	0	1	1	0	0	1	0	0
0	1	0	0	0	1	0	0	1
0	1	0	1	0	1	1	0	1
0	1	1	0	1	0	0	0	1
0	1	1	1	1	0	1	0	1
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1	1
1	0	1	1	0	0	0	1	1

Solution:

a) Moore, since in all the states the Outputs are the same regardless of the input.

b)



c)

$$T0 = \overline{Q_2}\ \overline{Q_0}\ A + \overline{Q_2}\ Q_0\ \overline{A} + Q_2\ Q_0\ A$$

$$Y = Q_1 + Q_2\ Q_0$$

FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.28. The following table represents the state and output equations of a state machine. The state is defined by Q_2, Q_1 y Q_0, where A and B are the inputs apart from the clock and the reset. The output is Z. The combinations not defined in the table are impossible combinations, which must be used to minimize the circuit.:

a) Determine if the machine is Mealy or Moore, justifying the answer (there will be no qualification without justification).

b) Minimized expression as **the sum of Z products**.

c) If Q_0 is implemented with a flip-flop type D, minimized expression as **a product of sums** of theD_0.

Current State					Next State			
Q_2	Q_1	Q_0	A	B	Q'_2	Q'_1	Q'_0	Z
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	1	0	1
0	0	1	0	0	0	0	1	1
0	0	1	0	1	0	1	0	0
0	0	1	1	0	0	1	0	1
0	1	0	0	0	0	1	0	1
0	1	0	0	1	0	1	1	1
0	1	0	1	0	0	1	1	1
0	1	1	0	0	0	1	1	1
0	1	1	0	1	1	0	0	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	1
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1

Solution:

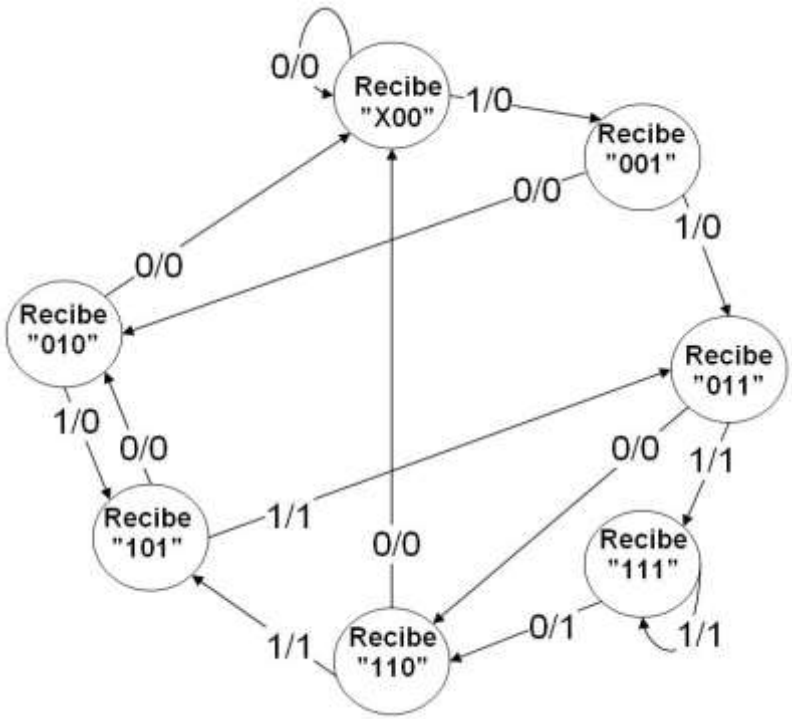
a) Mealy, since in some states (001, 011 and 100) the output varies with the entries**.**

b) $Z = \overline{B} + \overline{Q_2}\ \overline{Q_0}$

c) $D_0 = (Q_0 + A + B)\ (\overline{Q_0} + \overline{B})\ (Q_1 + \overline{A})$

U4.29. A team of engineers has developed a digital device capable of measuring heart beats. When the number of pulses is greater than a certain threshold value, the output of the device is set to "1", remaining at "0" below said threshold. The output of the device is synchronized with a clock signal, so that normal cycles (output 0) and stress cycles (output 1) can be defined. A team of doctors has come to the conclusion that for an athlete to face a decisive match these conditions must be fulfilled, in a previous training, for every 4 clock cycles, the number of cycles of excess should not exceed the normal cycles.
Using the synchronized digital output of the described apparatus as input, design a Mealy circuit that informs the coach about the pace of effort of their players. The circuit must have an entry that must be activated in case the medical criterion is not met. That is, the output must be set to 1 if during 4 cycles in the input there have been more ones than zeroes (and it is set to one as soon as three "1" are reached even though all four cycles have not been completed).
Design the state diagram using the necessary states of the attached diagrams, adding more if necessary or leaving blank those that are not needed.

Solution:



FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.30. The following table represents the state and output equations of a state machine. The state is defined by Q_2, Q_1 y Q_0, where A is the only input apart from the clock and the reset. The output is X:

a) Determine if the machine is Mealy or Moore, justifying the answer (there will be no qualification without justification).

b) Draw the state diagram using the states of the attached diagram, adding more if necessary or leaving blank those that are not needed.

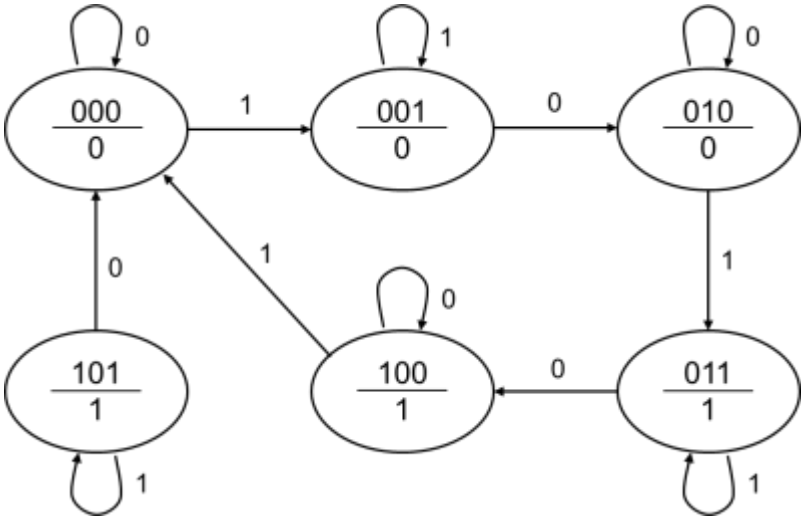
c) Q_0 is implemented with a T-type flip-flop. The minimized expression is requested as the sum of products of T0 and X.

CURRENT STATE (n)				NEXT STATE (n+1)			
Q_2	Q_1	Q_0	A	Q'_2	Q'_1	Q'_0	X
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	1	0	0	1
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	1	0	1	1

Solution:

a) Moore, since in all the states the Outputs are the same regardless of the input.

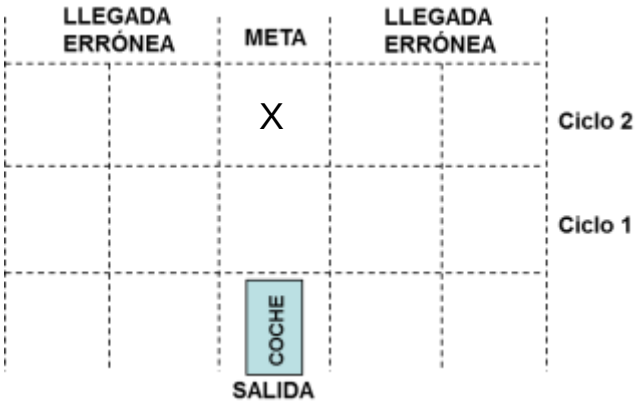
b)



c) $T_0 = \overline{Q_2}\ \overline{Q_0}\ A + Q_0\ \overline{A}$; $X = Q_2 + Q_1\ Q_0$

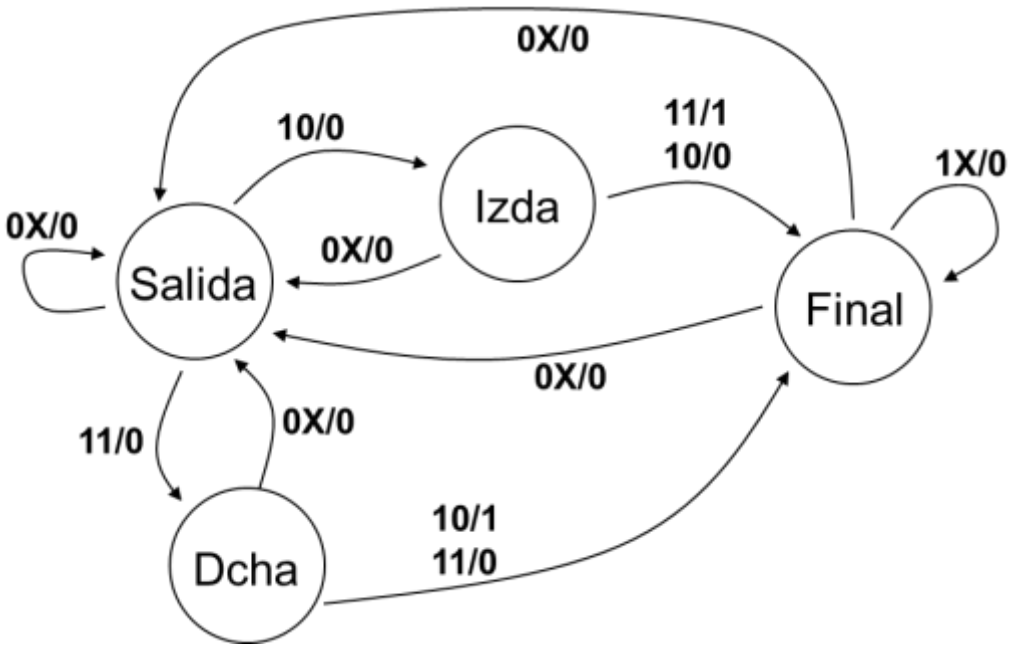
FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.31. An automaton is designed using a Mealy machine, a simple simulator for a car that moves along a lane. The system has two data entries. One of them, x1, set to "0" causes the car to return to the starting position while "1" makes the car move forward. The other entry, x2, set to "0" causes the front wheels of the car to move to the left, while "1" causes the front wheels to move to the right.
When the car advances with the wheels turned in one direction during a clock cycle, it moves to the right or left lane, depending on the direction of rotation. In order for the car to reach the goal, it must advance two clock cycles with the correct turns of wheels. The automaton output, z, is set to "1" during a single cycle when the car reaches the finish line (box X). After that, the car must be returned to the place of departure (it does not do it alone) to make a new simulation, just as if it arrives incorrectly at the end (erroneous arrival).



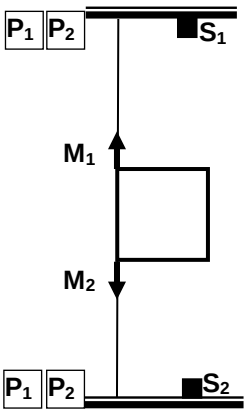
The nomenclature to follow is: x1x2 / z. Make the state diagram using the necessary states of the attached diagram, adding more if necessary or leaving blank those that are not needed.

Solution:



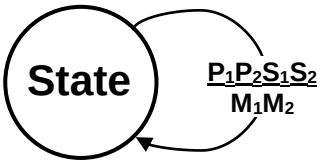
FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

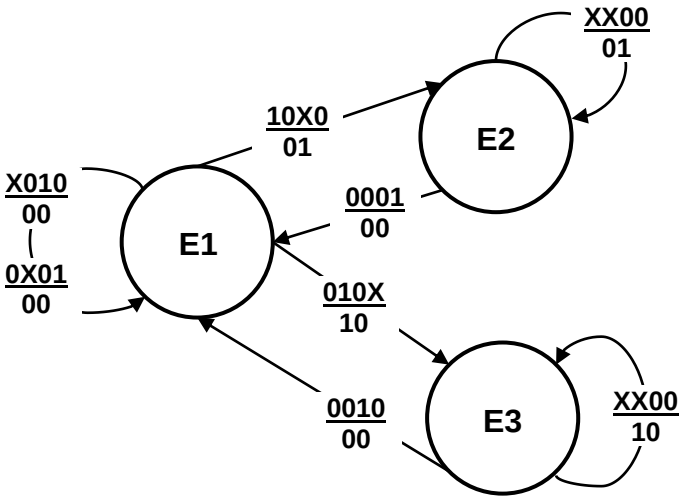
U4.32. We want to design a Mealy state machine that controls a system of a lift elevator used to communicate the kitchen (below) with the dining room (above) in a restaurant setting. The system has two buttons P1 and P2, to send the forklift to the kitchen or dining room respectively. Depending on the button, the control system activates the corresponding motor M1 (up) or M2 (down). The presence of two other sensors S1 (in the dining room) and S2 (in the kitchen), serve to indicate that the desired destination has been reached. Once the forklift is in operation, the system does not obey the buttons P1 and P2, until it reaches its destination indicated by S1 or S2. Once the forklift has reached the dining room or kitchen, the movement to that stay is disabled.



Design the state diagram, only for cases that make sense and / or are really possible.

Solution:





E1: The forklift is stopped (kitchen or dining room).

E2: The forklift is going down to the kitchen.

E3: The forklift is going up towards the dining room.

FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.33. The attached table represents the transition table of an FSM configured with 5 states represented by $Q_2Q_1Q_0$, a single input X and two Outputs Z_1 and Z_0.

CURRENT STATE			NEXT STATE $Q_2^{n+1}\,Q_1^{n+1}\,Q_0^{n+1}$ // OUTPUTS $Z_1\,Z_0$	
Q_2^n	Q_1^n	Q_0^n	X = 0	X = 1
0	0	0	1 1 0 // 0 0	1 0 1 // 0 0
1	0	0	1 1 0 // 1 0	1 0 1 // 1 0
1	0	1	1 0 0 // 0 1	1 1 1 // 0 0
1	1	0	1 1 0 // 0 1	0 0 1 // 0 1
1	1	1	1 0 0 // 1 1	0 0 0 // 1 1

Note: Consider the states not included in the table as unspecified states, which under any circumstances the system can reach.

a) Implement the transition equations of the three flip-flops assuming that Q_2 is an FF-JK, Q_1 is an FF-T and Q_0 is FF-D.

Solution:

Q_0X / Q_2Q_1	00	01	11	10
00	1	1	X	X
01	X	X	X	X
11	x	x	x	x
10	x	x	x	x

$J_2 = 1$

Q_0X / Q_2Q_1	00	01	11	10
00	x	x	X	X
01	X	X	X	X
11	0	1	1	0
10	0	0	0	0

$K_2 = Q_1X$

Q_0X / Q_2Q_1	00	01	11	10
00	1	0	X	X
01	X	X	X	X
11	0	1	1	1
10	1	0	1	0

$T_1 = \overline{Q_1}\ \overline{Q_0}\ \overline{X} + Q_1X + Q_1Q_0 + Q_0X$

Q_0X / Q_2Q_1	00	01	11	10
00	0	1	X	X
01	X	X	X	X
11	0	1	0	0
10	0	1	1	0

$D_0 = \overline{Q_0}\,X + \overline{Q_1}\,X$

b) Implement the output equations Z_1 and Z_0.

Q_0X / Q_2Q_1	00	01	11	10
00	0	0	X	X
01	X	X	X	X
11	0	0	1	1
10	1	1	0	0

$Z_1 = Q_2\,\overline{Q_1}\ \overline{Q_0} + Q_1Q_0$

Q_0X / Q_2Q_1	00	01	11	10
00	0	0	X	X
01	X	X	X	X
11	1	1	1	1
10	0	0	0	1

$Z_0 = Q_0\,\overline{X} + Q_1$

c) Indicate if it is a WSF of Moore or Mealy necessarily justifying the answer

It is a Mealy FSM because the output (Z_0) depends on the input as shown in the equation of the previous section.

FUNDAMENTOS DE COMPUTADORES
EJERCICIOS U4: Circuitos Secuenciales

U4.34. The attached table represents the transition table of an FSM configured with 5 states represented by $Q_2Q_1Q_0$, a single input X and two outputs Z_1 y Z_0.

CURRENT STATE			NEXT STATE $Q_2^{n+1}\,Q_1^{n+1}\,Q_0^{n+1}$ // OUTPUTS $Z_1\,Z_0$	
Q_2^n	Q_1^n	Q_0^n	X = 0	X = 1
0	0	0	0 1 0 // 0 0	0 0 1 // 0 0
0	0	1	1 0 0 // 0 0	0 0 1 // 1 0
0	1	0	1 0 0 // 0 0	0 0 1 // 0 0
0	1	1	1 0 0 // 0 1	0 0 0 // 0 1
1	0	0	0 1 0 // 1 1	0 0 1 // 1 1

Note: Consider the states not included in the table as unspecified states, which under any circumstances the system can reach.

a) Implement the transition equations of the three flip-flops assuming that Q_2 is an FF-JK, is an FF-T and Q_0 is an FF-D.

Solution:

Q_0X / Q_2Q_1	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	X	X	X	X
10	x	x	X	X

$J_2 = Q_1\,\overline{X} + Q_0\,\overline{X}$

Q_0X / Q_2Q_1	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	X	X	X	X
10	1	1	X	X

$K_2 = 1$

Q_0X / Q_2Q_1	00	01	11	10
00	1	0	0	0
01	1	1	1	1
11	X	X	X	X
10	1	0	X	X

$T_1 = \overline{Q_0}\;\overline{X} + Q_1$

Q_0X / Q_2Q_1	00	01	11	10
00	0	1	1	0
01	0	1	0	0
11	X	X	X	X
10	0	1	X	X

$D_0 = \overline{Q_0}\,X + \overline{Q_1}\,X$

b) Implement the output equations Z_1 y Z_0.

Q_0X / Q_2Q_1	00	01	11	10
00	0	0	1	0
01	0	0	0	0
11	X	X	X	X
10	1	1	X	X

$Z_1 = \overline{Q_1}\,Q_0X + Q_2$

Q_0X / Q_2Q_1	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	X	X	X	X
10	1	1	X	X

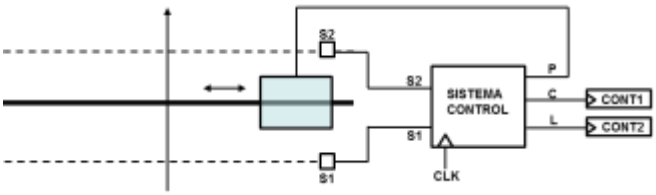
$Z_0 = Q_1Q_0 + Q_2$

c) Indicate if it is a Moore or Mealy FSM, necessarily justifying the answer

It is a Mealy FSM because the output (Z_1) depends on the X input, as shown in the equation of the previous section

Computer Basics
U4 EXERCISES: Sequential Systems

U4.35. We want to design the control system of a sliding door of a warehouse that opens and closes automatically when passing vehicles (see figure). The operation of the system is as follows:



- Vehicles travel exclusively in the direction and direction indicated by the vertical arrow, at the same constant speed and always maintain a distance of 4 m or more between them.
- Two infrared sensors, S1 and S2, separated by a distance of 4 meters, detect when a vehicle is on the front and back lines of the door respectively (broken lines), generating an output of value "1" as long as it is detected the vehicle.
- The door opens when a vehicle reaches the line of S1 and closes when it passes (stops detecting) the line of S2.
- The door motor is controlled by the signal P, so that it opens for P = 1 and closes for P = 0, the motor stops automatically when the door reaches the open position (P = 1) or closed (P = 0).
- We want to count how many vehicles pass through the door of length less than 4 meters and of length greater than or equal to 4 meters, for which the counters CONT1 and CONT2 respectively are used, connected as shown in the figure.

It is requested to design the control system of the door that receives the inputs S1 and S2 of the sensors and produces the Outputs P, C and L for the correct functioning of the system, using a Moore machine.

The initial asynchronous reset also serves to initialize both counters. It is noted that the counters are activated with signals C and L per rising edge.

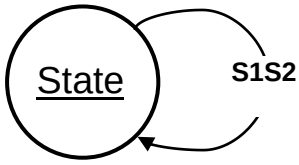
Design only the cases that are really possible for the tickets.

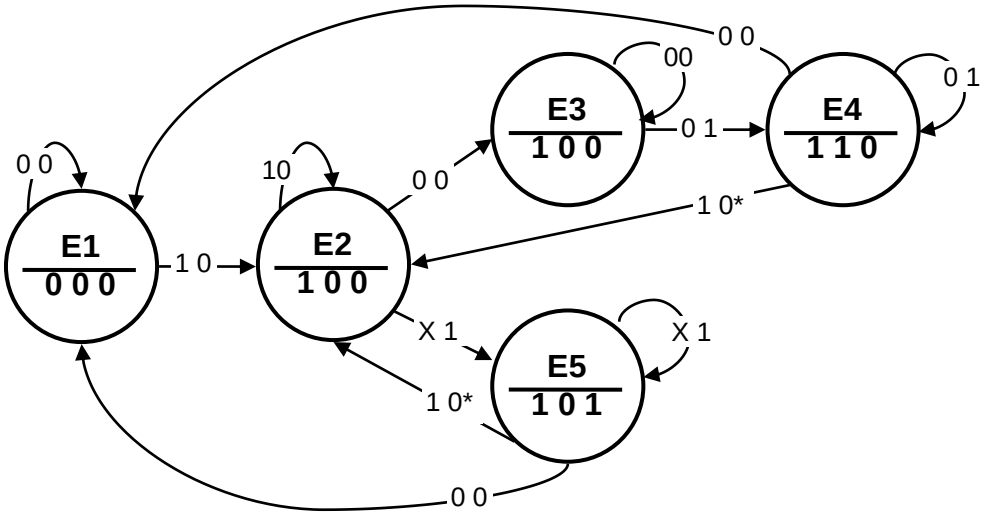
Solution:

E1: Start, waiting for a new vehicle

E2: The S1 sensor detects a vehicle.

E3: The S1 sensor loses the vehicle but the S2 has not yet captured it, it is short, but it does not count yet.





E4: The sensor S2 detects the lost vehicle by S1. Count a unit < 4 m.

E5: The sensor S2 detects a car but the S1 continues to detect it (11) or has just lost it (01). Count a unit ≥ 4 m.

* This case contemplates the arrival of a new vehicle just 4 meters from the previous one (rare but possible)

Computer Basics
U4 EXERCISES: Sequential Systems

U4.36. The table below represents the transition table of an FSM configured with 4 states represented by Q_1Q_0, a single output Z and two inputs X_1 y X_0:

CURRENT STATE		NEXT STATE: $Q_1^{n+1}\,Q_0^{n+1}$ // OUTPUT Z			
Q_1^n	Q_0^n	$X_1X_0 = 0\,0$	$X_1X_0 = 0\,1$	$X_1X_0 = 1\,0$	$X_1X_0 = 1\,1$
0	0	0 1 // 0	1 1 // 0	0 1 // 0	0 1 // 0
0	1	1 0 // 0	0 0 // 0	0 1 // 0	1 1 // 0
1	0	1 0 // 1	1 1 // 1	1 1 // 1	1 0 // 1
1	1	0 1 // 0	1 1 // 0	0 1 // 0	1 0 // 0

a) Indicate if it is a Moore or Mealy FSM.

It is a Moore type FSM since the output ($Z = Q_1\,\overline{Q_0}$) doesn't depend on any input.

b) Write the equations for the state transition (excitation equation), Q1, assuming FF-JK

X_1X_0 / Q_1Q_0	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	X	X	X	X
10	X	X	X	X

X_1X_0 / Q_1Q_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	1	0	0	1
10	0	0	0	0

it is an

$J_1 = Q_0\,\overline{X_1}\,\overline{X_0} + Q_0\,X_1\,X_0 + \overline{Q_0}\,\overline{X_1}\,X_0$

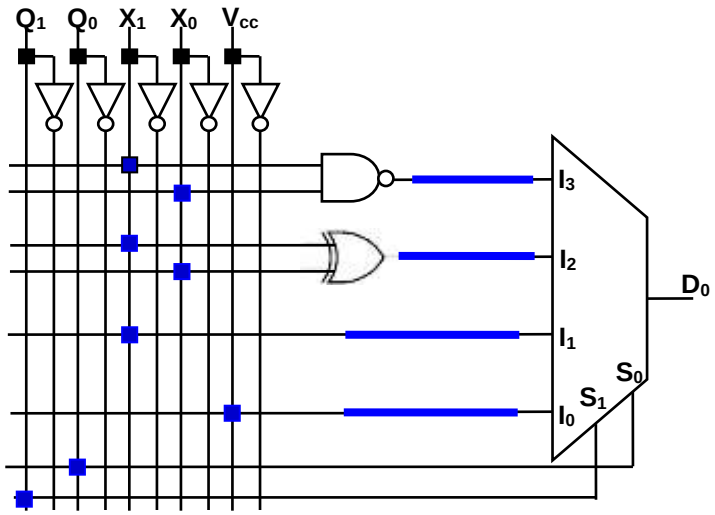
$K_1 = Q_0\,\overline{X_0}$

X_1X_0 / Q_1Q_0	00	01	11	10	
00	1	1	1	1	$\rightarrow I_0$
01	0	0	1	1	$\rightarrow I_1$
11	1	1	0	1	$\rightarrow I_3$
10	0	1	0	1	$\rightarrow I_2$

c) Write the equation for the state transition (excitation equation), for flip-flop Q_0, assuming it is an FF-D. Draw (implement) said equation using multiplexer 4-1 of the attached figure and the minimum number of necessary logic gates chosen among those indicated in the diagram.

$$D_0 = \overline{Q_1}\,\overline{Q_0} + \overline{Q_1}\,X_1 + X_1\,\overline{X_0} + Q_1\,\overline{X_1}\,X_0 + Q_1\,Q_0\,\overline{X_1} =$$

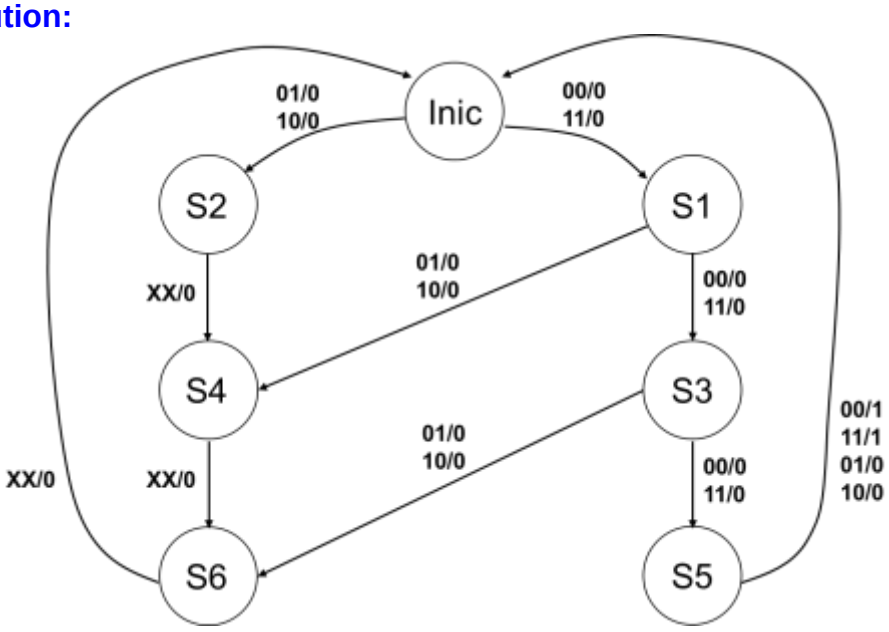
$$= (\overline{Q_1} + Q_0 + X_1 + X_0)\,(Q_1 + \overline{Q_0} + X_1)\,(\overline{Q_1} + \overline{X_1} + \overline{X_0})$$

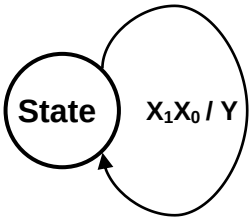


U4.37. Design a circuit, using a Mealy automaton, which compares serial entries of four-bit packets in two channels and which provides an output 1 when the four bits of each packet match. Therefore, we will have two inputs X_1 y X_0 that are accepting the bits one by one in each clock cycle and when the fourth bit is reached the system produces an output Y = 1 if the four bits received in the two channels match, being the Y = 0 in the remaining cases. Once the reading of the four bits is completed, it starts with four others and so on. For example:

$X_1 \rightarrow$ 0111 0101 1110…
$X_0 \rightarrow$ 0101 0101 1000…
Y $\rightarrow$ 0000 0001 0000…

Solution:





Start: Initial state without memory, waiting for the 1st bit of 4

S1: Received 1st bit, both are equal.

S2: Received 1st bit, they are different numbers.

S3: Received 2nd bit, until now they are equal numbers.

S4: Received 2nd bit, they are different numbers.

S5: Received 3rd bit, until now they are equal numbers.

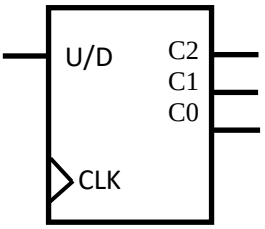
S6: Received 3rd bit, they are different numbers.

Computer Basics
U4 EXERCISES: Sequential Systems

U4.38. We want to design a 3-bit number cyclic counter with the following characteristics:

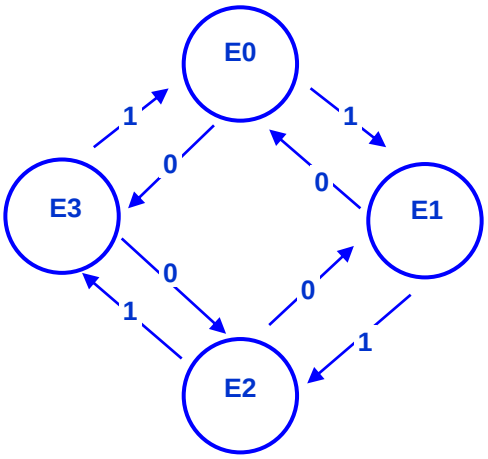
- Only counts prime numbers. (With three bits will be 2, 3, 5 and 7)
- It has a synchronous input, called U / D, which allows you to select whether it counts up (U / D = 1) or descending (U / D = 0)
- The output is updated only with the rising edges of the clock
- If you were in a state that does not belong to the sequence, the next state would be the closest prime number, depending on the value of U / D.

a) Represent the state diagram (the use of the smallest number of states will be assessed).
b) Design the counter, using the lowest number of FF type D possible. It is only necessary to indicate the state equations of each flip-flop and the output equations, it is not necessary to draw the resulting scheme.



Solution:

The sequence of numbers to count, that is, the prime numbers, are 2, 3, 5 and 7. Since the different states are 4, one for each number, they can be encoded with only 2 FF. With 2 FF, there are only possible combinations table, so the system can never fall into a state that represents a number that is not prime, that is, it is not necessary to design an anti-blocking system. On the other hand, in order to generate the counter output, the states must be decoded.



Assignment and codification of the states:

Name	Coding	Output value
E0	00	010 (2)
E1	01	011 (3)
E2	10	101 (5)
E3	11	111 (7)

Current Input and State			Current State		Outputs		
U/D	Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	C2	C1	C0
0	0	0	1	1	0	1	0
0	0	1	0	0	0	1	1
0	1	0	0	1	1	0	1
0	1	1	1	0	1	1	1
1	0	0	0	1	0	1	0
1	0	1	1	0	0	1	1
1	1	0	1	1	1	0	1
1	1	1	0	0	1	1	1

Since the counter is implemented with FF type D, the state equations match those of the Next State:

$$D_1 = Q_1^{n+1} = \sum m\,(0,3,5,6) = \overline{U/D}\,.\,\overline{Q_1}\,.\,\overline{Q_0} + \overline{U/D}\,.Q_1.Q_0 + U/D.Q_1.\overline{Q_0} + U/D.\overline{Q_1}\,Q_0$$

$$D_0 = Q_0^{n+1} = \overline{Q_0}$$

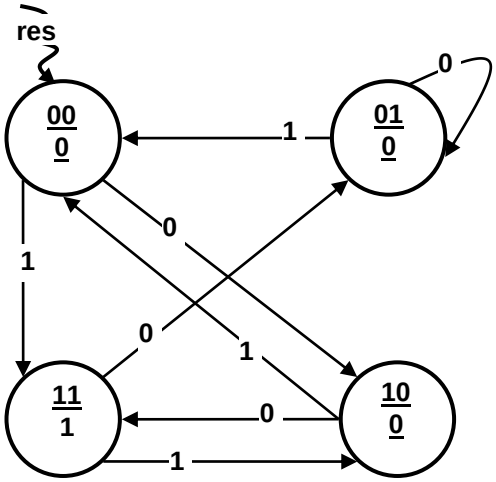
$$C_2 = Q_1^n \qquad C_1 = \overline{Q_1^n} + Q_0^n \qquad C_0 = Q_1^n + Q_0^n$$

NOTE:
This exercise can also be done using three FFs and sending the states that do not belong to the sequence to the nearest prime number, according to the statement. In this case it would not be necessary to decode the state, since it could be directly the exit of the counter. This Solution would not be optimal, since it does not use the minimum number of flip-flops, although it has also been taken into account in the correction.

Computer Basics
U4 EXERCISES: Sequential Systems

U4.39. The attached state diagram represents a Moore FSM. Knowing that for each state the values of the variables Q_1Q_0 / Z are indicated:

- **a.** Draw the corresponding transition and state table.
- **b.** Find the excitation equations for each FF, assuming that Q1 is an FF-D, while Q0 is an FF-JK and the equation for the output function Z.
- **c.** Draw the circuit for Q1 using a MUX 4-1, with the variables Q1Q0 as control signals, taking Q1 as the most significant.



Solution:

a)

Current state		Next state: $Q_1^{n+1}\,Q_0^{n+1}$		OUTPUT Z
Q_1^n	Q_0^n	X = 0	X = 1	
0	0	1 0	1 1	0
0	1	0 1	0 0	0
1	0	1 1	0 0	0
1	1	0 1	1 0	1

b)

Q_1Q_0 \ X	0	1
00	1	1
01	0	0
11	0	1
10	1	0

$D_1 = \overline{Q_1}\,\overline{Q_0} + Q_0\,\overline{X} + Q_1Q_0X$

Q_1Q_0 \ X	0	1
00	0	1
01	X	X
11	X	X
10	1	0

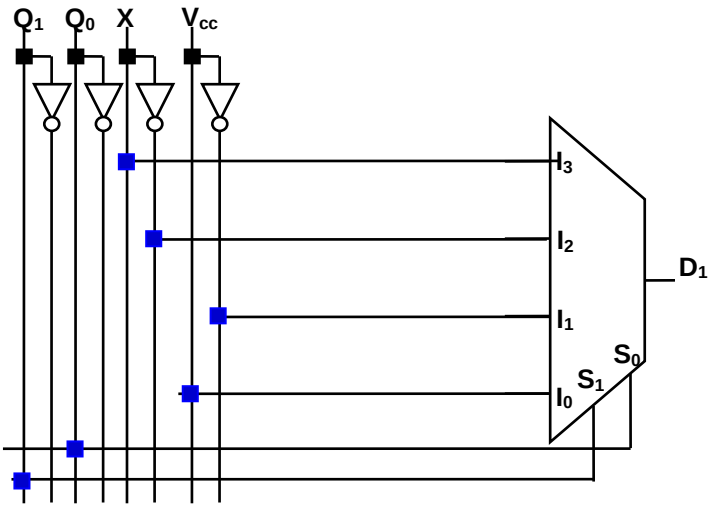
$J_0 = Q_1\,\overline{X} + \overline{Q_1}\,X$

Q_1Q_0 \ X	0	1
00	X	X
01	0	1
11	0	1
10	X	X

$K_0 = X$

$Z = Q_1\,Q_0$

c)

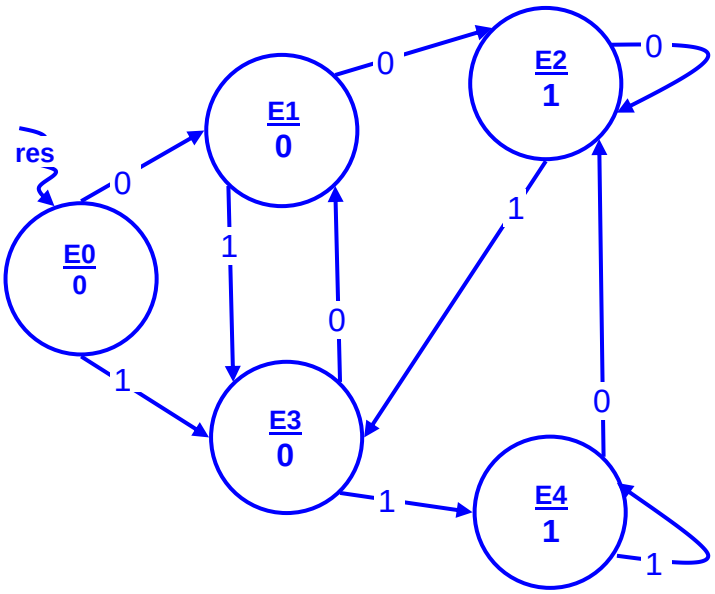


Computer Basics
U4 EXERCISES: Sequential Systems

U4.40. Design a) a Moore FSM; b) a Mealy FSM, for a system that has a single data entry in X series, and a single Z output. The FSM is a sequence detector that activates the output (Z = '1'), when the two previous values of the input were either '1' or two '0', otherwise the output remains inactive (Z = '0').

Solution :

a) Moore FSM



E0: Initial state after reset. State without previous memory

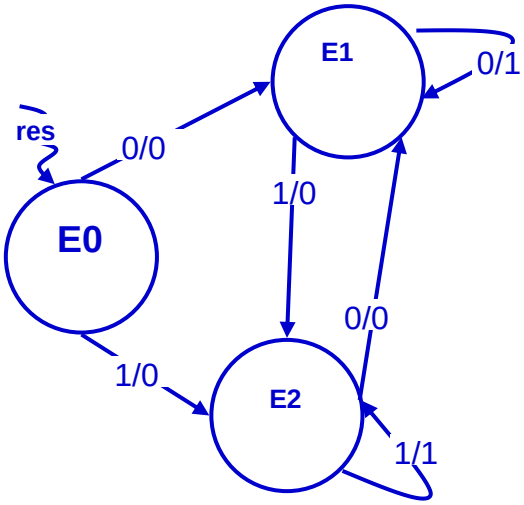
E1: Receive a first '0'

E2: Receive a second consecutive '0', exit at '1'

E3: Receive a first '1'

E4: Receive a second consecutive '1', exit at '1'

b) Mealy FSM



E0: Initial state after reset. State without previous memory

E1: Receive a first '0', successive and consecutive zeros, exit 1

E2: Receive a first '1', successive and consecutive, exit to 1

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U4 EXERCISES: Sequential Systems

U4.41. Table 1 shows the state transition of a specific finite state machine (FSM), whose five states are represented by the values given for Q2Q1Q0. The table also includes the value of the only input X and its two associated Outputs Z1 and Z0.

a) Find the excitation equation (minimum) for flip-flop FF2, if it is assumed to be D-type.
b) Find the (minimum) excitation equations for flip-flop FF0, if it is assumed to be JK-type.
c) Indicate if the FSM is of the Moore or Mealy type, **justifying your answer**.

Current state				Next State			Outputs	
Q_2^n	Q_1^n	Q_0^n	X	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Z_1	Z_0
0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	1	1	0
0	0	1	0	0	1	0	0	1
0	0	1	1	0	1	1	0	1
0	1	0	0	1	0	0	0	0
0	1	0	1	1	0	1	0	0
1	0	0	0	0	0	1	1	0
1	0	0	1	0	0	0	1	1
1	0	1	0	0	0	1	0	0
1	0	1	1	1	0	0	0	0

SOLUTION:

a) $D_2 = \overline{Q_2}\ \overline{Q_0}\ X + Q_2\ Q_0\ X + Q_1$

b) $J_0 = \overline{Q_2}\ X + Q_2\ \overline{X}$

$K_0 = Q_2\ X + \overline{Q_2}\ \overline{X}$

c) It is a Mealy FSM, as can be seen from the output Z0, where for the state Q2 = '1', Q1 = '0' and Q0 = '0', the value of the output Z0 changes depending on the input X.

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U4 EXERCISES: Sequential Systems

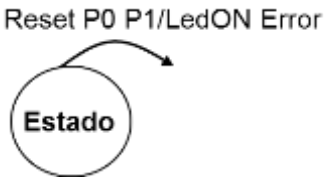
U4.42. We want to design an FSM that detects a sequence of key presses, specifically the sequence 0-1-0. For this, there are two buttons, P0 and P1. P0 is the button used to enter the "0" and P1 is used to enter the "1". The system will also have a synchronous reset input with the clock signal, so that each time this input is activated it will return to the initial state.

The FSM will have two outputs: **Led-ON** "that will be activated (will be" 1 ") when the searched sequence is detected and **Error**, which will only be activated when P0 and P1 are pressed at the same time, remaining in this case in the Current state.

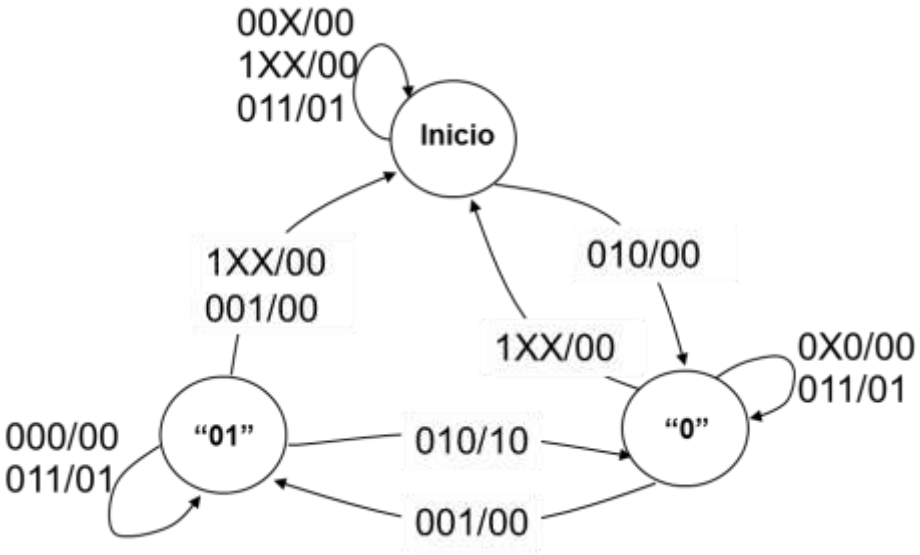
Overlapping sequences will be allowed.

Design the state diagram using the necessary states of the attached diagram, adding more if necessary or leaving blank those that are not needed.

The nomenclature to follow is:



SOLUTION:



Start: Initial state or "Without Relevant Memory"

"0": A zero (valid) has been received as the first digit

"01": One (valid) has been received as second digit

Computer Basics
U4 EXERCISES: Sequential Systems

U4.43. The following table shows the state transition of a specific finite state machine (FSM), whose states are represented by the values given for Q1Q0. The table also includes the values of the inputs E1E0 and their two associated Outputs Z1 and Z0.

a) Find the excitation equations (minimum) for flip-flop FF0, if it is assumed to be JK-type.
b) Indicate necessarily justifying the answer if the FSM is of the Moore or Mealy type.
c) Draw the state diagram for the FSM.

Note: It is NOT required to draw any type of circuit.

	$Q^{n+1}{}_1Q^{n+1}{}_0$ / Z_1Z_0		
$Q^n{}_1Q^n{}_0$	E_1E_0=0X	E_1E_0=10	E_1E_0=11
00	00/00	10/00	11/01
10	10/01	00/01	00/01
11	11/10	00/10	00/10

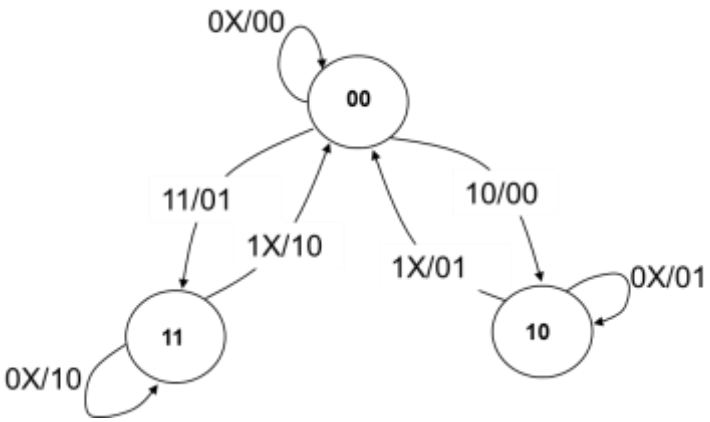
Solution

a) $J_0 = \overline{Q_1}\, E_1E_0$

$K_0 = E_1$

b) It is a Mealy FSM, as can be seen in the output Z0, where for the state Q1 = '0', Q0 = '0', the value of the output Z0 changes as a function of the inputs E1E0.

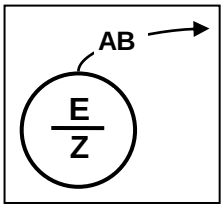
c)



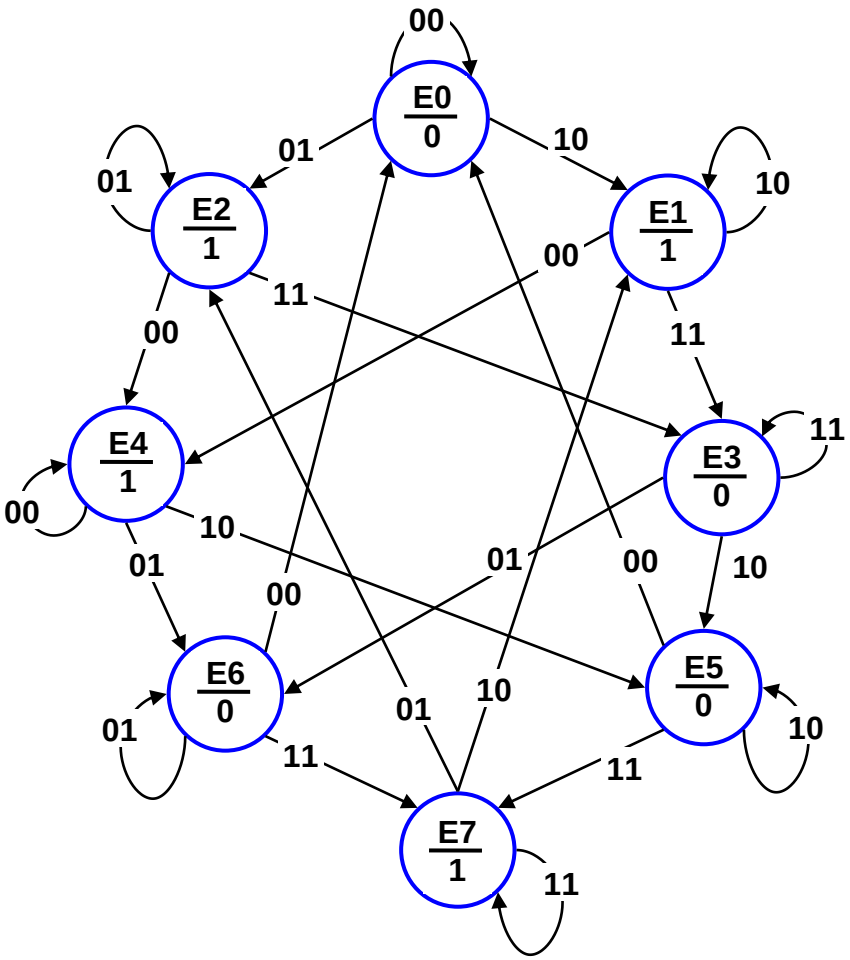
Computer Basics
U4 EXERCISES: Sequential Systems

U4.44. We want to design a finite Moore state machine, which serves to control the ignition system of the alarm light in a safety enclosure.

a. In two different places of the enclosure there are two buttons A and B, so that you can turn on and off the light from each one of them. Each button produces a logical '1' while it is pressed, and a logical '0' when it is not.
b. It is desired that, each time any button is pressed, the light (Z) changes state: if it is off, it must be turned on, and vice versa.
c. It must be taken into account the case in which, while pressing a button, you can press the other. For example, if the light is off, someone presses A to turn on the light. But if while pressing A someone press B, then the light will turn off again.
d. To reduce the number of transitions and thereby facilitate the design, it can be considered that the clock frequency is high enough so that a simultaneous state change of the two pushbuttons in the same clock cycle is impossible.



Solution



Design justification:

E0: A state OFF, B state OFF. Light off
E1: A state ON, B state OFF, Light on.
E2: A state OFF, B state ON. Light on.
E3: A state ON, B state ON. Light off.
E4: A state OFF, B state OFF. Light on.
E5: A state ON, B state OFF, Light off.
E6: A state OFF, B state ON. Light off.
E7: A state ON, B state ON. Light on.

Computer Basics
U4 EXERCISES: Sequential Systems

U4.45. The following table shows the state transition of a specific finite state machine (FSM), whose states are represented by the values given for Q2Q1Q0. The table also includes the values of the input E and its two associated Outputs Z1 and Z0.

a) Find the (minimum) excitation equations for flip-flop FF0, if it is assumed to be JK-type.
b) Find the excitation equation (minimum) for flip-flop FF1, if it is assumed to be T-type.
c) Signify necessarily justifying the answer if the FSM is of the Moore or Mealy type.
d) Using the attached diagram, draw the state diagram of the FSM.

Note: It is NOT required to draw any type of circuit.

	$Q^{n+1}_2Q^{n+1}_1Q^{n+1}_0$ / Z_1Z_0	
$Q^n_2Q^n_1Q^n_0$	E=0	E=1
000	010/01	011/01
010	110/00	011/00
011	010/00	111/00
110	110/10	011/10
111	110/11	111/11

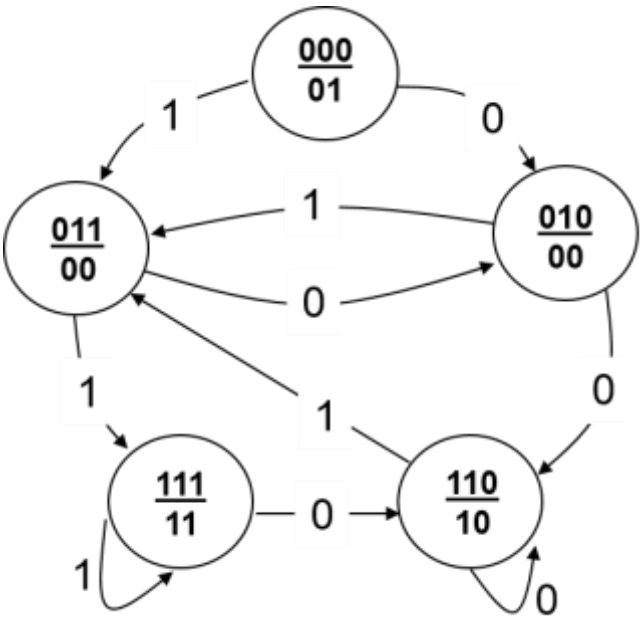
Solution

d) $J_0 = E$
$K_0 = \overline{E}$

e) $T_1 = \overline{Q_1}$

f) It is a Moore's FSM because, for each state, the two Outputs Z1Z0 do not depend on the E input, but only on the state they are in.

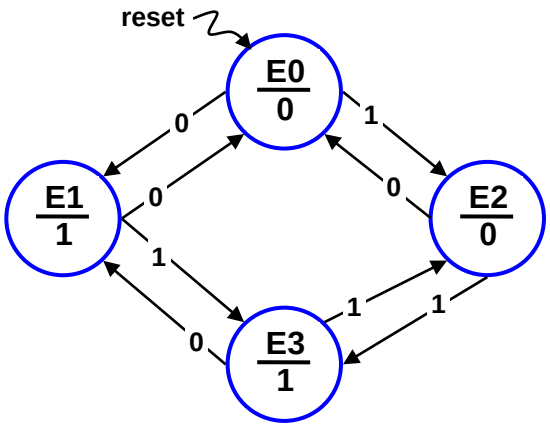
g)



Computer Basics
U4 EXERCISES: Sequential Systems

U4.46. It is requested to construct a finite state machine of Moore, which, from an initial value of reset, sequentially attends to a string of bits and complements the bits in the even position, without modifying the rest. That is, for a sequence of inputs b_0, b_1, b_2, b_3, b_4, b_5, b_6, etc..... the output must be $\overline{b_0}$, b_1, $\overline{b_2}$, b_3, $\overline{b_4}$, b_5, $\overline{b_6}$, etc... The operation must be maintained as long as a new reset is not pressed. It is requested to design the diagram of states of the FSM indicated.

Solution:



Design Justification:

E0: Initial state, receives a bit value '0' in odd order => the output is like the input.

E1: It receives a bit of value '0' in order par => the output is complement of the input.

E2: It receives a bit of value '1' in order par => the output is complement of the input.

E3: Receive a bit of value '1' in odd order => the output is like the input.

Computer Basics
U4 EXERCISES: Sequential Systems

U4.47. Given the attached transition table:

a. Calculate the transition equation for Q_1 assuming it is a JK type flip flop.

b. Indicate if it is a Moore or Mealy FSM, justify the answer.

CURRENT STATE		INPUTS		NEXT STATE		OUTPUTS	
Q^n_1	Q^n_0	X_1	X_0	Q^{n+1}_1	Q^{n+1}_0	Z_1	Z_0
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	0
1	0	0	0	0	0	0	1
1	0	0	1	1	0	0	1
1	0	1	0	1	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	0	1	0

Solution
a)

Table J_1

Q_1Q_0 \ X_1X_0	00	01	11	10
00	X	X	1	0
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

Table K_1

Q_1Q_0 \ X_1X_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	1	X	X
10	1	0	X	0

Excitation equations:

$J_1 = X_0$

$K_1 = \overline{Q_0}\,\overline{X_1}\,\overline{X_0} + Q_0X_0$

Transition equations: $Q_1^{n+1} = \overline{Q_1}\,J_1 + Q_1\overline{K_1}$ => $Q_1^{n+1} = \overline{Q_1}\,X_0 + Q_1\overline{(\overline{Q_0}\,\overline{X_1}\,\overline{X_0} + Q_0X_0)}$

$Q_1^{n+1} = Q_0\overline{X_0} + \overline{Q_0}\,X_0 + Q_1X_1$

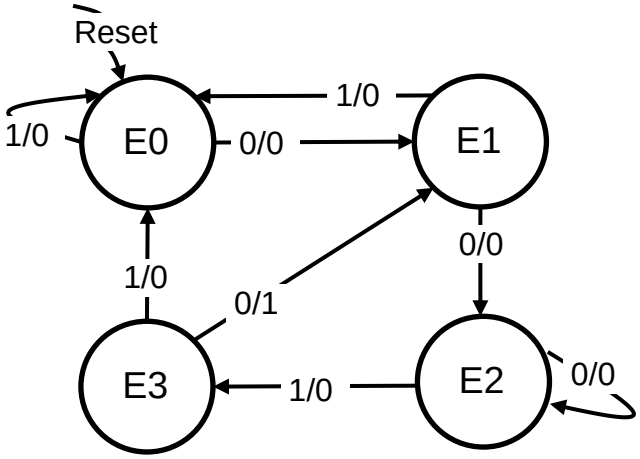
Note: The requested transition equation can be obtained directly, proposing a unique combinational logic function, that is, a single Karnaugh table: $Q_1^{n+1} = f(Q_1, Q_0, X_1, X_0)$

b) It is a Mealy FSM. The output Z_1 in the state $Q_1Q_0 = 00$, presents different values for different combinations of the inputs.

Computer Basics
U4 EXERCISES: Sequential Systems

U4.48. For a serial data input synchronized with a clock, it is expected to find the bit sequence "0010" with overlap. Design the state diagram of a Mealy finite state machine that serves to detect said binary sequence. Indicate briefly, i.e. in no more than one line, the meaning of each one of the defined states.

Solution



State description:

E0. No memory waiting for a valid first bit '0'.

E1. Find a valid first bit '0' in the sequence

E2. Find a second valid bit '00' in the sequence

E3. Find a third valid bit '001' in the sequence

Computer Basics
U4 EXERCISES: Sequential Systems

U4.49. Given the attached transition table for a given sequential circuit:

CURRENT STATE			INPUT	NEXT STATE			OUTPUT
Q^n_2	Q^n_1	Q^n_0	X_0	Q^{n+1}_2	Q^{n+1}_1	Q^{n+1}_0	Z_0
0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0
0	1	0	0	1	0	1	0
0	1	0	1	1	1	0	0
1	0	1	0	0	1	0	1
1	0	1	1	1	1	1	1
1	1	0	0	1	0	1	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	0	0	1

a. Calculate the **excitation equations** of flip-flop Q_0, assuming this is a flip-flop type J-K.

Karnaugh map for J_0

Q_2Q_1 \ Q_0X_0	00	01	11	10
00	0	0	X	X
01	1	0	X	X
11	1	0	X	X
10	X	X	X	X

Karnaugh map for K_0

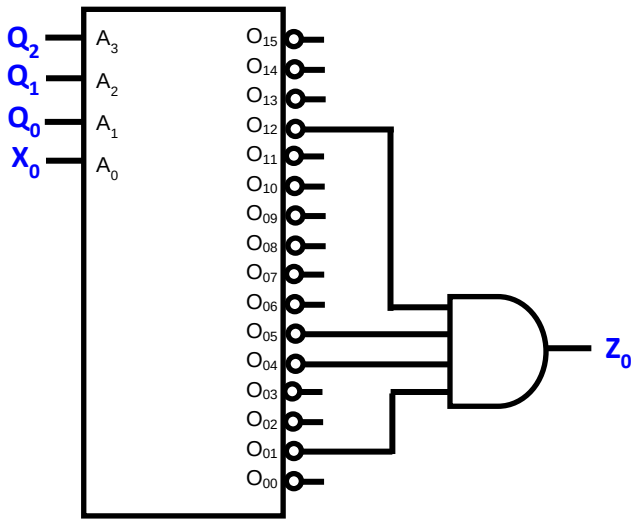
Q_2Q_1 \ Q_0X_0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	1	1
10	X	X	0	1

Excitation Equations:

$$J_0 = Q_1 \overline{X_0}$$

$$K_0 = Q_1 + \overline{X_0}$$

b. Implement the output equation Z0 using the decoder 4-16 of the attached figure, in which the Outputs are active in low. Use the necessary additional logical gates, but the use of the least number of gates with the least number of entries that are necessary will be valued.
NOTE: In the solution of the exercise, all the decoder inputs must be connected to some signal or value.



c. Indicate if it is a Moore or Mealy FSM, **justifying the answer necessarily**.

It is a Mealy FSM. The output Z_0 for the state $Q_2Q_1Q_0 = 000$ and $Q_2Q_1Q_0 = 110$, presents different values for the two values of the input, i.e. the output also depends on the value of the input.

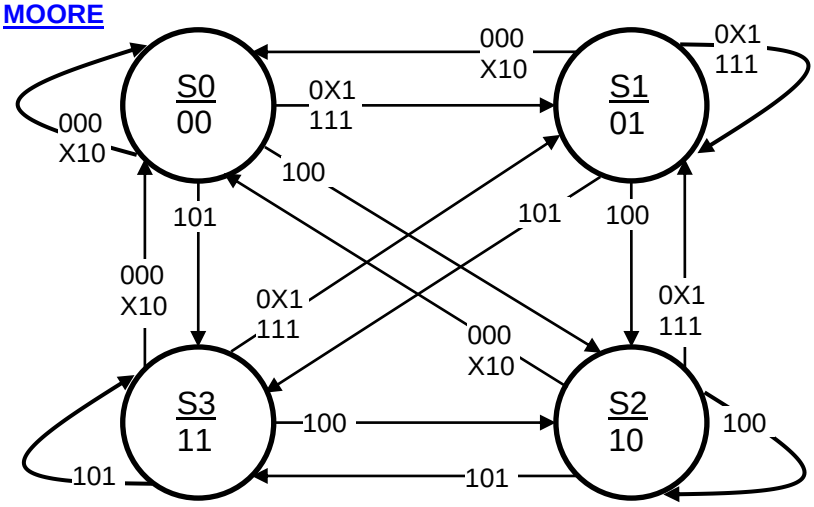
Computer Basics
U4 EXERCISES: Sequential Systems

U4.50. The aim is to design a sequential circuit that controls irrigation in a greenhouse. For this purpose, a series of sensors is available, which are:

- Humidity sensor (S_H). Placed on the ground, it is programmed to take a 1 if the humidity level of the earth is below a certain value and it is necessary to water. If it is at zero, it should not be watered.
- Temperature sensor (S_T). Placed inside the greenhouse, it is programmed to take a 1 if the temperature is below a certain value. In this case, it should NOT be irrigated due to freezing problems, regardless of the value of the humidity sensor.
- Light sensor (S_L). Placed outside the greenhouse, it is programmed so that its output is worth 1 if the solar illumination is below a certain value, in that case it will have to turn on an internal illumination of the greenhouse.

The Outputs of the circuit are the irrigation activation, R, and the lighting activation, L.
Only the design of the state diagram of the circuit is requested, for the two types of Moore and Mealy state machines. Indicate **necessarily** and briefly, a comment that helps to understand the meaning of each one of the defined states.
In the designs, indicate the variables in the declared order, i.e. SH ST SL for the sensors and R L for the outputs.

MOORE



In the Moore design, every possible state of the Outputs is associated with a single state. That is to say:

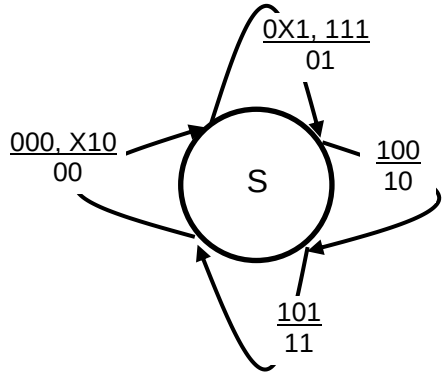
S0. There is neither Irrigation (**R**) nor **L**ight.

S1. There is no irrigation (**R**), but there is **L**ight.

S2. There is no **L**ight but there is Irrigation (**R**).

S3. There is Irrigation (**R**) and **L**ight

MEALY



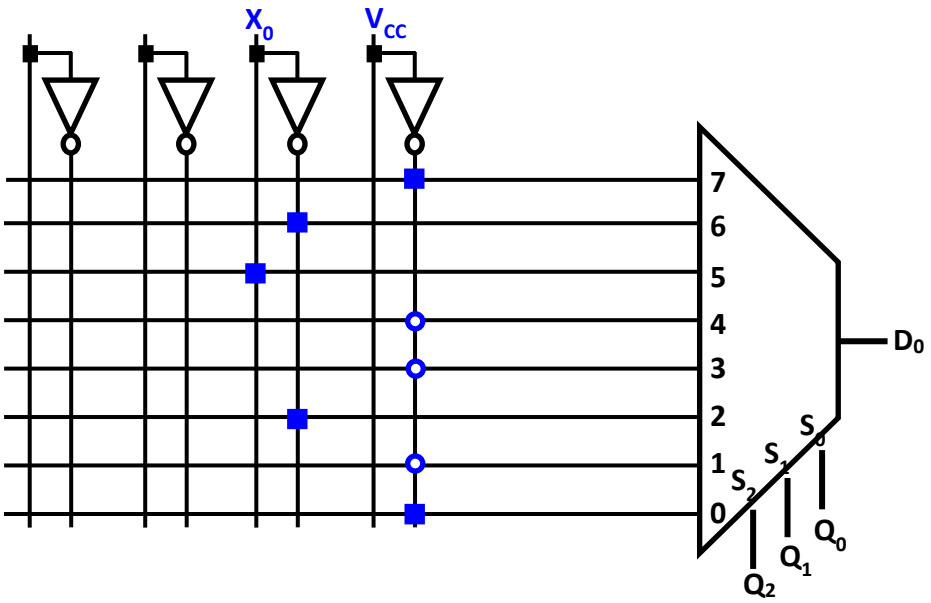
Both for the Moore and Mealy designs, in the proposed system, the Outputs do not depend on the previous state, but only on the value of the sensors, in this case the inputs to the system. For the Mealy design, with a single state it serves to solve the sequential circuit.

Computer Basics
U4 EXERCISES: Sequential Systems

U4.51. Given the attached transition table:

CURRENT STATE			INPUT	NEXT STATE			OUTPUT	
Q^n_2	Q^n_1	Q^n_0	X_0	Q^{n+1}_2	Q^{n+1}_1	Q^{n+1}_0	Z_1	Z_0
0	0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0	0
0	1	0	0	1	0	1	0	1
0	1	0	1	1	1	0	0	1
1	0	1	0	0	1	0	0	0
1	0	1	1	1	1	1	1	0
1	1	0	0	1	0	1	1	0
1	1	0	1	1	1	0	1	0
1	1	1	0	1	1	0	0	0
1	1	1	1	0	0	0	0	0

a. Using the minimum number of elements provided in the attached figure, implement the **excitation equation** of flip-flop Q_0, assuming it is a type D flip-flop.



Note: Circles can be connected indistinctly to GND or VCC.

b. Calculate the **transition equation** for Q_2 assuming it is a type T flip-flop. Use the attached table.

Karnaugh map for Q^{n+1}_2

Q_2Q_1 \ Q_0X_0	00	01	11	10
00	1	0	X	X
01	1	1	X	X
11	0	0	1	0
10	X	X	0	1

$$Q_2^{n+1} = Q_1Q_0X_0 + \overline{Q_2}\,\overline{X_0} + \overline{Q_1}\,\overline{X_0} + \overline{Q_2}Q_1$$

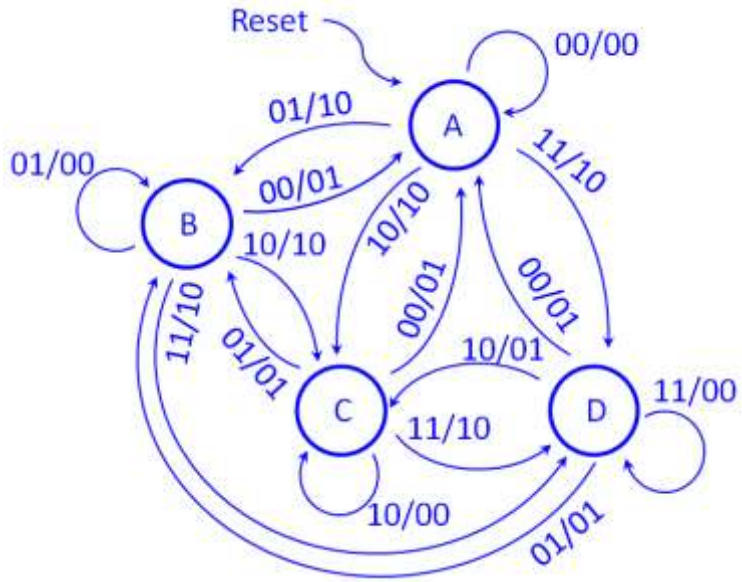
c. Indicate if it is a Moore or Mealy FSM, **justifying the answer necessarily**.

It is a Mealy FSM. The output Z_1 for the state $Q_1Q_1Q_0 = 101$, presents different values for the two values of the input, that is, the output also depends on the value of the input.

4.52. A sequential circuit has two inputs and two outputs. The inputs, A_1A_0, represent binary numbers of two bits that are introduced into the circuit synchronously with the clock signal. The Outputs are X_1X_0.

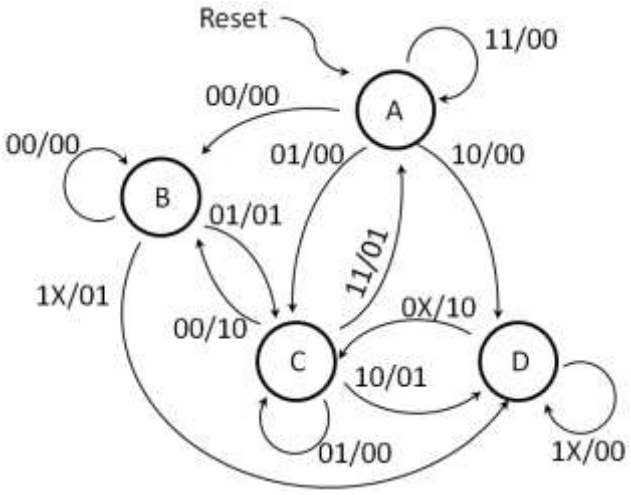
The circuit operates so that if the current number is less than the previous one, the output X_0 is activated ($X_0 = 1$), if it is greater, X_1 is activated ($X_1 = 1$) and in any other case both Outputs remain at zero.

Represent the state diagram of the machine described as a Mealy machine. Suppose that the initial state, after the reset, is interpreted as the last number that has arrived is $A_1A_0 = 00$. Make a brief description of the meaning of each of the states. Use the notation A_1A_0 / X_1X_0.



State A: The last number received was 00
State B: The last number received was 01
State C: The last number received was 10
State D: The last received number was 11

4.53. Given the state diagram represented in the figure on the right, obtain the table of state transitions, including the outputs. In this table, also represent the input functions of the flip-flops necessary to implement the circuit, with type JK containing the most weight status bit, type T being the least weight, and the rest of the student's choice, if any.



To represent the transitions table, the first thing to do is to code each state. This coding can be done any which way. Since there are four states, two bits are enough, which will correspond to both flip-flops, Q_1Q_0.
The chosen coding is:

State	Q_1	Q_0
A	0	0
B	0	1
C	1	0
D	1	1

Q_1	Q_0	X_1	X_0	Q^+_1	Q^+_0	Z_1	Z_0	J_1	K_1	T_0
0	0	0	0	**0**	**1**	**0**	**0**	**0**	**X**	**1**
0	0	0	1	**1**	**0**	**0**	**0**	**1**	**X**	**0**
0	0	1	0	**1**	**1**	**0**	**0**	**1**	**X**	**1**
0	0	1	1	**0**	**0**	**0**	**0**	**0**	**X**	**0**
0	1	0	0	**0**	**1**	**0**	**0**	**0**	**X**	**0**
0	1	0	1	**1**	**0**	**0**	**1**	**1**	**X**	**1**
0	1	1	0	**1**	**1**	**0**	**1**	**1**	**X**	**0**
0	1	1	1	**1**	**1**	**0**	**1**	**1**	**X**	**0**
1	0	0	0	**0**	**1**	**1**	**0**	**X**	**1**	**1**
1	0	0	1	**1**	**0**	**0**	**0**	**X**	**0**	**0**
1	0	1	0	**1**	**1**	**0**	**1**	**X**	**0**	**1**
1	0	1	1	**0**	**0**	**0**	**1**	**X**	**1**	**0**
1	1	0	0	**1**	**0**	**1**	**0**	**X**	**0**	**1**
1	1	0	1	**1**	**0**	**1**	**0**	**X**	**0**	**1**
1	1	1	0	**1**	**1**	**0**	**0**	**X**	**0**	**0**
1	1	1	1	**1**	**1**	**0**	**0**	**X**	**0**	**0**

4.54. Given a finite state machine (FSM), its state transition table and the truth table for the two Outputs Z_1 and Z_0 are attached. This machine has five states, which are encoded by the values $Q_2Q_1Q_0$, corresponding to the state of three flip-flops. The FSM has a single input called E:

a. Determine the (minimum) excitation equations for flip-flop FF2, if it is assumed to be J-K type.
b. Determine the (minimum) excitation equation for flip-flop FF1, if it is assumed to be type D.
c. Determine the (minimum) excitation equation for flip-flop FF0, if it is assumed to be type T.
d. Indicate, reasoning necessarily the answer, if it is a Moore or Mealy type FSM.

Note: In these three sections it is NOT required to draw any type of circuit.

e. Implement the circuit for the OutputsZ_1 and Z_0, using a memory of 16 positions with a data bus width of 4 bits. Both the schema, with all the connections, and the content of the program that the memory must have programmed are requested.

Current state				**Next State**			**Outputs**	
Q_2^n	Q_1^n	Q_0^n	**E**	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	Z_1	Z_0
0	0	0	0	0	0	0	1	0
0	0	0	1	1	1	1	1	0
0	0	1	0	0	1	1	0	1
0	0	1	1	0	1	1	0	1
0	1	1	0	1	0	0	0	0
0	1	1	1	1	1	1	0	1
1	0	0	0	1	0	0	1	1
1	0	0	1	0	0	0	1	1
1	1	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0

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a)

Current state				Next State			FF2	
Q_2^n	Q_1^n	Q_0^n	E	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	J_2	K_2
0	0	0	0	0	0	0	0	X
0	0	0	1	1	1	1	1	X
0	0	1	0	0	1	1	0	X
0	0	1	1	0	1	1	0	X
0	1	1	0	1	0	0	1	X
0	1	1	1	1	1	1	1	X
1	0	0	0	1	0	0	X	0
1	0	0	1	0	0	0	X	1
1	1	1	0	0	0	0	X	1
1	1	1	1	1	0	0	X	0

Q_2Q_1 \ Q_0E	00	01	11	10
00	0	1	0	0
01	X	X	1	1
11	X	X	X	X
10	X	X	X	X

Q_2Q_1 \ Q_0E	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	0	1
10	0	1	X	X

$$J_2 = Q_1 + \overline{Q_0}.E$$

$$K_2 = \overline{Q_0}.E + Q_0.\overline{E} = Q_0 \oplus E$$

b)

Current state				Next State			
Q_2^n	Q_1^n	Q_0^n	E	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	D
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	1
0	1	1	0	1	0	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	1	0	0	0

Q_2Q_1 \ Q_0E	00	01	11	10
00	0	1	1	1
01	X	X	1	0
11	X	X	0	0
10	0	0	X	X

$$D_1 = \overline{Q_2}.E + \overline{Q_2}.\overline{Q_1}.Q_0$$

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Current state				Next State			
Q_2^n	Q_1^n	Q_0^n	E	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	T
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	0
1	1	1	0	0	0	0	1
1	1	1	1	1	0	0	1

c)

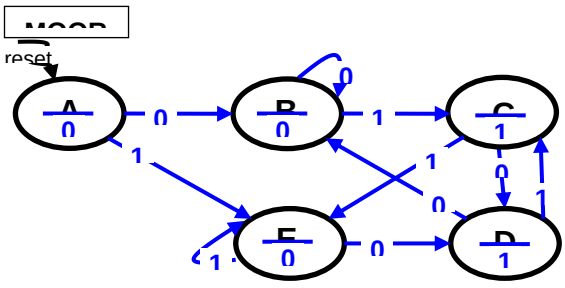
Q_2Q_1 \ Q_0E	00	01	11	10
00	0	1	0	0
01	X	X	0	1
11	X	X	1	1
10	0	0	X	X

$$T_0 = Q_2.Q_0 + Q_1.\overline{E} + \overline{Q_2}.\overline{Q_0}.E$$

e) It is a Mealy machine, because for the same state (the 011) there are two Outputs: 00 and 01.

4.55. We want to design a finite state machine that detects the consecutive sequence of two bits "10" or "01" whenever it occurs. The system must set its output to 1 whenever one of the two indicated sequences is present. Consider that there may be overlapping between two consecutive sequences.

Totally or partially using the attached diagrams, design each state machine:
a) For a Moore machine
b) For a Mealy machine.
It is necessary to briefly indicate the meaning of each one of the defined states.



A: Start without memory. Output 0

B: 1st valid bit sequence "01"

C: 2nd valid bit sequence "01". Exit 1.

D: 2nd valid bit sequence "10". Exit 1.

E: 1st valid bit sequence "10"

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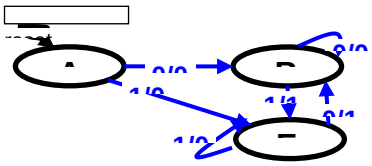

Brief state description

A: Start without memory. Output 0

B: 1st valid bit sequence "01" with output '0' and 2nd valid bit sequence "10" with output 1.

E: 1st valid bit sequence "10" with output '0' and 2nd valid bit sequence '"01" with output 1.