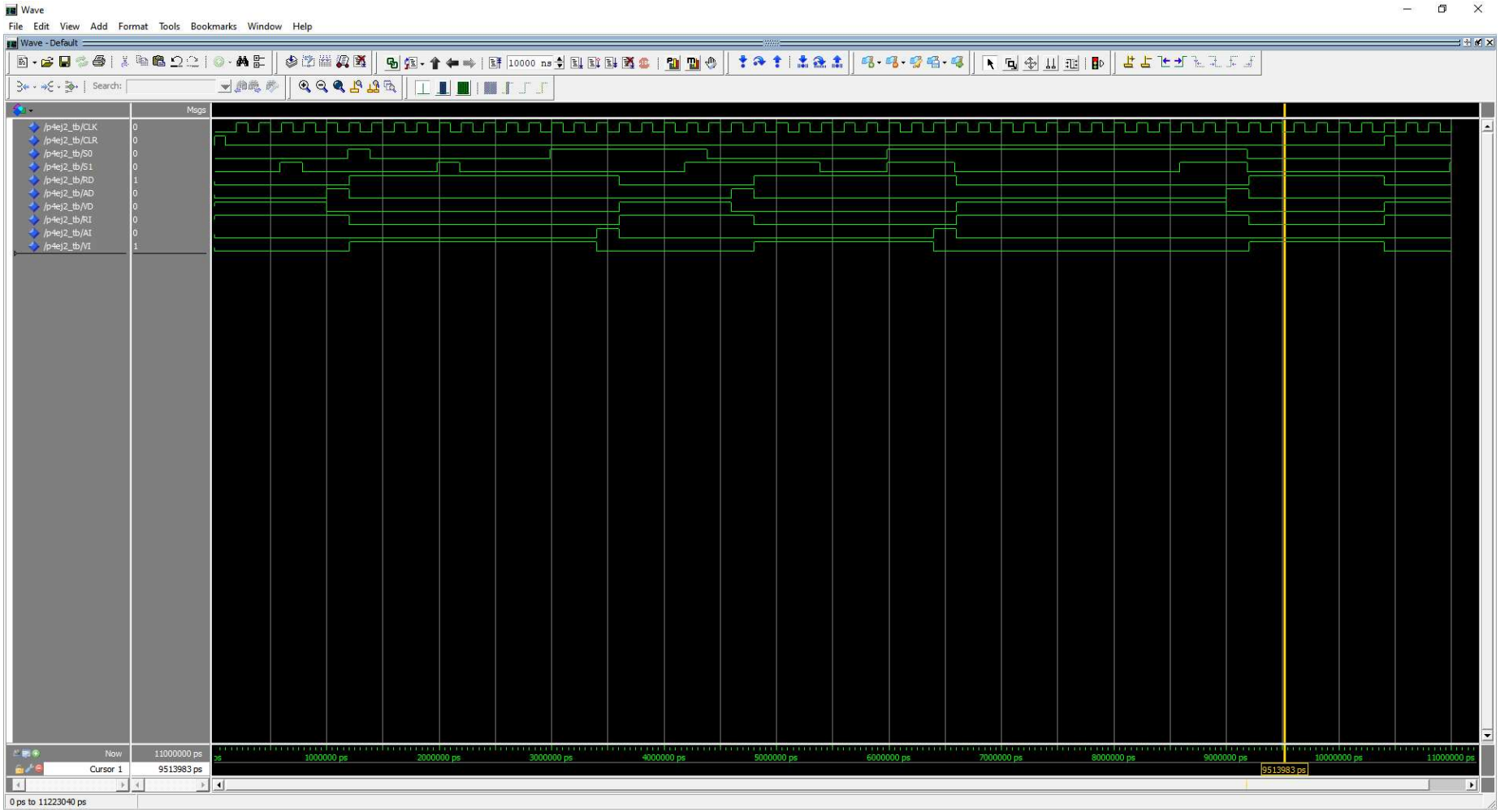

As we can see, when the signal S1 turns 1 during the rising edge of the CLK, the system stays the same (VD==1 and RI==1, the rest 0) for two clock cycles. Then, for a clock cycle, AD==1 and RI==1, the rest 0. The next rising edge turns AD and RI off and sets VI and RD to 1. The same happens when the signal S0 turns 1.

For exercise 2 the simulation is exactly the same, as both designs implement the same functions.