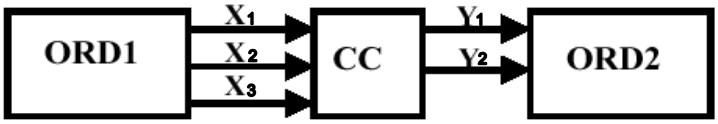
COMPUTER BASICS
U2 Exercises: Combination circuits

U2_1. You want to transmit the first four letters of the alphabet from one computer ORD1 to another ORD2. In the first computer, the four letters are coded in one word of three bits (X1X2X3) and in only two bits in the second computer, (Y1Y2), according to the attached table. Draw and solve a combinational circuit that, using only NAND gates, serves to perform the code conversion as shown in the figure. NOTE: An "X" in the table indicates that the variable can take any value among the possible ones. Note that the letter "A" has two possible encodings, 01X or 100.

	A	B	C	D
X1	0 ó 1	1	0	1
X2	1 ó 0	1	0	0
X3	X ó 0	X	X	1
Y1	0	0	1	1
Y2	0	1	0	1



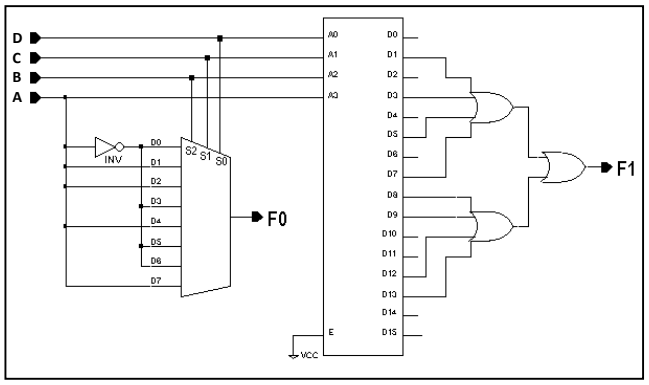
Solution:

$$Y1 = \overline{(X1 \cdot \overline{X2}) \cdot (\overline{X2} \cdot X3)}$$

$$Y2 = \overline{X1 \cdot X2} \cdot \overline{X1 \cdot X3}$$

U2_2. Given the following circuit, formed by a 4-16 decoder and an 8-1 multiplexer:

a) Deduct the system truth table
b) Simplify the logical functions F1 and F0
c) Obtain expressions that use only XOR gates and some inverters if necessary for F0 and only NAND gates for F1



Solution:

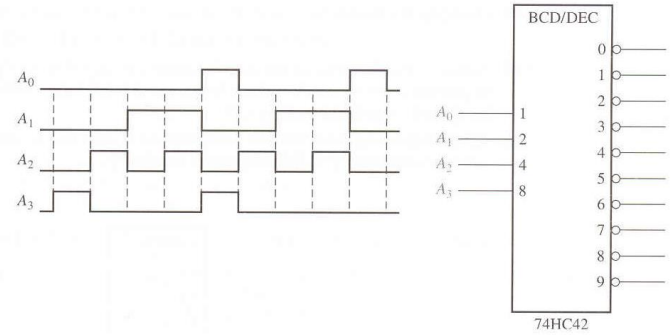
a) $F_0 = \Sigma\, m\,(0,3,5,6,9,10,12,15)$;
$F_1 = \Sigma\, m\,(1,3,5,7,8,9,12,13)$

b) $F_0 = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D} + \overline{A}\,B\,C\,\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,\overline{D} + A\,B\,C\,D$
$F_1 = \overline{A}D + A\overline{C}$

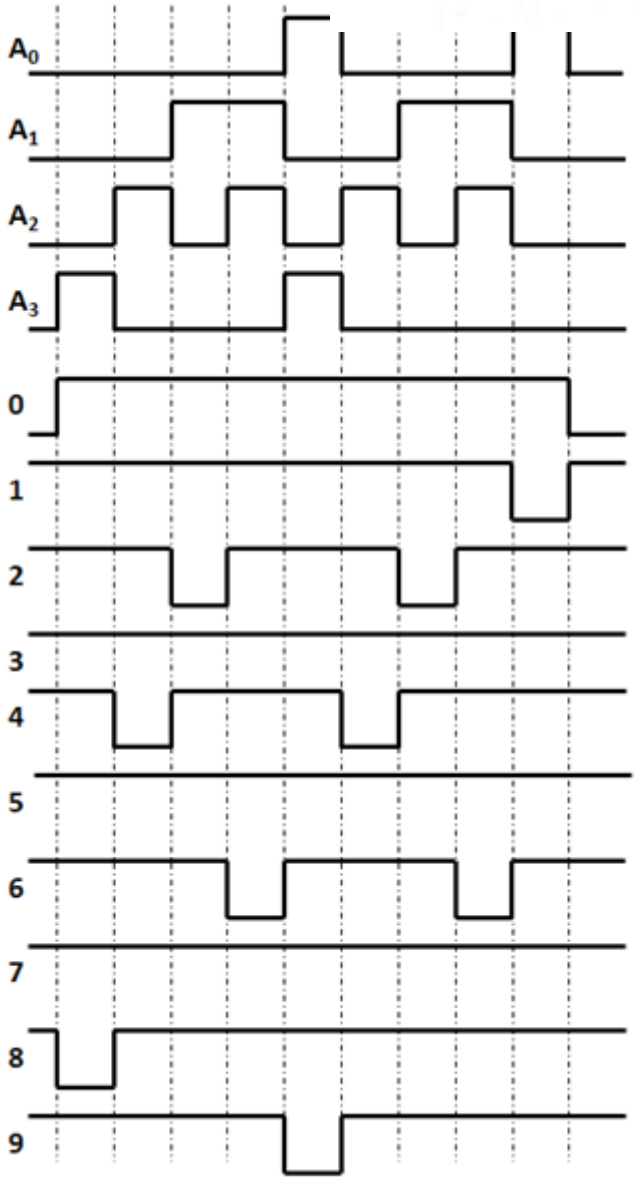
c) $F_0 = \overline{(A \oplus B \oplus C \oplus D)}$
$F_1 = \overline{A\overline{C}}\;\overline{\overline{A}D}$

COMPUTER BASICS
U2 Exercises: Combination circuits

U2_3. The BCD numbers are sequentially applied to the BCD-Decimal converter of the following figure (activation of the outputs is LOW):
Draw a time diagram showing each output in relation to the rest of the output signals and the inputs (assume A0 LSB and A3 MSB of the BCD).

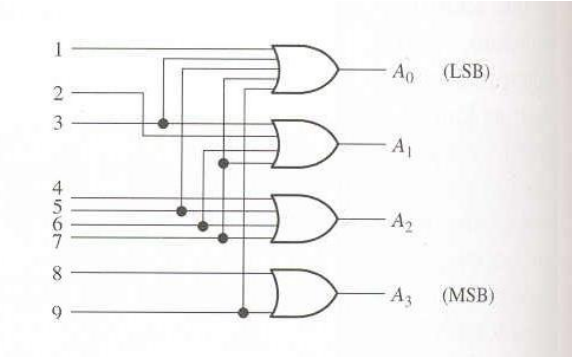


Solution:



COMPUTER BASICS
U2 Exercises: Combination circuits

U2_4. Assume that the decimal-BCD logical encoder of the following figure has inputs 3 and 9 at the HIGH level. What is the exit code? Is this a valid BCD code?

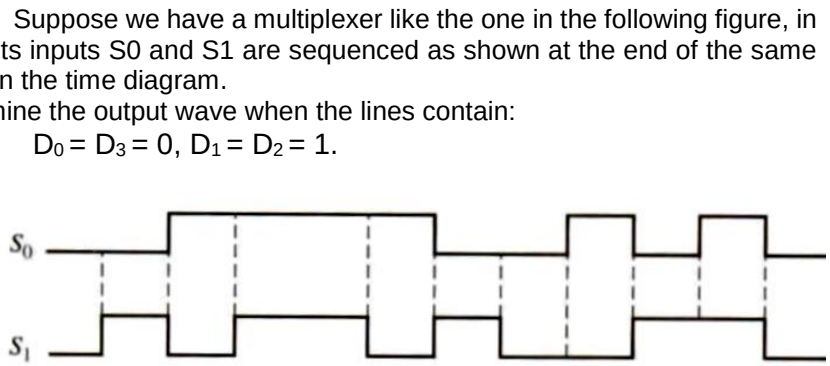


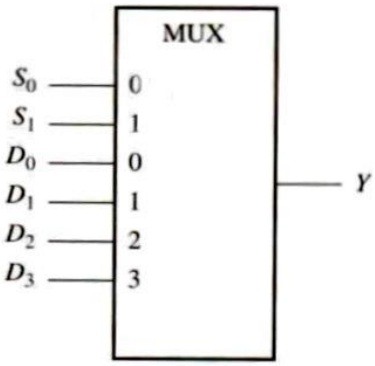
Solution:

$A_3A_2A_1A_0 = 1011$. **Invalid BCD code.**.

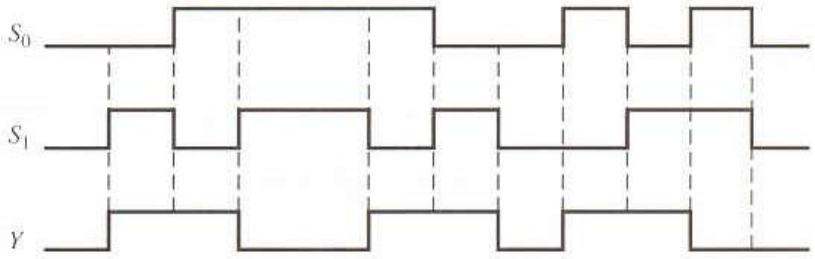
U2_5. Suppose we have a multiplexer like the one in the following figure, in which its inputs S0 and S1 are sequenced as shown at the end of the same figure in the time diagram.
Determine the output wave when the lines contain:

$D_0 = D_3 = 0$, $D_1 = D_2 = 1$.

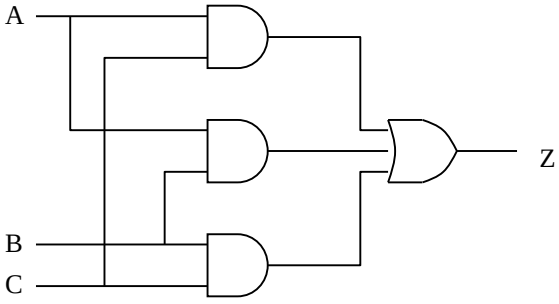




Solution:



U2_6. Obtain the expression for the circuit:
a) Using only NAND gates.
b) Using only NOR gates.



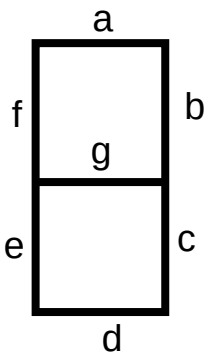
Solution:

a) $Z = \overline{\overline{AC}\ \overline{AB}\ \overline{BC}}$

b) $Z = \overline{\overline{\overline{A} + \overline{C}}\ \overline{\overline{A} + \overline{B}}\ \overline{\overline{B} + \overline{C}}}$

COMPUTER BASICS
U2 Exercises: Combination circuits

U2_7. Using Karnaugh tables, calculate the 7 logical expressions corresponding to each one of the segments of a visualizer that uses BCD active high inputs (being D3 the MSB bit and D0 the LSB), with visualizer elements as active high .



Solution:

BCD	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

$a = D_3 + D_1 + D_2D_0 + \overline{D_2}$

$b = D_1D_0 + \overline{D_2} + \overline{D_1}\ \overline{D_0}$

$c = \overline{D_1} + D_2 + D_0$

$d = D_3 + D_1\overline{D_0} + \overline{D_2}\ \overline{D_0} + \overline{D_2}\ D_1 + D_2\overline{D_1}\ D_0$

$e = D_1\overline{D_0} + \overline{D_2}\ \overline{D_0}$

$f = D_3 + \overline{D_1}\ \overline{D_0} + D_2\overline{D_1} + D_2\overline{D_0}$

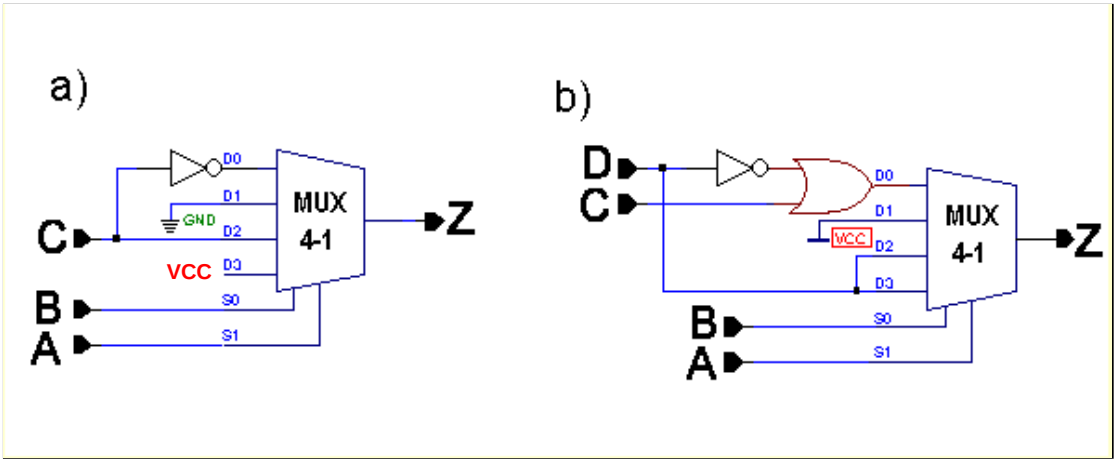
$g = D_3 + D_1\overline{D_0} + \overline{D_2}\ D_1 + D_1\overline{D_0}$

U2_8. Using a 4-1 multiplexer, deduct the circuit that fulfills the function:

a) $Z = AB + AC + \overline{A}\ \overline{B}\ \overline{C}$ **b)** $Z = \overline{A}\ B + AD + CD + \overline{A}\ \overline{D}$

NOTA: Add gates if necessary. Use variables A and B as control variables.

Solution:



COMPUTER BASICS
U2 Exercises: Combination circuits

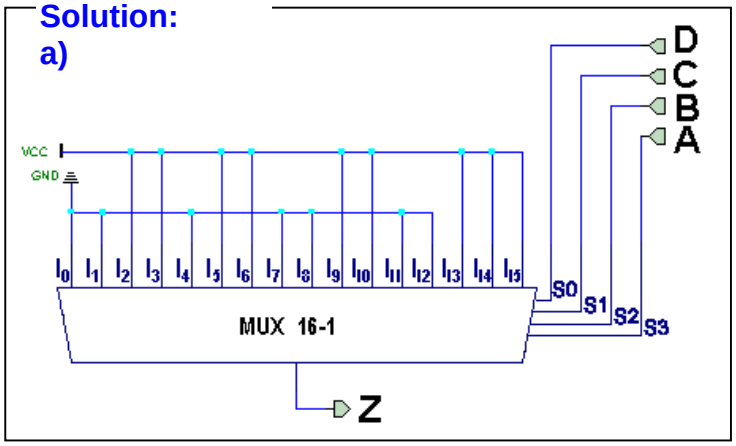
U2_9. Obtain the function S (A,B,C,D) = Σm(2,3,5,6,9,10,13,14,15)

a) Using a 16 input multiplexer
b) Using a 8 input multiplexer
c) Using a 4 input multiplexer

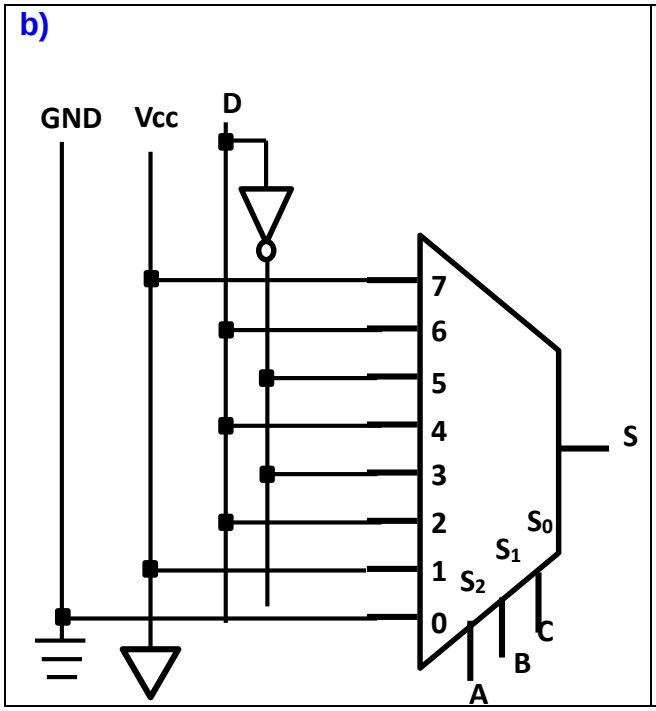
Add in each case the minimum number of logical gates needed, using in each case the variables of more weight as control.

Solution:

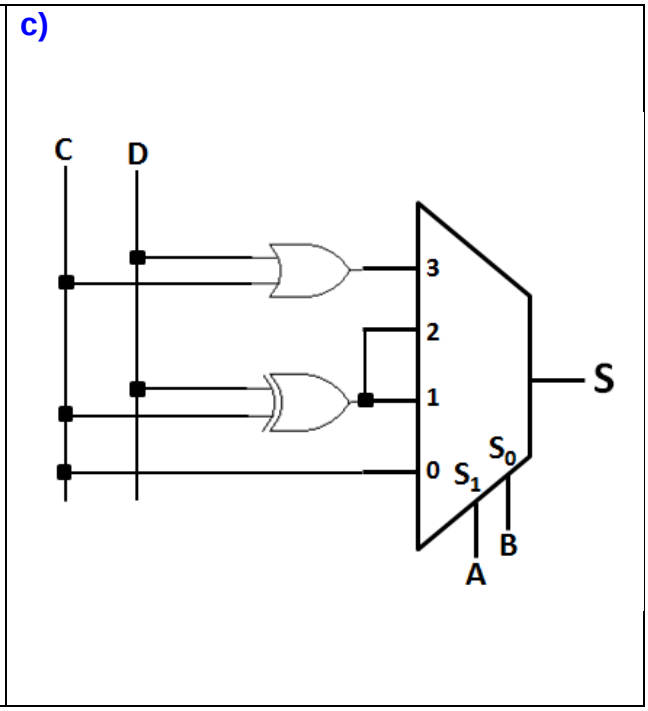
a)



b)

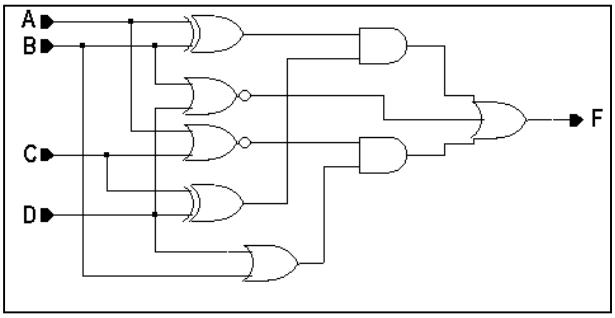


c)

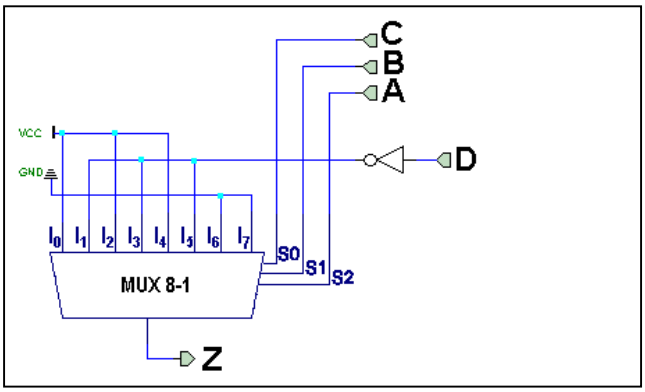


COMPUTER BASICS
U2 Exercises: Combination circuits

U2_10. Given the circuit in the figure, perform the same logic function using an 8-1 multiplexer and the minimum number of logical gates needed, using variables A, B and C as control.



Solution:



U2_11. A certain logic circuit with 4 input variables A, B, C, and D serves to solve the logical functions F and G. The function F is '1' as long as two or more signals from the input are '1', in any other case F is worth '0'. Function G is '1' as long as '1' is an even number of signals from the input, otherwise G is the complement of F. It is requested:

a) Design a circuit for the function F using a 4-16 decoder, with active outputs at low level using the minimum number of logical gates needed

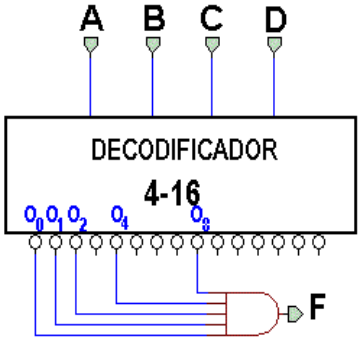
b) Design a circuit for the function G that uses only an 8-1 multiplexer and the minimum number of logical gates needed

c) Design a circuit for functions F and G that uses the minimum number of doors using only NAND gates

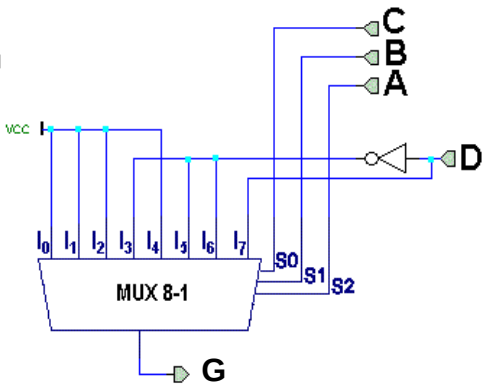
Use the most representative variables as control variables

Solution:

a)



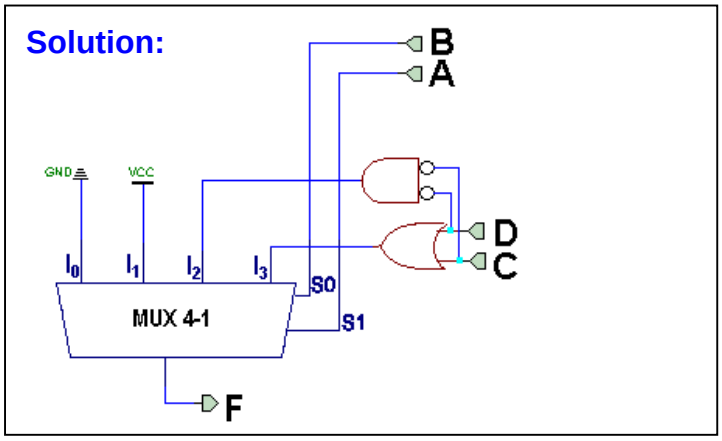
b)



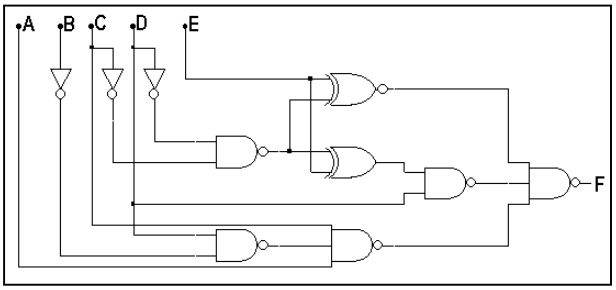
COMPUTER BASICS
U2 Exercises: Combination circuits

U2_12. Implement the following function F(A,B,C,D) = Σm(4,5,6,7,8,13,14,15), using a 4-1 multiplexer and the minimum number of logic gates possible. Use the most significant variables as control variables.

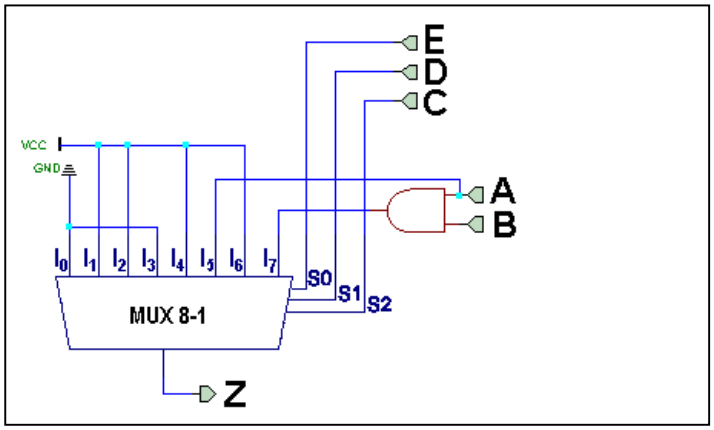
Solution:



U2_13. We wish to perform the same 5-variable logic function performed by the circuit in the figure, using a multiplexer 8-1. Use the variables C, D and E as control lines from highest to least weight respectively



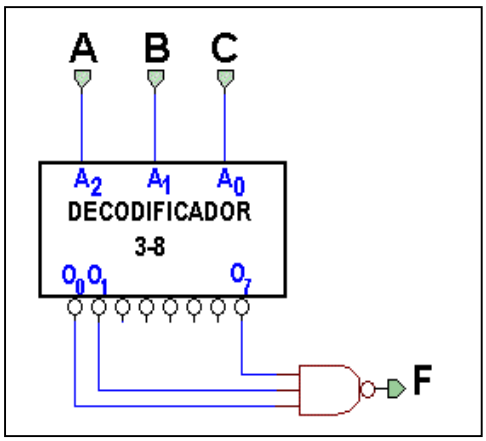
Solution:



COMPUTER BASICS
U2 Exercises: Combination circuits

U2_14. Given the following 3 variable function $F = (A \oplus \overline{B})(C + \overline{B})$, implement said function using a 3-8 decoder with active low outputs and using the minimum number of gates possible. Take A as the most weighted variable.

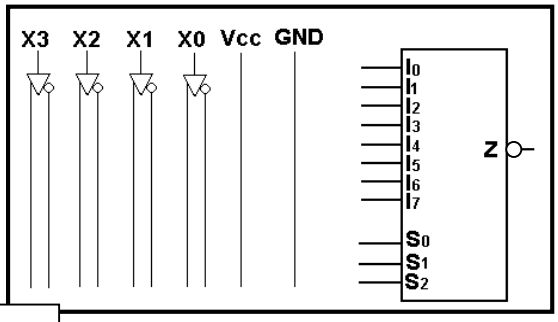
Solution:



U2_15. Given the 4 variable function f(X3,X2,X1,X0) = Σm(0,2,5,8,10,12,14), where X3 is the MSB, using the les weighted variables as control:

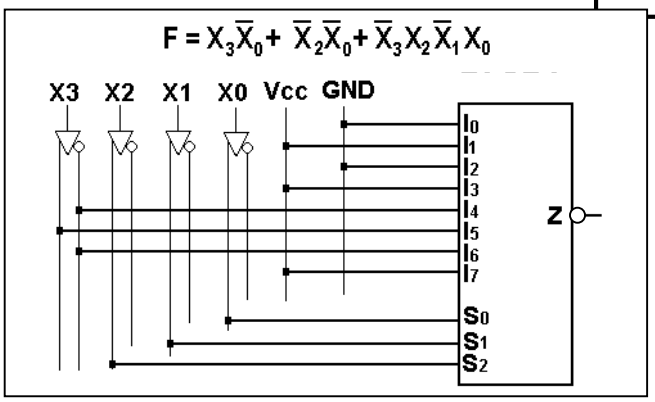
a) Materialize this function using a multiplexer like the one in the figure. Remember that the output of this circuit is active at low level. Make the corresponding connections in the diagram as in the figure.

b) Simplify **f** using a Karnaugh map.

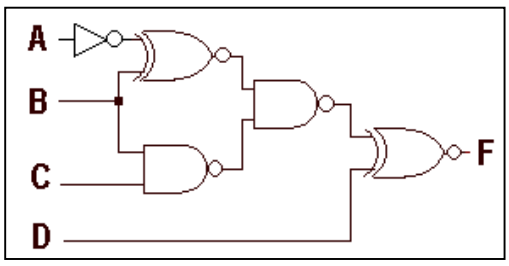


c) Solution:

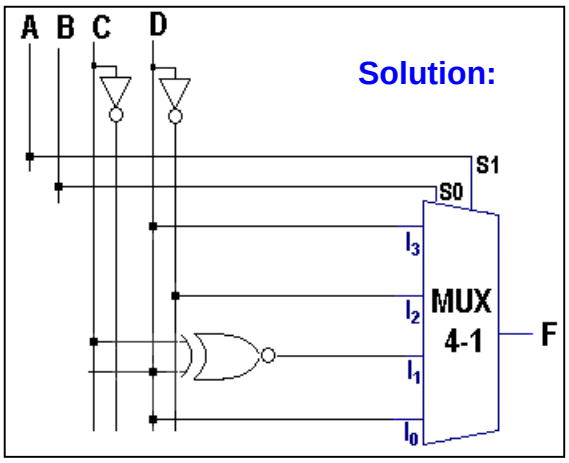
$$F = X_3\overline{X}_0 + \overline{X}_2\overline{X}_0 + \overline{X}_3X_2\overline{X}_1X_0$$



U2_16. Given the circuit in the figure, solve the same function F using a 4-1 multiplexer. Use A and B as control signals S1 and S0, respectively.



COMPUTER BASICS
U2 Exercises: Combination circuits



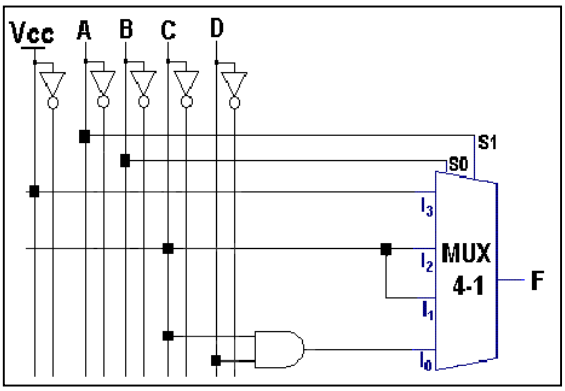
U2_17. Given the 4 variable function F(ABCD) = AB + AC/D + BC + CD:

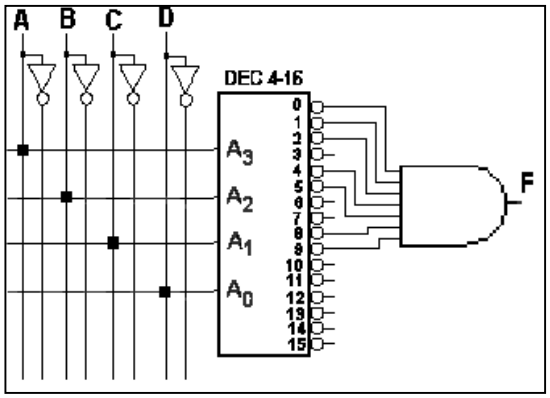
a) Express F using a 4-1 multiplexer.

b) Design F using the 4-16 decoder with active outputs on low.

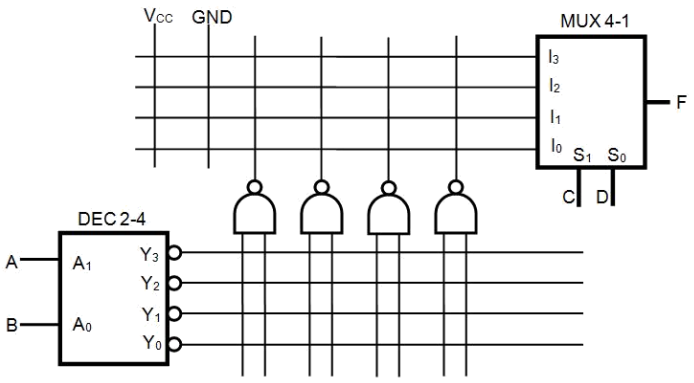
Add in each case the minimum additional gates that are considered necessary.

Solution:



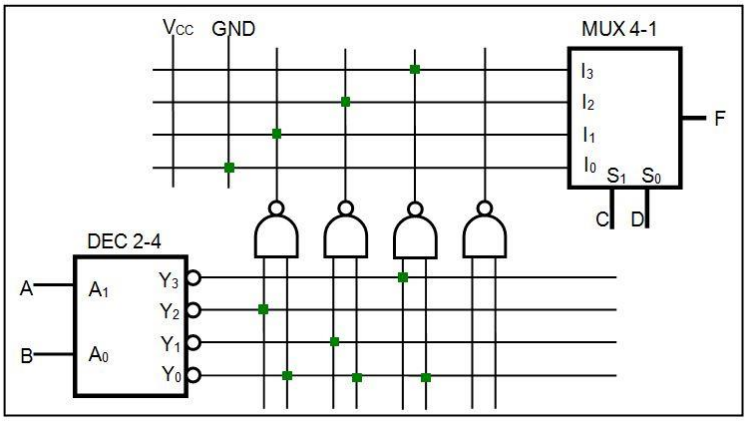


U2_18. Given the function F(A,B,C,D) = ∑m(1,2,3,6,9,15), implement it using EXCLUSIVELY the devices of the attached figures, marking with a point or a cross the cables that are connected.

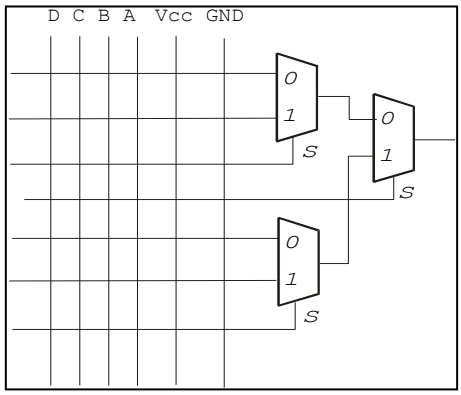


Solution:

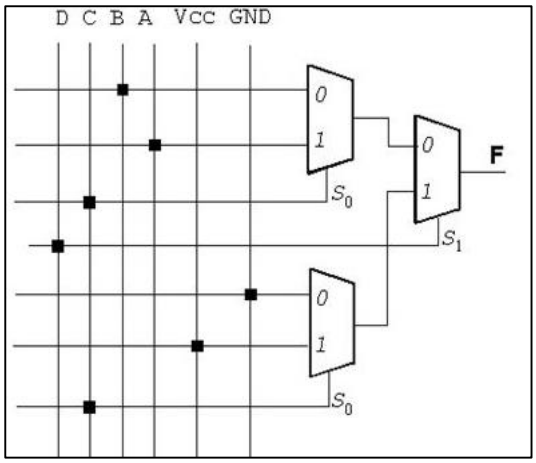
COMPUTER BASICS
U2 Exercises: Combination circuits



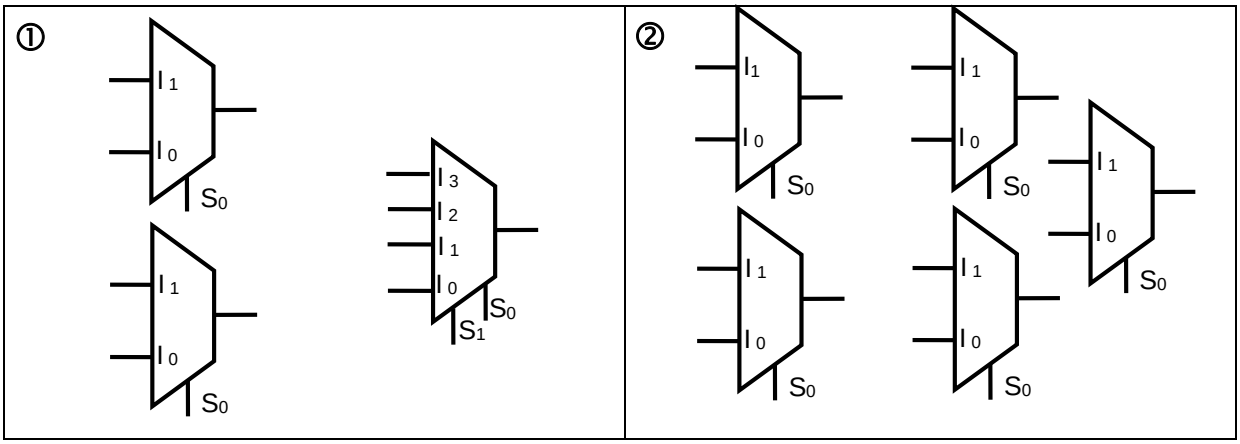
U2_19. The 2-1 multiplexers in the figure have a control signal S and two inputs (S = 0 selects the input as 0). We want to implement the logic function F (D, C, B, A) = Π M (0, 1, 4, 6, 8, 9, 10, 11) by completing the connections in the figure. The variable D is the most significant. Indicate with an x the cables that should be attached.



Solution:

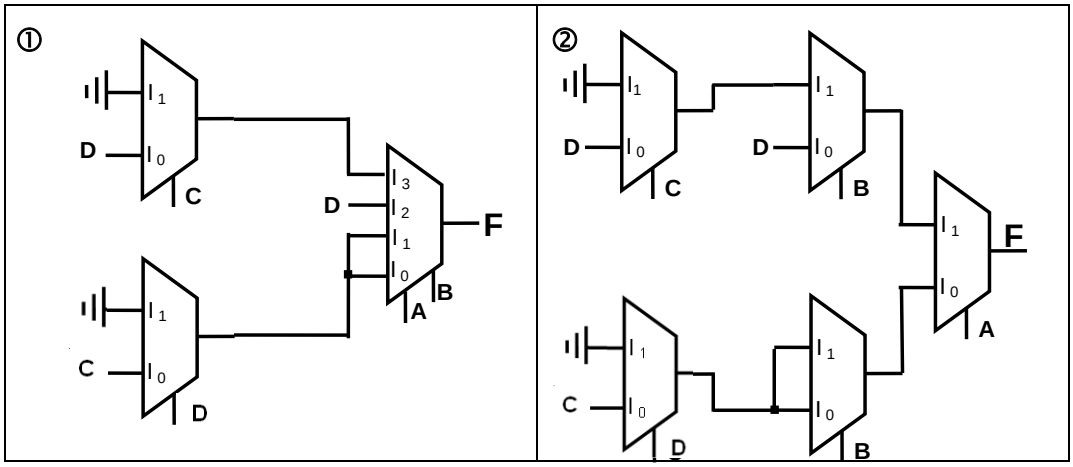


U2_20. Implement the function F(A,B,C,D) = Σm(2,6,9,11,13), using exclusively all the multiplexers of each of the two schemes shown.



COMPUTER BASICS
U2 Exercises: Combination circuits

Solution:



U2_21. The following table shows the X and Y data of two bits (X1X0 and Y1Y0) in twos complement
a) Write in a table the sum of said data (S2S1S0). Keep in mind that, since the numbers are given as a complement to two, the result will also be in addition to two.
b) Express function S2 in maxterms. Also express S2 in the most simplified form possible as a product of sums.

Solution:
a)

X_1	X_0	Y_1	Y_0	S_2	S_1	S_0	X_1	X_0	Y_1	Y_0	S_2	S_1	S_0
0	0	0	0	0	0	0	1	0	0	0	1	1	0
0	0	0	1	0	0	1	1	0	0	1	1	1	1
0	0	1	0	1	1	0	1	0	1	0	1	0	0
0	0	1	1	1	1	1	1	0	1	1	1	0	1
0	1	0	0	0	0	1	1	1	0	0	1	1	1
0	1	0	1	0	1	0	1	1	0	1	0	0	0
0	1	1	0	1	1	1	1	1	1	0	1	0	1
0	1	1	1	0	0	0	1	1	1	1	1	1	0

c) $S_2 = \Pi\, M(0,1,4,5,7,13) = (X_1+X_0+Y_1+Y_0)\,(X_1+X_0+Y_1+\overline{Y_0})\,(X_1+\overline{X_0}+Y_1+Y_0)$

$(X_1+\overline{X_0}+Y_1+\overline{Y_0})\,(X_1+\overline{X_0}+\overline{Y_1}+\overline{Y_0})\,(\overline{X_1}+\overline{X_0}+Y_1+\overline{Y_0})$

$S_2 = (X_1+Y_1)\,(X_1+\overline{X_0}+\overline{Y_0})\,(\overline{X_0}+Y_1+\overline{Y_0})$

U2_22. For the filling of a water tank there are two solenoid valves F1 and F2 that provide a flow rate of 50 and 10 liters / minute respectively. For this, the following criteria will be taken into account:

- **i.** When the amount of water in the tank is between 0 and 60% of the total capacity, the tank must be filled at a rate of 60 liters / minute.
- **ii.** If the water level is between 60 and 90%, the filling speed will be 50 liters / minute.
- **iii.** If the level is between 90 and 100%, it will proceed to finish filling the tank with a flow rate of 10 liters / minute.
- **iv.** If the level has reached its maximum point, that is, at 100%, both solenoid valves must be closed.

There are 3 sensors (S1, S2, and S3) that allow you to determine the level of the tank at any time, so that:

1. A '1' appears on sensor S1 when we have reached 100% of the capacity of the tank.
2. A '1' will appear on sensor S2 if the amount of water in the tank exceeds 90%.
3. And finally, the sensor S3 indicates by means of a '1' if the level is above 60%.

Calculate:

- **a.** The truth table of the system.
- **b.** Implement the control of the F1 actuator using a 3-8 decoder with the active outputs at low and the simplest logic gate you may need.

COMPUTER BASICS
U2 Exercises: Combination circuits

c. Implement the control of the F2 actuator using a multiplexer 4-1, with the minimum number of additional doors.

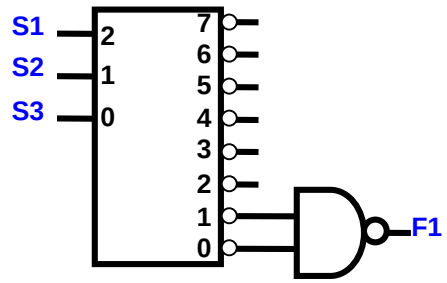
Note1: It is considered that a solenoid valve is open, that is, it allows the passage of water, when it receives a '1'; otherwise it is closed.

Note2: For those sensor combinations that can not occur, the output of the actuators (F1 and F2) will be considered as "0".

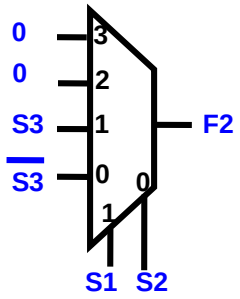
SOLUTION: a)

S1	S2	S3	F1	F2
0	0	0	**1**	**1**
0	0	1	**1**	**0**
0	1	0	**0**	**0**
0	1	1	**0**	**1**
1	0	0	**0**	**0**
1	0	1	**0**	**0**
1	1	0	**0**	**0**
1	1	1	**0**	**0**

b)



c)

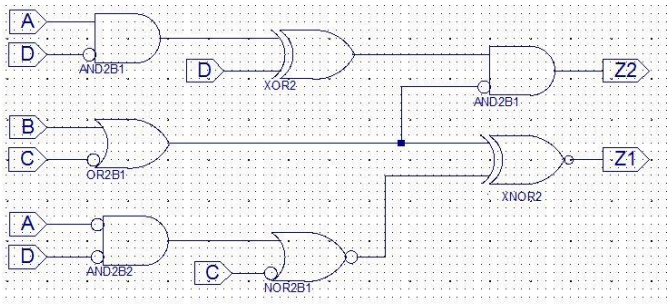


U2_23. Given the circuit of the figure:

a. Write the truth table of the system.

b. Implement the Z2 function using a 4-16 decoder with the active outputs at low and the simplest logic gate you may need.

c. Implement the Z1 function using an 8-1 multiplexer, with the minimum number of additional doors. Use the variables A, B and C as control variables, taking A as the most significant.

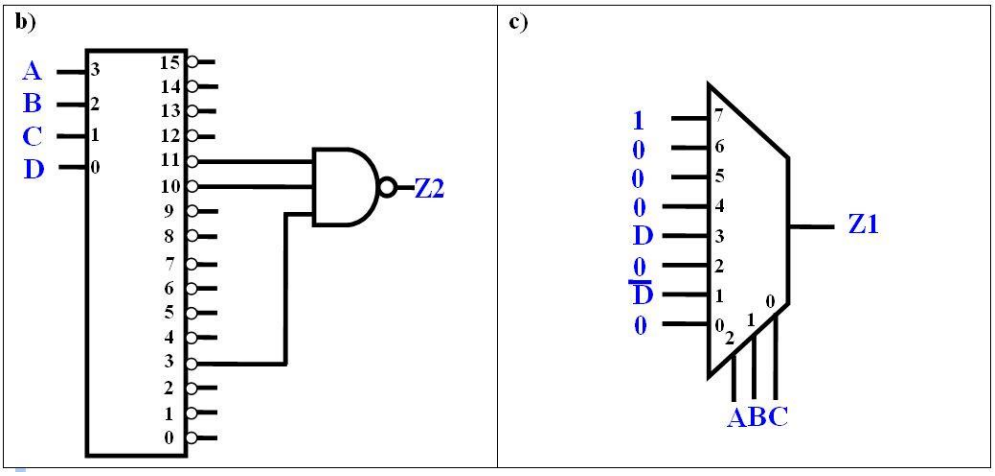


Note: Indicate the order of the inputs of the circuits and the inputs and outputs, which in each case are connected.

SOLUTION: a)

Nº	A	B	C	D	Z2	Z1		Nº	A	B	C	D	Z2	Z1
0	0	0	0	0	**0**	**0**		8	1	0	0	0	**0**	**0**
1	0	0	0	1	**0**	**0**		9	1	0	0	1	**0**	**0**
2	0	0	1	0	**0**	**1**		10	1	0	1	0	**1**	**0**
3	0	0	1	1	**1**	**0**		11	1	0	1	1	**1**	**0**
4	0	1	0	0	**0**	**0**		12	1	1	0	0	**0**	**0**
5	0	1	0	1	**0**	**0**		13	1	1	0	1	**0**	**0**
6	0	1	1	0	**0**	**0**		14	1	1	1	0	**0**	**1**
7	0	1	1	1	**0**	**1**		15	1	1	1	1	**0**	**1**

COMPUTER BASICS
U2 Exercises: Combination circuits



U2_24. Given the function of 4 variables F(A,B,C,D) = ΠM(0,5,7,9,10,12,14,15):

a) Write the truth table of the system.

b) Implement the function using the minimum number of gates and an 8-1 multiplexer. Use the most significant variables as the multiplexer control.

c) Implement the function using the minimum number of gates and a multiplexer 4-1. Use the most significant variables as the multiplexer control.

NOTE: In all the circuits the order of priority of the inputs must be specified and in all of them the input variable to which it is associated must be indicated.

Solution: a)

A	B	C	D	F		A	B	C	D	F
0	0	0	0	**0**		1	0	0	0	**1**
0	0	0	1	**1**		1	0	0	1	**0**
0	0	1	0	**1**		1	0	1	0	**0**
0	0	1	1	**1**		1	0	1	1	**1**
0	1	0	0	**1**		1	1	0	0	**0**
0	1	0	1	**0**		1	1	0	1	**1**
0	1	1	0	**1**		1	1	1	0	**0**
0	1	1	1	**0**		1	1	1	1	**0**

b) Using MUX 8-1

$I_0 = D$; $I_1 = 1$; $I_2 = \overline{D}$; $I_3 = \overline{D}$

$I_4 = \overline{D}$; $I_5 = D$; $I_6 = D$; $I_7 = 0$

c) Using MUX 4-1

$I_0 = (C+D)$; $I_1 = \overline{D}$

$I_2 = \overline{(C \oplus D)}$; $I_3 = \overline{C} \cdot D$

COMPUTER BASICS
U2 Exercises: Combination circuits

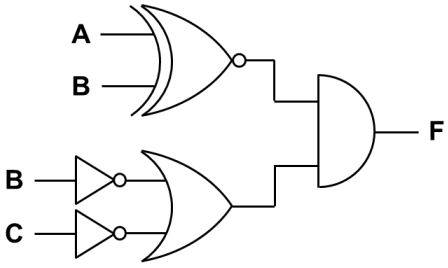
U2_25. Given the circuit of the figure:

a) Write the truth table of the system.

b) Implement the function used a decoder with active outputs at high level and the minimum number of gates of the smallest possible size. Use A as the most significant variable.

c) Implement the function using a decoder with active outputs at low level and the minimum number of doors of the smallest possible size. Use A as the most significant variable.

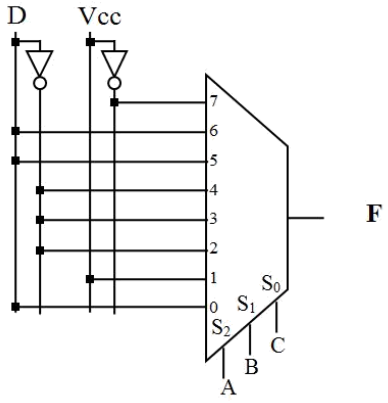
NOTE: In all the circuits the order of priority of the inputs must be specified and in all of them the input variable to which it is associated must be indicated.



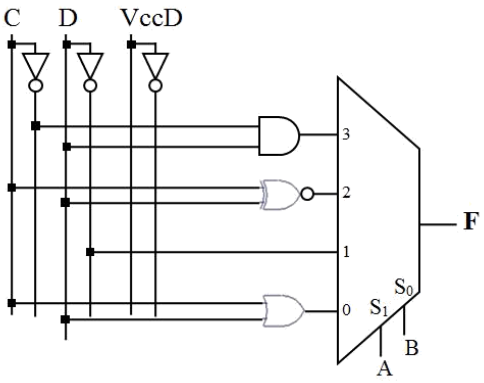
Solution: a)

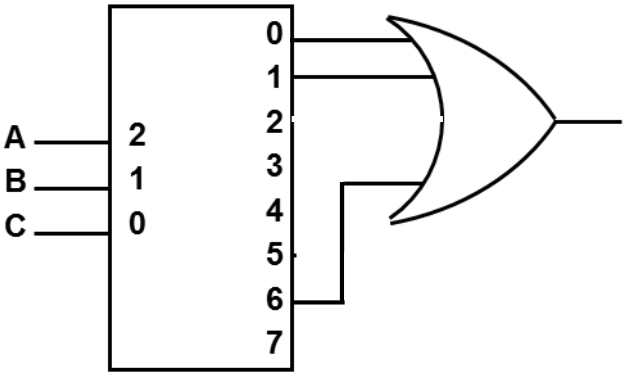
A	B	C	F
0	0	0	**1**
0	0	1	**1**
0	1	0	**0**
0	1	1	**0**
1	0	0	**0**
1	0	1	**0**
1	1	0	**1**
1	1	1	**0**

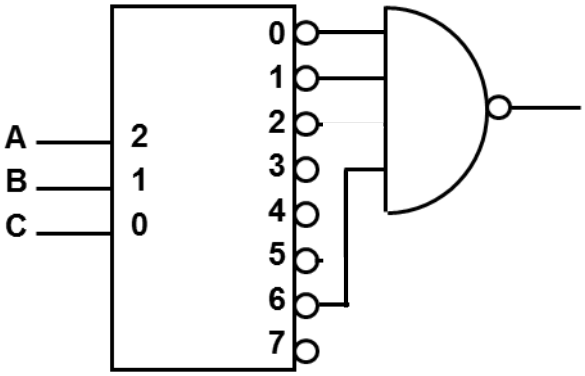
b)



c)

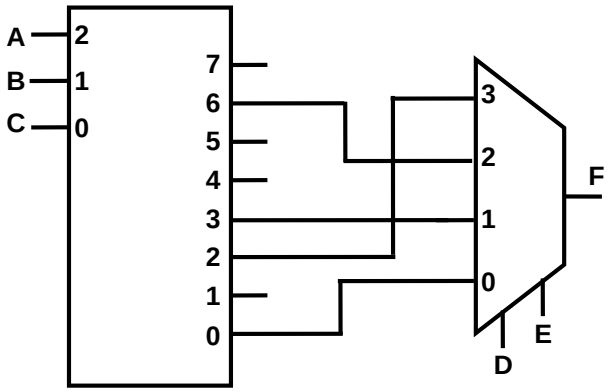






COMPUTER BASICS
U2 Exercises: Combination circuits

U2_26. A 3-8 decoder connected to a 4-1 multiplexer is shown in the circuit of the figure. The canonical form of the function of 5 variables F (A, B, C, D, E) is requested, given as a product of maxterms.



Solution:

The terms selected in the decoder are:

$$(A \cdot B \cdot \overline{C}),\ (\overline{A} \cdot B \cdot C),\ (\overline{A} \cdot B \cdot \overline{C})\ \text{y}\ (\overline{A} \cdot \overline{B} \cdot \overline{C})$$

These four terms act as inputs in the multiplexer, inputs that are selected by the four combinations of control variables:

$$F(A,B,C,D,E) = (\overline{A}.B.\overline{C})(D.E)+(A.B.\overline{C})(D.\overline{E})+(\overline{A}.B.C)(\overline{D}.E)+(\overline{A} \cdot \overline{B} \cdot \overline{C})(\overline{D} \cdot \overline{E}) = =$$

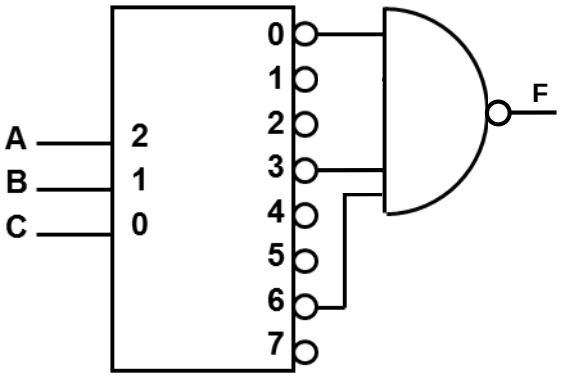
$$\Sigma\ m\ (11, 26, 13, 0)$$

$$F(A,B,C,D,E) =$$

$$= \Pi(1,2,3,4,5,6,7,8,9,10,12,14,15,16,17,18,19,20,21,22,23,24,25,27,28,29,30,31)$$

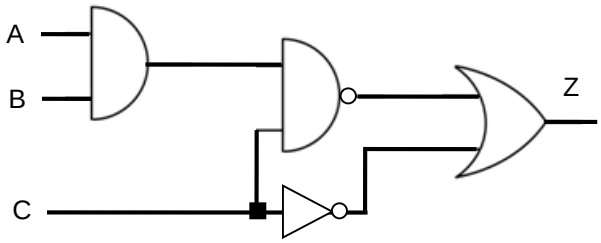
U2_27. Given the canonical form of the 3 variable function F(A,B,C) = Σ m(0,3,6), where A is considered the variable of greater weight, we want to implement this function F using a decoder 3-8 with active outputs in low and the smallest number of logical gates and of the simplest type that is possible. Design the circuit drawing the decoder and the gates used, indicating in each case the inputs and outputs used.

Solution:



COMPUTER BASICS
U2 Exercises: Combination circuits

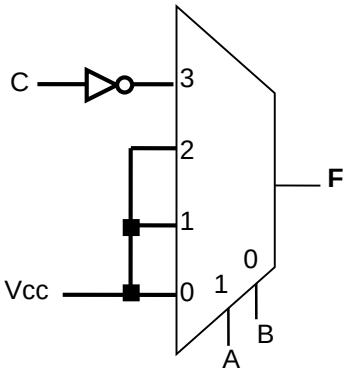
U2_28. Given the circuit of the attached figure, where the function Z(A,B,C), is represented, we want to implement said function Z using a multiplexer 4-1 and the smallest number of logical gates possible. Design the circuit, briefly justifying the design, drawing the multiplexer and the gates used, indicating in each case the inputs and outputs that are used in it. Use A and B as control variables, taking A as the most important variable.



Solution:

$Z = \overline{A.B.C} + \overline{C} = (\overline{A} + \overline{B} + \overline{C})$

C / AB	0	1
00	1	1
01	1	1
11	1	0
10	1	1



U2_29. Given the 4 variable function $F(A,B,C,D) = AB + AC\overline{D} + BCD$:

a) Obtain F in its canonical form as a product of sums.
b) Implement said function using a 4-1 multiplexer and the minimum number of logic gates possible.

Solution.

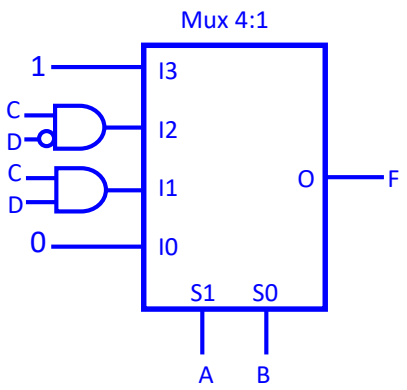
a. For ease, since the function is given as the sum of products, we obtain the canonical expression as sum of products and from there we obtain the expression as a product of sums (it can be done in other ways):

$F= AB + AC\overline{D} + BCD = AB(\overline{C}\,\overline{D} + C\overline{D} + \overline{C}D + CD) + AC\overline{D}(B + \overline{B}) + BCD(A + \overline{A})$

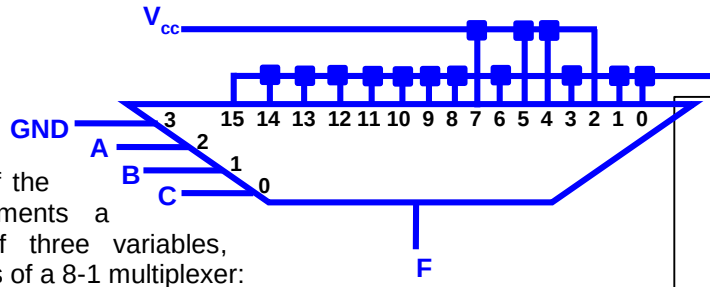
Operating, we obtain $F(A,B,C,D)= \sum m(7,10,12,13,14,15)$, therefore, expressed as a product of sums:

$$F= \prod M(0,1,2,3,4,5,6,8,9,11)$$

b. Using a 4:1 multiplexer, the implementation would result in:



COMPUTER BASICS
U2 Exercises: Combination circuits



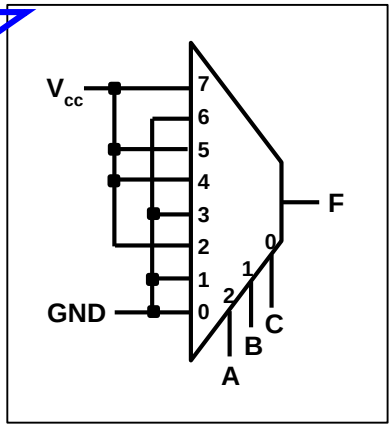
U2_30.

Given the circuit of the figure that implements a logical function of three variables, F(A,B,C), by means of a 8-1 multiplexer:

a) Using the minimum number of gates, implement the same function by means of a 3-8 decoder with the active outputs in low.

b) Using the minimum number of gates necessary, implement the same function by means of a 16- multiplexer.

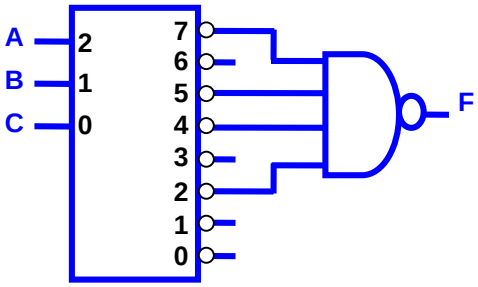
c) Using the minimum number of gates necessary, implement the same function by means of a 4-1 multiplexer.



Solution

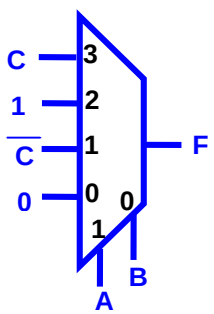
$F(A,B,C) = \Sigma\ (2,4,5,7)$

a)



b) One of the possible solutions, which corresponds to connecting the most significant bit of the multiplexer to "0"

c)



COMPUTER BASICS
U2 Exercises: Combination circuits

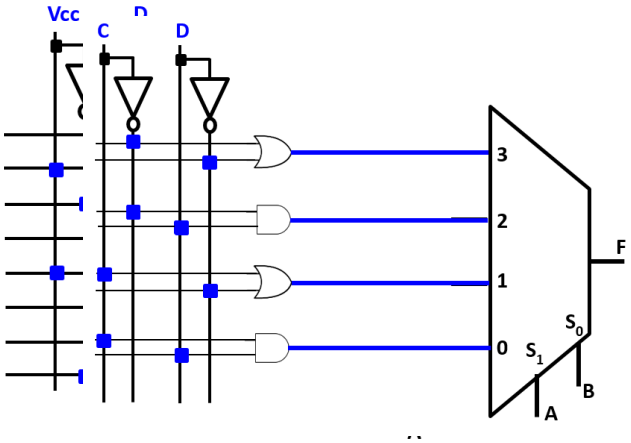
U2_31. Given the 4 variable function, F(A, B, C, D) = Σ m(3, 4, 6, 7, 9, 12, 13, 14), where A is the most significant variable:

a. Implement this function using an 8: 1 multiplexer and using as few gates as possible.

b. Implement this function using a 4:1 multiplexer and as few doors as possible.

Solution

a) **b)**



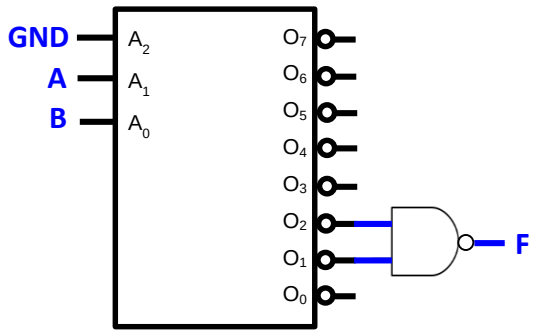
COMPUTER BASICS
U2 Exercises: Combination circuits

U2_32. Given the function of 2 variables F(A, B) = A $\overline{B}$ + $\overline{A}$ B:

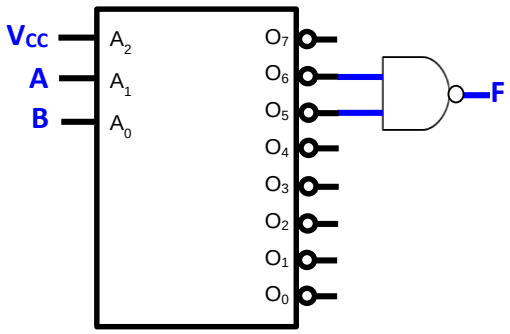
a. Implement this function using a 3-8 decoder like the one in the figure, in which the outputs are active in low. Using any necessary additional logical gates, the use of the least number of gates with the least number of entries considered necessary will be noted.

NOTE: In the Solution of the exercise, all the decoder inputs must be connected to some signal or value. Use the names Vcc and GND to represent the power and ground signals respectively.

Solution:



- Another valid solution would also be:



U2_33. The aim is to design a combinational circuit whose input ($E_3E_2E_1E_0$) is a 4-bit number and its output (S2S1S0) is the number of ones present in the input:

a) The truth table of the circuit.

b) The equations of the output functions, as follows:

- **i.** S0 in one of its canonical forms.
- **ii.** S1 in its maximum simplification as a product of sums.
- **iii.** S2 in its maximum simplification as sum of products.

c) Implement (design the circuit) the output functions in the following way.

- **i.** S2 with logical doors.
- **ii.** S1 with a 4: 1 multiplexer and the smallest number of logical gates possible.
- **iii.** S0 with an 8: 1 multiplexer and the smallest possible number of logic gates.

In this third section, the use of the least number of gates with the least number of entries necessary will be valued.

a)

Nº	E_3	E_2	E_1	E_0	S_2	S_1	S_0
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1
2	0	0	1	0	0	0	1
3	0	0	1	1	0	1	0
4	0	1	0	0	0	0	1
5	0	1	0	1	0	1	0
6	0	1	1	0	0	1	0
7	0	1	1	1	0	1	1

Nº	E_3	E_2	E_1	E_0	S_2	S_1	S_0
8	1	0	0	0	0	0	1
9	1	0	0	1	0	1	0
10	1	0	1	0	0	1	0
11	1	0	1	1	0	1	1
12	1	1	0	0	0	1	0
13	1	1	0	1	0	1	1
14	1	1	1	0	0	1	1
15	1	1	1	1	1	0	0

b)

i. $S_0 = \Pi\, M(0, 3, 5, 6, 9, 10, 12, 15)$ ó $S_0 = \Sigma\, m(1, 2, 4, 7, 8, 11, 13, 14)$

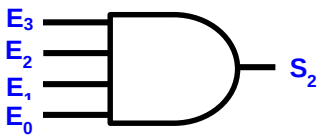
ii. $S_1 = (\overline{E_3} + \overline{E_2} + \overline{E_1} + \overline{E_0}).(E_3 + E_1 + E_0).(E_3 + E_2 + E_1).(E_2 + E_1 + E_0).(E_3 + E_2 + E_0)$

iii. $S_2 = (E_3\ .\ E_2\ .\ E_1\ .\ E_0)$

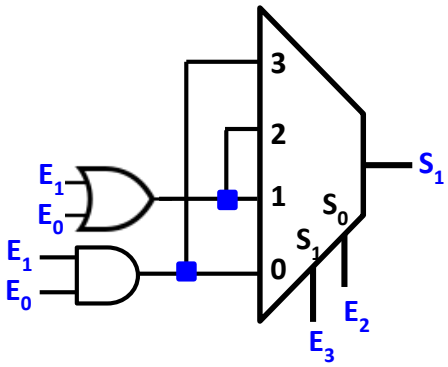
COMPUTER BASICS
U2 Exercises: Combination circuits

c)

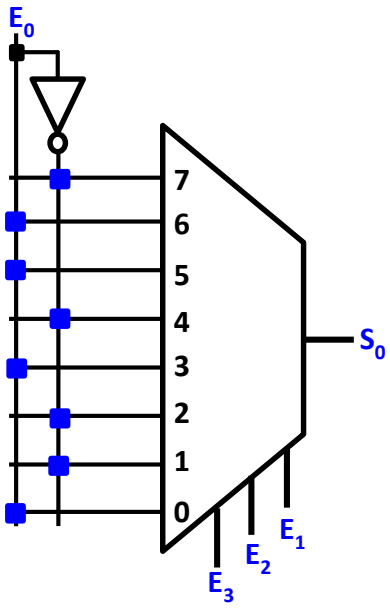
i.



ii.



iii.



U2_34. We want to design a combinational circuit that performs the division between two input numbers, A / B. The number A has three bits ($A_2A_1A_0$) and the number B has two (B_1B_0). The output will be two other numbers, C and R. C is the quotient, with three bits ($C_2C_1C_0$) and R the rest, with two bits (R_1R_0).
NOTE: The case of division by zero will never take place, that is, the combination B1B0 = 00 will never be given

Justifying all your answers:

- **a)** Truth table of the complete circuit ordered
- **b)** Canonical expression of C0, as a product of sums.
- **c)** Canonical expression of R1, as a sum of products.
- **d)** Implement the C1 function with logical gates, in the most simplified way possible.
- **e)** Implement the R0 function using exclusively an 8: 1 multiplexer and a 2: 4 decoder.
  Use the variables A2A1A0 as control inputs of the MUX, with A2 being the most important.

a)

A_2	A_1	A_0	B_1	B_0	C_2	C_1	C_0	R_1	R_0
0	0	0	0	0	X	X	X	X	X
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0
0	0	1	0	0	X	X	X	X	X
0	0	1	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0	0	1
0	0	1	1	1	0	0	0	0	1
0	1	0	0	0	X	X	X	X	X

COMPUTER BASICS
U2 Exercises: Combination circuits

0	1	0	0	1	**0**	**1**	**0**	**0**	**0**
0	1	0	1	0	**0**	**0**	**1**	**0**	**0**
0	1	0	1	1	**0**	**0**	**0**	**1**	**0**
0	1	1	0	0	**X**	**X**	**X**	**X**	**X**
0	1	1	0	1	**0**	**1**	**1**	**0**	**0**
0	1	1	1	0	**0**	**0**	**1**	**0**	**1**
0	1	1	1	1	**0**	**0**	**1**	**0**	**0**
1	0	0	0	0	**X**	**X**	**X**	**X**	**X**
1	0	0	0	1	**1**	**0**	**0**	**0**	**0**
1	0	0	1	0	**0**	**1**	**0**	**0**	**0**
1	0	0	1	1	**0**	**0**	**1**	**0**	**1**
1	0	1	0	0	**X**	**X**	**X**	**X**	**X**
1	0	1	0	1	**1**	**0**	**1**	**0**	**0**
1	0	1	1	0	**0**	**1**	**0**	**0**	**1**
1	0	1	1	1	**0**	**0**	**1**	**1**	**0**
1	1	0	0	0	**X**	**X**	**X**	**X**	**X**
1	1	0	0	1	**1**	**1**	**0**	**0**	**0**
1	1	0	1	0	**0**	**1**	**1**	**0**	**0**
1	1	0	1	1	**0**	**1**	**0**	**0**	**0**
1	1	1	0	0	**X**	**X**	**X**	**X**	**X**
1	1	1	0	1	**1**	**1**	**1**	**0**	**0**
1	1	1	1	0	**0**	**1**	**1**	**0**	**1**
1	1	1	1	1	**0**	**1**	**0**	**0**	**1**

b) Canonical expression of C0 as a Sum Product: the combinations of the input variables for which the function is worth 0 are included.

$$C_0 = \prod M\ (1,2,3,6,7,9,11,17,18,22,25,27,31)$$

c) Canonical expression of R1 as Sum of Products:

$$R_1 = \sum m\ (11,23)$$

d) To obtain the most simplified expression of C1, Karnaugth maps are used. Given that in this case there are 5 variables, two tables of four variables are made depending on the value of the fifth:

Para A_2=1

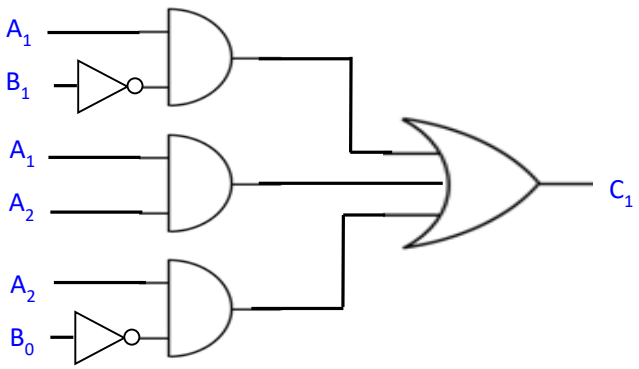
B_1B_0 / A_1A_0	00	01	11	10
00	X	0	0	0
01	X	0	0	0
11	X	1	0	0
10	X	1	0	0

Para A_2=0

B_1B_0 / A_1A_0	00	01	11	10
00	X	0	0	1
01	X	0	0	1
11	X	1	1	1
10	X	1	1	1

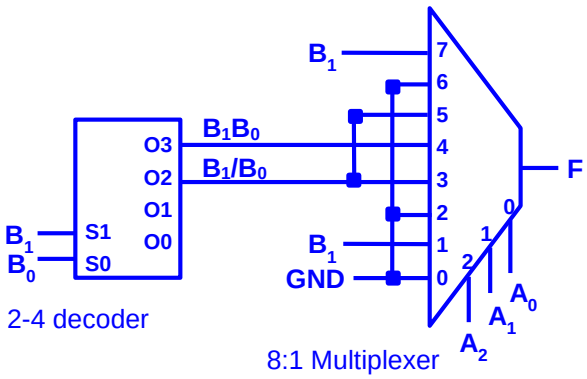
$C_1 = A_1\overline{B_1} + A_2A_1 + A_2\overline{B_0}$ as a sum of products (note that the grouping in yellow relates the two tables)

$C_1 = (A_1 + \overline{B_0})(A_2 + \overline{B_1})$ as a product of sums. Only one was requested, it can be either one of the two.



COMPUTER BASICS
U2 Exercises: Combination circuits

e)



U2_35. We would like to design the controller of the gyro motors of a crane used in construction. For this, the system has two push buttons, one to turn left (PI) and another to turn to the right (PD). To avoid shocks when turning, the system also has two sensors that alert of obstacles, one if the direction of rotation is to the left (OI) and another if it is to the right (OD). In addition, it has an alarm input (ST). The outputs are three, one that activates the left-turning engine (MI), another one on the right (MD) and another that turns on a powerful red alarm light (LA).

The operation is as follows:

- If no pushbutton is activated (active at high level), the motor turn signal is not activated (active at high level) and the light on signal is not activated (active at low level).
- If a pushbutton, and only one, is activated, the corresponding turning motor is activated, provided that the corresponding obstacle sensor (active at low level) is not activated. In this last case, the motor does not activate while the alarm light would activate.
- If the two buttons are activated at the same time, the crane will turn in the direction that the obstacle sensors allow, and the warning light will not turn on. If there is no sensor activated or both are activated, the crane will not move, and the alarm light will come on.
- If the alarm signal is activated (active at low level), it stops any movement of the crane, regardless of the value of the rest of the inputs, turning on the alarm light.

It is requested:

a. Complete the truth table of the system (in the first row of the table, put the variables in the following order, for the entries: ST / PI / PD / OI / OD, and for the outputs: MI / MD / LA.

b. Obtain the most simplified expression of the MI function, as a sum of products, making its implementation with as few logical gates as possible.

c. Implement the LA function using an 8:1 multiplexer and the minimum number of logical gates possible. Point out the value of all the inputs you need from the multiplexer.

a)

ST	PI	PD	OI	OD	MI	MD	LA
0	X	X	X	X	**0**	**0**	**0**
1	0	0	0	0	**0**	**0**	**1**
1	0	0	0	1	**0**	**0**	**1**
1	0	0	1	0	**0**	**0**	**1**
1	0	0	1	1	**0**	**0**	**1**
1	0	1	0	0	**0**	**0**	**0**
1	0	1	0	1	**0**	**1**	**1**
1	0	1	1	0	**0**	**0**	**0**

COMPUTER BASICS
U2 Exercises: Combination circuits

1	0	1	1	1	**0**	**1**	**1**
1	1	0	0	0	**0**	**0**	**0**
1	1	0	0	1	**0**	**0**	**0**
1	1	0	1	0	**1**	**0**	**1**
1	1	0	1	1	**1**	**0**	**1**
1	1	1	0	0	**0**	**0**	**0**
1	1	1	0	1	**0**	**1**	**1**
1	1	1	1	0	**1**	**0**	**1**
1	1	1	1	1	**0**	**0**	**0**

b)

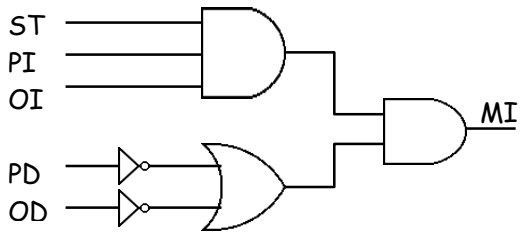
Para ST=0

OI OD / PI PD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

Para ST=1

OI OD / PI PD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	1
10	0	0	1	1

$$MI = ST.PI.OI.\overline{PD} + ST.PI.OI.\overline{OD}$$



COMPUTER BASICS
U2 Exercises: Combination circuits

c)