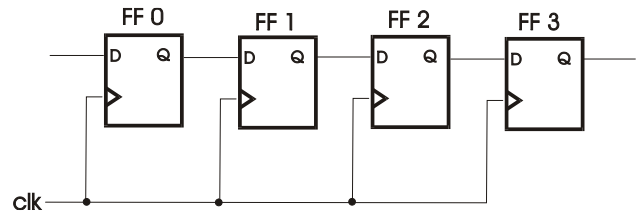


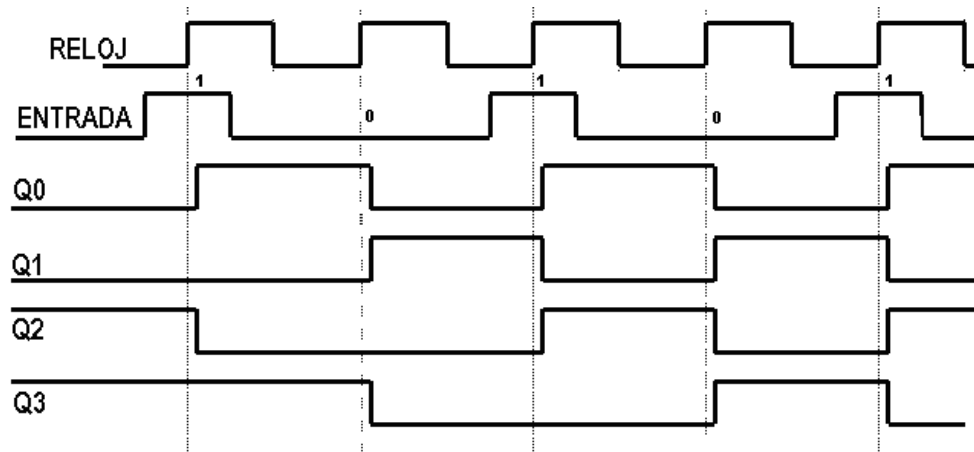
## Computer Basics

### Problems U3: Basic elements of sequential logic

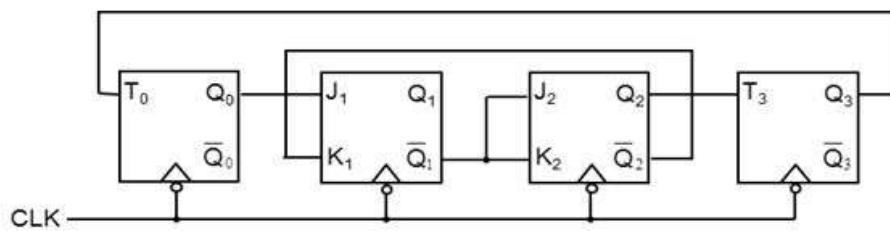
**U3\_1.** In the sequential system of the attached figure, it is assumed that initially  $Q_0 = Q_1 = 0$  and  $Q_2 = Q_3 = 1$ . Draw the output signal of each FF block, if an input sequence 10101 is applied to the input of FF0 (D0), synchronously with the clock signal clk.



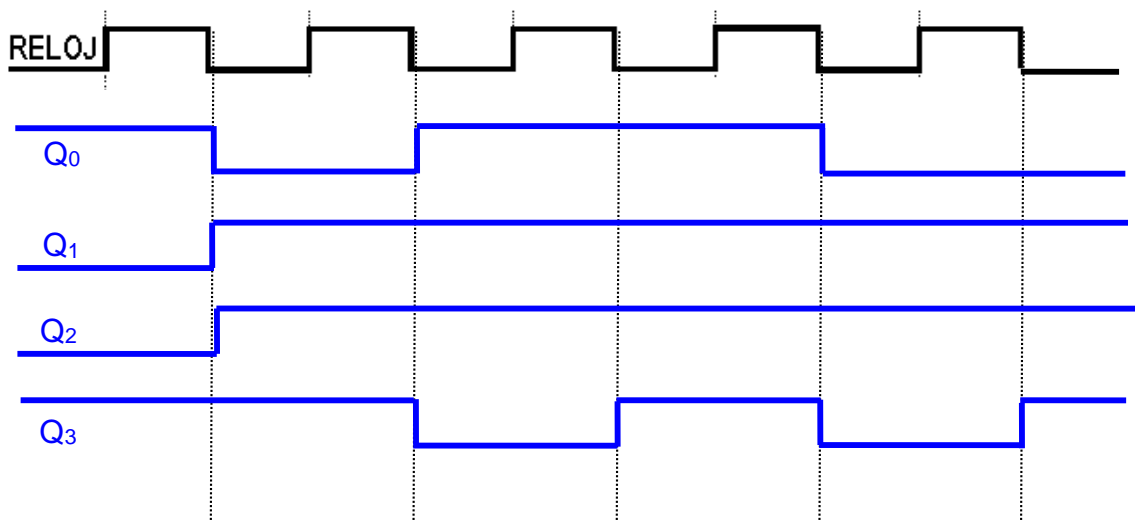
**Solution:**



**U3\_2.** In the sequential system of the figure, it is assumed that initially  $Q_0 = Q_3 = 1$ ,  $Q_1 = Q_2 = 0$ . Draw in a time diagram the output signals for the flip-flops 0, 1, 2 and 3 during five clock cycles.



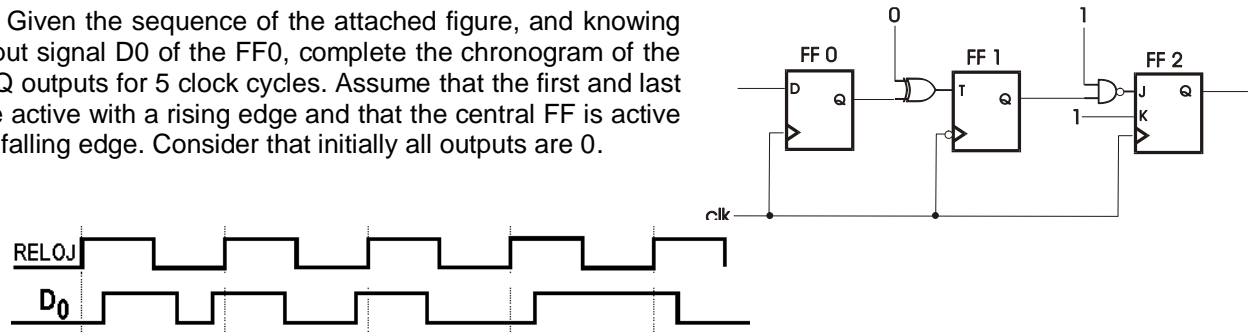
**Solution:**



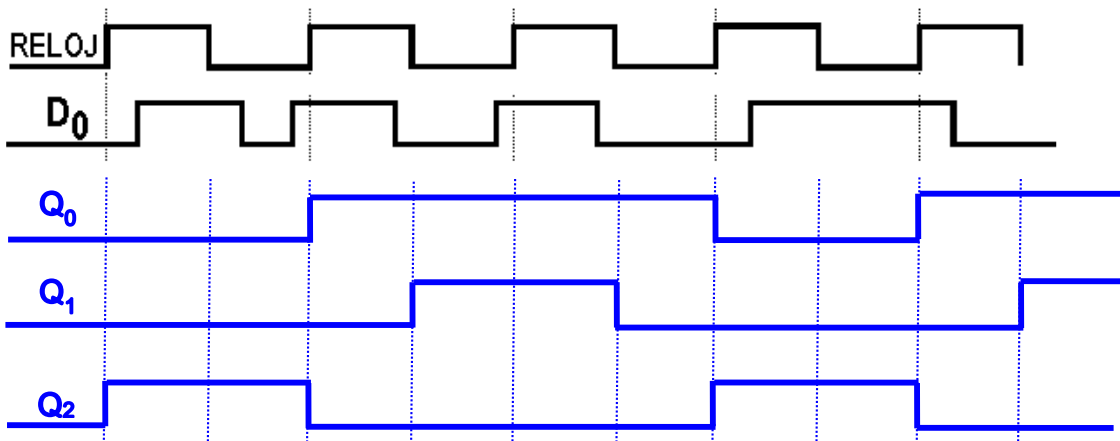
## Computer Basics

### Problems U3: Basic elements of sequential logic

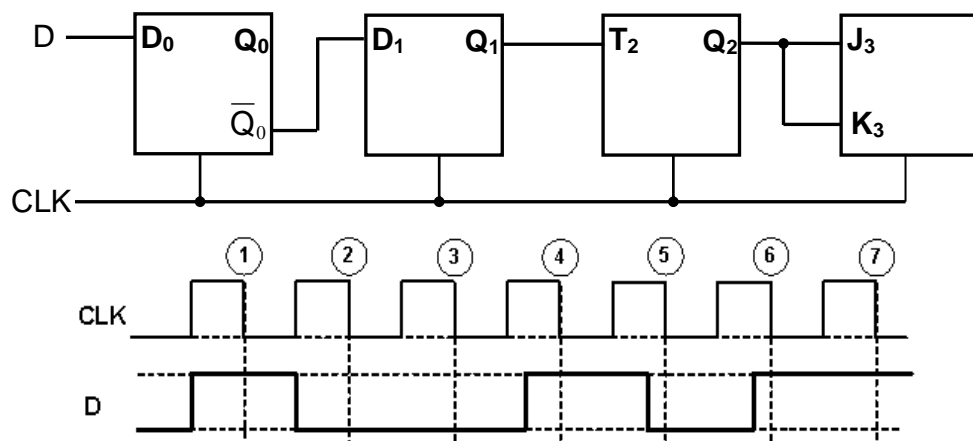
**U3\_3.** Given the sequence of the attached figure, and knowing the input signal D0 of the FF0, complete the chronogram of the three Q outputs for 5 clock cycles. Assume that the first and last FF are active with a rising edge and that the central FF is active with a falling edge. Consider that initially all outputs are 0.



**Solution:**

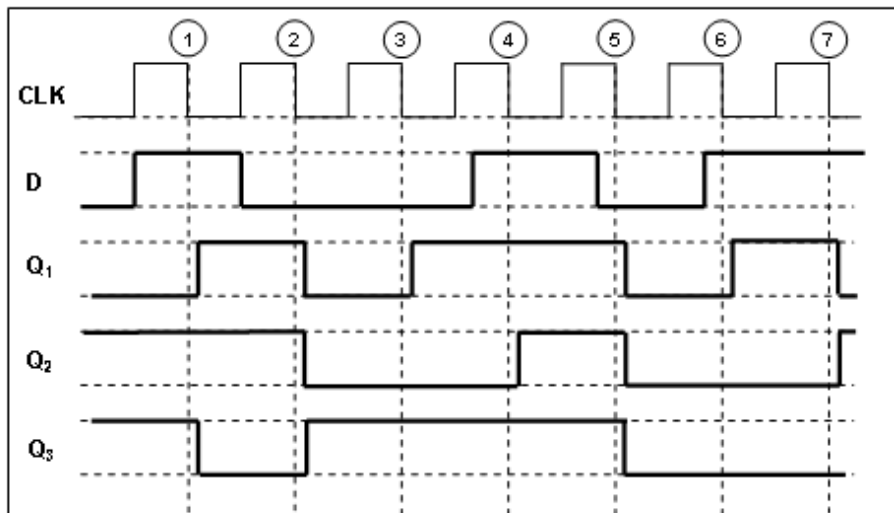


**U3\_4.** In the 4 flip-flops (FF) in the figure, it is assumed that initially  $Q_0 = Q_1 = 0$ ,  $Q_2 = Q_3 = 1$ . Draw the output signal of each flip-flop if the input sequence D is applied to D0 synchronously with the clock in a time diagram. Note that all FFs are activated by clock falling edge.

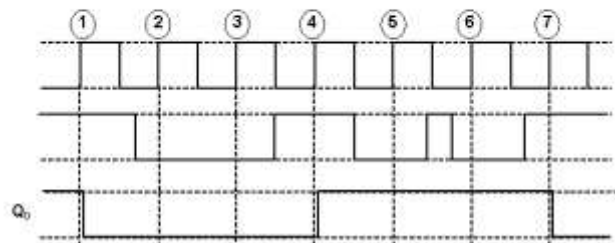
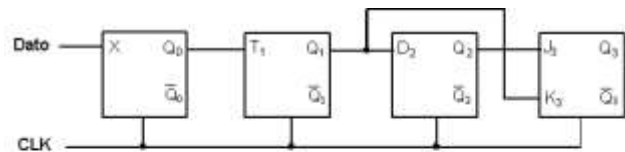


**Computer Basics**  
**Problems U3: Basic elements of sequential logic**

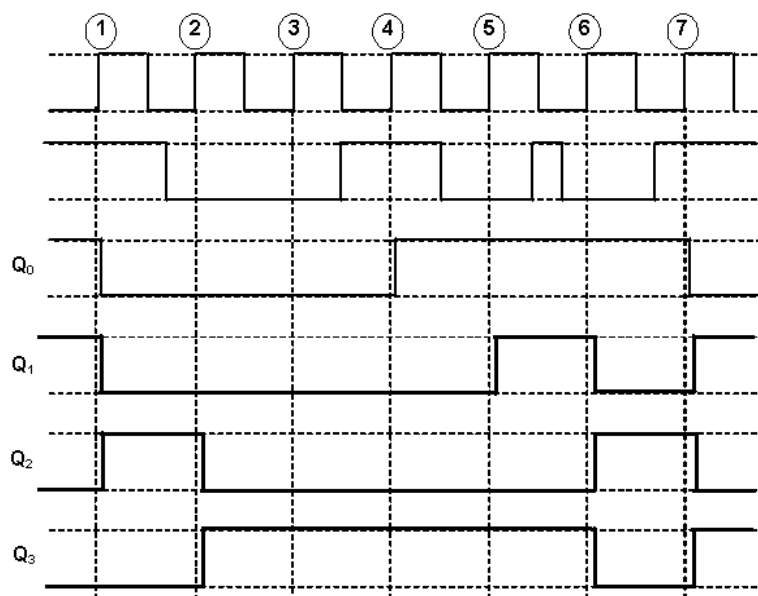
**Solution:**



**U3\_5.** In the sequence of the figure, it is assumed that initially  $Q_0 = Q_1 = 1$  and  $Q_2 = Q_3 = 0$ . Draw the output signal of the FF 1,2 and 3 in the time diagram and reasonably indicate which type of FF is 0 (the first on the left). Flip-flops are activated by rising clock edge.



**Solution:**

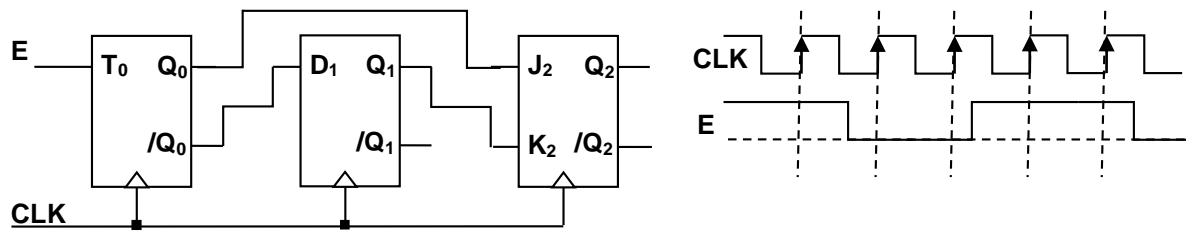


**U3\_6.** Given the sequence of flip-flops in the figure, complete the attached time diagram. Assume that all flip-

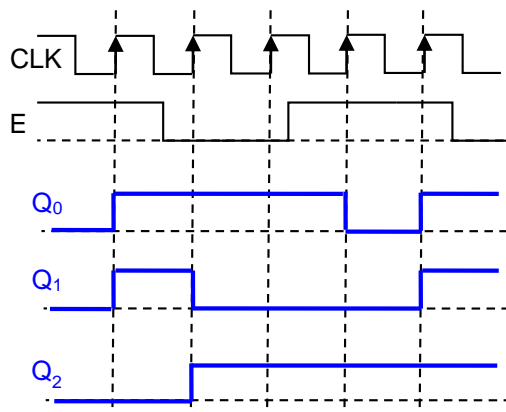
## Computer Basics

### Problems U3: Basic elements of sequential logic

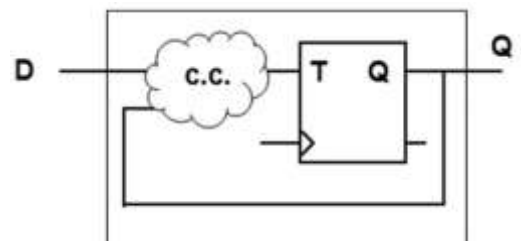
flops are initially in the state  $Q_i = '0'$ .



**Solution:**



**U3\_7.** Indicate the combinational circuit that allows to build a type D flip-flop from a type T flip-flop..



**Solution:**

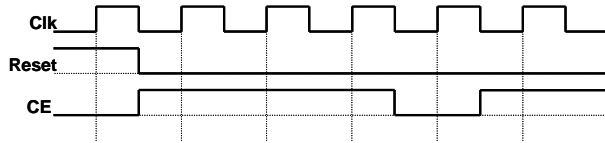
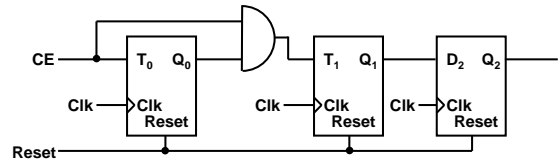
$D^n$	$Q^n$	$Q^{n+1}$	$T^n$
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

$$T^n = D^n \oplus Q^n$$

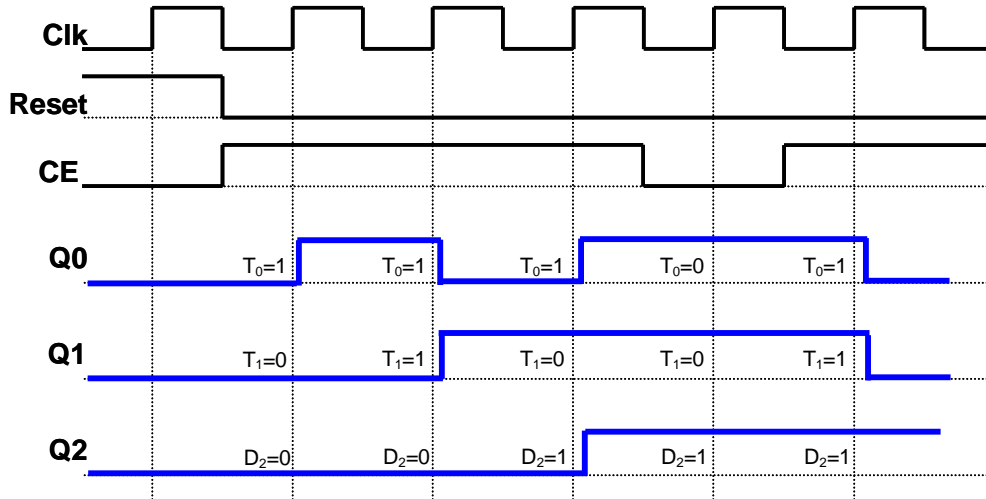
## Computer Basics

### Problems U3: Basic elements of sequential logic

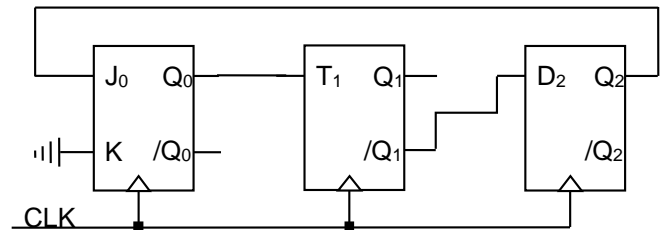
**U3\_8.** Given the circuit of the figure, and knowing that the reset is asynchronous, active by high level and initializes all the flip-flops to '0', fill the attached time diagram.



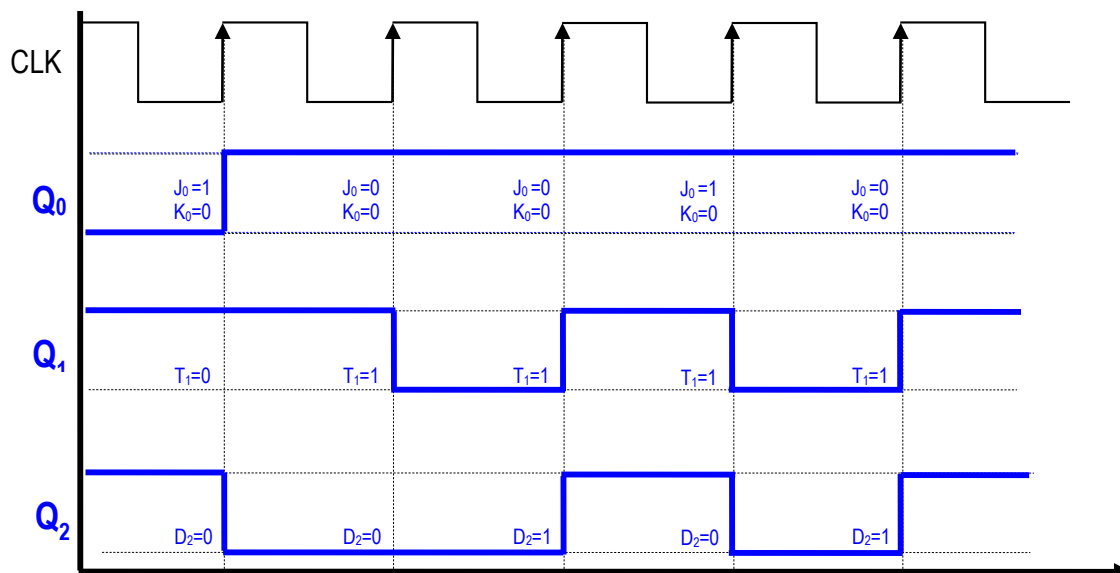
**Solution:**



**U3\_9.** From the diagram of the figure, draw a chronogram for 5 complete clock cycles. The initial values for the flip-flops are  $Q_0 = 0$ ,  $Q_1 = 1$  and  $Q_2 = 1$

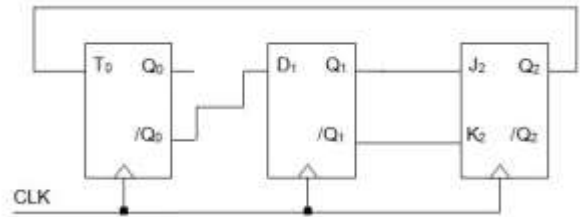


**Solution:**

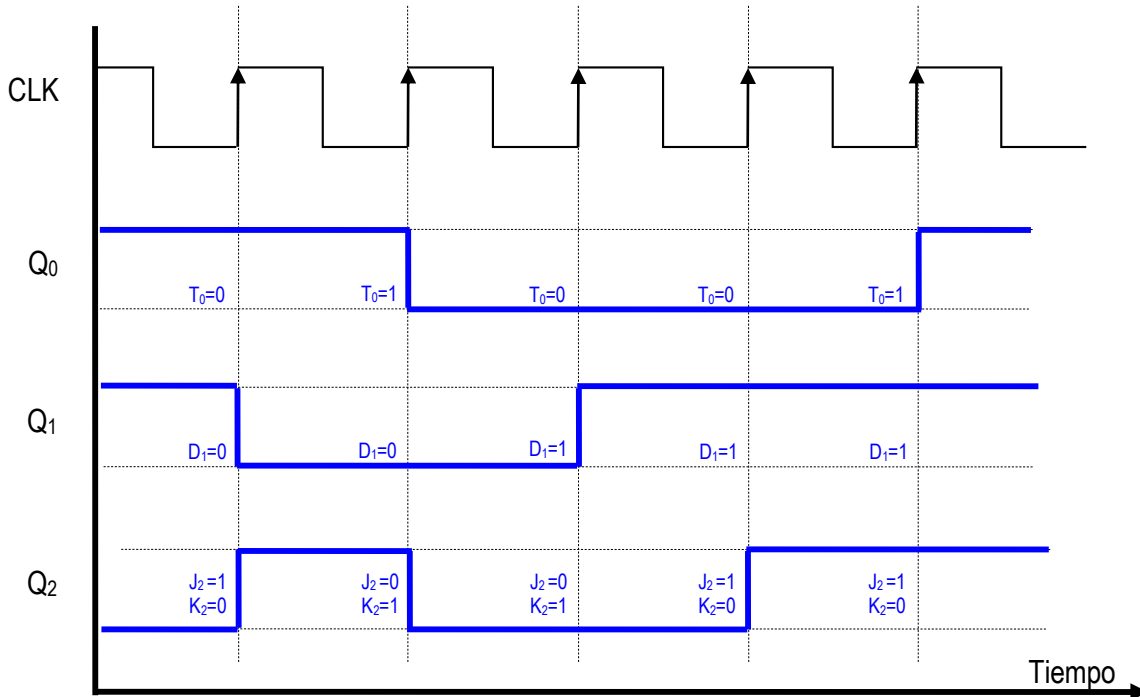


**Computer Basics**  
**Problems U3: Basic elements of sequential logic**

**U3\_10.** From the diagram of the figure, draw a chronogram for 5 complete clock cycles. The initial values for the flip-flops are  $Q_0 = 1$ ,  $Q_1 = 1$  and  $Q_2 = 0$



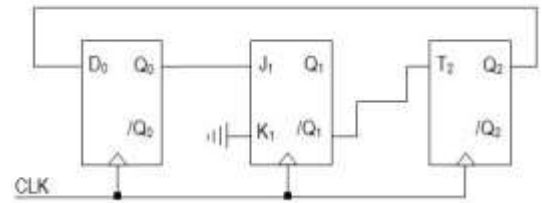
**Solution:**



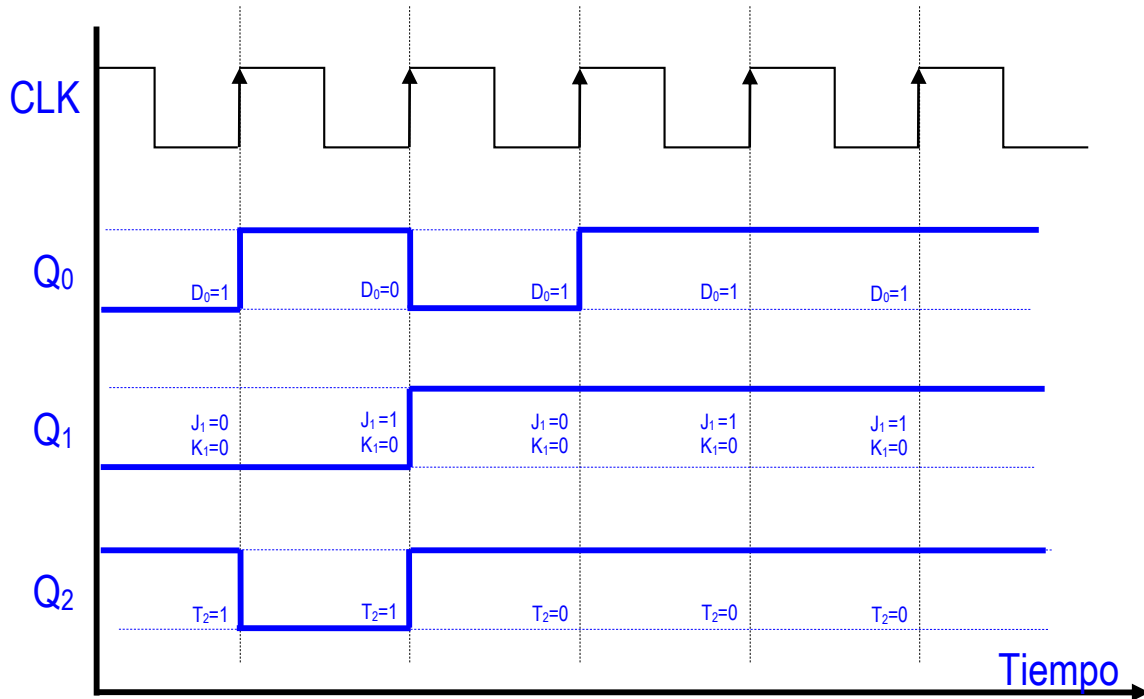
## Computer Basics

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**U3\_11.** From the diagram in the figure, it is requested to draw a chronogram for 5 complete clock cycles. The initial values for the flip-flops are  $Q_0 = 0$ ,  $Q_1 = 0$  and  $Q_2 = 1$



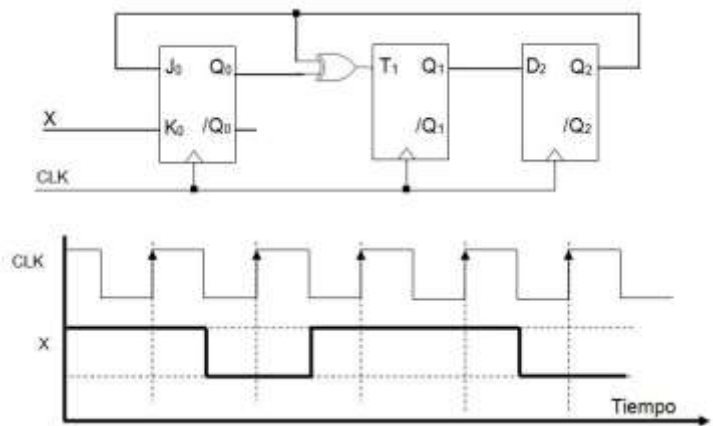
**Solution:**



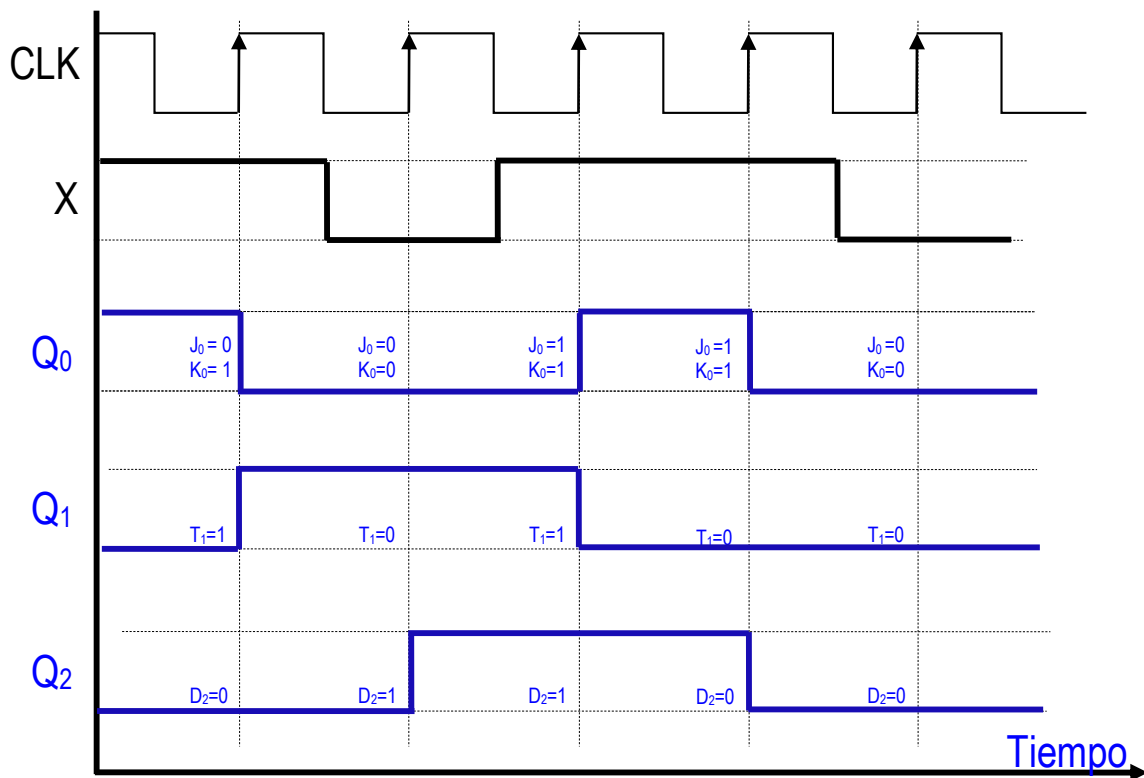
## Computer Basics

### Problems U3: Basic elements of sequential logic

**U3\_12.** From the diagram in the figure, complete the attached schedule for the 5 clock cycles indicated. As indicated in the schedule, the initial values for the flip-flops are  $Q_0 = 1$ ,  $Q_1 = 0$  and  $Q_2 = 0$



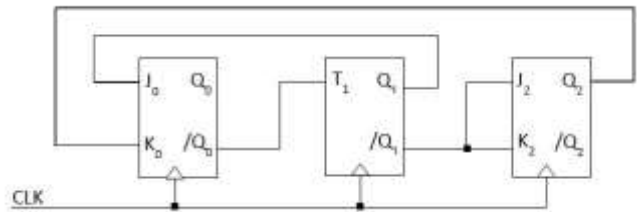
**Solution:**



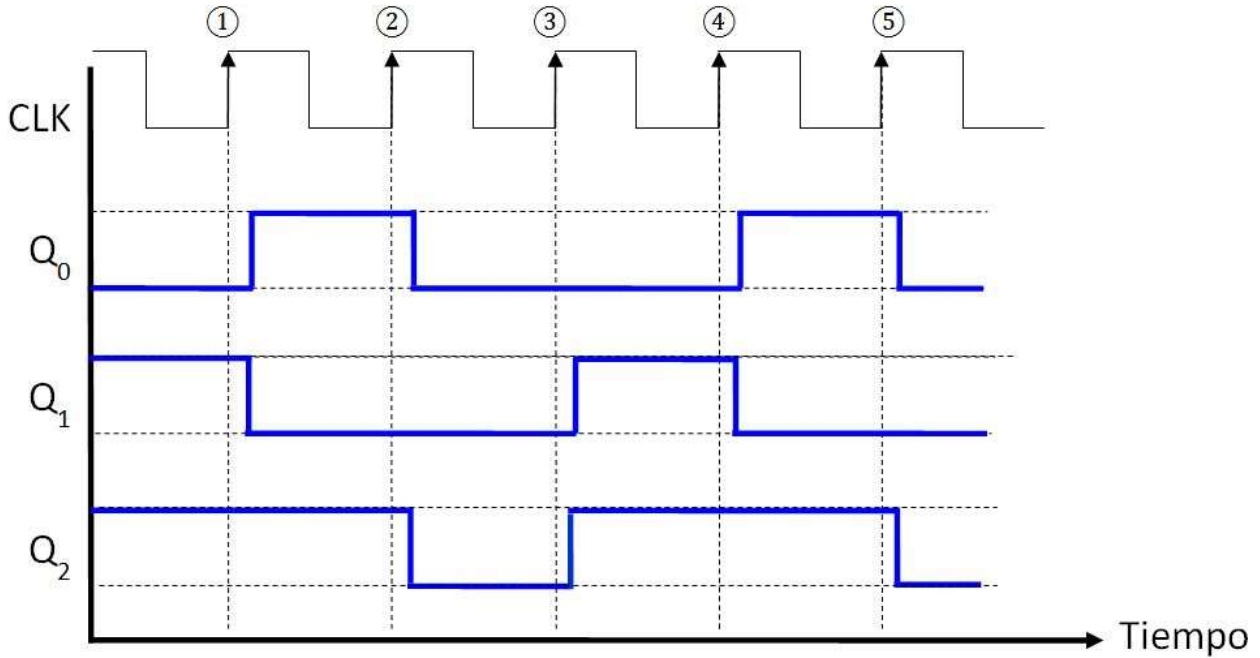


# **Computer Basics** **Problems U3: Basic elements of sequential logic**

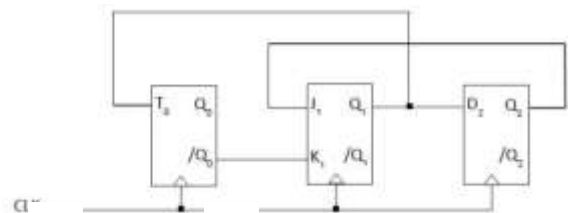
**U3\_13.** Given the sequential circuit of the figure, design a chronogram for 5 clock cycles. The initial values for the flip-flops are  $Q_0 = 0$ ,  $Q_1 = 1$  and  $Q_2 = 1$



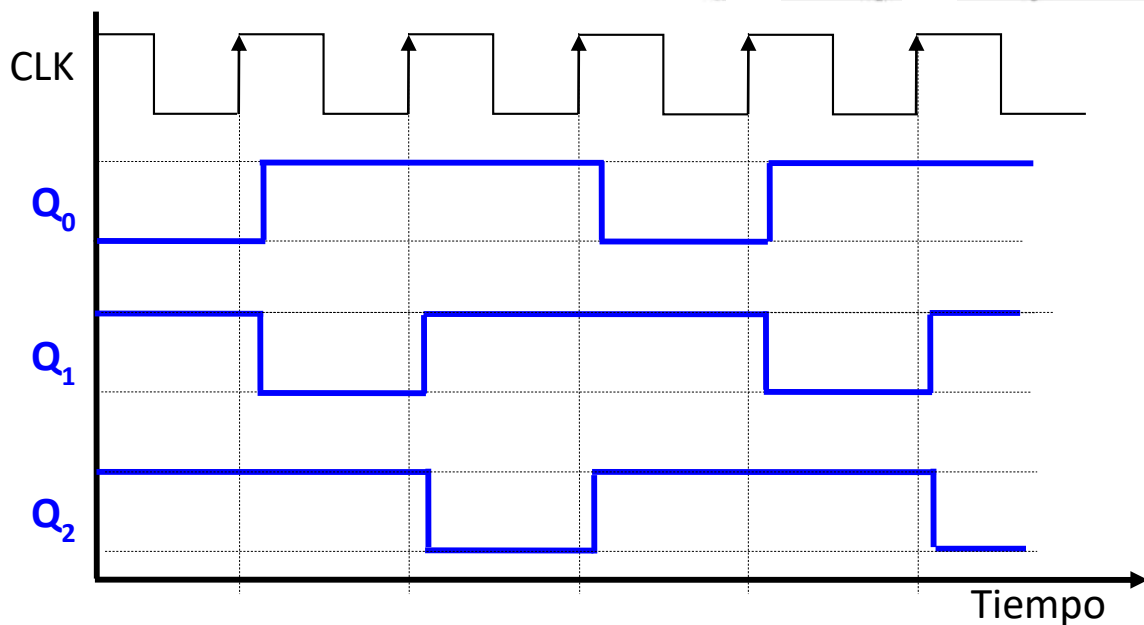
**Solution:**



**U3\_14.** From the diagram of the figure, make a chronogram for 5 clock cycles. The initial values for the flip-flops are  $Q_0 = 0$ ,  $Q_1 = 1$  and  $Q_2 = 1$



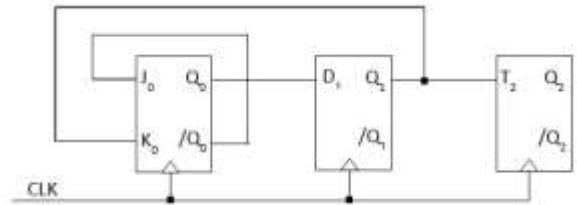
**Solution:**



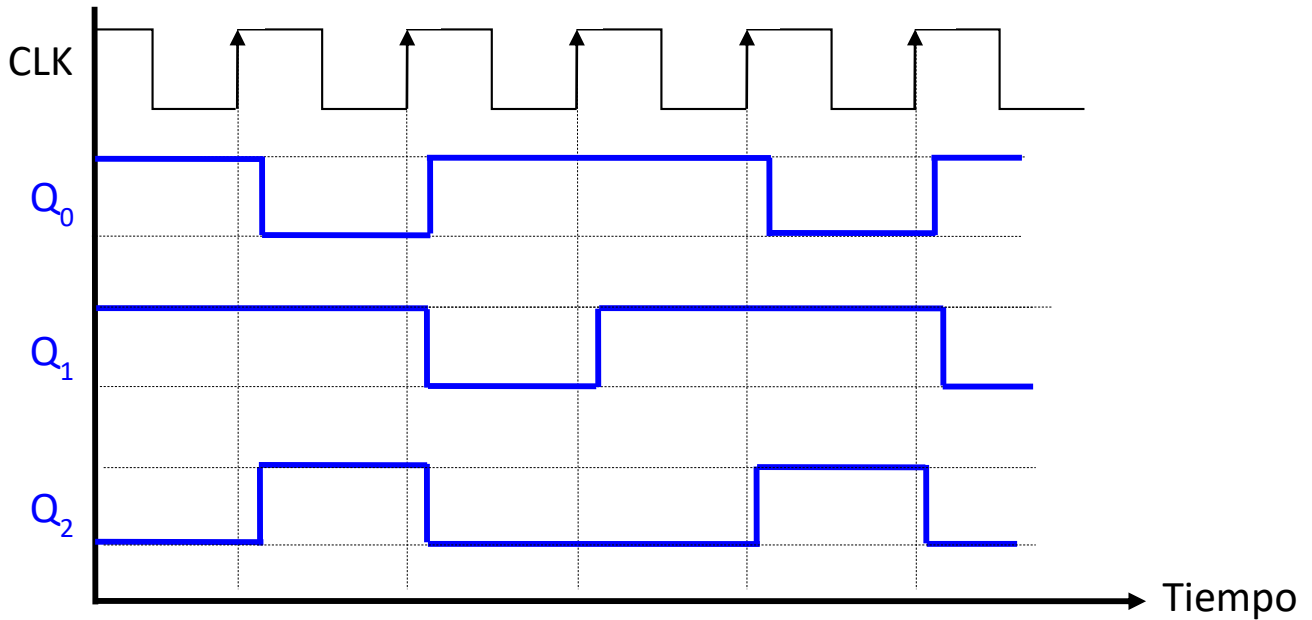
## Computer Basics

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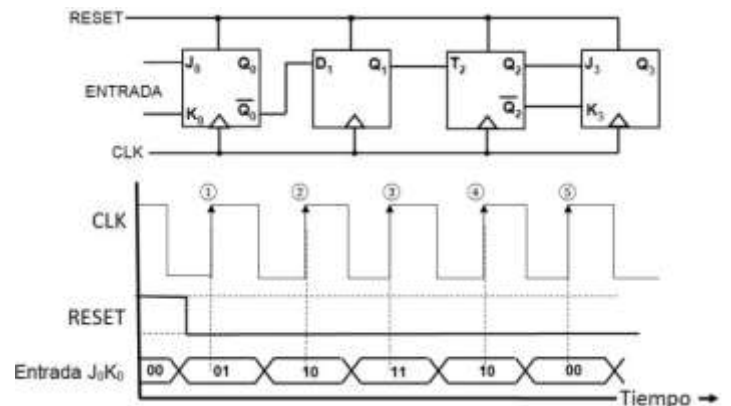
**U3\_15.** From the diagram of the figure, make a chronogram for 5 clock cycles. The initial values for the flip-flops are  $Q_0 = 1$ ,  $Q_1 = 1$  y  $Q_2 = 0$



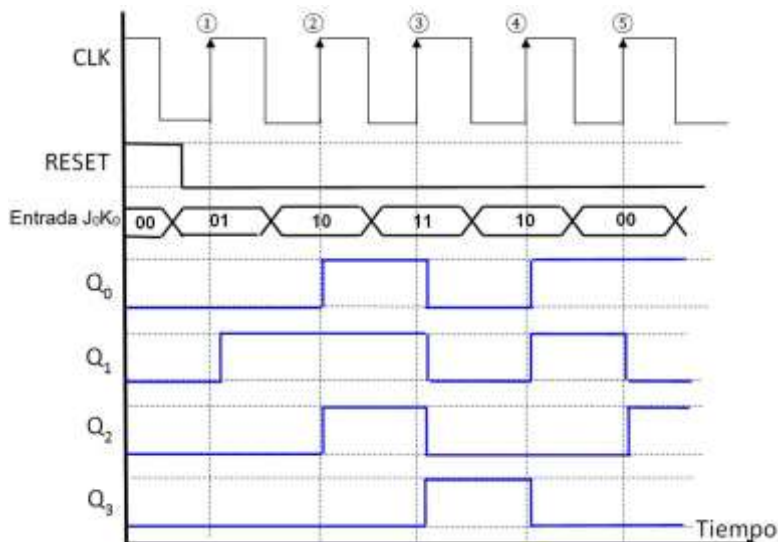
**Solution:**



**U3\_16.** The 4-bit register of the figure is formed by 4 FF of different types. It is requested to complete the diagram for the outputs  $Q_0$ ,  $Q_1$ ,  $Q_2$  y  $Q_3$ . Note: The Reset is asynchronous.



**Solution:**

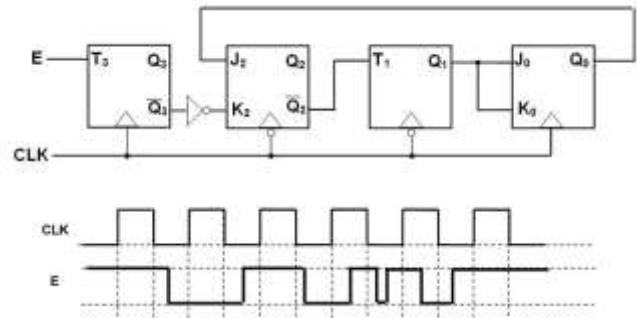


## Computer Basics

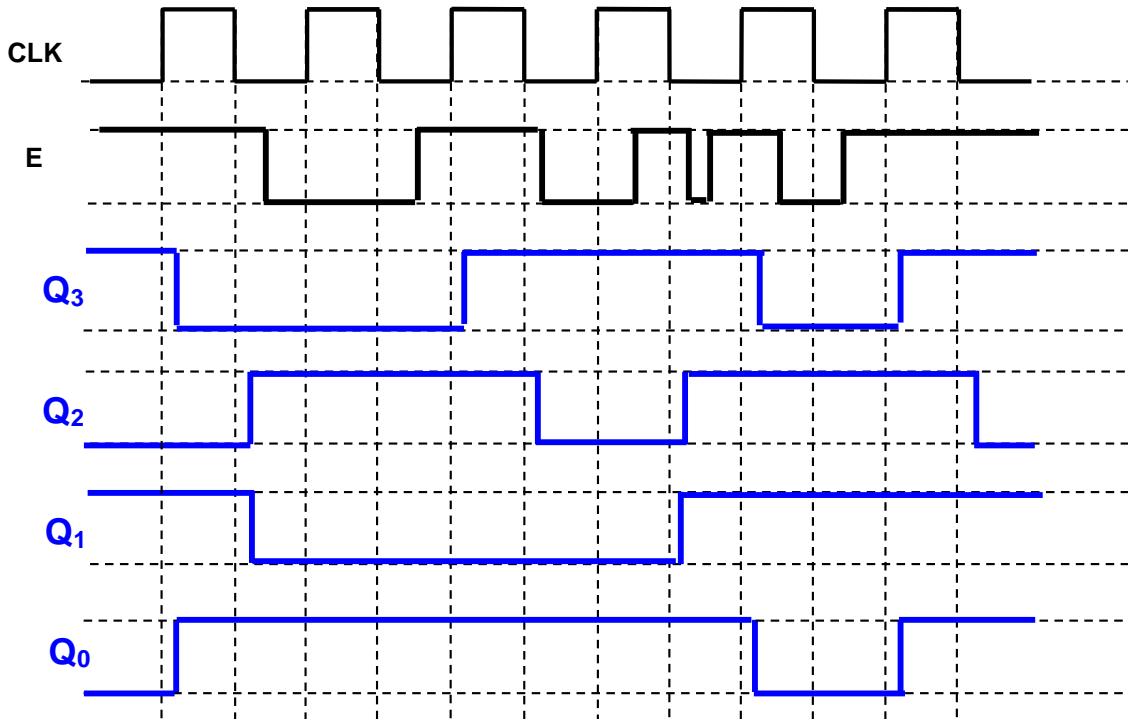
### Problems U3: Basic elements of sequential logic

**U3\_17.** Complete the schedule of the attached figure, knowing that in the initial state the values of the flip-flops are:  $Q_3=Q_1=1$  y  $Q_2=Q_0=0$

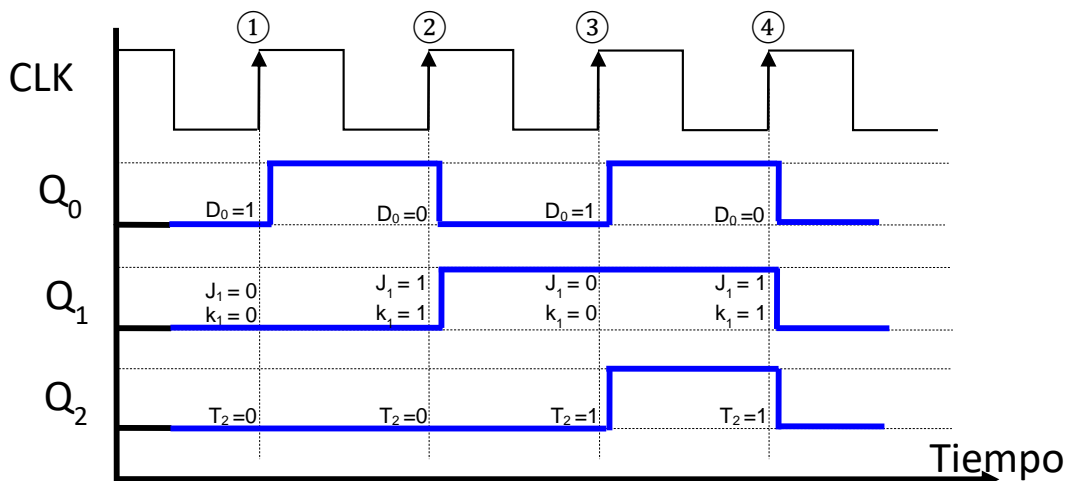
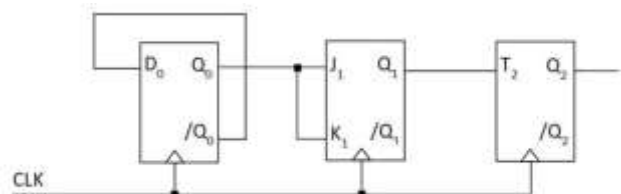
**Note:** Take into account the appropriate flank activation of each FF



**Solution:**



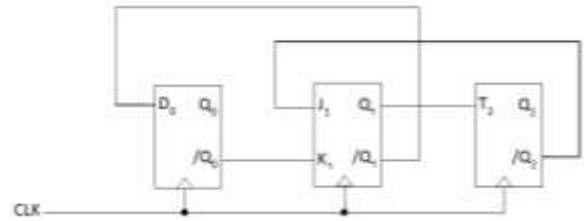
**U3\_18.** Given the following circuit, represent 4 consecutive clock cycles in the facilitated schedule, knowing that the initial state is  $Q_0 = Q_1 = Q_2 = 0$ .



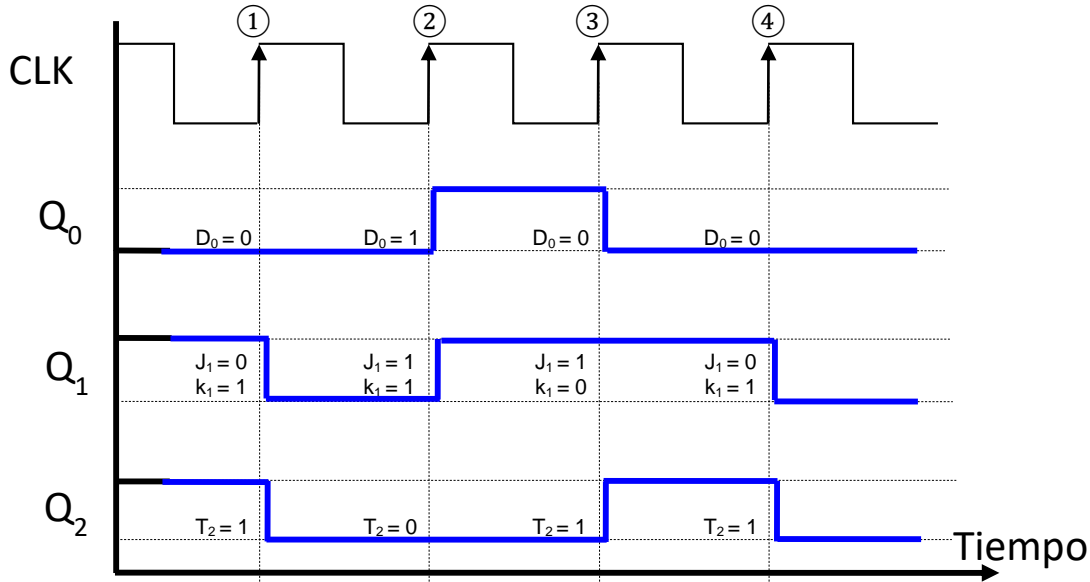
## Computer Basics

### Problems U3: Basic elements of sequential logic

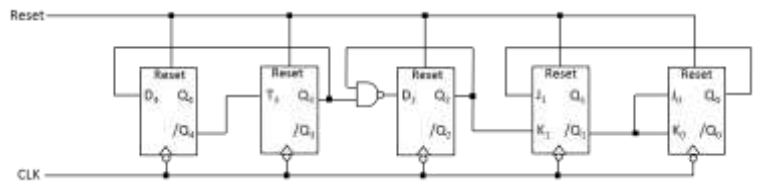
**U3\_19.** Given the circuit in the attached figure, and starting from the indicated initial state, complete the given schedule for the 4 clock cycles indicated. The initial states are:  $Q_0 = 0$ ,  $Q_1 = Q_2 = 1$



**Solution:**



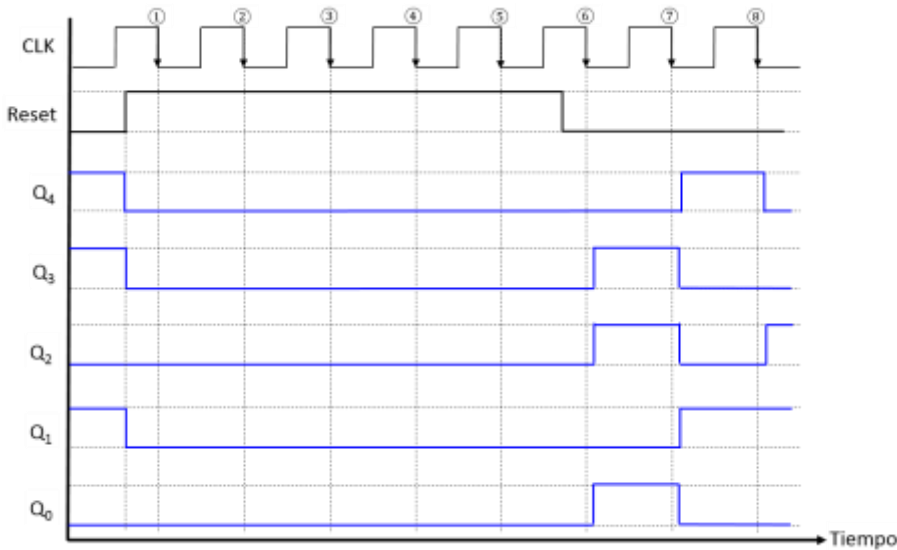
**U3\_20.** In the sequential system of the attached figure, it is assumed that initially  $Q_0 = Q_2 = 0$  y  $Q_1 = Q_3 = Q_4 = 1$ . Complete the attached schedule with the output signal of each FF, knowing that the reset signal is asynchronous.



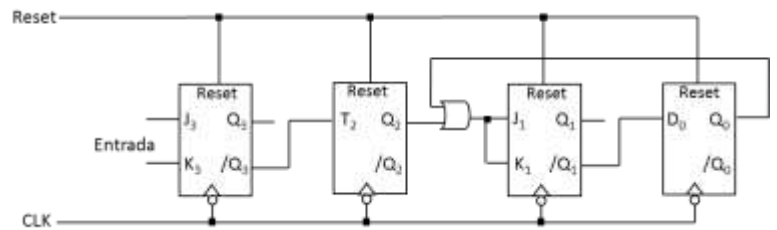
**Solution:**

## Computer Basics

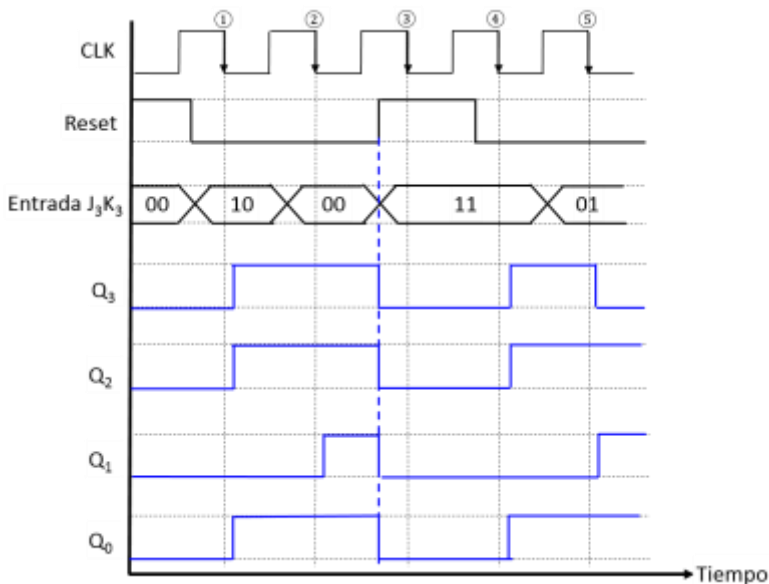
### Problems U3: Basic elements of sequential logic



**U3\_21.** Given the sequential system of the attached figure, complete the given schedule with the output signal of each FF, knowing that the reset signal is asynchronous.



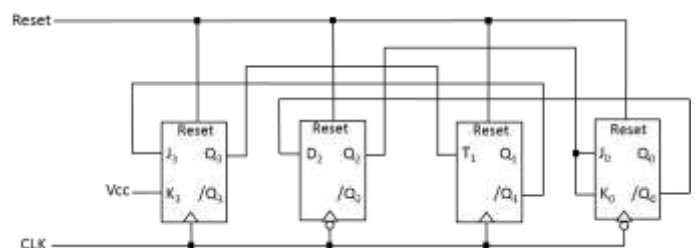
**Solution:**



**U3\_22.** Given the sequential system of the attached figure, complete the given diagram with the output signal of each FF.

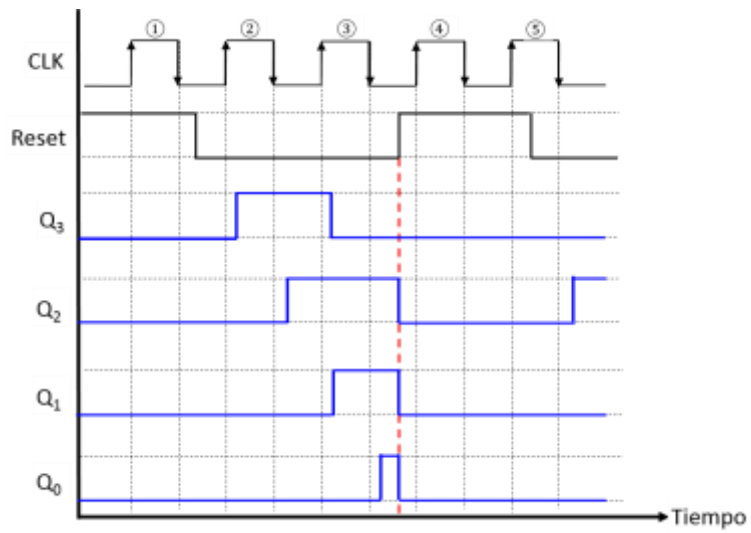
**Notes:**

- The Reset signal is **asynchronous**
- Consider the operation of each FF on its corresponding clock edge

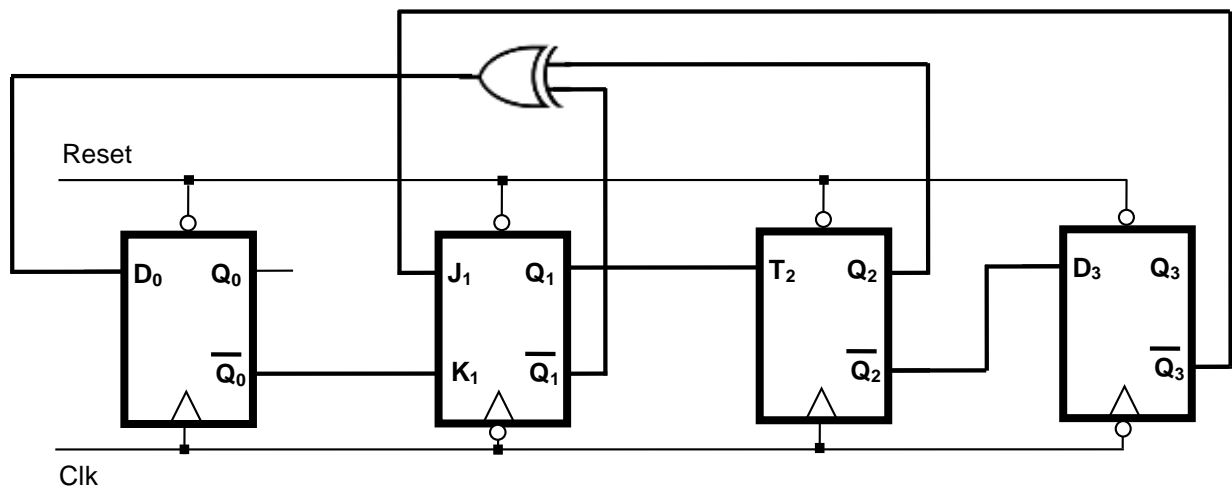


**Computer Basics**  
**Problems U3: Basic elements of sequential logic**

**Solution:**



**U3\_23.** Given the sequential system of the attached figure, complete the given diagram with the output signal of each FF, knowing that the Reset signal is asynchronous.  
 NOTE: Attention to the clock edge of each of the FF.



**Solution**

**Computer Basics**  
**Problems U3: Basic elements of sequential logic**

