Basic elements in sequential logic

Computer Fundamentals

Escuela Politécnica Superior U.A.M

Parte del material utilizado en este capítulo ha sido cedido por el grupo DIE de la ETSII de la UPM

Summary of the lecture

U3. Basic elements in sequential logic.

U3.1. Sequential Circuits.

U3.2. Latch. Types of latches.

U3.3. Flip-Flop. Types of Flip-Flops.

U3.4. Circuits with Flip-Flops.

Timing diagrams.

U3.5. Registers. Shift registers.

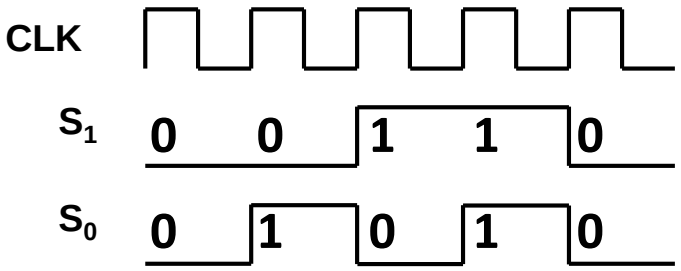
Escuela Politécnica Superior

Sequential Circuits

Motivation:

There are problems that can not be solved following a combinational approach

Example: Build a circuit to count the transitions of aninput signal (CLK).



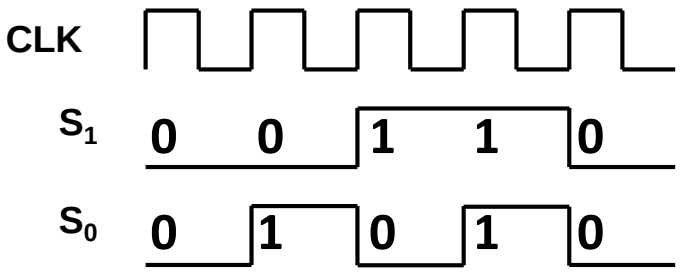
S_1 and S_0 functions can not be implemented using an standard combinational approach the same output is reached for the same input.

Solution:

We need a new type of circuit in which the "next" output is a function of the inputs and the "previous" output value.

Escuela Politécnica Superior

Sequential Circuits



COMBINATIONAL

CLK	S_1	S_0
0	0	0
1	0	1
0	0	0
1	0	1

Let's take into account the previous input value

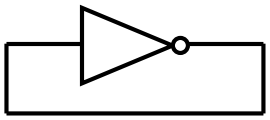
SEQUENTIAL

S_1	S_0	CLK	$S'_1S'_0$
0	0	↓	0 1
0	1	↓	1 0
1	0	↓	1 1
1	1	↓	0 0

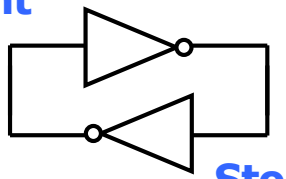
How to?:

- We need memory
- We need feedback (output signal is also an input) … but how can we create and stable system

Unstable feedback logic element



Stable feedback logic element



Stores (in memory) a '0' or a'1'

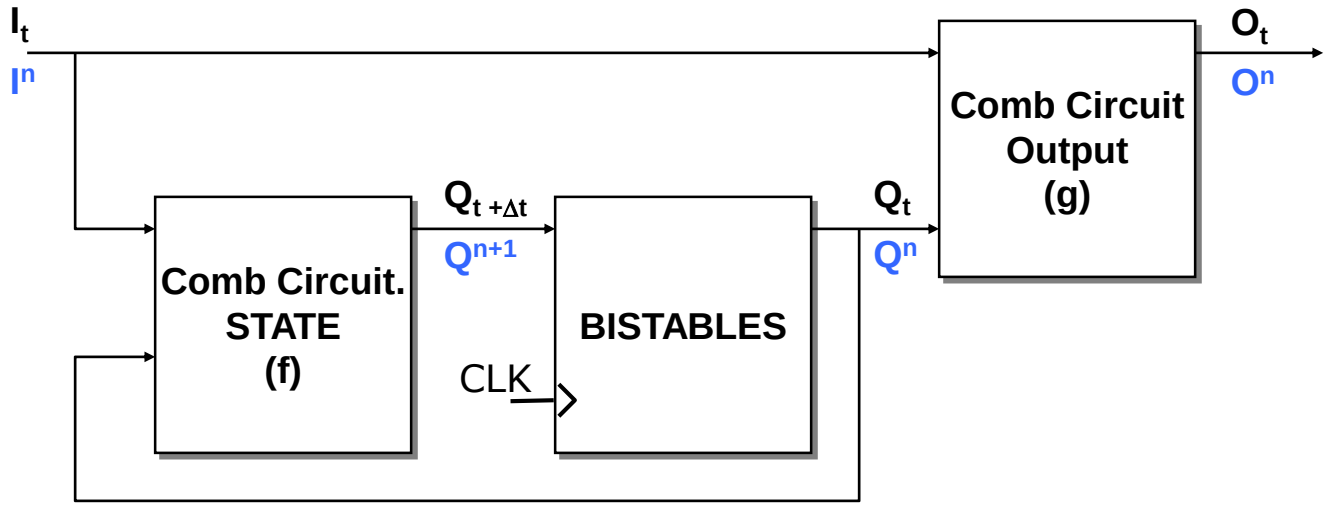
Escuela Politécnica Superior

Sequential Circuits

Formal Definition

In a sequential circuit the outputs are dependent on the inputs and on the previous state.

- ✓The value of the "previous" state is stored in elements with memory capacity.
- ✓Each bit of information about the previous state is stored in a flip-flop.

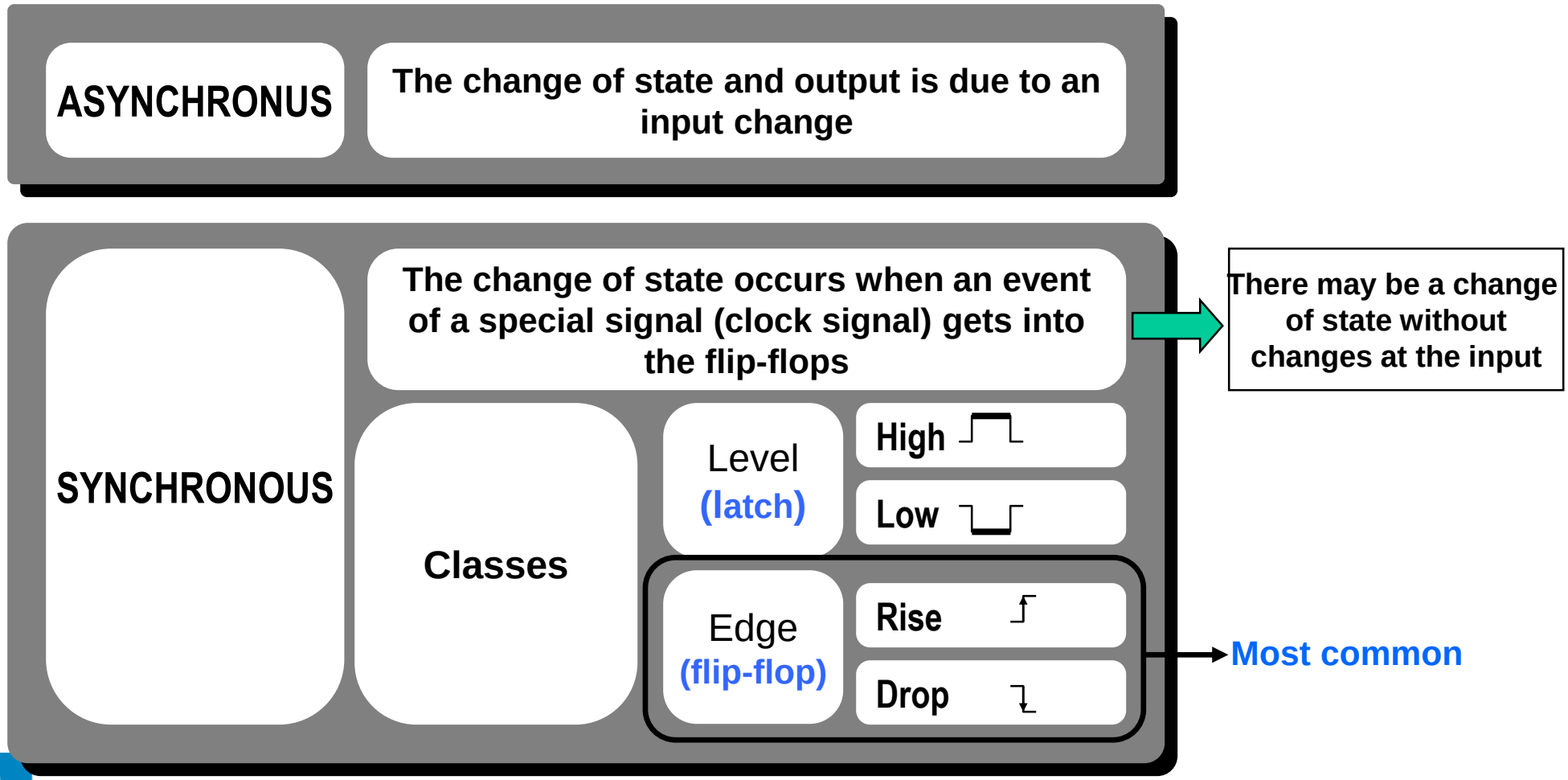


$Q_{t+\Delta t} = f(I_t, Q_t)$ **STATE equations** ← **TEMPORARY EVOLUTION**

$O_t = g(I_t, Q_t)$ **OUTPUT equation** ← **INSTANTANEOUS VALUES**

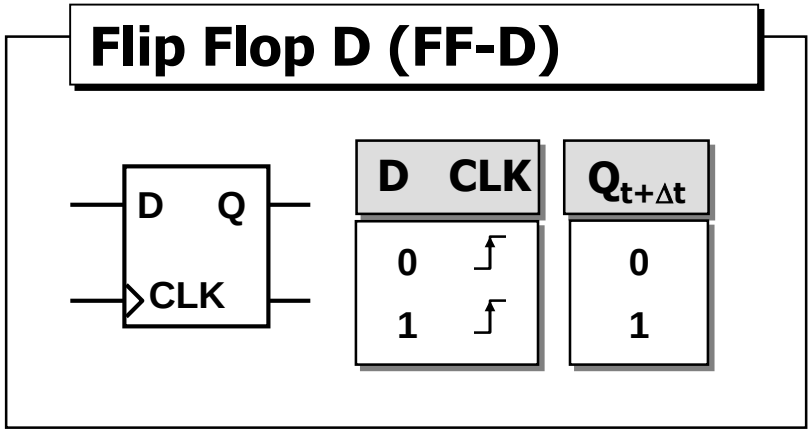
Escuela Politécnica Superior

Asynchronus and Synchronous sequential logic

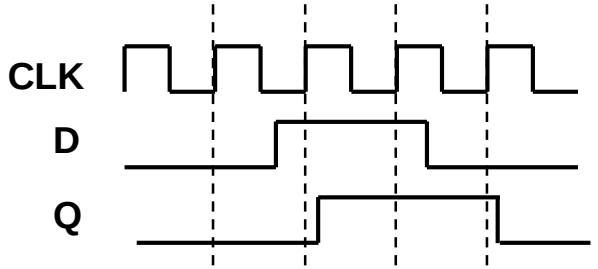


Escuela Politécnica Superior

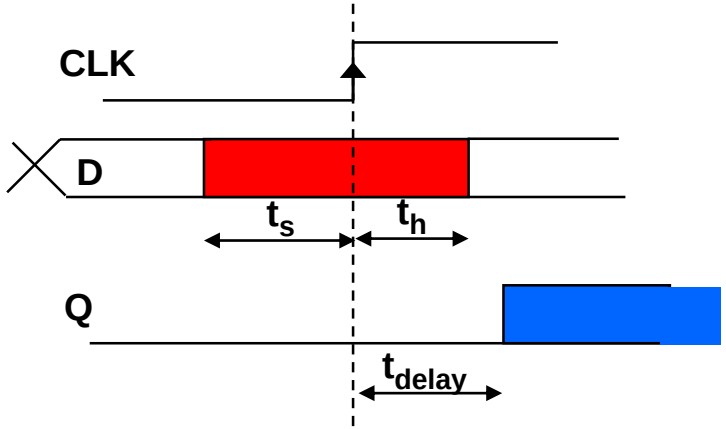
Flip Flop D



Timing diagram of a D type flip-flop



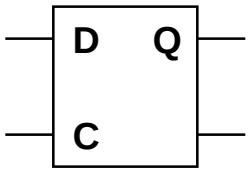
Important timing parameters: t_{setup}, t_{hold} y t_{delay}



Escuela Politécnica Superior

Other Flip Flops

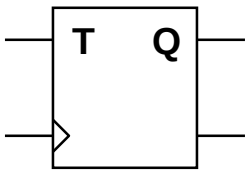
Latch D



D	C	Q^{n+1}	
X	0	Q^n	Closed
0	1	0	Transparent mode
1	1	1	

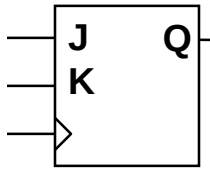
Synchronous by level

Flip-Flop FF-T



T	CLK	Q^{n+1}
0	↑	Q^n
1	↑	$/Q^n$

Flip-Flop FF-JK

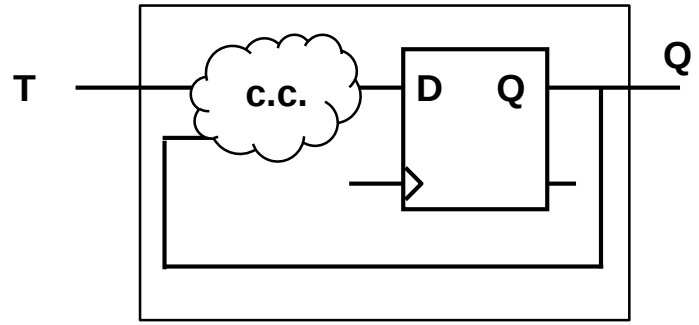


J	K	CLK	Q^{n+1}
0	0	↑	Q^n
0	1	↑	0
1	0	↑	1
1	1	↑	$/Q^n$

Escuela Politécnica Superior

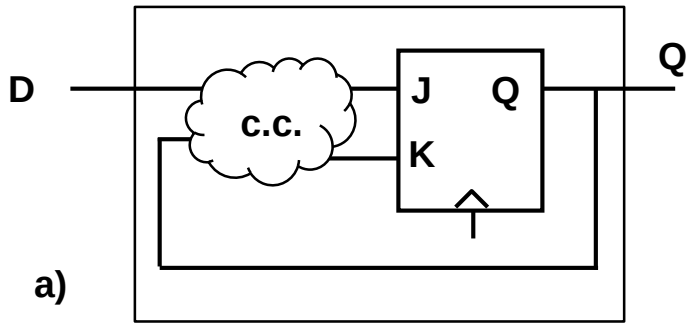
Conversion among Flip-Flops

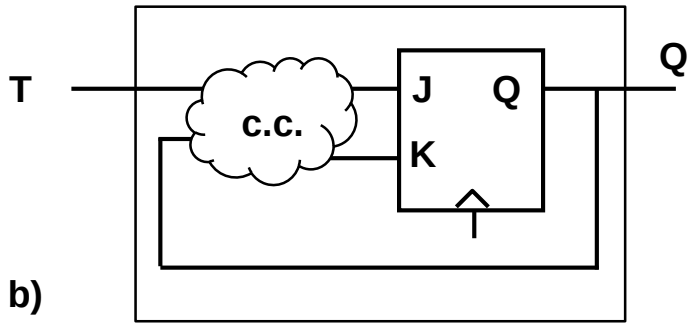
Example: from a flip-flop D, build a flip-flop T



T	Q^n	Q^{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

Example: from a flip-flop JK, build **a)** a flip-flop D y **b)** a flip-flop T





Escuela Politécnica Superior

Initialization of a Flip-Flop

	0	1
ASYNCHRONOUS	reset	preset
SYNCHRONOUS	clear	set

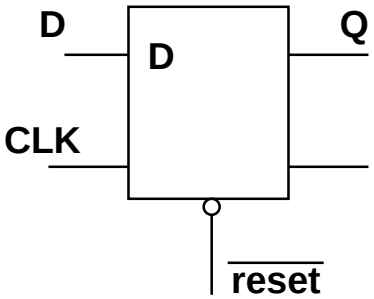
The initial value can be ‘0’ or ‘1’

The asynchronous initialization is immediate

The synchronous initialization occurs in synchrony with the CLK

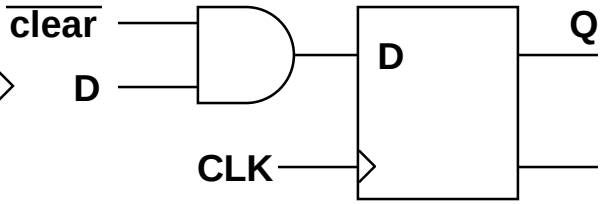
Initialization signals are generally active at low level

Example:
Flip-Flop D with reset



The synchronous initialization can be considered as part of its functionalities

Example:
Flip-Flop D with clear

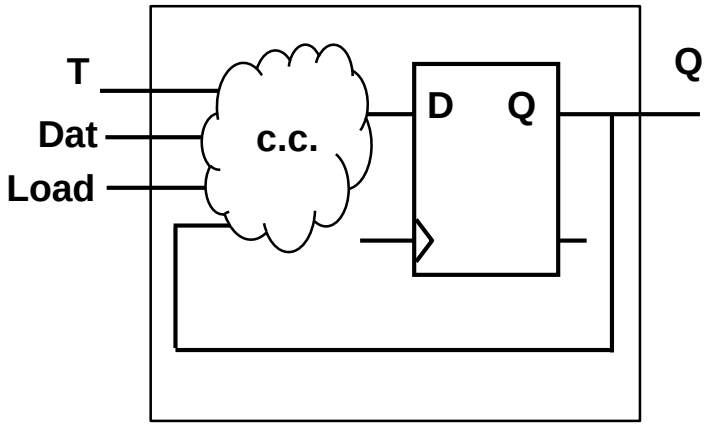


Escuela Politécnica Superior

Application: Loading a Flip-Flop

In the synchronous Flip-Flops, it is possible to load a '0' or a '1' by means of a special input known as "L" (Load). Similar to *enable* in the combinational circuits.

Example: from a flip-flop D, build a flip-flop T with Load Functionality



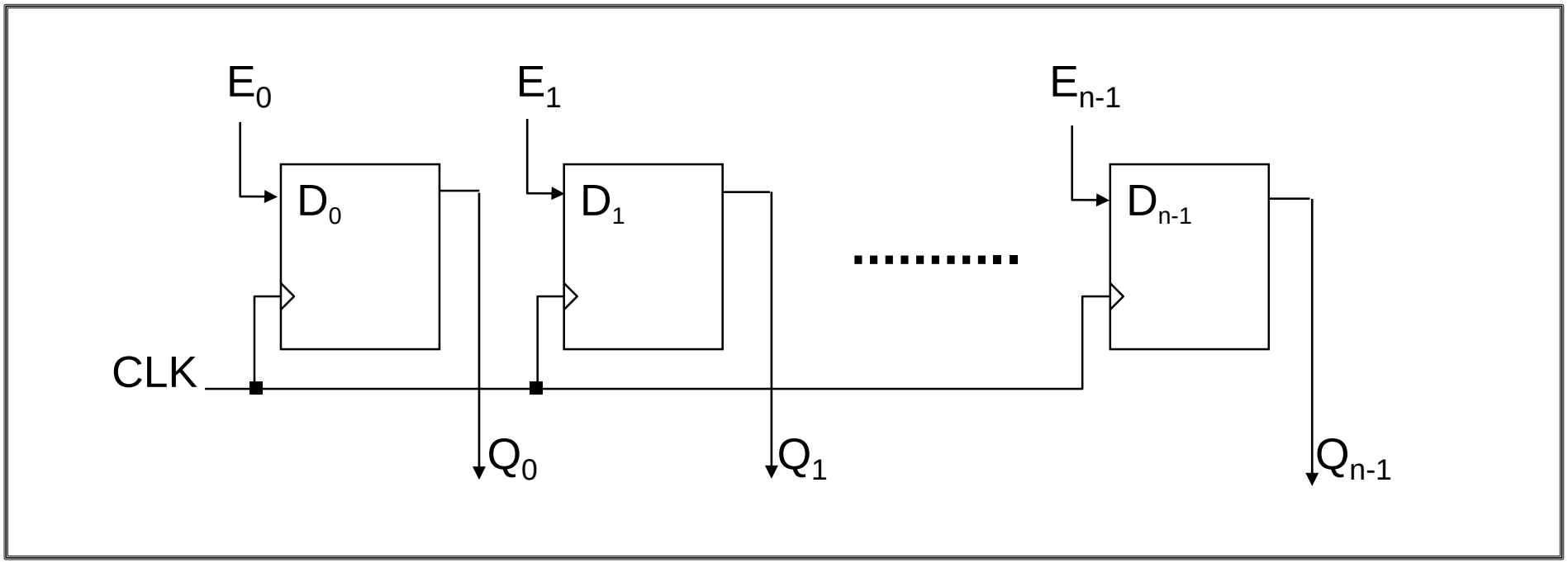
L	Dat	T	Q^{n+1}
1	0	X	0
1	1	X	1
0	X	0	Q^n
0	X	1	$/Q^n$

Escuela Politécnica Superior

Registers

Register:

- ✓ Sequential system formed by a set of flip-flops of the same type sharing a CLK signal.



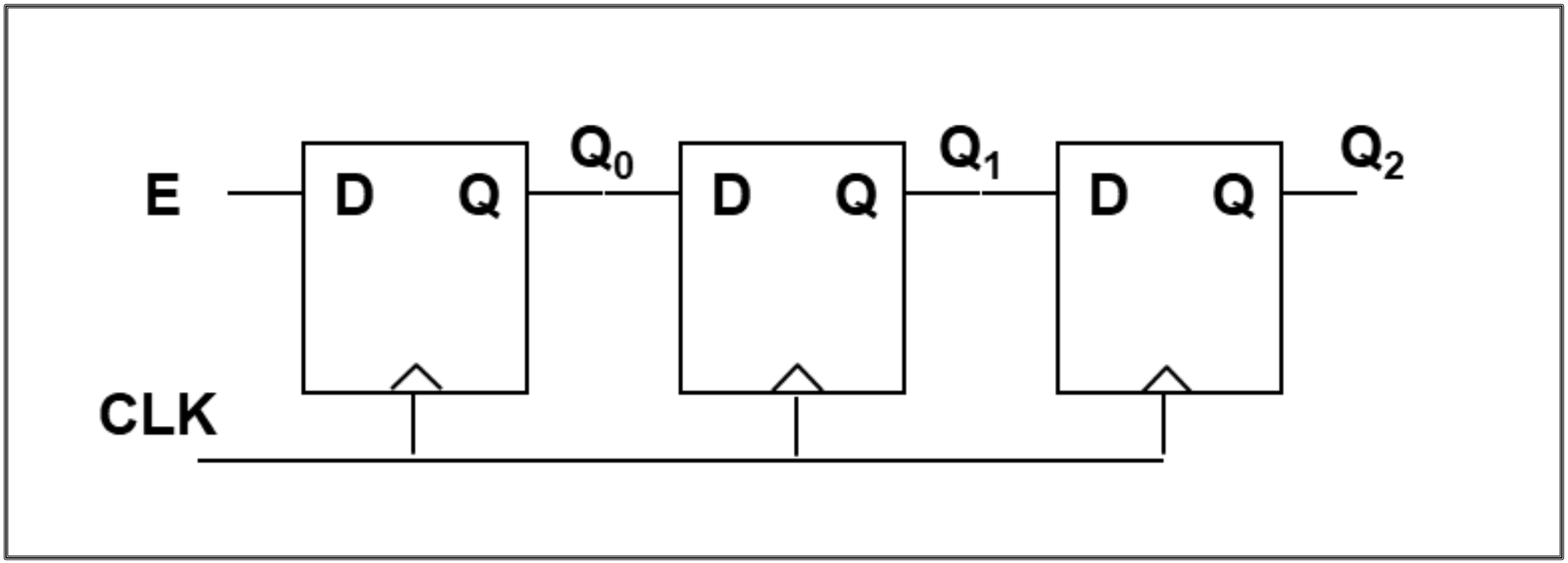
Example: Register of n bits

Escuela Politécnica Superior

Registers

Shift register:

- ✓ Output of the FF is connected to the input of the next FF

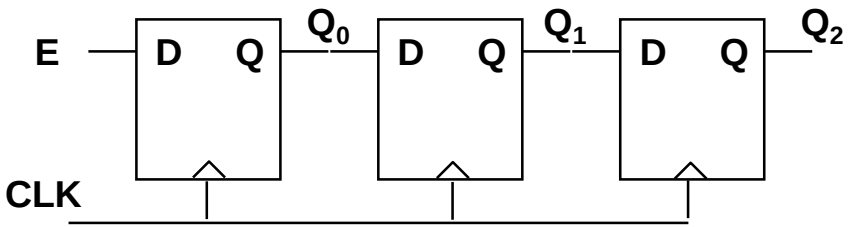


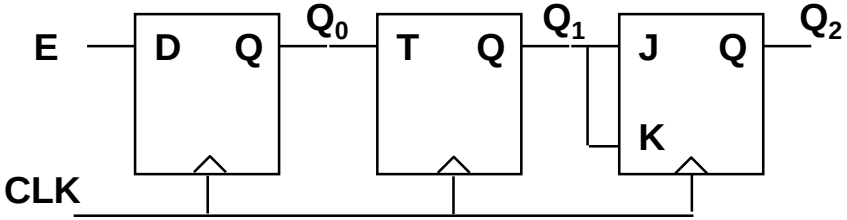
Example: Shift Register of 3 bits

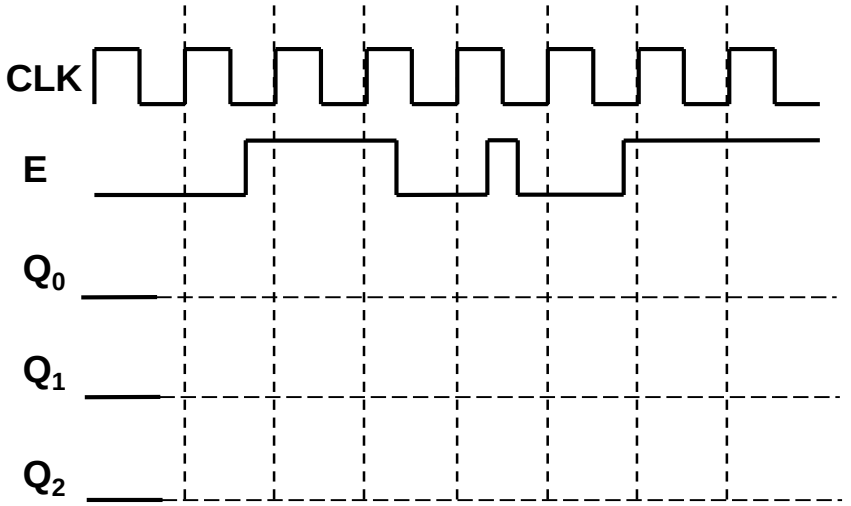
Escuela Politécnica Superior

Timing diagrams with Flip-Flops

Example: Complete the time diagram of the figure for each of these circuits



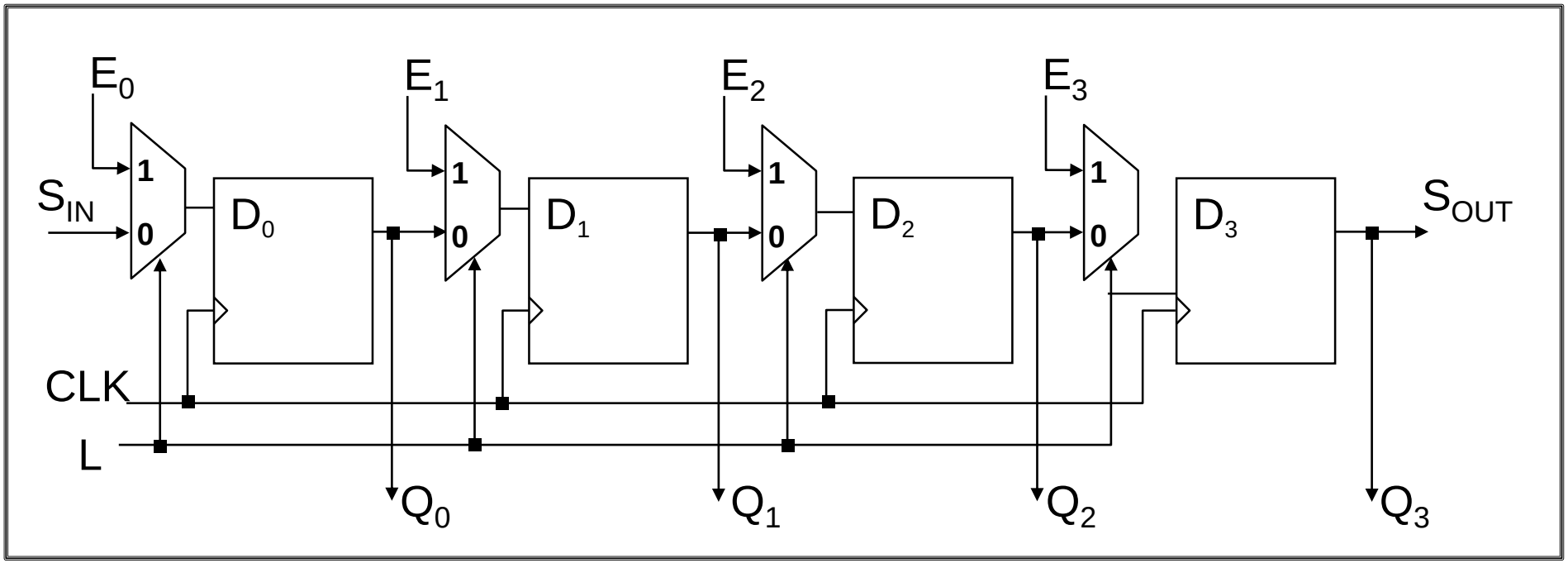




Escuela Politécnica Superior

Shift Register with Load input

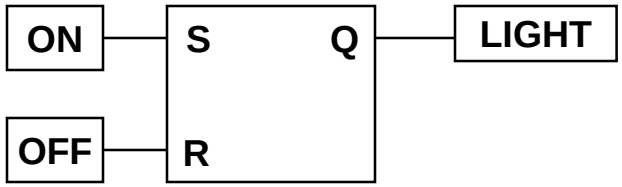
- ✓ **Register with load input:** A load signal L, allows to load synchronously in the register any desired value.



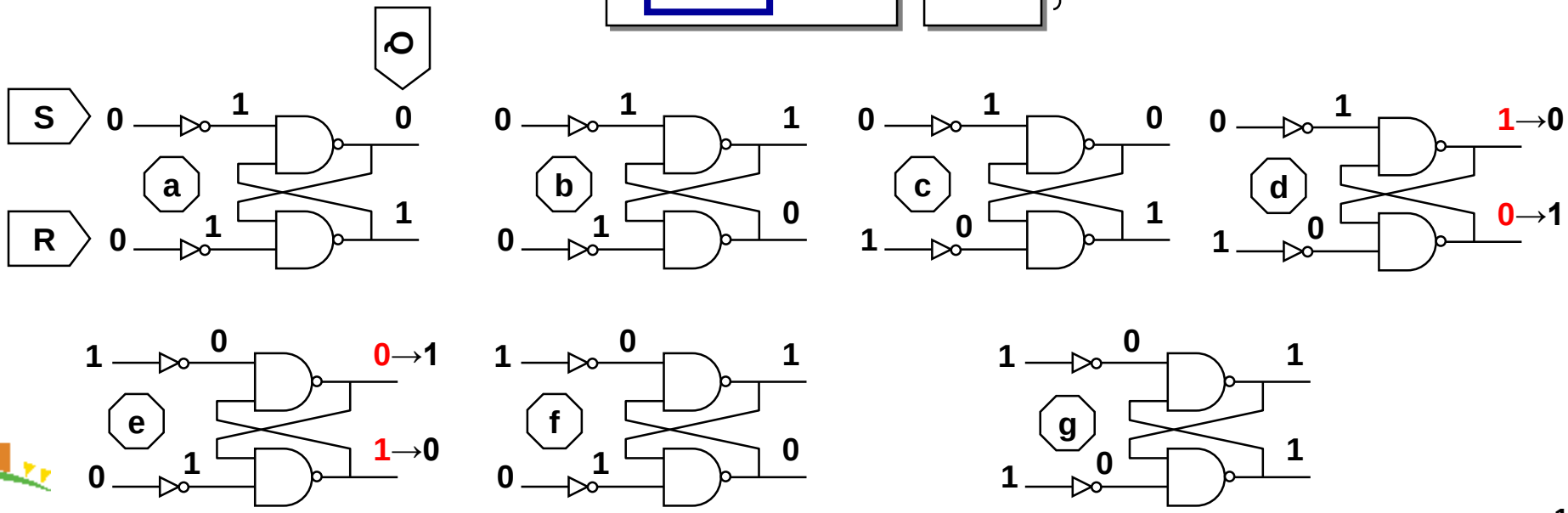
Example: Shift register (4bits) with load input.

Escuela Politécnica Superior

ANNEX
Asynchronous Flip-Flop RS



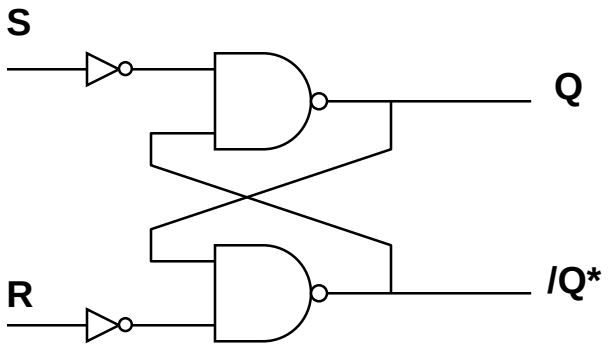
S	R	Q_t	$Q_{t+\Delta t}$	
0	0	0	0	a, b) Keep the state
0	0	1	1	
0	1	0	0	c, d) Reset
0	1	1	0	
1	0	0	1	e, f) Set
1	0	1	1	
1	1	0	1	g) Prioritary registration
1	1	1	1	



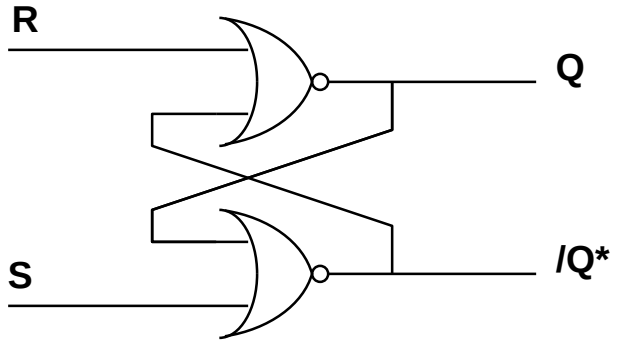
ANNEX
Asynchronous flip-flop RS

With R=S='1', outputs are not complementary and depend on the internal design of the flip-flop.

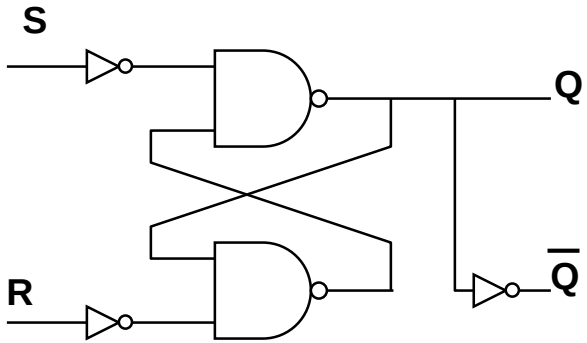
Priority Registration



Priority Erasure



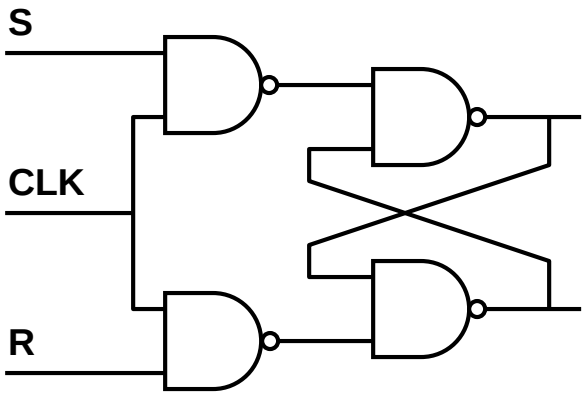
How to get that/Q* is always /Q?



Escuela Politécnica Superior

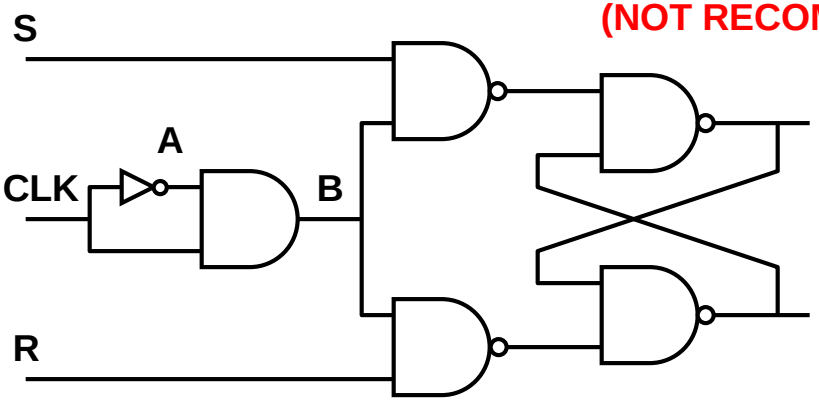
ANNEX
Synchronous Flip-Flop RS

Active by level

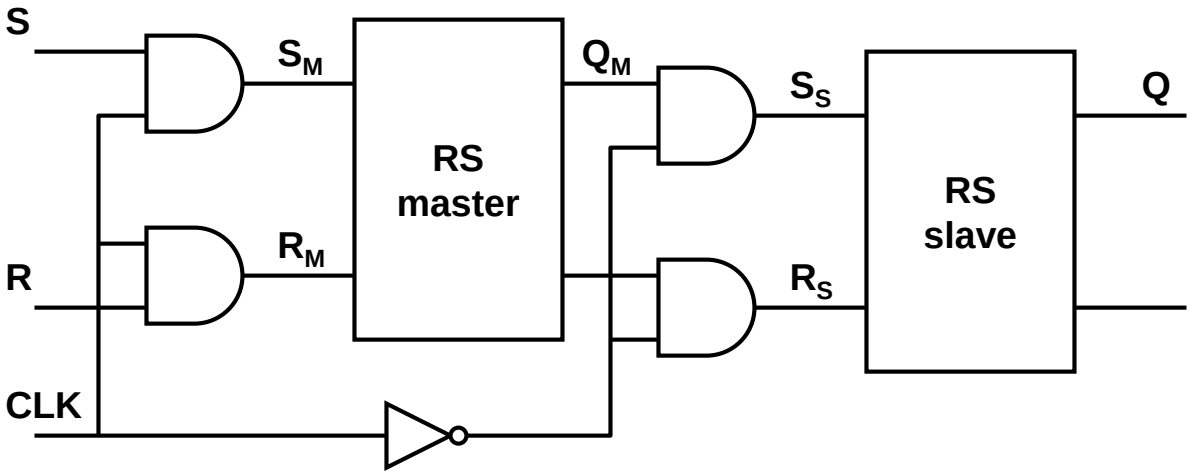


Active by edge (edge-triggered)

(NOT RECOMMENDED)



Active by edge (master-slave)



Escuela Politécnica Superior