UNIVERSIDAD AUTÓNOMA DE MADRID

17816 - COMPUTER BASICS

Syllabus Information

Code - Course title: 17816 - COMPUTER BASICS

Degree: 473 - Graduado/a en Ingeniería Informática
474 - Graduado/a en Ingeniería Informática y Matemáticas
722 - Graduado/a en Ingeniería Informática
734 - Graduado/a en Ingeniería Informática y Matemáticas (2019)

Faculty: 350 - Escuela Politécnica Superior

Academic year: 2019/20

1.Course details

1.1.Content area

Ingeniería de computadores, Informática

1.2.Course nature

Basic Training

1.3.Course level

Grado (MECES 2)

1.4.Year of study

473 - Graduado/a en Ingeniería Informática: 1
722 - Graduado/a en Ingeniería Informática: 1
474 - Graduado/a en Ingeniería Informática y Matemáticas: 1
734 - Graduado/a en Ingeniería Informática y Matemáticas (2019): 1

1.5.Semester

First semester

1.6.ECTS Credit allotment

6.0

1.7.Language of instruction

Spanish, English

1.10.Minimum attendance requirement

Two evaluation modalities are proposed: CONTINUOUS assessment and NON-CONTINUOUS assessment.

These modalities can be applied **independently for the theoretical contents and for the practical contents.** By default, it is assumed that all students choose a CONTINUOUS assessment modality.

The application of CONTINUOUS assessment for the theoretical contents is linked to the completion and obtaining of a minimum grade of the proposed activities during the development of the course.

The application of the CONTINUOUS evaluation for the practical contents is linked to the attendance and the realization and obtaining of a minimum grade of the activities proposed in the practical sessions in the laboratory.

CONTINUOUS and NON-CONTINUOUS ASSESSMENTS FOR THEORETICAL CONTENTS.

In both modalities, the theory class attendance is not mandatory but strongly recommended.

VERY IMPORTANT
Without the need to notify previously, tests can be done in any class. These tests have their weight only in the Continuous Evaluation. The absence during these sessions implies a grade of zero points in the activity.

The details about the evaluation regulations for each of the two modalities are included in the "Regular Assesment" section of this guide.

CONTINUOUS ASSESSMENT FOR PRACTICAL CONTENTS (LABORATORY).

In the CONTINUOUS evaluation modality, the student must attend all the practical classes and develop the activities that are proposed.
Always for duly justified reasons, the student may miss a maximum of 2 practice sessions (4 hours). In the case of reaching a greater number of faults, it will be excluded from this evaluation modality.

NON-CONTINUOUS ASSESSMENT FOR PRACTICAL CONTENTS (LABORATORY).

In this modality, the attendance to the practical lessons is not mandatory but strongly recommended.
The details about the evaluation regulations for each of the two modalities are included in the "Regular Assesment" section of this guide.

1.11.Faculty data

Coordinador de la Asignatura

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1.12.Competences and learning outcomes

1.12.1.Competences

B5 Conocimiento de la estructura, organización, funcionamiento e interconexión de los sistemas informáticos, los fundamentos de su programación, y su aplicación para la resolución de problemas propios de la ingeniería.

1.12.2.Learning outcomes

Ability to know, understand and evaluate the structure and architecture of computers, as well as the basic components that make them up.

Ability to design and build digital systems, including computers, microprocessor-based systems and communications systems.

1.12.3.Course objectives

In this course, it is learned basic techniques of analysis and creation of elemental digital circuits. The knowledge acquires in this subject is very important to study of complex design in the following courses. It is studied the basic units of information which are used in digital circuits, elemental operations which are used in digital designs and their properties. The operative elements of complexity immediately superior to the most elementary ones are studied to realize the design of a digital circuit. The most basic data storage units are studied, as well as the construction fundamentals of some basic sequential circuits. At the end of the course, the student must know how to construct logical functions in an efficient way and use the operative elements of immediately superior complexity. You must also know how to analyze and build a basic sequential circuit efficiently.

SPECIFIC OBJECTIVES	
1st TOPIC. - Boole Algebra and Logic Design.	
1.1.	Given a natural number, represented in reference to a certain base, obtain its representation in reference to any other base.
1.2.	Define the following concepts in your own words: digit, bit, binary logic variable, logical function y truth table.
1.3.	Define and know how to apply the basic properties and theorems of Boolean algebra.
1.4.	Be able to draw the symbol, specify the truth table and express the logical operation that implements each of the following doors: NOT, AND, OR, NAND, NOR and XOR, with two or more inputs.
1.5.	Be able to write the logical expression of said function as a sum of minterms and product of maxterms, and to draw the logic diagram of the circuit from the truth table of a function.
1.6.	Be able to simplify a certain function using Karnaugh maps.
2nd TOPIC. - Combinational Components.	
2.1.	Define combinational logic circuit. Draw the symbol, specify the table of truth, give a logical expression of each of the outputs, draw the internal logic diagram using basic doors and describe the functionality of the combinational words with their own words: Decoder, multiplexer, priority encoder, comparator of magnitude, semi-adder, full adder.
2.2.	Obtain, from a truth table, the combinational circuit that it represents. Obtain the truth table of a combinational circuit from its logical scheme.
2.3.	Be able to use decoders and multiplexers as generators of logical functions.
3rd TOPIC. - Basic elements of sequential logic.	
3.1.	Define the concept of bistable and clock signal. Be able to define and distinguish the concepts of bolt (latch) and flanged flip flop (flip-flop).
3.2.	Define and know the operation of the SR, JK and D locks associated with the concepts of memory, current state and next state, asynchronous inputs and clock signal.
3.3.	Define the different flip-flops (JK, D and T) and draw the symbol used in the logical diagrams to represent them. Express your functionality in your own words. Express its functionality through the tables of transitions (table of the truth of the following state) and output.
3.4.	Draw the chronogram of the output signal Q of a given flip-flop from the chronogram of the input signal and the clock signal.
3.5.	Define what a record is. Design and be able to use displacement records. Show the operation of these records using schedules

4th TOPIC. – Sequential circuits	
4.1.	Express with your own words what is a sequential circuit and the differences between combinational circuit and sequential circuit.
4.2.	Define, design and use counters. Check the operation of a meter using a schedule.
4.3.	Be able to define and distinguish Moore type designs and Mealy type designs.
4.4.	Perform sequential Moore type and Mealy type designs.
5th TOPIC. – Memory components.	
5.1.	Define random access memories. Be able to explain how it works
5.2.	Recognize, define and use read-only memories.
5.3.	Reconocer, definir y utilizar las memorias de sólo lectura.
6th TOPIC. – Digital representation of numbers	
6.1.	Write a whole number (positive or negative) in its representation sign-magnitude and complement to 2. Justify the advantages of the representation in two's complement in front of the sign-magnitude representation.
6.2.	Be able to perform addition and subtraction operations with numbers in binary.
6.3.	Define and implement an adder circuit with serial carry.
6.4.	Write a real number (positive or negative) in its representation in a fixed coma.
6.5.	Recognize and use codes for error detection.

1.13.Course contents

Summarized syllabus

UNIT 1. Boolean Algebra and Logical Design.
UNIT 2. Combinational circuits.
UNIT 3. Basic elements of sequential logic.
UNIT 4. Sequential circuits.
UNIT 5. Memory components.
UNIT 6. Digital representation of numbers.

Detailed syllabus

1. **Boolean algebra and Logical Design.**
   - 1.1. Binary numerical system. Conversion between systems.
   - 1.2. Properties and basic theorems of Boolean algebra.
     - 1.2.1. Boolean operations and expressions.
     - 1.2.2. Laws and rules of Boolean algebra.
     - 1.2.3. DeMorgan's theorems.
   - 1.3. Digital logic doors
     - 1.3.1. Boolean expressions and truth table.
     - 1.3.2. Extension to several inputs.
     - 1.3.3. Functional habilitation.
     - 1.3.4. Door implementations.
   - 1.4. Karnaugh maps.
     - 1.4.1. Minimization of a sum of products through the Karnaugh map.
     - 1.4.2. Minimization of a product of sums using the Karnaugh map.
2. **Combinational circuits.**
   - 2.1. Implementation of combinational logic. Logical functions
   - 2.2. Basic combinational circuits: Decoder, multiplexer, priority encoder, comparator circuit.
   - 2.3. Decoders and multiplexers as function generators.
3. **Basic elements of sequential logic.**

3.1. Principles of sequential circuits
3.2. Locks. Types of locks.
3.3. Flip-Flops. Types of Flip-Flops.
3.4. Circuits with Flip-Flops. Temporary chronograms.
3.5. Records. Scroll records.

4. Sequential circuits.
4.1. Counters.
4.1.1. Ring counter.
4.1.2. Other synchronous counters. Analysis and synthesis
4.2. Sequential systems. Finite state machine.
4.3. Circuits of Moore and Mealy. Synthesis of states.
4.4. Examples of finite state machines.

5. Memory components.
5.1. Storage devices.
5.2. Random Access Memory (RAM).
5.2.1. Structure of a semiconductor RAM. Size.
5.2.2. Volatility of memories.
5.2.3. Organization of internal memory in one and two dimensions.
5.2.4. Dynamic RAM memories. Refresh.
5.3. Read-Only Memory (ROM).
5.3.1. Programable ROM (PROM) and Erasable ROM(EPROM).
5.3.2. Usage of ROM as function generators.
5.4. Extension of memories.

6. Digital representation of numbers.
6.1. Representation of integers, positive and negative.
6.2. Operations in complement to 2.
6.3. Binary addition.
6.4. Fixed-point representation of real numbers.
6.5. Other binary codes: BCD and ASCII.
6.6. Codes for the treatment of errors.

1.14.Course bibliography

1. Fundamentos de Sistemas Digitales. Thomas L. Floyd. Prentice Hall. 9ª Ed. 2006. Ref_UAM: INF/C5400/FLO. Acceso electrónico en: http:\\bit.ly/1AWeOk6
2. Digital Design and Computer Architecture. David Money Harris y Sarah L. Harris. Morgan Kaufmann. Second Edition 2013. ISBN: 9780123944245. Ref_UAM: INF/C5200/HAR.
3. Fundamentos de diseño lógico y de computadoras. M. Morris Mano y Charles R. Kime. Prentice Hall. 3ª Ed. 2005. ISBN: 8420543993. Ref_UAM: INF/C5200/MAN. Acceso electrónico en: http:\\bit.ly/1ztybUs
4. Sistemas Digitales. Principios y Aplicaciones. Tocci y Widmer. Prentice Hall. 10ª Ed. 2008. ISBN: 9789702609704. Ref_UAM: INF/C5400/TOC
5. Sistemas Digitales y Tecnología de Computadores. J. García Zubía, I. Angulo Martínez, J.M. Angulo Usategui. Thomson. 2ª Ed. 2007. ISBN: 9788497324861. Ref_UAM: INF/C5400/GAR.
6. Fundamentos de Diseño Lógico. Charles H. Roth. Thomson. 5ª Ed.2004. ISBN: 849732286X. Ref_UAM: INF/C5200/ROT.
7. Sistemas Digitales. A. Lloris Ruíz, A. Prieto Espinosa, L. Parrilla Roure. McGraw-Hill. 2003. ISBN: 9788448191887. Ref_UAM: INF/C5400/LLO.

Main and secondary Bibliography associated with the proposed topics:

UNIT 1. Boolean Algebra and Logical Design.
Main: Ref. 1: Chapters 2 (sections 2.1, 2.2 y 2.3), 3, 4 y 5
Secondary:
Ref. 2: Chapters 1 (section 1.5) y 2 (sections 2.1 a 2.7)
Ref. 3: Chapter 2
Ref. 4: Chapters 2, 3 y 4
Ref. 5: Chapters 3 y 4 (sections 4.2 y 4.3)
Ref. 6: Chapters 2, 3, 4, 5, 7 y 8
Ref. 7: Chapters 1 y 2

UNIT 2. Combinational circuits.

Main: Ref. 1: Chapter 6
Secondary:
Ref. 2: Chapter 2 (sections 2.8 y 2.9)
Ref. 3: Chapter 4 (sections 4.1 a 4.6) y Chapter 5 (sections 5.1 a 5.5)
Ref. 5: Chapter 4 (sections 4.4 a 4.8)
Ref. 6: Chapter 9 (sections 9.1 a 9.4)
Ref. 7: Chapter 5 (sections 5.1 y 5.2), Chapter 6 (section 6.5)

UNIT 3. Basic elements of sequential logic.
Main: Ref. 1: Chapters 7 y 9.
Secondary:
Ref. 2: Chapter 3 (sections 3.1 y 3.2)
Ref. 3: Chapter 6 (sections 6.1 a 6.6)
Ref. 4: Chapter 5 (sections 5.1 a 5.12)
Ref. 5: Chapter 7
Ref. 6: Chapter 11
Ref. 7: Chapter 7

UNIT 4. Sequential circuits.
Main: Ref. 1: Chapter 8 y Ref. 2. (sections 3.3, 3.4, 3.5.1 y 3.5.2)
Secondary:
Ref. 1: Chapter 8
Ref. 3: Chapter 7 (section 7.6) y Chapter 8 (sections 8.1 a 8.4)
Ref. 4: Chapter 7 (sections 7.1 a 7.15), Chapter 9
Ref. 6: Chapter 12 (sections 12.3 a 12.6), Chapter 14, Chapter 19
Ref. 7: Chapter 8 (sections 8.2 y 8.3), Chapter 9

UNIT 5. Memory Components.
Main: Ref. 1: Chapter 9, Chapter 10, Chapter 11 (section 11.1)
Secondary:
Ref. 2: Annex A (section A.3)
Ref. 3: Chapter 9
Ref. 4: Chapter 11, Chapter 12 (sections 12.1 y 12.2)
Ref. 5: Chapter 11
Ref. 7: Chapter 8 (sections 8.4 8.7.1)

UNIT 6. Digital representation of numbers.
Main: Ref. 1: Chapter 2
Secondary:
Ref. 2: Chapter 1 (sections 1.3 y 1.4)
Ref. 3: Chapter 1 (sections 1.2 y 1.3)
Ref. 4: Chapter 2
Ref. 5: Chapter 2
Ref. 6: Chapter 1
Ref. 7: Chapter 6 (sections 6.1, 6.2 y 6.4)

2.Teaching-and-learning methodologies and student workload

2.1.Contact hours

	#hours
Contact hours (minimum 33%)	78
Independent study time	72

2.2.List of training activities

Activity	# hours
Lectures	42
Seminars	
Practical sessions	
Clinical sessions	
Computer lab	

Laboratory	26
Work placement	
Supervised study	
Tutorials	
Assessment activities	10
Other	

3.Evaluation procedures and weight of components in the final grade

3.1.Regular assessment

CONTINUOUS ASSESSMENT

Students can choose the modality of CONTINUOUS EVALUATION (CE) for the theoretical part, the practical part, or both of them.

Each part, theory and practice, is independent and involves different regulations.

Continuous Evaluation: Theoretical

For the EC in theory, although it is highly recommended, class attendance is not mandatory. The subject is evaluated with a set of in-person activities to be developed during the course. All the activities will take place, whenever possible, in the common schedule enabled in the calendar or otherwise in the same class schedule. These activities include two partial tests that can eliminate course content for the final exam.

The liberatory nature of the first two partial tests, P1 and P2, implies that, in the case of passing any of them (ExaP1, ExaP2 ³ 5.0), it is not necessary to re-examine the contents associated with said partials in the final exam of the subject in the ordinary call.

In the case of not passing any of them (ExaP1 or ExaP2 < 5.0), it is necessary to take part in the partial content not passed, always as well as the third partial ExaP3, in the final exam of the subject in the ordinary call.

In the case of not passing either of the two partial tests (ExaP1 and ExaP2 < 5.0), the student must take the final exam of the subject, as if you were a student who had opted for the non-continuous assessment method, as explained later.

After the final exam in the ordinary call, there will be a set of qualifications, one for each partial, either that obtained during the course or in the final exam and a fourth of the other activities developed during the course.

In the event that a student with a passed partial exam takes the corresponding part of the final exam, the final exam grade will prevail.

The grade corresponding to the part of Theory (**Not_Teo**) is the one that results from the weighted average between all these tests, according to the expression:

Not_Teo: 0,30*ExaP1 + 0,35*ExaP2 + 0,25*ExaP3 + 0,10*OtherActivities

In the case that (Not_Teo < 5.0), you must take the final exam of the subject in your extraordinary session, as if you were a student who had opted for the non-continuous assessment method, as explained below.

Continuous evaluation: Practical sessions

The grade corresponding to the part of Laboratory (**Not_Lab**) is the one that results from carrying out the practices programmed in the course.

- To pass the practical part, the student must attend all the practical sessions. Always for duly justified reasons, a student may miss a maximum of 2 practice sessions (4 hours) and must present the corresponding reports. Otherwise, the student must perform a practice exam consisting of a practice of greater complexity to those performed in the laboratory.

The qualification of the practical part will take into account the quality of the designs made and the level of the results obtained, as well as the result of the specific tests that can be proposed for each practice. The validity of the results obtained in each of the sections that have been established for their implementation in the scripts of the practices will also be assessed. The procedure and the particular evaluation method for ach practice will be described previously to its respective beginning, in each of the corresponding scripts.

NON-CONTINUOUS EVALUATION

For students who opt for the NON-CONTINUOUS evaluation mode in the theoretical part, in the practices part or in

both, their grades will be obtained in the following way:

a. The grade corresponding to the theory part is the one that results from:

- The qualification of the final test (100%).

The final test will consist of a written test, whose content will cover all the objectives that students must reach in the full course. This test may include both theoretical issues and problem solving.

b. The note corresponding to the practical part (**Not_Lab**) is the one that results from:

- The qualification of the final practical test (100%).

The final test will consist of a single practical exam, which allows to evaluate all the concepts developed in the laboratory practices proposed in the subject

For both evaluation modalities CONTINUOUS and NOT CONTINUOUS:

Both parts, theory and practices, are scored on 10 points.

- The final grade of the subject is obtained from the theory and practical notes by means of the following expression:

Mark: 0,4*Not_Lab + 0,6*Not_Teo

- To pass the subject it is mandatory to obtain a grade greater than or equal to 5 points, both in theory and in laboratory practice. Otherwise, the final grade on record will be:

Mark: (0,4*Mín(5, Not_Lab) + 0,6*Mín(5, Not_Teo))

- The theory grade is preserved only for the extraordinary call in the same academic year.
- The practical part grade is kept for the extraordinary call in the same academic year.

VERY IMPORTANT: When any type of copying or cheating is detected in any of the evaluation activities, whether theoretical or practical, the information reflected in Chapter IV of the document " Normativa de Evaluación Académica de la EPS", approved by the Board of the Center on November 4, 2013, will be applied.

3.1.1.List of evaluation activities

Evaluatory activity	%
Final exam	15%-60%
Continuous assessment	85%-40%

3.2.Resit

For students who opt for the resit in the theoretical part, in the practices part or in both, their grades will be obtained in the following way:

a. The grade corresponding to the theory part is the one that results from:

- The qualification of the final test (100%).

The final test will consist of a written test, whose content will cover all the objectives that students must reach in the full course. This test may include both theoretical issues and problem solving.

b. The note corresponding to the practical part (**Not_Lab**) is the one that results from:

- The qualification of the final practical test (100%).

The final test will consist of a single practical exam, which allows to evaluate all the concepts developed in the laboratory practices proposed in the subject

Note:

- Both parts, theoretical and practical, are scored between 0 and 10.
- The final mark of the subject is obtained from the theory and practice marks following the equation:

Calificación: 0,4*Not_Lab + 0,6*Not_Teo

- To pass the subject it is mandatory to obtain a mark greater than or equal to 5 points, both in theory and in practice. Otherwise, the final note will be:

Calificación: (0,4*Mín(5, Not_Lab) + 0,6*Mín(5, Not_Teo))

VERY IMPORTANT: When any type of copying or cheating is detected in any of the evaluation activities, whether theoretical or practical, the information reflected in Chapter IV of the document " Normativa de Evaluación Académica de la EPS", approved by the Board of the Center on November 4, 2013, will be applied.

3.2.1.List of evaluation activities

Evaluatory activity	%
Final exam	40%-100%
Continuous assessment	60%-0%

4.Proposed workplan

Week	In-Person Activity		At-home Activity
	Theoretical class	Practical Laboratory Session	
1ª	UNIT 1		• Study of the bibliography provided for U1. • U1 exercise resolution
2ª	UNIT 1	Session 0a: **ISE Xilinx Tutorial**	
3ª	UNIT 2	Session 0b: **Mounting plate Tutorial**	• Study of the bibliography provided for U2. • U2 exercise resolution
4ª	UNIT 2		
5ª	UNIT 2	Session 1: **CDC design with discrete elements.**	
6ª	UNIT 3		• Study of the bibliography provided for U3. • U3 exercise resolution
7ª	UNIT 3	Session 2: **Design and assembly of CDC using multiplexers and decoders.**	
8ª	UNIT 4		• Study of the bibliography provided for U4. • U4 exercise resolution
9ª	UNIT 4	Session 3: **Design and implementation of CDS: counters.**	
10ª	UNIT 4		
11ª	UNIT 5	Session 4: **Global design. Project.**	• Study of the bibliography provided for U5. • U5 exercise resolution
12ª	UNIT 6		• Study of the bibliography provided for U6. • U6 exercise resolution
13ª	UNIT 6		
14ª	Exercises		• Exercise resolution.

May	• Final Ordinary exam	• Final exam preparation
June	• Final Extraordinary exam	• Final exam preparation.