Sequential circuits

Computer Fundamentals

Escuela Politécnica Superior. U.A.M

Index of unit 4

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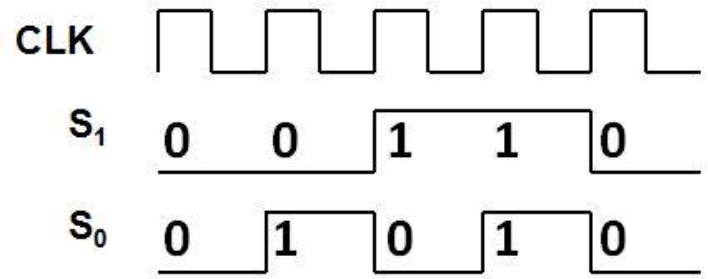
Synchronous counters

Counter. Sequential system which changes the value (state) when the clock signal changes.

- ✓ They are used for counting events in the digital systems.
  Ex.: count clock pulses (edges [ ] flip-flops used).



- ✓ Module of a counter is the máximum number of states it can count (for n bits, Module = 2^n). → Number of bits of the counter

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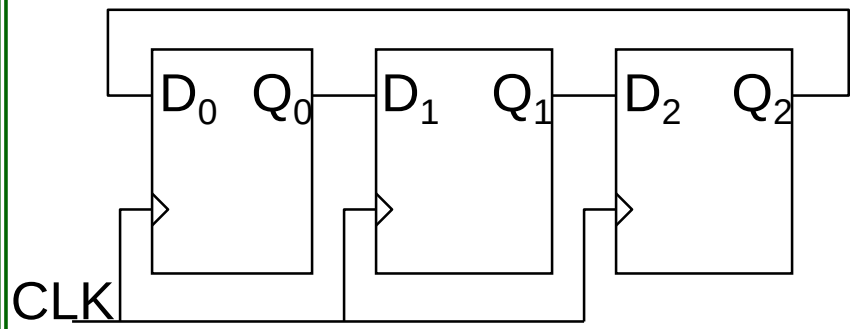
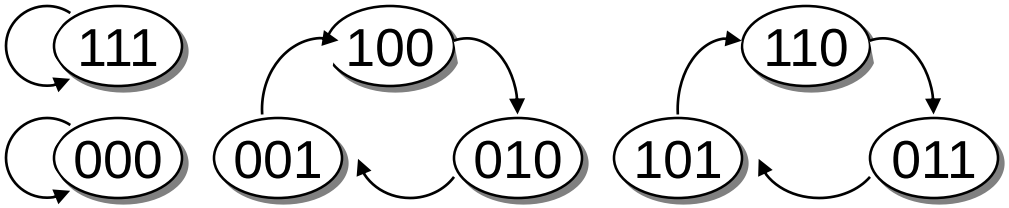
Synchronous counters. Analysis

Using shift registers

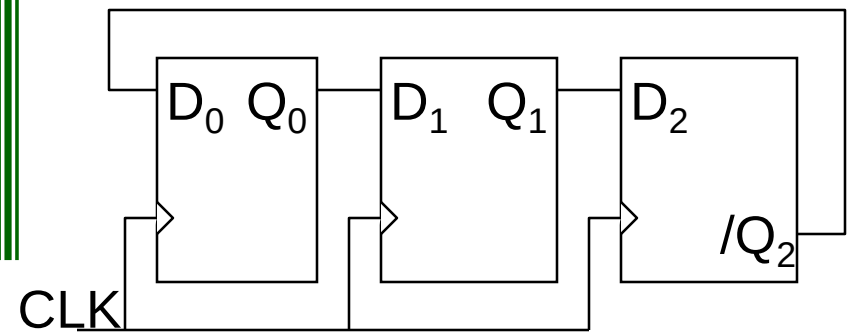
a) Ring counter

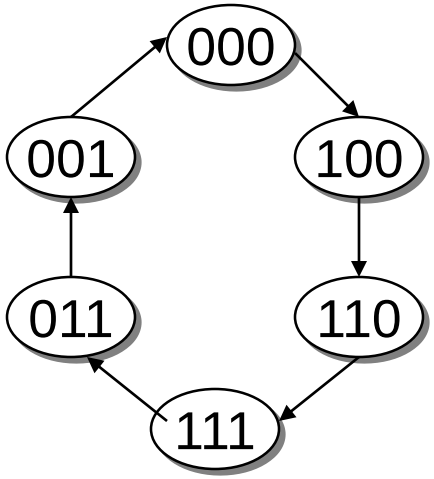


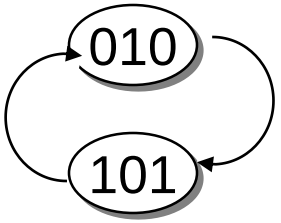


Initializations

b) Johnson counter







Initializations

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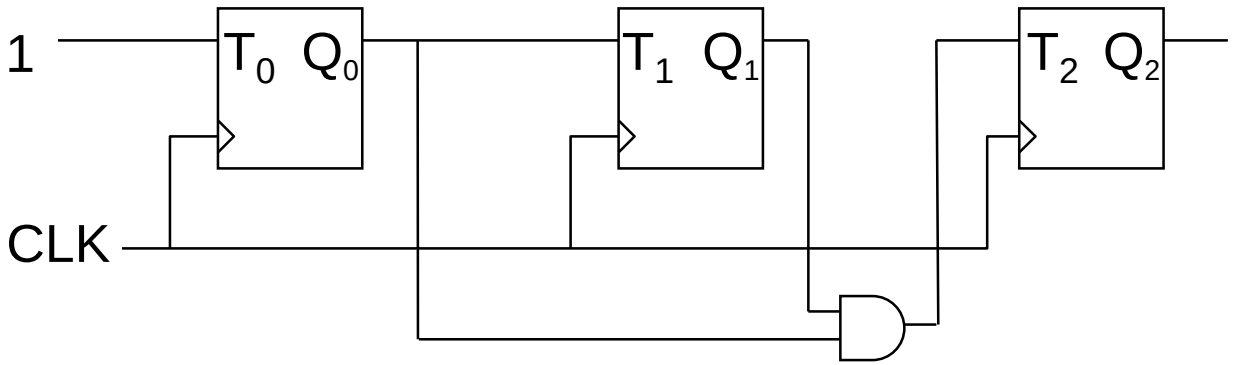
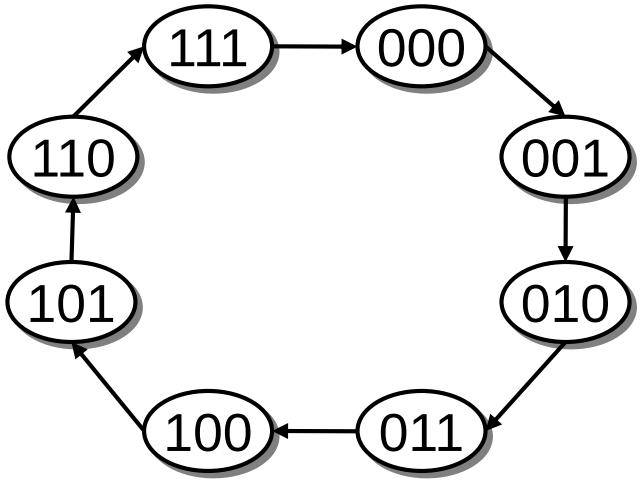
Synchronous counters. Analysis

Using shift registers

c) Binary counter 3b of máximum module (8 states).

	Q_2	Q_1	Q_0
S_0	0	0	0
S_1	0	0	1
S_2	0	1	0
S_3	0	1	1
S_4	1	0	0
S_5	1	0	1
S_6	1	1	0
S_7	1	1	1





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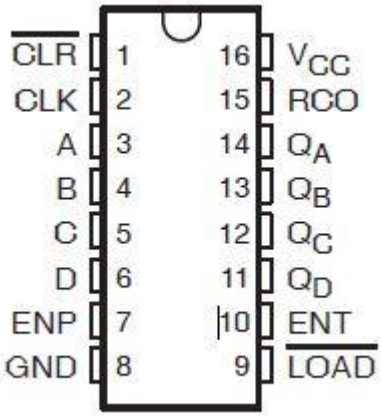
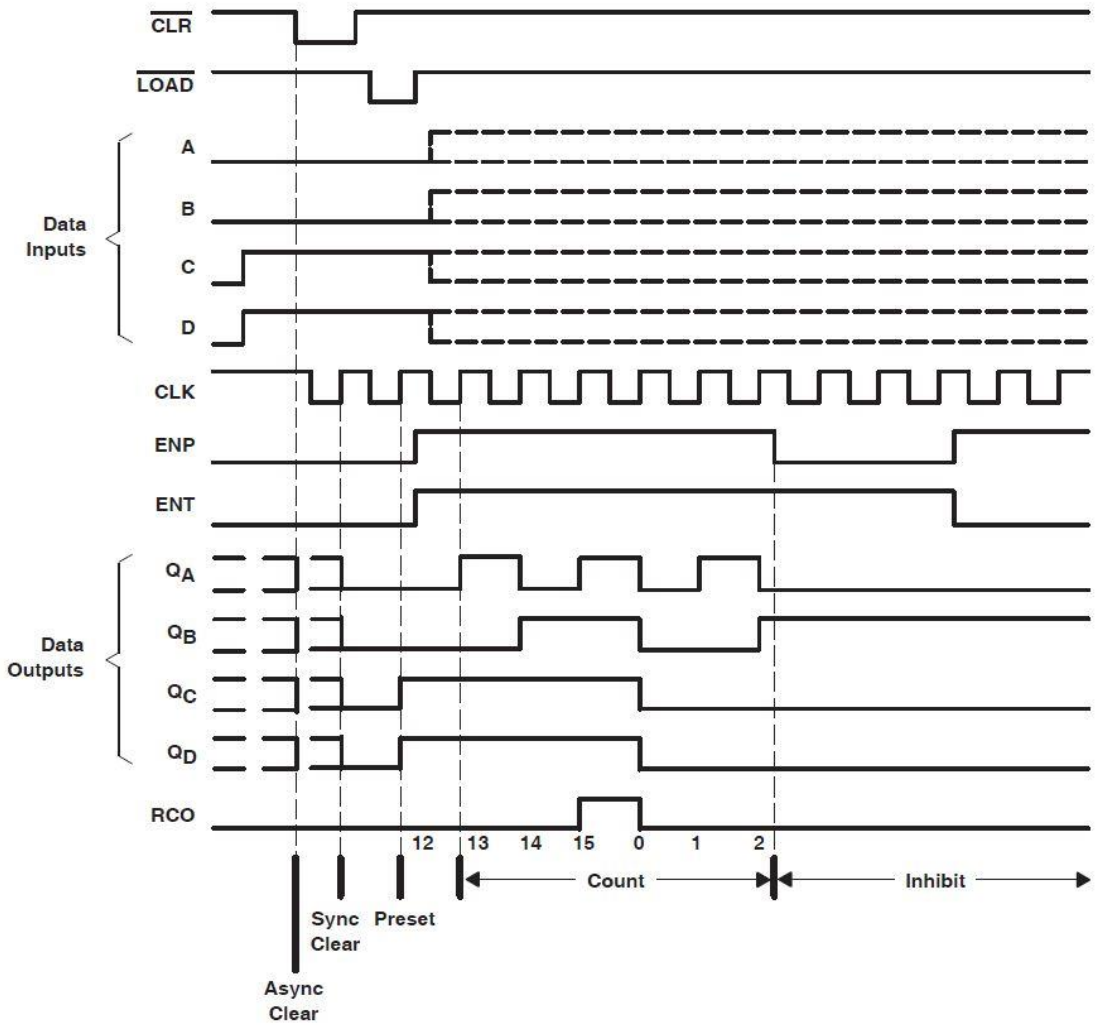
Synchronous counters. Analysis

d) Binary counter 4b: 74HC163





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Synchronous counters. Synthesis

✓ Steps to follow for designing counters of **m** states.

- The number of states m determines the minimun number of flip-flops n,

$$2^n \geq m$$

- Choose the order in which the states will be run (states diagram).
- Define an initial state.
- Define a solution for possible locking situations? How….

HARDWARE Synthesis

- Write the transition table between states:

  Actual state (n) → Next state (n+1).

- Choose the type of flip-flop to make the design (**D**, T, JK).
- Write the State equations { $g(Q_i^n, E_i^n)$ }

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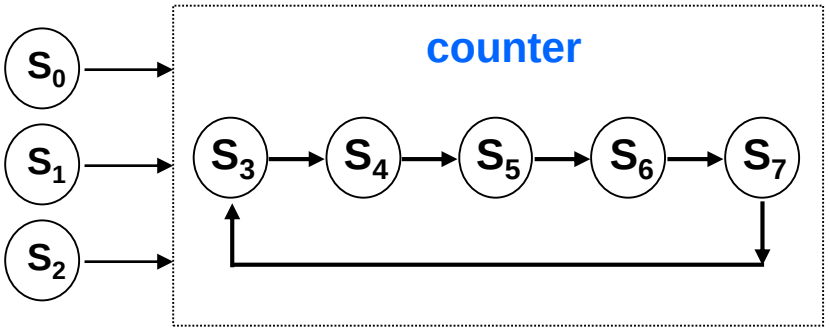
Synchronous counters. Synthesis

EXAMPLE

- ✓ Counter of 5 states. $2^3 > 5 > 2^2$ => (3 flip-flops)
- ✓ Sequential states: S_3,S_4,S_5,S_6,S_7; $Q_2Q_1Q_0 = (011,100,101,110,111)$
- ✓ Add antiblock (Since I want 5 states, I can do): if S_0, S_1 o S_2 => S_4



ACTUAL state			
	Q_2^n	Q_1^n	Q_0^n
S_0	0	0	0
S_1	0	0	1
S_2	0	1	0
S_3	0	1	1
S_4	1	0	0
S_5	1	0	1
S_6	1	1	0
S_7	1	1	1

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Sequential systems

Characteristics:

- A sequential circuit is a finite state machine(FSM).
- The change from the current state (t = n) to the next state(t+Δt = n+1) is synchronously produced with the clock signal of the system (↑ or ↓).
- The system state is defined by the values associated to the outputs (Q_i) of the flip-flops conforming the system.
- The transition to the next state (Q_i^{n+1}) depends on the actual state (Q_i^n) and the inputs applied to the system (X_i^n) in the clock edge.
- Regarding the changes in the output:

The outpts (S_i) depend only in the state (Q_i) → **FSM-MOORE: $S^n = g(Q^n)$**

The outputs (S_i) depend on the state (Q_i) and on the inputs (E_i) → **FSM-MEALY: $S^n = g(Q^n, E^n)$**

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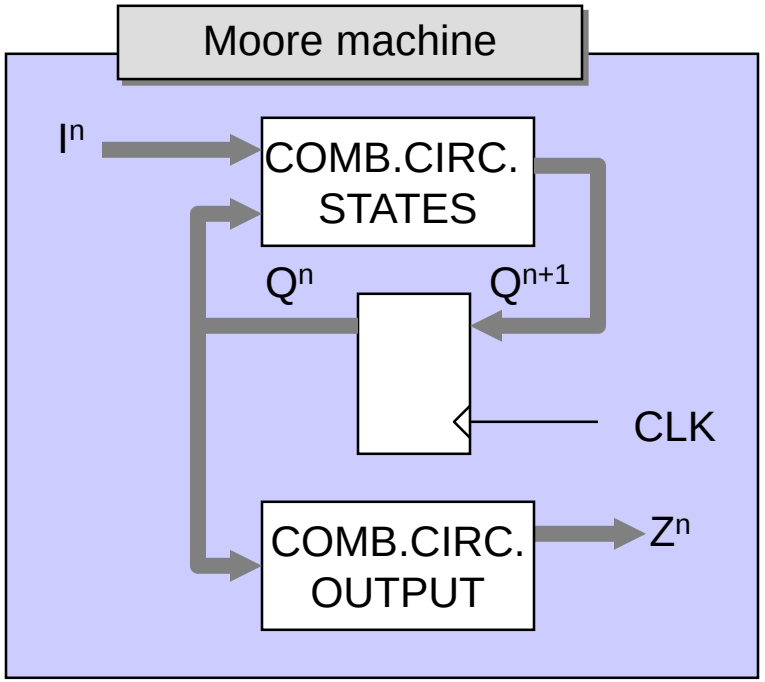
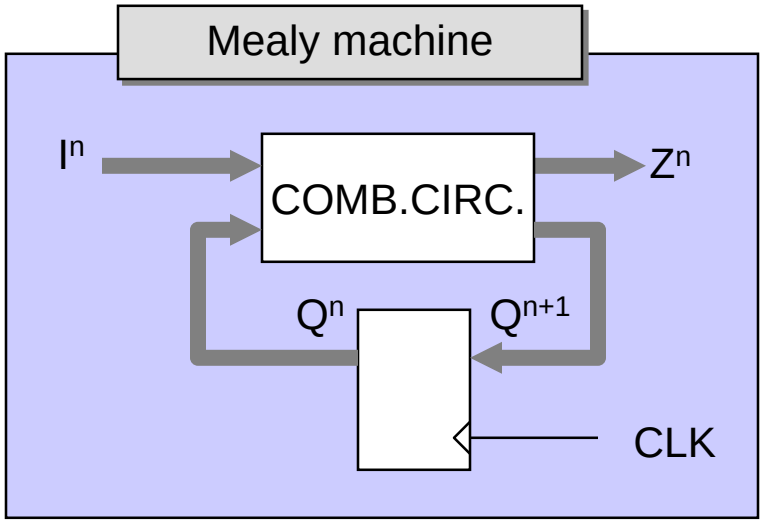
Sequential systems

STATE DIAGRAMS

✓ Represents the functionality of a system in a structured way

SYNTHESIS: State diagrams ⇨ Circuit





The type of FSM is determined by the combinational circuits it contains

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Sequential systems. Implementation

A	Identification of inputs and outputs.
B	State diagrams
C	Checking and diagram reduction
D	Determining of the number and type of flip-flops
E	Asigning the states
F	Truth Table
G	Minimization of logic functions
H	Circuit design

There can be changes as a function of the type of implementation

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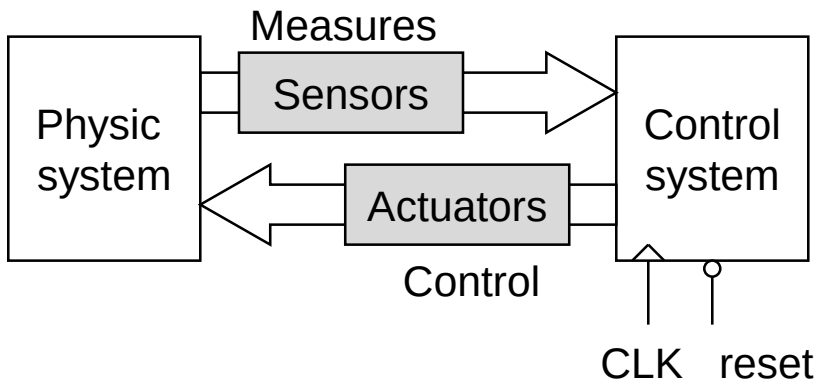
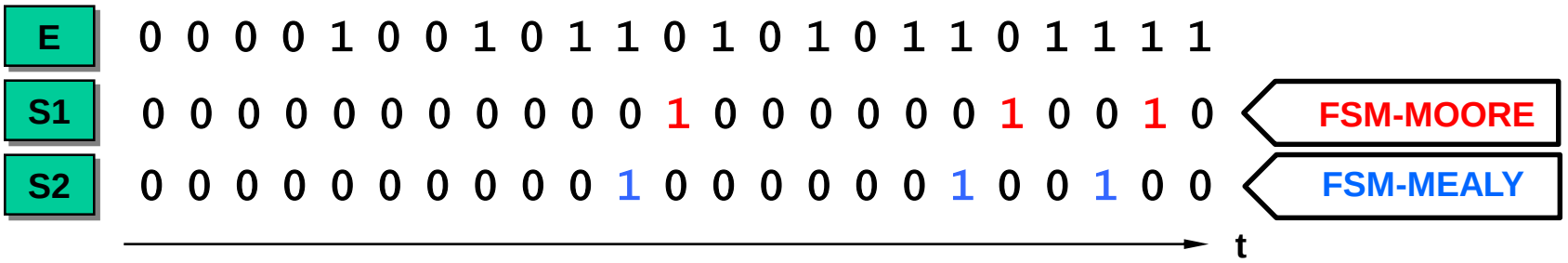
Sequential systems. Implementation



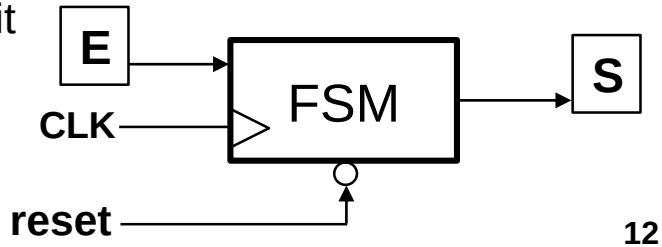
In the control systems, sensors are the inputs for the circuits and the actuators are the outputs.

Example_1: Detect the sequences overlap of value“1011” synchronous with a clock.



A Identification of inputs and outputs

- Determine the input and output signals of the designed circuit
- The clock and the reset must always appear, and they are not considered as inputs



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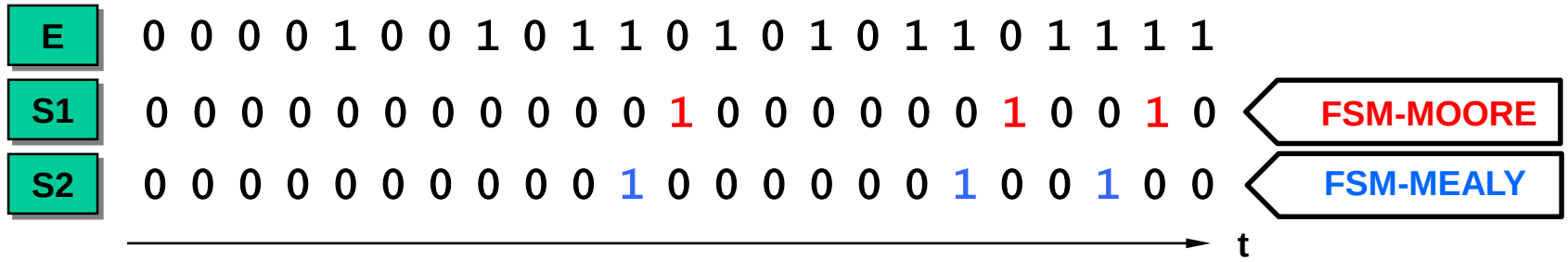
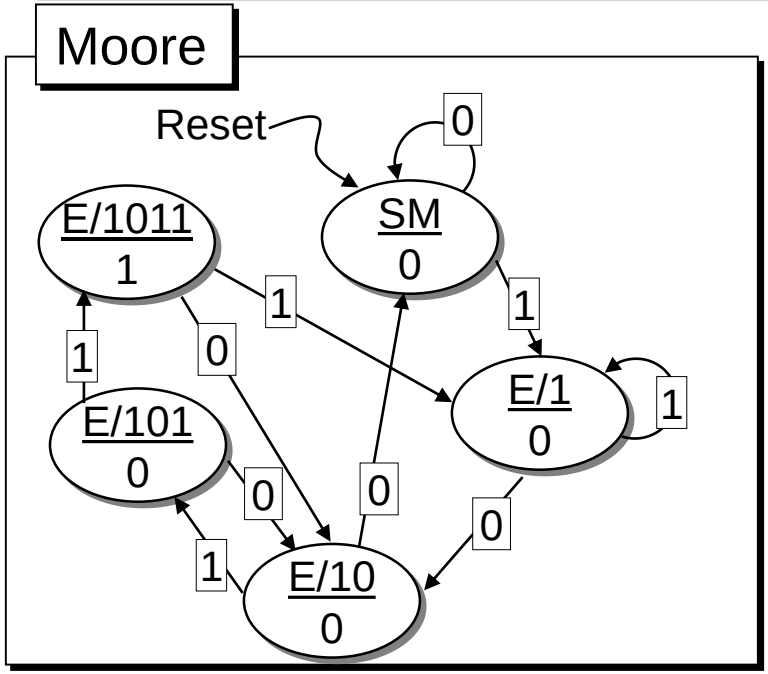
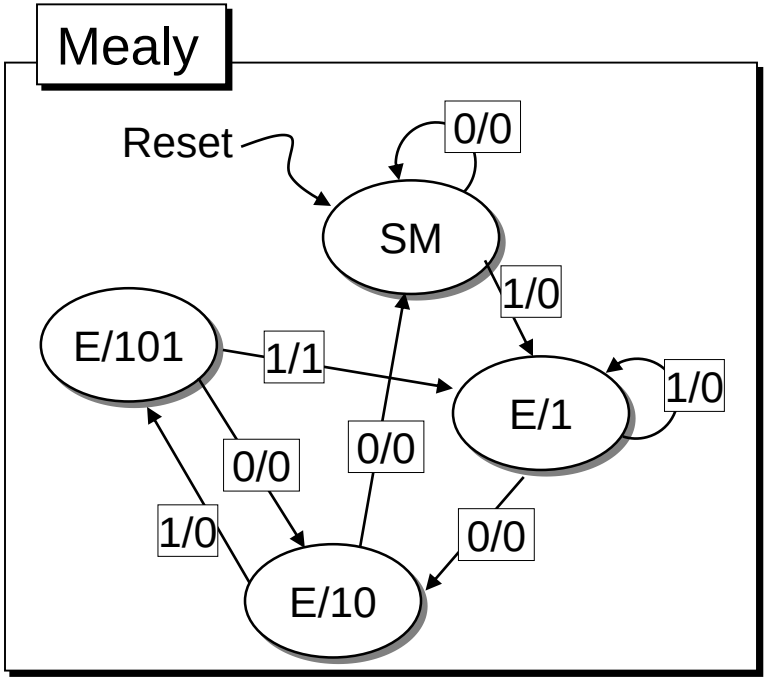
Sequential systems. Implementation

Example_1: Detect the sequence “1011” acepting overlap .



B States diagram (NOT AUTOMATABLE (there is no systematic method)





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Sequential systems. Implementation

Example_1: Detect the sequence "1011" (overlap allowed) synchronous with a clock.

D Determine the number and type of flip-flops

N states ⇨ n flip-flops such that $2^n \geq N$

Moore

5 states → 3 flip-flops

Mealy

4 states → 2 flip-flops

E Asign the states

Moore

STATE	Binary value Q_2	Q_1	Q_0
SM	0	0	0
E/1	0	0	1
E/10	0	1	0
E/101	1	0	0
E/1011	1	1	1

Mealy

STATE	Binary value Q_1	Q_0
SM	0	0
E/1	0	1
E/10	1	0
E/101	1	1

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Sequential systems. Implementation

Example_1: Detect the sequence “1011” (overlap allowed) synchronous with a clock.

F Truth tables: State and output (Moore)

Actual State			
Q_2^n	Q_1^n	Q_0^n	E^n
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
1	0	0	0
1	0	0	1
1	1	1	0
1	1	1	1

Next state		
Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	0	0
0	0	1
0	1	0
0	0	1
0	0	0
1	0	0
0	1	0
1	1	1
0	1	0
0	0	1

Output
S_1
0
0
0
0
0
0
0
0
1
1

State Eq.(3)

Output Eq.

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Sequential systems. Implementation

Example_1: Detect the sequence "1011" (overlap allowed) synchronous with a clock.

F Truth table: State and output (Mealy)

Actual state			Next state		Output
Q_1^n	Q_0^n	E^n	Q_1^{n+1}	Q_0^{n+1}	S_2
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	0	1	1

State Eq.(2)

Output Eq.

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Sequential systems. Implementation

Example_1: Detect the sequence “1011” (overlap allowed) synchronous with a clock.

G Minimization of logic functions

H Circuit designs

- The state equations depends on the type of flip-flops selected. In each case the transition equations which must be applied are:

$Q_i^n \rightarrow Q_i^{n+1}$	D_i^{n+1}	T_i^{n+1}	J_i^{n+1}	K_i^{n+1}
0 → 0	0	0	0	X
0 → 1	1	1	1	X
1 → 0	0	1	X	1
1 → 1	1	0	X	0

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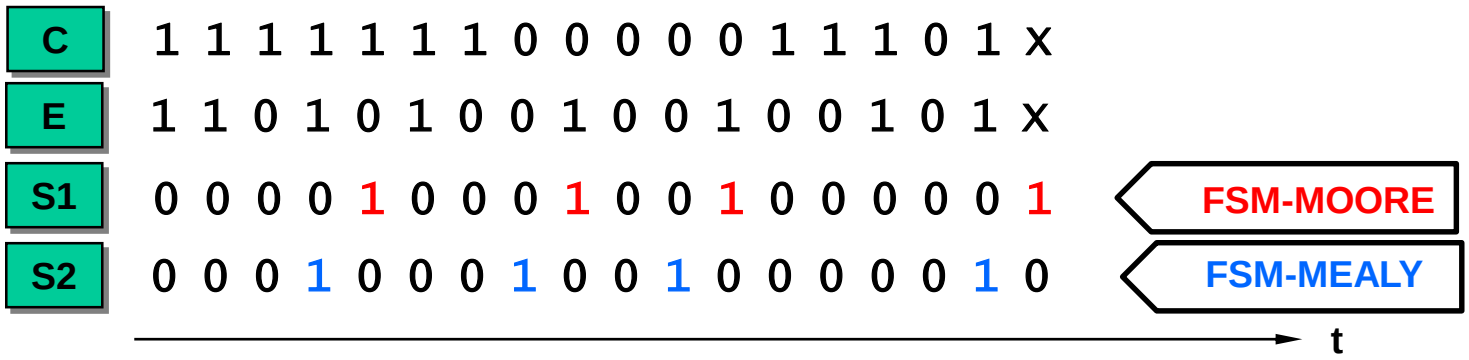
Other Moore or Mealy circuits

Example_2: Detect a complete sequence without overlapping of three consecutive bits as a function of a control signal C (if C = 0 sequence 100, if C = 1 sequence 101). If in the middle of the search for a valid sequence, the control signal is changed, the circuit must respond on the next clock edge to the new signal.



Other Moore or Mealy circuits

Example_3: You are asked to control a beverage vending machine. The inputs to the circuit are signals that come from the input of coins. The outputs are signals that must be sent to dispense the drink (only) and activate the return of the change when necessary. The price of the drink is € 1.5, the system only accepts coins of 50 cents, € 1 and € 2, coins that are detected one by one independently and in a single cycle of the system. Design the system using Moore and Mealy approaches.

Example_4: There are two processors that share the same memory area but the memory only accepts the access from one at a time. The processors can request access to the memory by the Xi lines (i = 1,2). Upon a request of access by any of the processors, the FSM to design, activates one of the Zi lines (i = 1,2), to indicate which processor grants the permission use. If the memory is busy, no new requests are answered, until it is free. If the memory is free, the request of the processor that demands it is accepted. In the case of a simultaneous request, the FSM applies the following priority protocol, the highest priority is for the processor that has not used the memory for a longer time. It is requested to design the Moore diagram for this control FSM.

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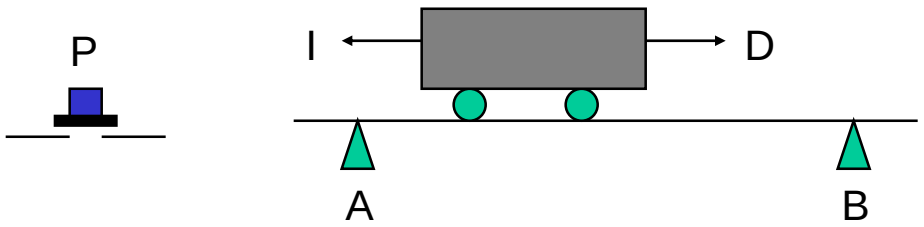
Other Moore or Mealy circuits

Example_5: In order to control the movement of a material transport trolley between two points A and B, two presence sensors are available at those points and one Push-button. The motor is controlled by two signals (D and I) to move to the left and right. . The operation of the system must be as follows:

- Initially, the trolley is stopped at position A.
- When the Push button (P) is pressed, the trolley will start to move through position B without stopping. Once arrived at B, the trolley starts moving in the opposite direction, without stopping, until reaching the starting point A. During the movement, the value of P is not taken into account by the system.
- If the P button is not pressed at the point A, the trolley will stop. If the P button is pressed when reaching A, a new movement will be started.

Determine:

a) Mealy states diagram
b) Truth table
c) Minimized state equations



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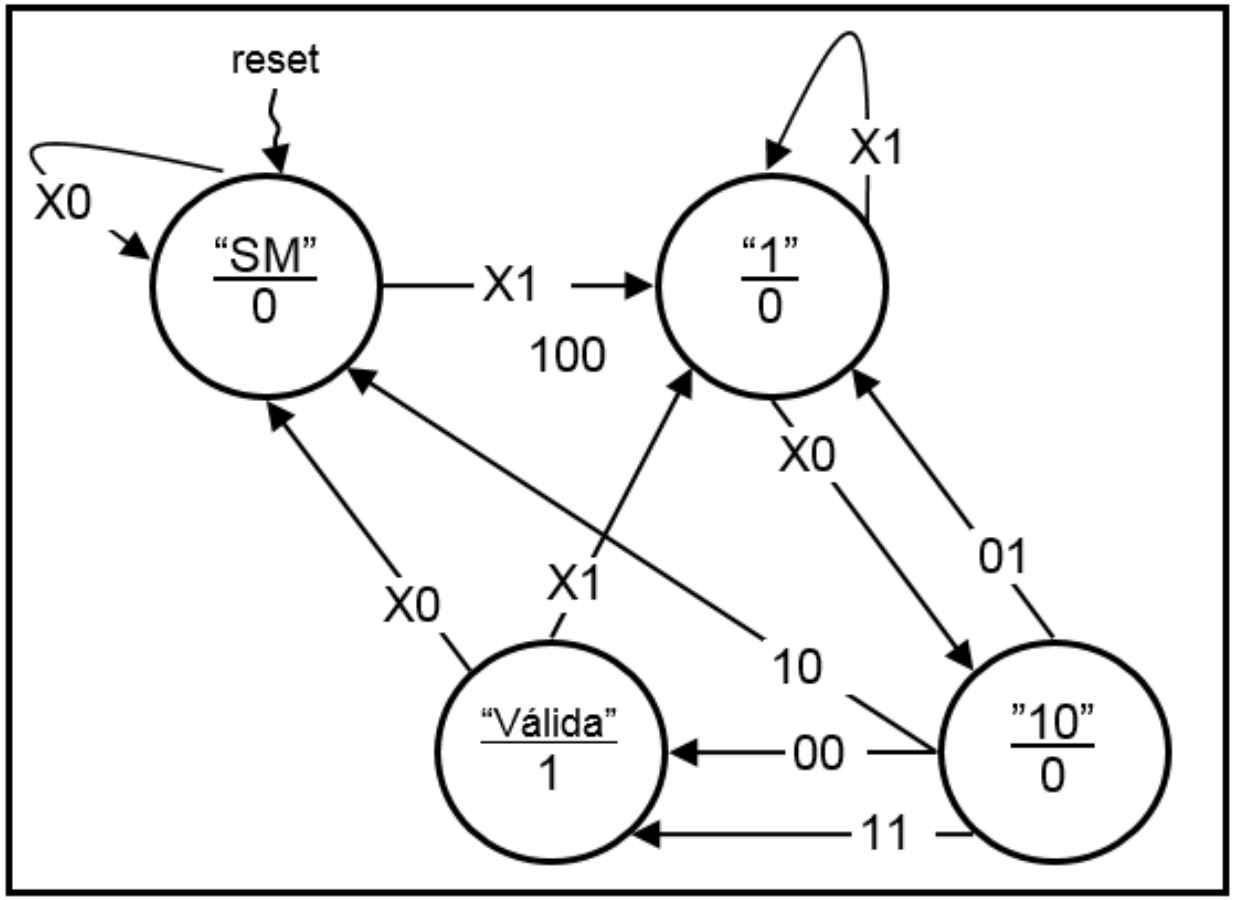
Example_2:

Solution:



States assignment in the order of detection of a valid sequence: SM (00), "1" (01), "10" (10) and "Valid Sequence" (11).If the inputs to the system are S and X and the output is 1 in the state 11 Output and State equations are:

$$D_0 = X + Q_1 \overline{Q_0}\ \overline{S}$$

$$D_1 = \overline{Q_1}\ Q_0 \overline{X} + Q_1 \overline{Q_0} SX + Q_1 \overline{Q_0}\ \overline{S}\ \overline{X}$$

$$Z = Q_1 Q_0$$

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Example_3:

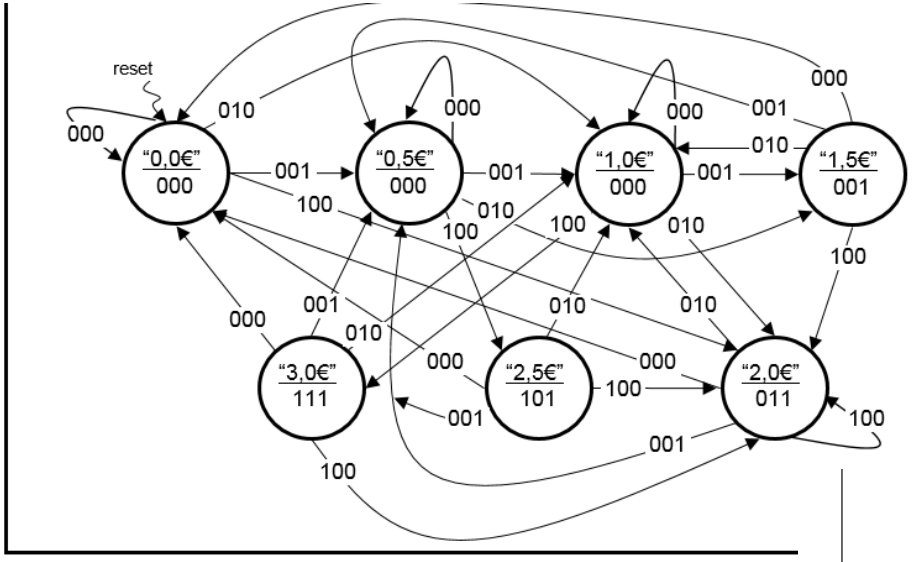
Solution:

Asign the inputs X2, X1, X0 is equal to introduce a coin of 2€, 1€ and 0.5€ respectively.

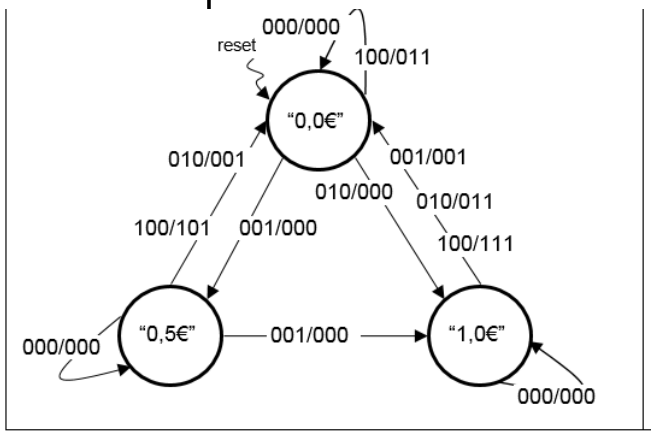
Any combination which implies receive more than one coin at a time is not considered.

Output assignment Z2, Z1, Z0 is equal to give back 1€, 0.5€ and dispense drink respectively.

Moore Design (7 states)



Mealy design (3 states)



Solution:

Asign the states:

Q_1Q_0 = 00 Receives 0 €

Q_1Q_0 = 01 Receives 0.5 €

Q_1Q_0 = 10 Receives 1 €

Output Equation: $Z_0=X_2+Q_0X_1+Q_1X_1+Q_1X_0$; $Z_1=Q_1X_1+\overline{Q_0}X_2$; $Z_2=Q_1X_2+Q_0X_2$

State Equation: : $D_0=\overline{Q_1}\ \overline{Q_0}X_0+Q_0\overline{X_2}\ \overline{X_1}X_0$; $D_1=Q_0X_0+\overline{Q_1}\ \overline{Q_0}X_1+Q_1\overline{X_2}\ \overline{X_1}\ \overline{X_0}$

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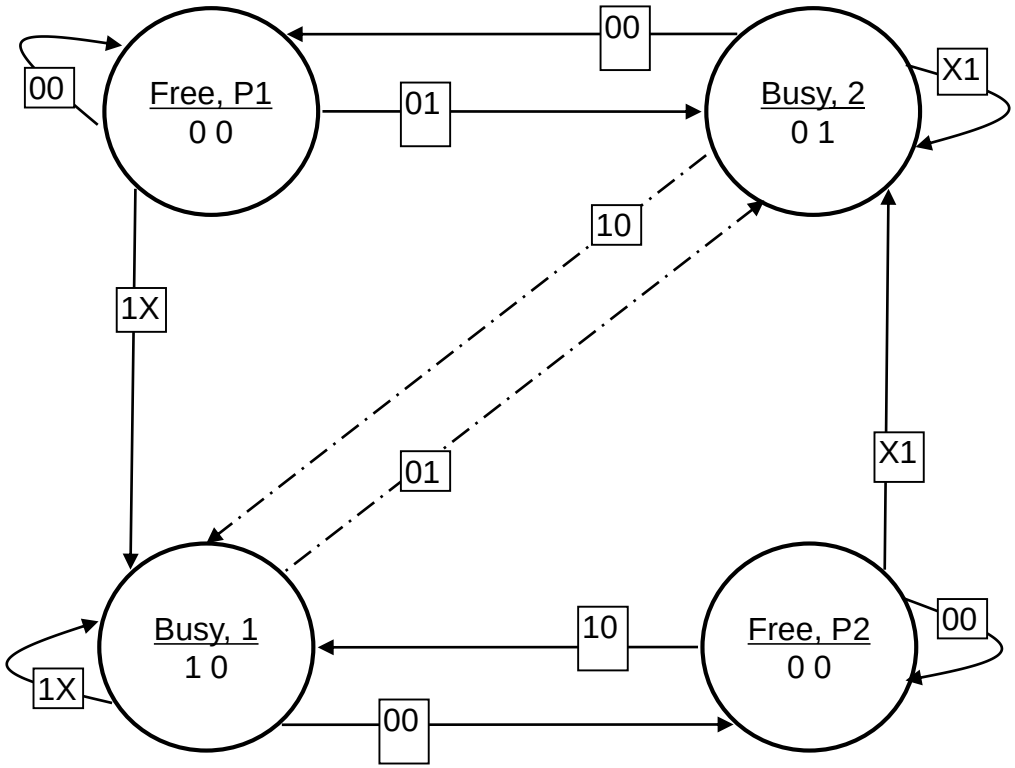
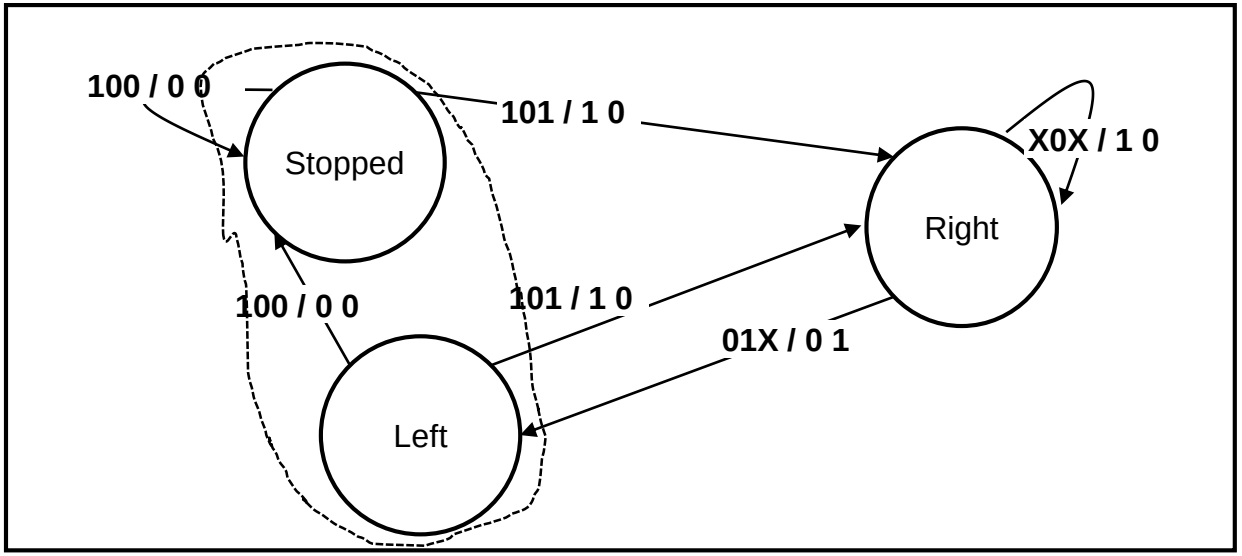
Example_4:

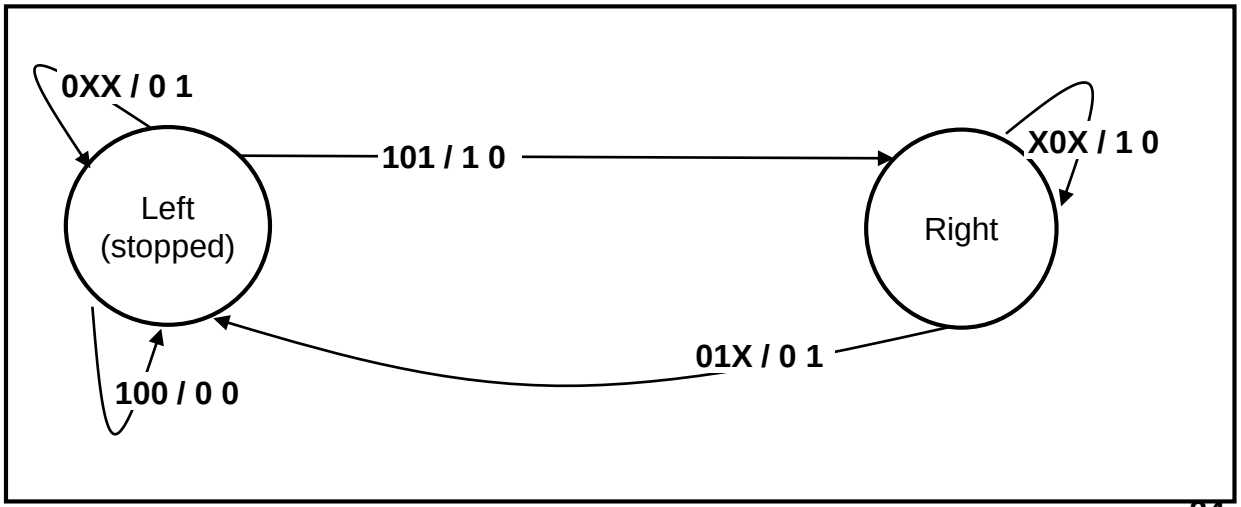

Free, P1
0 0
Busy, 2
0 1
Busy, 1
1 0
Free, P2
0 0
00
01
10
1X
X1
00
X1
01
10
00
1X
00

Example_5:



ABP / D I

If left ≡ Stopped



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