Combinational Circuits

Computer Fundamentals

Escuela Politécnica Superior. U.A.M

Unit 2 - Index

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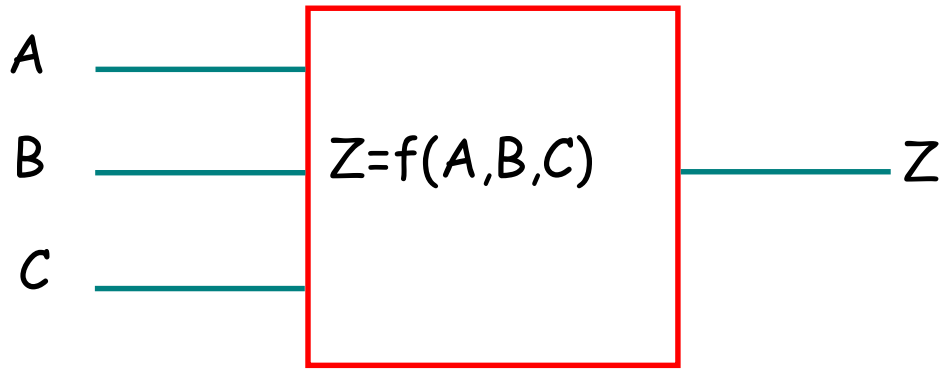
U2. Combinational circuits

- **Circuit without memory**, outputs are a function of one or more of the inputs.
- For a certain combination of input variables a deterministic output is obtained (after a certain delay).



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Steps to solve any logic function

- Represent the truth table for the function
- Simplify the function (Karnaugh map).
- Construct the combinational circuit with the lowest number of logic gates.
  - Most efficient NAND or NOR (number of Transistors)

Example 1: Given a circuit of 4 inputs representing a binary number (ABCD). The circuit has an output Z_1 that must be activated (Z_1=1) when the binary number is a multiple of 3 and an output of Z_2 that must be activated when the binary number is a multiple of 2.

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Steps to solve any logic function

- Example 1:

#	A	B	C	D	Z_1	Z_2
0	0	0	0	0	1	1
1	0	0	0	1	0	0
2	0	0	1	0	0	1
3	0	0	1	1	1	0
4	0	1	0	0	0	1
5	0	1	0	1	0	0
6	0	1	1	0	1	1
7	0	1	1	1	0	0
8	1	0	0	0	0	1
9	1	0	0	1	1	0
10	1	0	1	0	0	1
11	1	0	1	1	0	0
12	1	1	0	0	1	1
13	1	1	0	1	0	0
14	1	1	1	0	0	1
15	1	1	1	1	1	0

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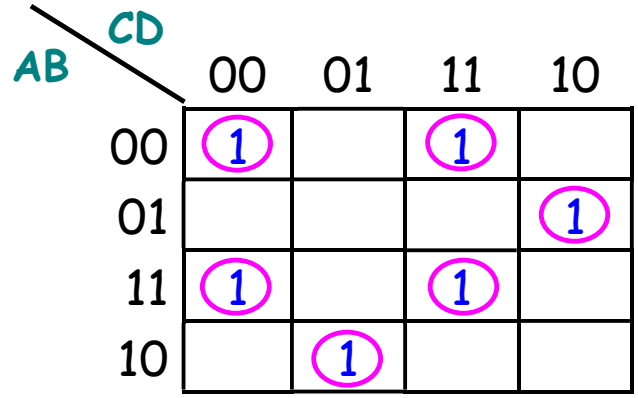
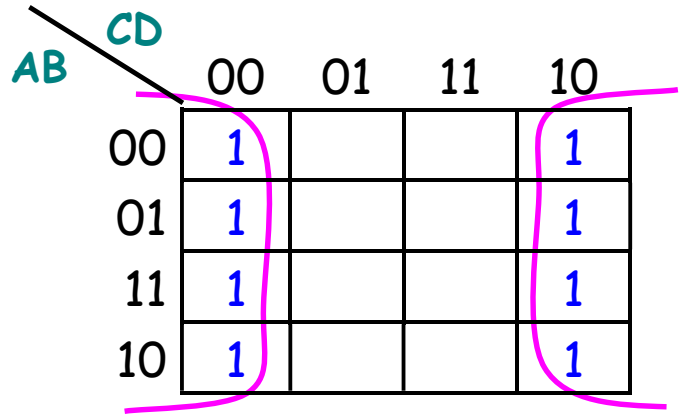
Steps to solve any logic function

- Example 1:

#	A	B	C	D	Z_1	Z_2
0	0	0	0	0	1	1
1	0	0	0	1	0	0
2	0	0	1	0	0	1
3	0	0	1	1	1	0
4	0	1	0	0	0	1
5	0	1	0	1	0	0
6	0	1	1	0	1	1
7	0	1	1	1	0	0
8	1	0	0	0	0	1
9	1	0	0	1	1	0
10	1	0	1	0	0	1
11	1	0	1	1	0	0
12	1	1	0	0	1	1
13	1	1	0	1	0	0
14	1	1	1	0	0	1
15	1	1	1	1	1	0



$$Z_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + ABCD + A\bar{B}\bar{C}D$$



$$Z_2 = \bar{D}$$

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Steps to solve any logic function

- Incompletely specified Functions
  - Output values defined for a subset of input values
  - Non defined output values are represented as "X".
  - When solving Karnaugh table "X"s are taken as 0 or 1, as convenient.

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Steps to solve any logic function

- Incompletely specified Function
  - Example 2: Example 1 defined from 0 to 9

#	A	B	C	D	Z_1	Z_2
0	0	0	0	0	1	1
1	0	0	0	1	0	0
2	0	0	1	0	0	1
3	0	0	1	1	1	0
4	0	1	0	0	0	1
5	0	1	0	1	0	0
6	0	1	1	0	1	1
7	0	1	1	1	0	0
8	1	0	0	0	0	1
9	1	0	0	1	1	0
10	1	0	1	0	X	X
11	1	0	1	1	X	X
12	1	1	0	0	X	X
13	1	1	0	1	X	X
14	1	1	1	0	X	X
15	1	1	1	1	X	X

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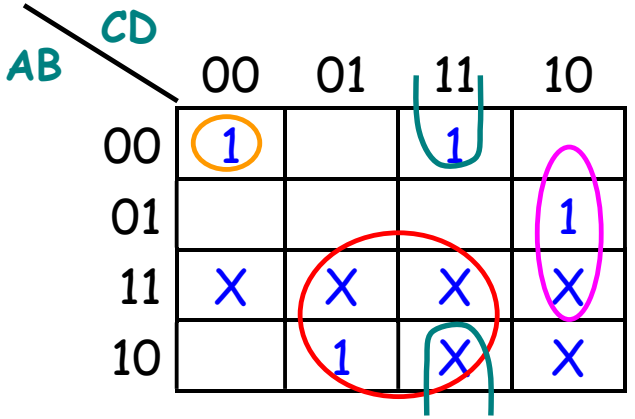
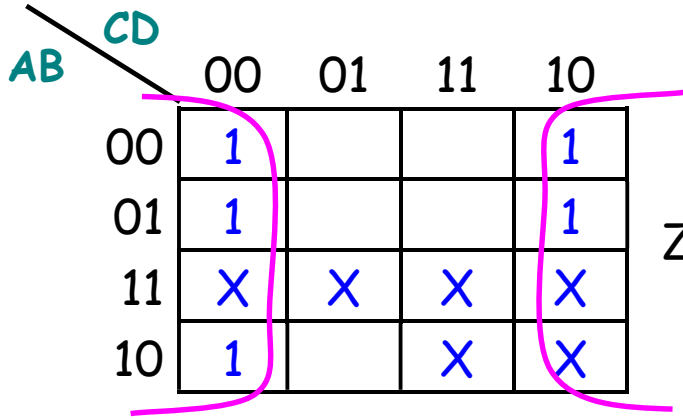
Steps to solve any logic function

- Incompletely specified Function
  - Example 2: Example 1 defined from 0 to 9

#	A	B	C	D	Z_1	Z_2
0	0	0	0	0	1	1
1	0	0	0	1	0	0
2	0	0	1	0	0	1
3	0	0	1	1	1	0
4	0	1	0	0	0	1
5	0	1	0	1	0	0
6	0	1	1	0	1	1
7	0	1	1	1	0	0
8	1	0	0	0	0	1
9	1	0	0	1	1	0
10	1	0	1	0	X	X
11	1	0	1	1	X	X
12	1	1	0	0	X	X
13	1	1	0	1	X	X
14	1	1	1	0	X	X
15	1	1	1	1	X	X



$$Z_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{B}CD + B\bar{C}\bar{D} + AD$$



$$Z_2 = \bar{D}$$

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U2.2. Basic combinational circuits

- **Decodifier (n-2^n):** n inputs y 2^n outputs (only one active).
- **Codifier (2^n-n):** n inputs (one or more active) y lg_2n outputs.
- **Multiplexer (n-1):** n inputs, 1 output y lg_2n control signals.
- **Demultiplexer (1-n):** 1 input, n outputs y lg_2n control signals.
- **Code converter (n-m):** n inputs y m outputs, without relation between them.
- **Other common combinational circuits:**
  - **Comparators**
  - **Semiadders y Adders**

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U2.2.1. Decodifier

- Combinatorial circuit of n inputs and 2^n outputs.
- Activates an unique output for each combination of inputs.

- Decodifier 2-4. 2 inputs and $2^2 = 4$ outputs
  - Truth table and equations:

A_1	A_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

$$O_0 = \overline{A_1} \cdot \overline{A_0}$$
$$O_1 = \overline{A_1} \cdot A_0$$
$$O_2 = A_1 \cdot \overline{A_0}$$
$$O_3 = A_1 \cdot A_0$$

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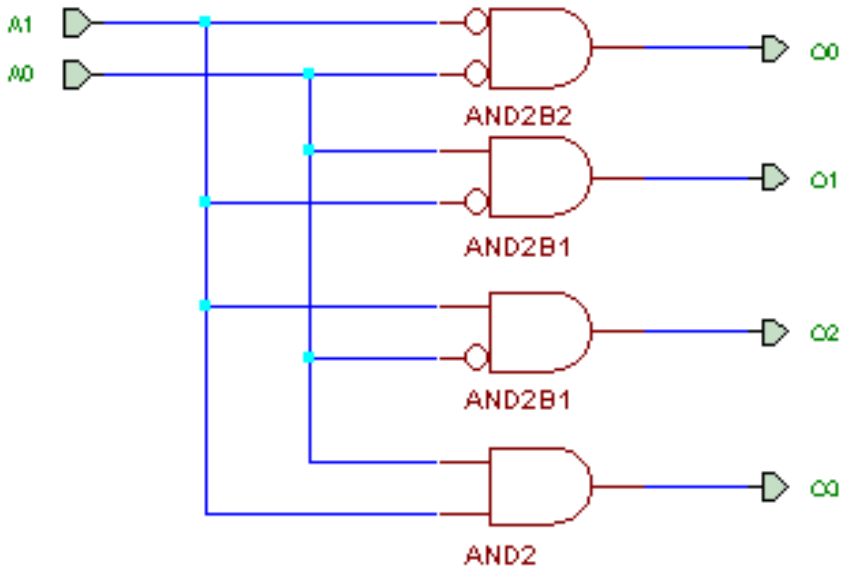
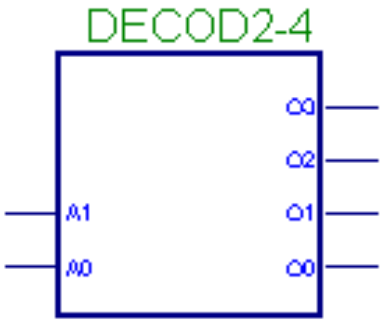
U2.2.1. Decodifier

- Decodifier 2-4. Logic circuit:

Squematic circuit:



Block diagram:



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U2.2.1. Decodifier

- Decodifier 2-4 with ENABLE signal
  - ENABLE = 1: Decodifier works normally
  - ENABLE = 0: No output active. Circuit "disabled"

  - Truth table and equations:

E	A_1	A_0	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$$O_0 = E \cdot \overline{A_1} \cdot \overline{A_0}$$
$$O_1 = E \cdot \overline{A_1} \cdot A_0$$
$$O_2 = E \cdot A_1 \cdot \overline{A_0}$$
$$O_3 = E \cdot A_1 \cdot A_0$$

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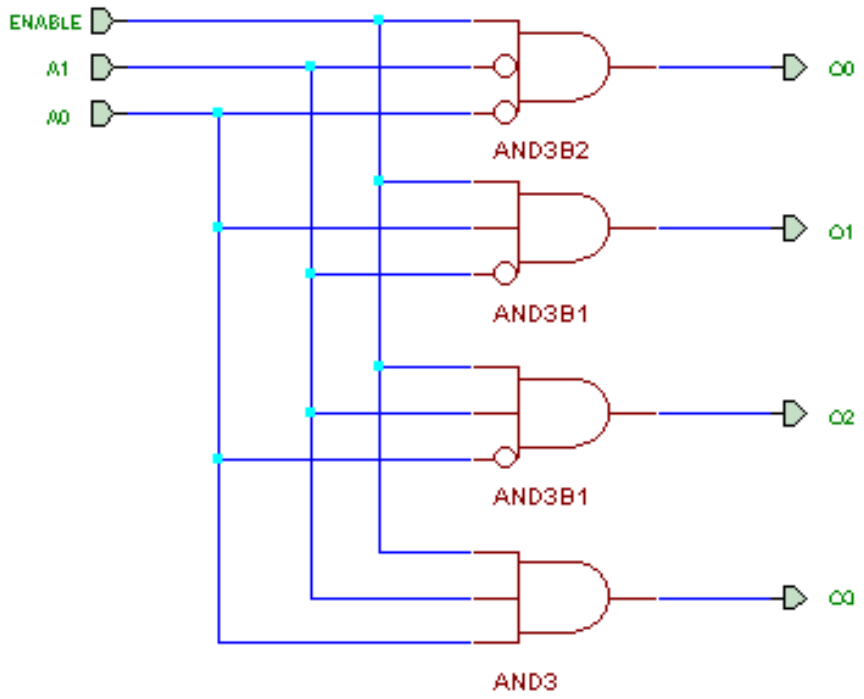
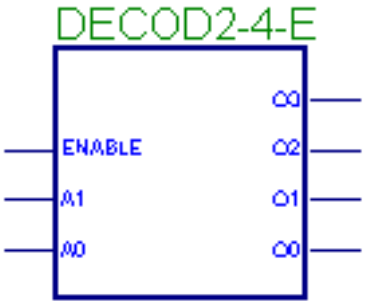
U2.2.1. Decodifier

- Decodifier 2-4 with ENABLE signal. Logic circuit:

Schematic circuit:



Block diagram:



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U2.2.1. Decodifier

- Decodifier 3-8. 3 inputs and $2^3 = 8$ outputs

  – Truth table and equations

A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

$$O_0 = m_0 = \overline{A_2} \cdot \overline{A_1} \cdot \overline{A_0}$$

$$O_1 = m_1 = \overline{A_2} \cdot \overline{A_1} \cdot A_0$$

$$O_2 = m_2 = \overline{A_2} \cdot A_1 \cdot \overline{A_0}$$

$$O_3 = m_3 = A_2 \cdot \overline{A_1} \cdot \overline{A_0}$$

$$\vdots$$

$$O_7 = m_7 = A_2 \cdot A_1 \cdot A_0$$

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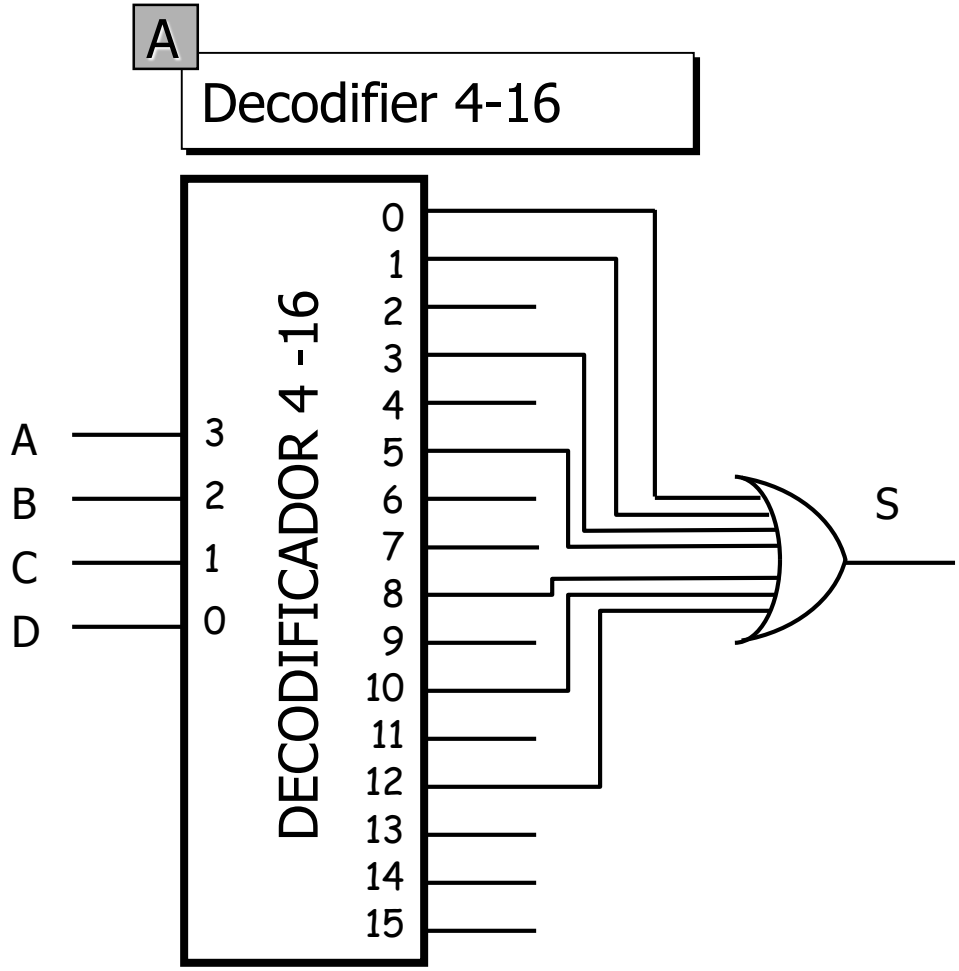
Logic functions with DEC

Example: A) Design F with a decodifier 4-16 and an OR-gate

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



- Asociate variables of the logic function to the inputs of the decodifier.
- Equivalent to the sum of products.

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U2.2.3. Codifiers

- Combinatorial circuit with n inputs and $\log_2 n$ outputs
  - **Elementary Codifier**: Each single input line activated, codifies at the ouput an specific number (the input number).

    What happens if more than one input is active?

  - **Priority Codifier**: If several input lines are activated, the output number is the one for the line with the highest priority (MSB)

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U2.2.3. Codifiers

- Priority codifier 8-3 with ENABLE
  - Among all active inputs, priority is assigned to the input with the highest index.

Truth table

E	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	A_2	A_1	A_0
0	X	X	X	X	X	X	X	X	0	0	0
1	1	X	X	X	X	X	X	X	1	1	1
1	0	1	X	X	X	X	X	X	1	1	0
1	0	0	1	X	X	X	X	X	1	0	1
1	0	0	0	1	X	X	X	X	1	0	0
1	0	0	0	0	1	X	X	X	0	1	1
1	0	0	0	0	0	1	X	X	0	1	0
1	0	0	0	0	0	0	1	X	0	0	1
1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0

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U2.2.3. Codifiers

- Priority codifier 8-3 with ENABLE

Equations:

$$A_0 = (I_7 + \overline{I_7}\,\overline{I_6} I_5 + \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4} I_3 + \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3}\,\overline{I_2} I_1)E$$

$$A_1 = (I_7 + \overline{I_7} I_6 + \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4} I_3 + \overline{I_7}\,\overline{I_6}\,\overline{I_5}\,\overline{I_4}\,\overline{I_3} I_2)E$$

$$A_2 = (I_7 + \overline{I_7} I_6 + \overline{I_7}\,\overline{I_6} I_5 + \overline{I_7}\,\overline{I_6}\,\overline{I_5} I_4)E$$

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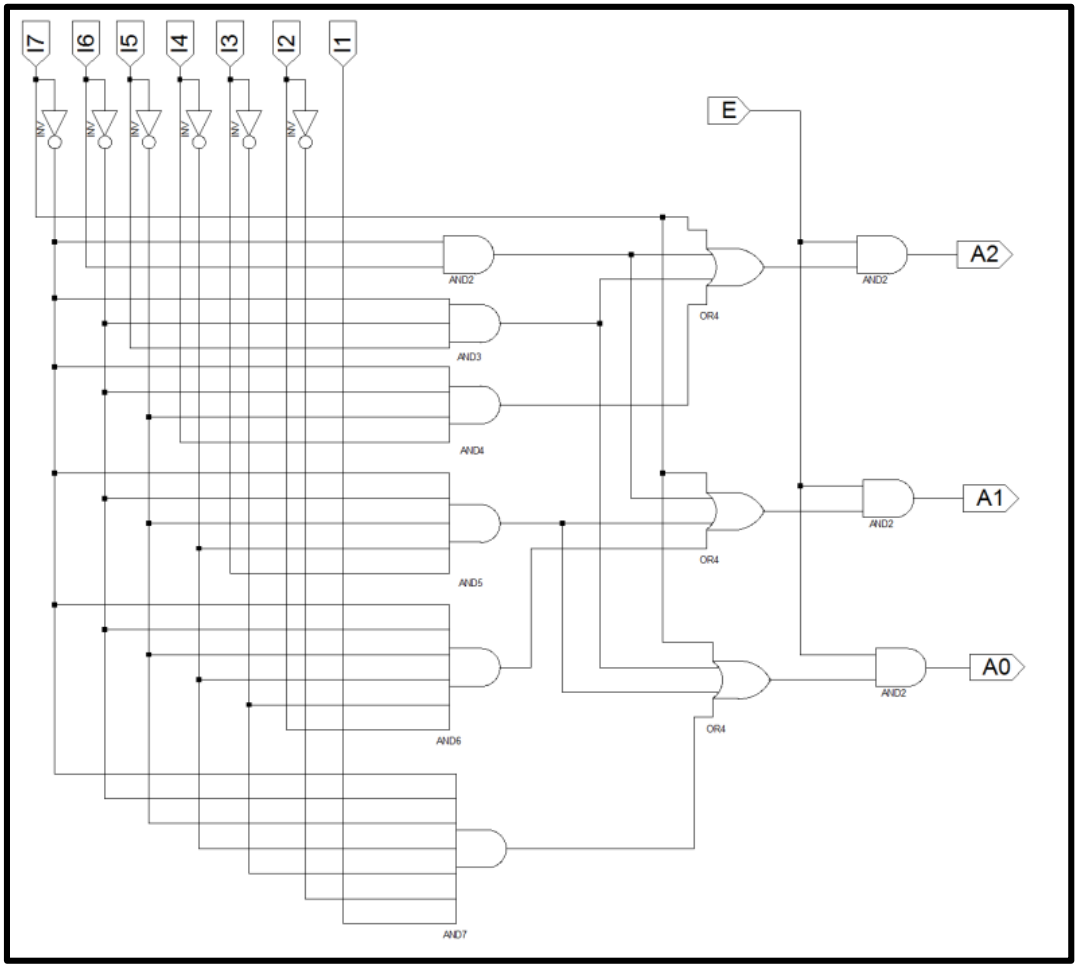
U2.2.3. Codifiers

- Priority codifier 8-3 with ENABLE

Circuit:



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U2.2.2 Multiplexer

- Data transmission from a selectable input to an unique output.
- It has n control lines that select (multiplex) one of the 2^n input lines and transmit it to the output.
- Each combination of control lines activates a gate.
- Two input types:
  - Data input
  - Control input

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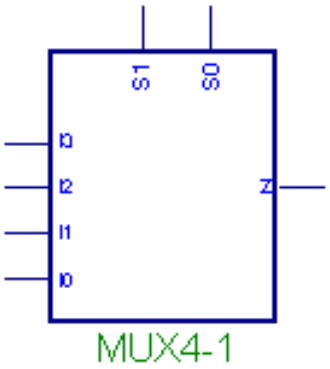
U2.2.2 Multiplexer

- Multiplexer 4-1. 4 inputs (data), 2 inputs (control) y 1 output
  - Truth table, equation and circuit:

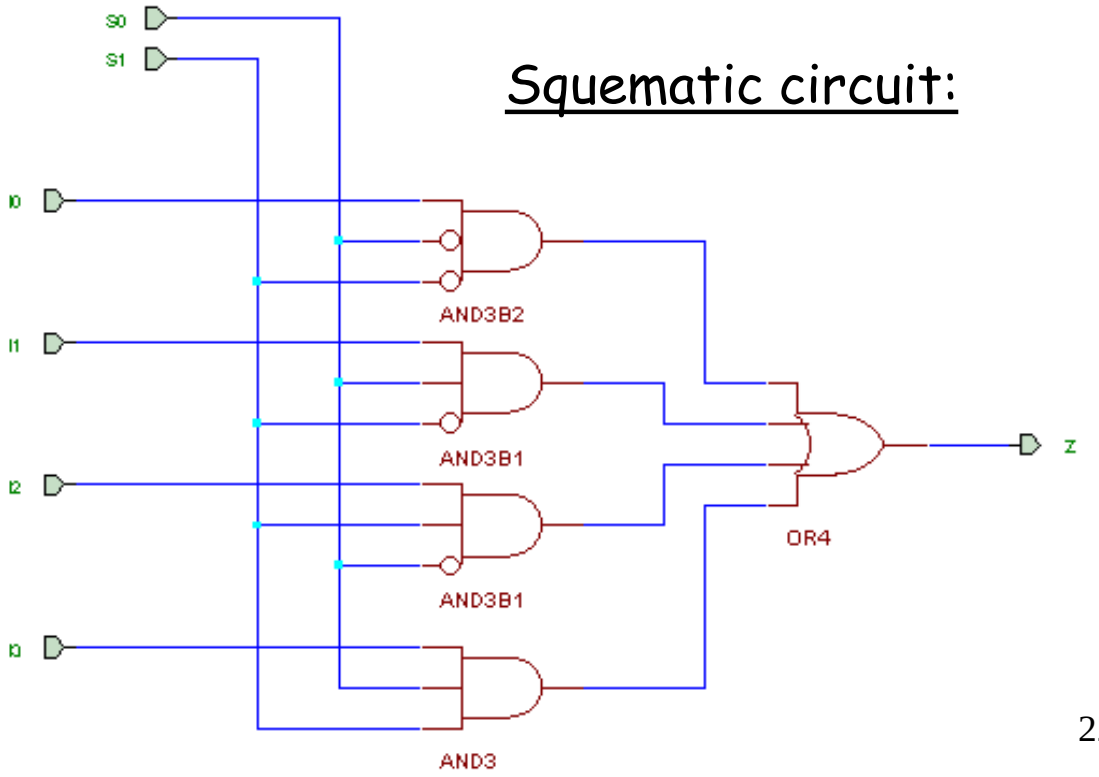
S_1	S_0	Output (Z)
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Z = S_1 S_0 I_3 + S_1 \overline{S_0} I_2 + \overline{S_1} S_0 I_1 + \overline{S_1}\,\overline{S_0} I_0$$



Block diagram:

Squematic circuit:



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U2.2.2 Multiplexer

- Multiplexer 8-1 with ENABLE signal. 8 inputs (data), 4 inputs (control) y 1 output

Truth table and equation

E	S_2	S_1	S_0	Z
0	X	X	X	0
1	0	0	0	I_0
1	0	0	1	I_1
1	0	1	0	I_2
1	0	1	1	I_3
1	1	0	0	I_4
1	1	0	1	I_5
1	1	1	0	I_6
1	1	1	1	I_7

$$Z = (S_2 S_1 S_0 I_7 + S_2 S_1 \overline{S_0} I_6 + S_2 \overline{S_1} S_0 I_5 + S_2 \overline{S_1}\,\overline{S_0} I_4 + \overline{S_2} S_1 S_0 I_3 + \overline{S_2} S_1 \overline{S_0} I_2 + \overline{S_2}\,\overline{S_1} S_0 I_1 + \overline{S_2}\,\overline{S_1}\,\overline{S_0} I_0) E$$

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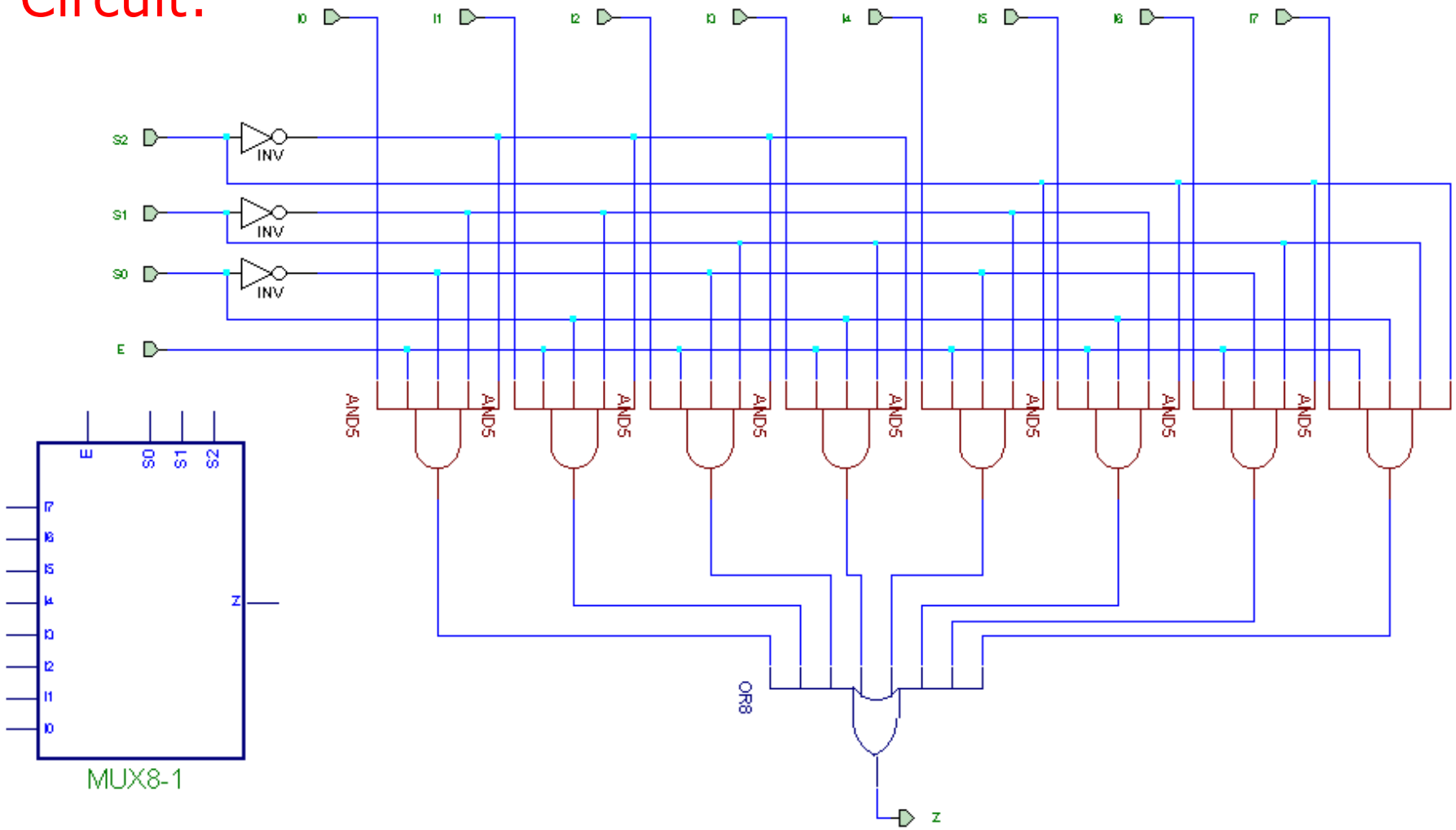
U2.2.2 Multiplexer

- Multiplexer 8-1 with ENABLE signal
  - Circuit:



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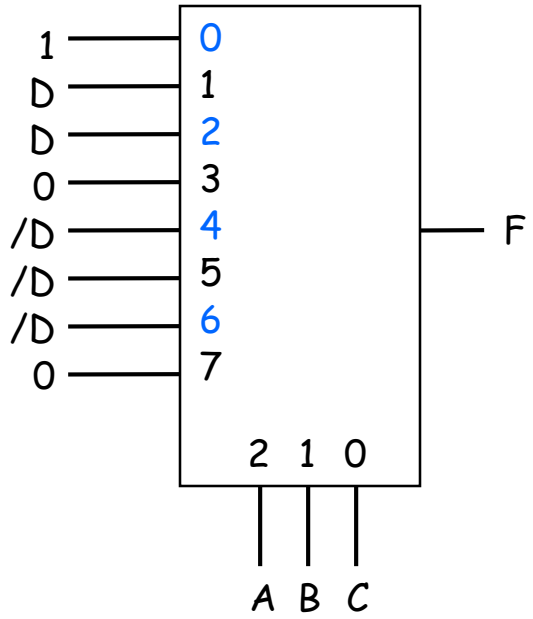
Logic functions with MUX

Example: B) Design F with a Multiplexer 8-1

A	B	C	D	F	
0	0	0	0	1	If is 11, input is put on 1
0	0	0	1	1	
0	0	1	0	0	If is 01, input is put on D
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	1	
0	1	1	0	0	If is 00, input is put on 0
0	1	1	1	0	
1	0	0	0	1	
1	0	0	1	0	
1	0	1	0	1	If is 10, input is put on /D
1	0	1	1	0	
1	1	0	0	1	
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	0	

B

Un MUX 8-1



1. Asociate variables (A,B,C,D,...) to control inputs (S_n...S_2,S_1,S_0).
2. Variables not associated with control are part of the inputs of the MUX
3. Variables associated with control are NEVER part of the inputs of the MUX
4. Some MUX inputs can be '0' or '1'

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U2.2.2 Demultiplexer

- They perform reversely to a multiplexer
- Data transmission can be directed from an unique input to a selectable output.
- Using n control lines, transmits (demultiplex) data from its unique input data line towards one of its 2^n outputs.
- It is equivalent to a decodifier with ENABLE, being the data line equivalent to ENABLE.

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U2.2.2 Demultiplexer

- Demultiplexer 1-4. 1 input (data), 2 inputs (control) and 4 outputs
  - Truth table and equations:

S_1	S_0	O_3	O_2	O_1	O_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

$$O_0 = \overline{S_1} \cdot \overline{S_0} \cdot I$$
$$O_1 = \overline{S_1} \cdot S_0 \cdot I$$
$$O_2 = S_1 \cdot \overline{S_0} \cdot I$$
$$O_3 = S_1 \cdot S_0 \cdot I$$

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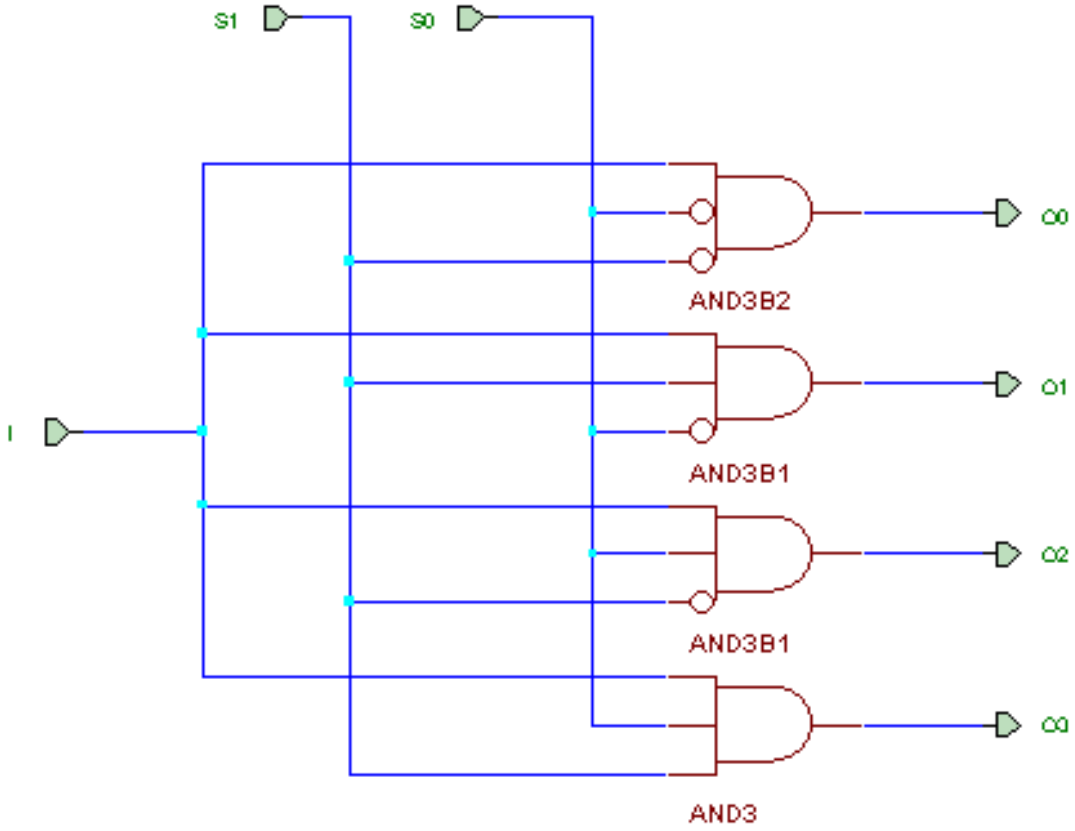
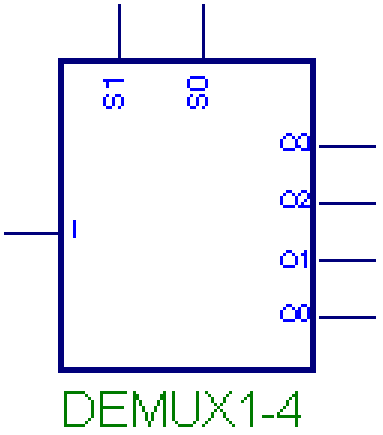
U2.2.2 Demultiplexer

- Demultiplexer 1-4. Circuit:

Schematic circuit:



Block diagram:



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U2.2.4. Code converter

- Each input word of n bits is converted or translateed to another word of m bits at the output.
- There may not be any relationship between input and output number of lines.
- Both words express the same information in different codes.

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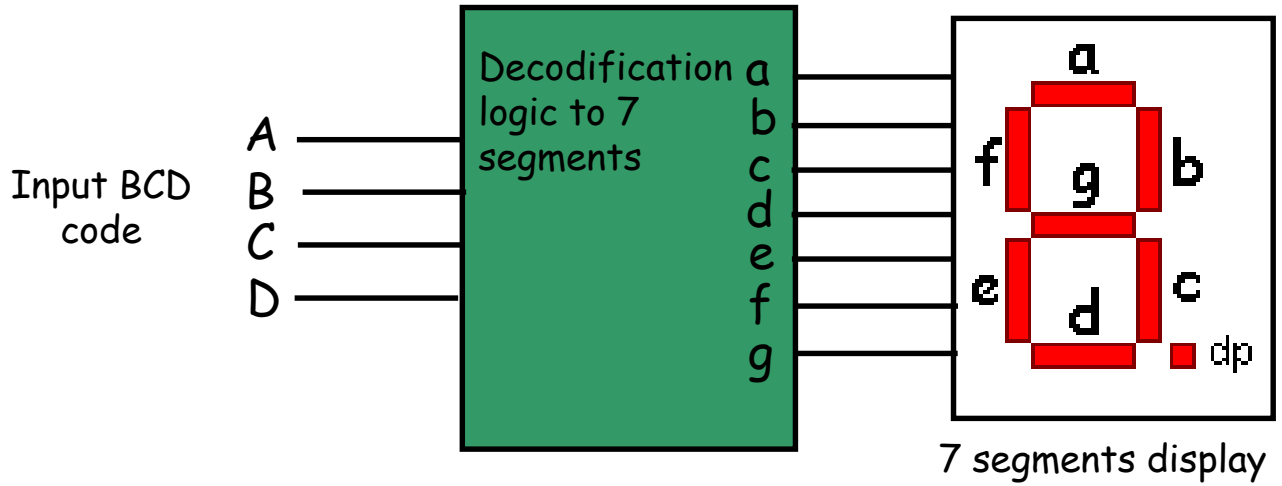
U2.2.4. Code converter

- BCD converter to 7 segments
  - Accepts BCD code (0..9) in its 4 inputs and outputs 7 lines correspondent to the 7 segments of the display.
  - Logic block diagram:



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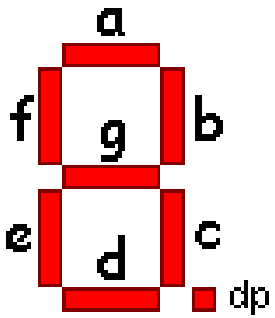
U2.2.4. Code converter

- BCD conversor to 7 segments
  - Segments corresponding to digits are:

Digit	Activated segments
0	a,b,c,d,e,f
1	b,c
2	a,b,d,e,g
3	a,b,c,d,g
4	b,c,f,g
5	a,c,d,f,g
6	a,c,d,e,f,g
7	a,b,c
8	a,b,c,d,e,f,g
9	a,b,c,d,f,g



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U2.2.4. Code converter

- BCD conversor to 7 segments
  - Truth table:

Digito Decimal	Entradas				Salidas de segmentos						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	X	X	X	X	X	X	X
11	1	0	1	1	X	X	X	X	X	X	X
12	1	1	0	0	X	X	X	X	X	X	X
13	1	1	0	1	X	X	X	X	X	X	X
14	1	1	1	0	X	X	X	X	X	X	X
15	1	1	1	1	X	X	X	X	X	X	X

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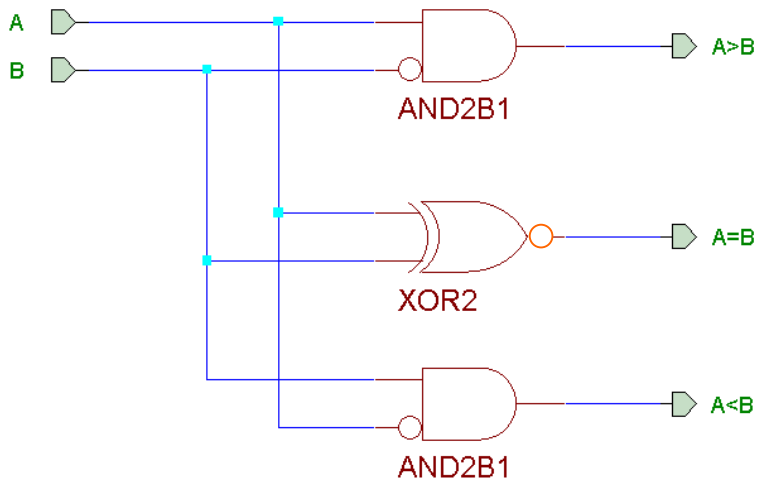
U2.2.5. Bit comparator

- **Bit comparator:** circuit with 2 inputs and 3 outputs used to compare bits
- 2-bit comparator: Truth table, equations and circuit

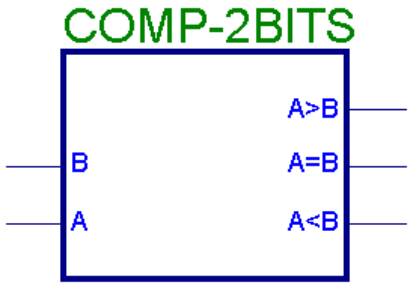
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0



$$A > B = A\overline{B}$$

$$A = B = \overline{A \oplus B}$$

$$A < B = \overline{A}B$$



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