Boolean Algebra. Logic design

Computer Fundamentals

Escuela Politécnica Superior. UAM

Some of the slides are extracted from the book "Digital Design & Computer Architecture, D.M Harris y S.L. Harris © Elsevier 2007.

Unit 1 Index

U1. Boolean Algebra and Logic Design

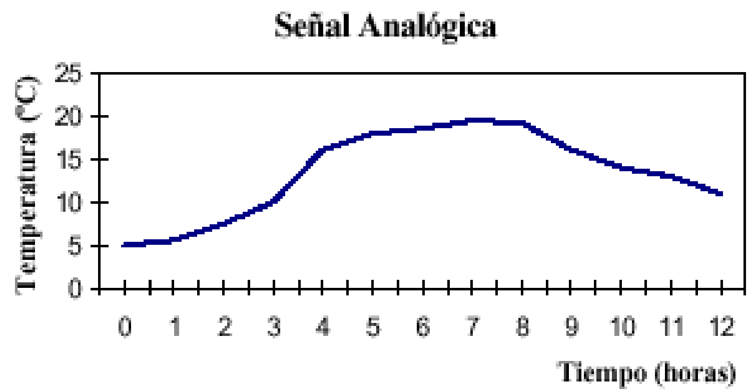
Escuela Politécnica Superior

U1.1. Analog vs. Digital

Analog vs Digital

Analog Systems:

- Work with analog signals.
- Physical signals to represent them: Analog signals
- Analog signal: Infinite posible real values. Vary continuously.
- Example: Mercury thermometer

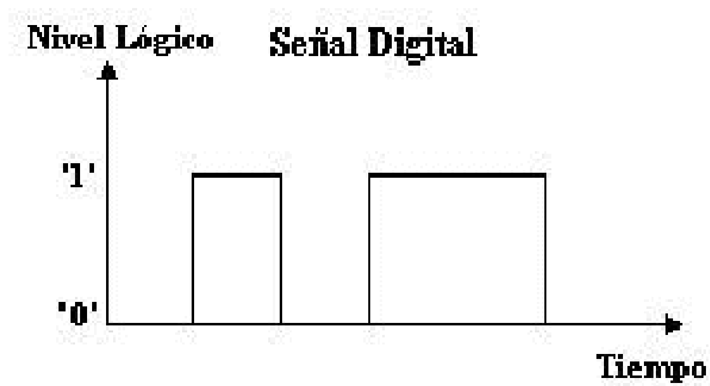


U1.1. Analog vs. Digital

Analog vs Digital

Digital systems:

- Work with digital signals.
  - 2 posible values.
  - Values are expressed through declarative sentences.
  - Both values are exclusive
- Physical values to represent them: Digital signals.
- Digital signal: Takes discrete values.
- Example: Light switch



Escuela Politécnica Superior

U1.2. Binary numerical system

Positional numerical system

Digit values depends on its position in the number.

- Decimal system:

10^3=1000's column	10^2=100's column	10^1=10's column	10^0=1's column	System base	Numerical equivalent in decimal system
5	3	7	4	10	

- Binary system:

2^3=8's column	2^2=4's column	2^1=2's column	2^0=1's column	System base	Numerical equivalent in decimal system
1	1	0	1	2	

Escuela Politécnica Superior

U1.2. Binary numerical system

Conversion between systems:

- Convert to decimal the number: 10101_2

- Convert to binary the number: 47_{10}

Escuela Politécnica Superior

U1.2. Binary numerical system

It is recommended to memorize:

- ✓ $2^0 = 1$
- ✓ $2^1 = 2$
- ✓ $2^2 = 4$
- ✓ $2^3 = 8$
- ✓ $2^4 = 16$
- ✓ $2^5 = 32$
- ✓ $2^6 = 64$
- ✓ $2^7 = 128$
- ✓ $2^8 = 256$
- ✓ $2^9 = 512$
- ✓ $2^{10} = 1024 = 1$ k

  ****

- ✓ $2^{20} = 1.048.576 = 1$ M
- ✓ $2^{30} = 1.073.741.824 = 1$ G
- ✓ $2^{32} = 2^2 * 2^{30} = 4$ G

Example:

$2^{13} =$?

$2^{24} =$?

$2^{15} =$?

Escuela Politécnica Superior

U1.2. Binary numerical system

Binary system representation range:

- A number with n decimal digits (0 - 9) can represent **10^n** different numbers in the range **$[0, 10^n-1]$**.
  - Example: when n = 3: 10^3 = 1000 different numbers. in the range [0, 999].

- A number with n binary digits (0 and 1) can represent **2^n** different numbers in the range **$[0, 2^n-1]$**.
  - Example: when n = 3: 2^3 = 8 different number in the range [0, 7].

Escuela Politécnica Superior

U1.2. Binary numerical system

Hexadecimal system:

The hexadecimal system is a positional numerical system with **base 16**, commonly used to abbreviate binary numbers.

Hexadecimal digit	Decimal equivalent	Binary Equivalent	Hexadecimal digit	Decimal equivalent	Binary equivalent
0	0	0000	8	8	1000
1	1	0001	9	9	1001
2	2	0010	A	10	1010
3	3	0011	B	11	1011
4	4	0100	C	12	1100
5	5	0101	D	13	1101
6	6	0110	E	14	1110
7	7	0111	F	15	1111

Escuela Politécnica Superior

U1.2. Binary numerical system

Conversion between systems. Examples:

- Convert **to binary** from hexadecimal: $4AF_{16}$ (also 0x4AF)

- Convert **to decimal** from hexadecimal: 0x4AF

Escuela Politécnica Superior

U1.2. Binary numerical system

- Bits

$$\underbrace{1}_{\substack{\text{Most}\\\text{Significant}\\\text{Bit}\\\text{(msb)}}}\;0\;0\;1\;1\;0\;1\;\underbrace{1}_{\substack{\text{Least}\\\text{Significant}\\\text{Bit}\\\text{(lsb)}}}$$

- Bytes & Nibbles

$$\overbrace{1\;0\;0\;1\;\underbrace{1\;0\;1\;1}_{\text{Nibble = 4 bits}}}^{\text{Byte = 8 bits}}$$

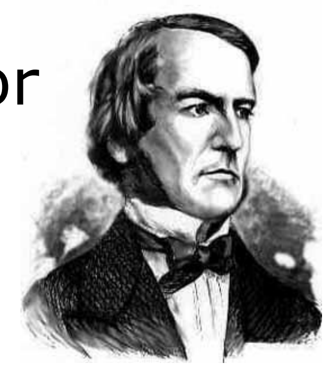
- Bytes

$$\underbrace{\text{FC}}_{\substack{\text{Most}\\\text{Significant}\\\text{Byte}\\\text{(MSB)}}}\quad \text{A5}\quad \text{C0}\quad \underbrace{\text{8D}}_{\substack{\text{Least}\\\text{Significant}\\\text{Byte}\\\text{(LSB)}}}$$

Escuela Politécnica Superior

U1.3. Basic boolean algebra properties and theorems

Boolean Algebra: matehmatical tool used for analysis and synthesis of binary digital



George Boole
British Mathematician
(1815-1864)

Boolean variable: digital signal which only has 1 out of 2 posible values in an instant. Both values are mutually exclusive.

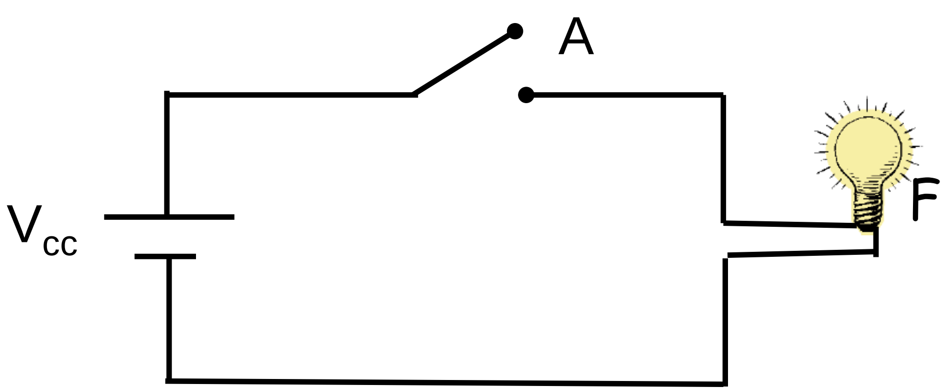
Represented as: **0** and **1**; **OFF** and **ON**; **HIGH** and **LOW** ; **etc…**

Escuela Politécnica Superior

U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- Logic variables and electric circuits:



- Switch A state:
  - Open (0)
  - Closed (1)
- Light bulb F state:
  - OFF (0)
  - ON (1)

State of logic variable “light bulb” is a function of logic variable “switch”.

Function: “Light bulb is ON **if** switch is closed”

U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- **Logic function:** Circuit accepting input logical values and outputs a logical value.
- **Truth table:** describes logic function working principle
  - Specifies all posible outputs for all posible input logic values.
  - Grapgical representationg of all cases that can happen in an algebraic relation and its respective results.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

- **Logic gates:** Implementation of most basic logic functions.

Escuela Politécnica Superior

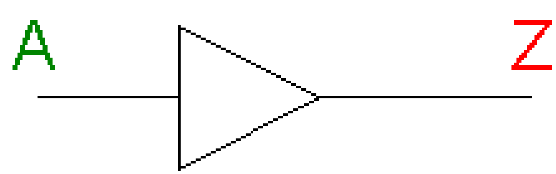
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- Amplifier (BUFFER)
  - Simplest logic gate
  - One input(A) and one output (Z)
  - Truth table:

A	Z
1	1
0	0

  - Logic equation: **Z = A**
  - Graphical representation:



Escuela Politécnica Superior

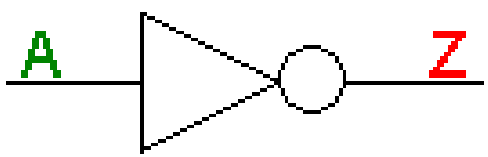
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- NOT gate (or INVERTER)
  - One input(A) and one output (Z)
  - Truth table:

A	Z
1	0
0	1

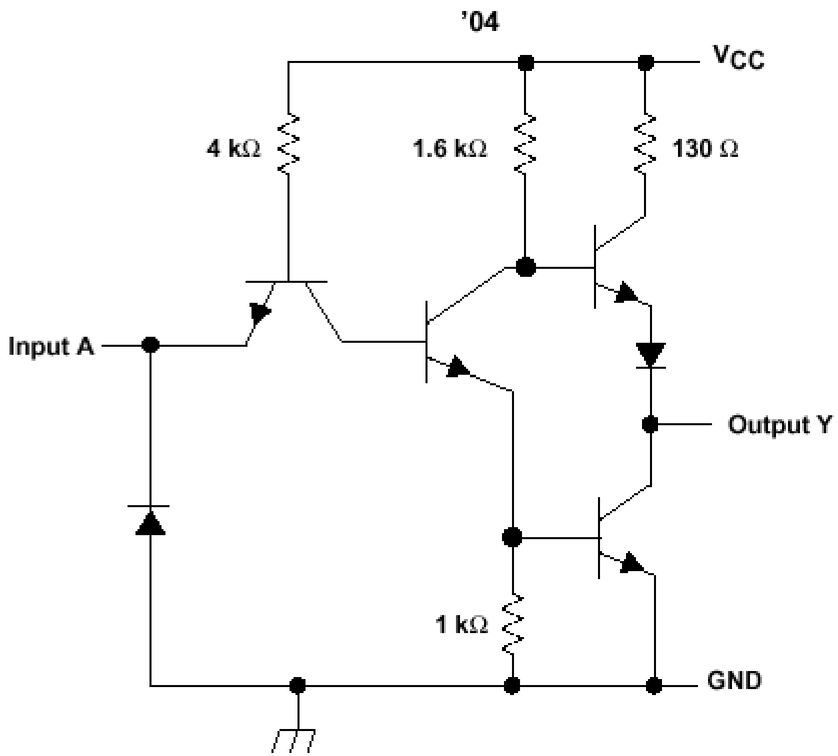
  - Logic equation: $Z = \overline{A}$
  - Graphical representation:



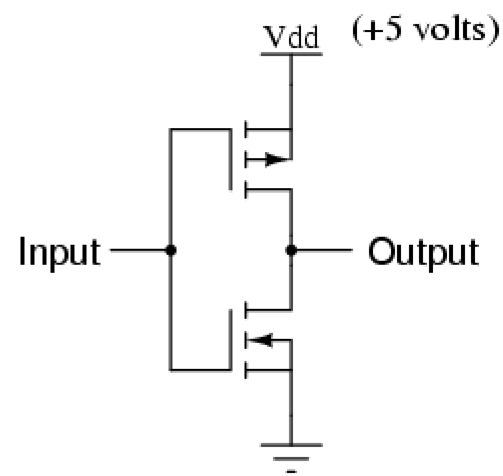
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- NOT gate (or INVERSOR)
  - Internal logic of NOT gate:

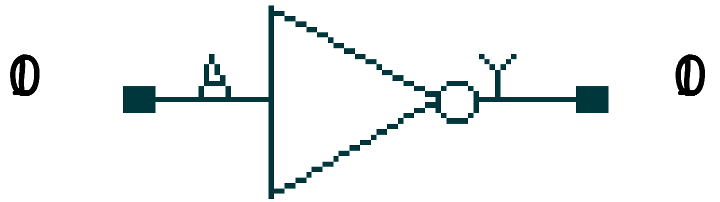


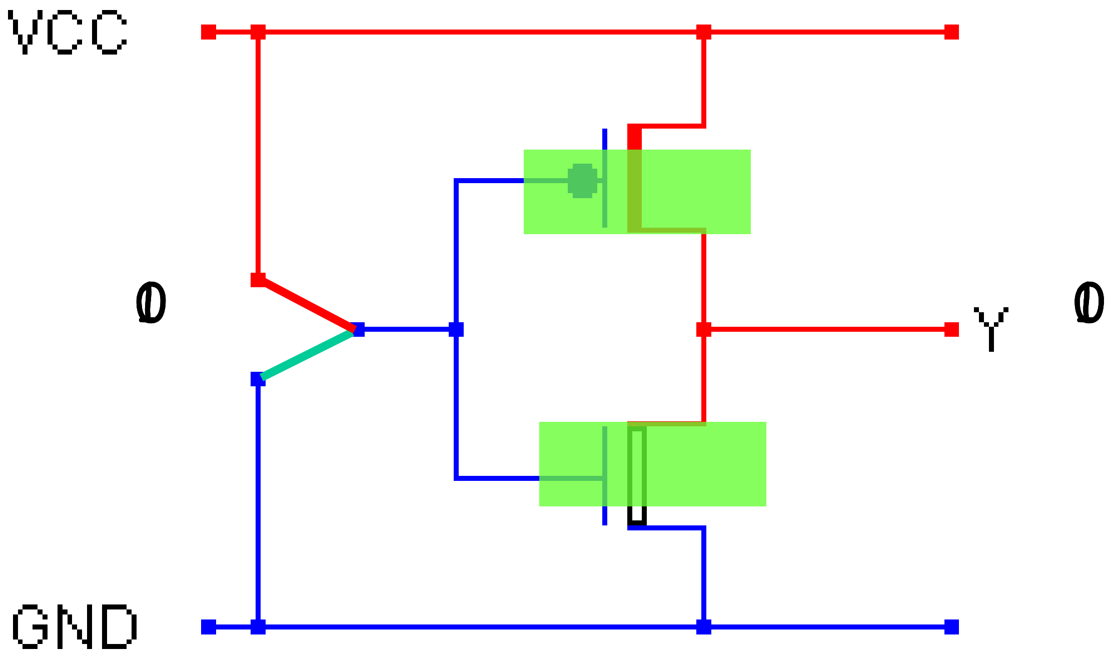
Inverter circuit using IGFETs



U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

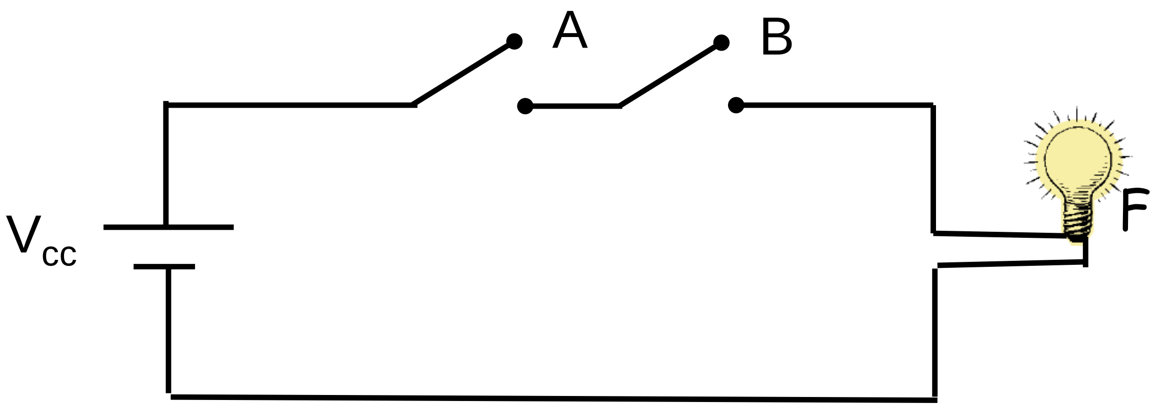




U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- AND gate:
  - AND gate illustrated as switches:



Function: Light bulb F is ON if:

"switch A **AND** switch B are <u>both</u> closed".

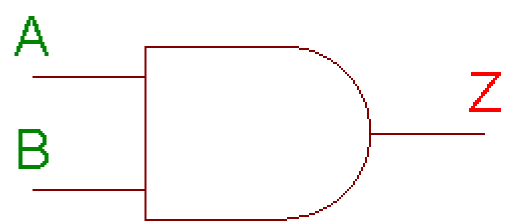
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- AND gate (2 inputs {A,B} and 1 output {Z})
  - Z=1 if both inputs A and B are simultaneously at 1
  - Truth table:

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

  - Logic equation: **$Z = A \bullet B$**
  - Graphical representation:

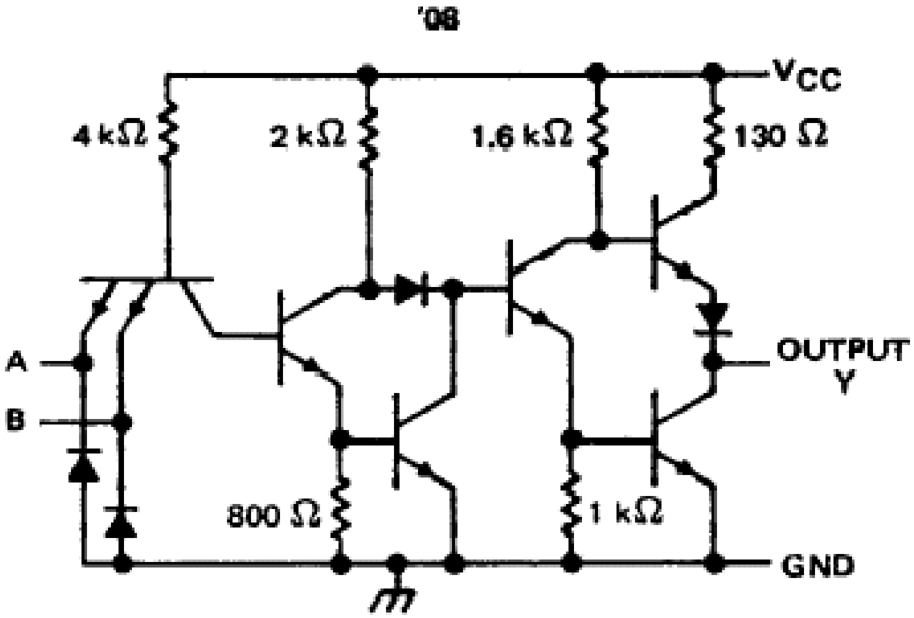


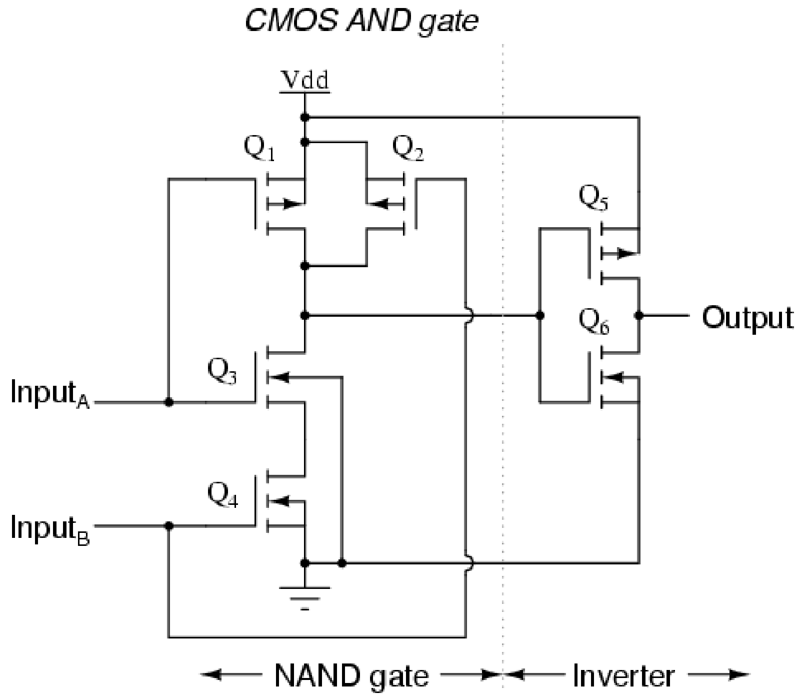
AND gate with multiple inputs?

U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- AND gate:
  - Internal logic

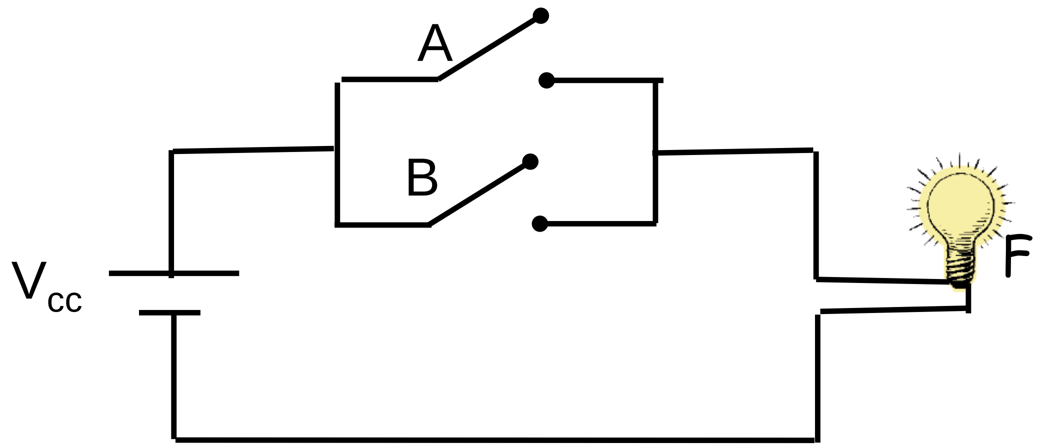




U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- OR gate
  - OR gate illustrated as switches:



Function: Light bulb f is ON if:

"switch A **OR** switch B **OR** both are closed"

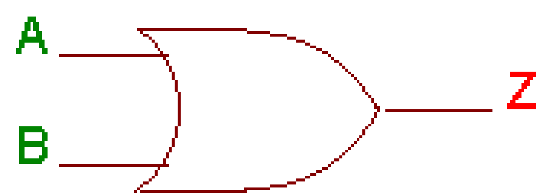
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- OR gate: (2 inputs {A,B} and 1 output {Z})
  - Z = 1 if at least one of the inputs is 1
  - Truth table:

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

  - Logic equation: $Z = A + B$
  - Graphical representation:



OR gate of multiple inputs?

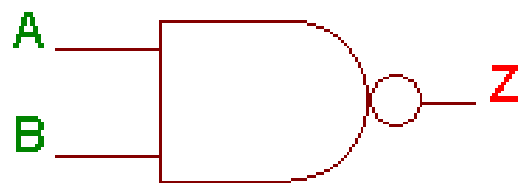
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- NAND gate: (2 inputs {A,B} and 1 output {Z})
  - Z=1 if at least one of the inputs is at 0
  - Truth table:

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

  - Logic equation: $Z = \overline{A \cdot B}$
  - Graphical representation:



NAND gate of multiple inputs?

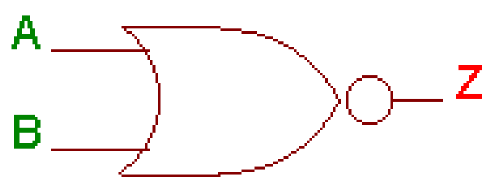
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- NOR gate: (2 inputs {A,B} and 1 output {Z})
  - Z=0 if at least one of the inputs is 1
  - Z=1 if both inputs are 0
  - Truth table:

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

  - Logic equation: $Z = \overline{A + B}$
  - Graphical representation:



NOR gate of multiple inputs?

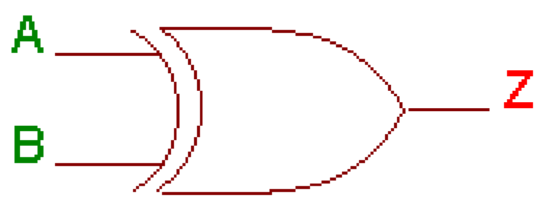
U1.3. Basic boolean algebra properties and theorems

U1.3.1. Boolean expression and operations:

- XOR gate (OR-exclusive):
  (2 inputs {A,B} and 1 output {Z})
  - Z=1 if and only if one input is 1
  - Truth table:

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

  - Logic equation: $Z = A \oplus B$
  - Graphical representation:



Escuela Politécnica Superior

XOR gate of multiple inputs?

U1.3. Basic boolean algebra properties and theorems

U1.3.2. Boolean algebra rules and laws:

Name		Theorem		Dual
Identity	**T1**	$B \bullet 1 = B$	**T1'**	$B + 0 = B$
Annulment	**T2**	$B \bullet 0 = 0$	**T2'**	$B + 1 = 1$
Idempotent	**T3**	$B \bullet B = B$	**T3'**	$B + B = B$
Double negation	**T4**	$//B = B$		
Complement	**T5**	$B \bullet /B = 0$	**T5'**	$B + /B = 1$
Commutative	**T6**	$B \bullet C = C \bullet B$	**T6'**	$B + C = C + B$
Associative	**T7**	$(B \bullet C) \bullet D = B \bullet (C \bullet D)$	**T7'**	$(B + C) + D = B + (C + D)$
Distributive	**T8**	$(B \bullet C) + (B \bullet D) = B \bullet (C + D)$	**T8'**	$(B + C) \bullet (B + D) = B + (C \bullet D)$
De Morgan Law	**T12**	$/(B_0 \bullet B_1 \bullet \ldots \bullet B_{n-2} \bullet B_{n-1}) =$ $= (/B_0 + /B_1 + \ldots + /B_{n-2} + /B_{n-1})$	**T12'**	$/(B_0 + B_1 + \ldots + B_{n-2} + B_{n-1}) =$ $= (/B_0 \bullet /B_1 \bullet \ldots \bullet /B_{n-2} \bullet /B_{n-1})$

Escuela Politécnica Superior

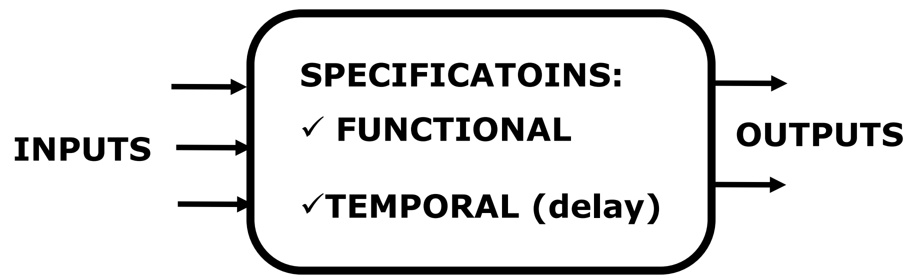
Dual equations on Boolean algebra

LOGIC CIRCUITS

The combination of different logic values at the input causes different logic values at the output
=> LOGIC CIRCUIT

A logic circuit is composed of:

- Inputs
- Outputs
- Functional specification
- Temporal specification

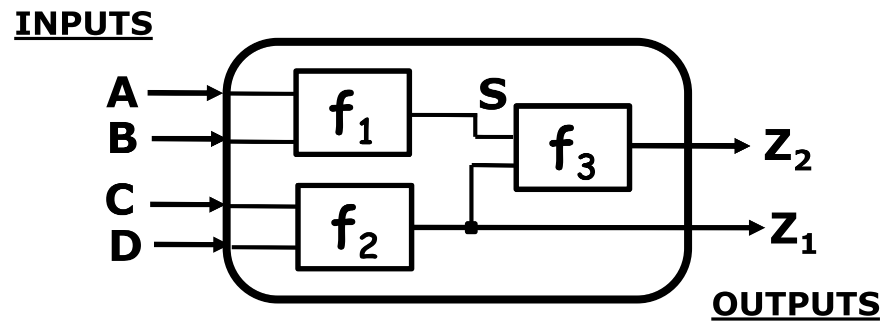


Any logic function can be expressed using AND, OR and NOT gates.

LOGIC CIRCUITS

Logic circuit example:

- inputs: A, B, C y D
- Outputs: Z_1 y Z_2
- Functional specification
  - $S = \mathbf{f_1}(A, B)$
  - $Z_1 = \mathbf{f_2}(C, D)$
  - $Z_2 = \mathbf{f_3}(S, Z_1) = (A, B, C, D)$
- Temporal specification: ($\Delta t_{Z2} = MAX\{\Delta t_{f1}, \Delta t_{f2}\} + \Delta t_{f3}$)



Combinational logic: output state depends exclusively of inputs states. Circuit without memory.

Sequential logic: output state also depends on previous state of the system. Circuit with memory.

U1.4. Logic functions

- **Logic function:** Boolean expression that relates logic variables directly or complemented by the use of AND and OR operations.

- Logic functions are represented as logic circuits with 2 levels whose **canonical form** can be:
  - Sum Of Products of all variables or their conjugates:

    Sum of **Minterms** // **SOP** Circuits (*Sum Of Products*)

  - Product Of Sums of all variables or their conjugates :

    Product of **Maxterms** // **POS** Circuits (*Product Of Sums*)

Escuela Politécnica Superior

U1.4. Logic functions

- All Boolean equations can be represented as a sum of minterms (SOP).
- Each row of a truth table is a **minterm.**
- A minterm is a product (AND) of variables and their complement.
- Each minterm is TRUE ('1') for that row (and only for that row)
- Function is constructed as the sum (OR) of minterms whose output is TRUE.
- It is then a sum (OR) of products (AND)

A	B	Y	minterm
0	0	0	$\overline{A}\ \overline{B}$
0	1	1	$\overline{A}\ B$
1	0	0	$A\ \overline{B}$
1	1	1	$A\ B$

$$Y = F(A, B) = \overline{A}B + AB$$

Escuela Politécnica Superior

U1.4. Logic functions

- All Boolean equations can be represented as a product of maxterms (POS).
- Each row of a truth table is a maxterm.
- A maxterm is a sum (OR) of variables and their complement.
- Each maxterm is FALSE ('0') for that row (and only for that row)
- Function is constructed as the product (AND) of maxterms whose output is FALSE.
- It is then a product (AND) of sums (OR)

A	B	Y	maxterm
0	0	0	$A + B$
0	1	1	$A + \overline{B}$
1	0	0	$\overline{A} + B$
1	1	1	$\overline{A} + \overline{B}$

$$Y = F(A, B) = (A + B)\ (\overline{A} + B)$$

Escuela Politécnica Superior

U1.4. Logic functions

- Example: Cannonical development of a function from its truth table.

#	A	B	C	F(A,B,C)		Minterms		Maxterms
0	0	0	0	1	$\rightarrow$	$(\overline{A}\cdot\overline{B}\cdot\overline{C})$		
1	0	0	1	0			$\rightarrow$	$(A+B+\overline{C})$
2	0	1	0	1	$\rightarrow$	$(\overline{A}\cdot B\cdot\overline{C})$		
3	0	1	1	1	$\rightarrow$	$(\overline{A}\cdot B\cdot C)$		
4	1	0	0	0			$\rightarrow$	$(\overline{A}+B+C)$
5	1	0	1	0			$\rightarrow$	$(\overline{A}+B+\overline{C})$
6	1	1	0	1	$\rightarrow$	$(A\cdot B\cdot\overline{C})$		
7	1	1	1	1	$\rightarrow$	$(A\cdot B\cdot C)$		

Escuela Politécnica Superior

U1.4. Logic functions

- Using Minterms:

$$F = (\overline{A} \cdot \overline{B} \cdot \overline{C}) + (\overline{A} \cdot B \cdot \overline{C}) + (\overline{A} \cdot B \cdot C) + (A \cdot B \cdot \overline{C}) + (A \cdot B \cdot C) =$$

$$= m_0 + m_2 + m_3 + m_6 + m_7 = \sum m(0,2,3,6,7)$$

- Using Maxterms:

$$F = (A + B + \overline{C}) \cdot (\overline{A} + B + C) \cdot (\overline{A} + B + \overline{C}) = M_1 \cdot M_4 \cdot M_5 = \prod M(1,4,5)$$

- Logic function implementation through minterms and maxterms requires a higher amount of resources. It is convenient then (if possible) to obtain simplified expressions.

U1.5. Karnaugh diagrams

- Karnaugh diagrams (k maps)
  - Make easier the planning of logic designs with simpler gate structure → More economic design.
  - Sequence of **cells** where each one represents a binary value of an input. Each cell contains the corresponding value for said combination.
  - Cells are arranged so that the simplification of an expression consists on grouping adecuately the cells.
  - Can be used for expression of 2, 3, 4, 5 (or 6 variables.)
  - For n variables 2^n cells are needed.
  - For a higher number of variables, other methods are used:
  - (e.g. Quine-McClusky method or CAD methods.)

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

• Karnaugh mapping. Adjacent cells

- Cells on a Karnaugh map are disposed so that only one variable changes in between adjacent cells.
  - Adjacent cells: values differ in one variable
  - Non-adjacent cells: values differ in more than one variable
- Physically, each cell is adjacent to every inmediate next cell (4 sides)
- Adjacent cells have a Hamming distance of 1.
- Cells cannot be adjacent diagonally.
- Upper cells are adjacent to its inmmediate lower cells and left cells are adjacent to its inmediate right ➔ Cyclical adjacency

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Karnaugh maps of 3 variables
  - A, B, C: Variables. Matrix of 8 cells
  - Binary values of A and B are located left and C ones on the top (this can be done inversely also)

AB \ C	0	1
00	1	0
01	0	0
11	0	0
10	0	1

AB \ C	0	1
00	$(\overline{A}\cdot\overline{B}\cdot\overline{C})$	$(\overline{A}\cdot\overline{B}\cdot C)$
01	$(\overline{A}\cdot B\cdot\overline{C})$	$(\overline{A}\cdot B\cdot C)$
11	$(A\cdot B\cdot\overline{C})$	$(A\cdot B\cdot C)$
10	$(A\cdot\overline{B}\cdot\overline{C})$	$(A\cdot\overline{B}\cdot C)$

Example: Function has value '1' in the top left corner cell, which corresponds to a value of 000 of variables A, B and C (/A./B./C). On bottom right cell has a variable value of 101 (A./B.C)

U1.5. Karnaugh diagrams

- Karnaugh map of an standard sum of products
  - For every term of the sum of products expression a '1' is added in the Karnaugh map cell correspondent to the product value.

$$\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + AB\overline{C} + A\overline{B}\,\overline{C}$$

000 001 110 100

AB \ C	0	1
00	1	1
01		
11	1	
10	1	

U1.5. Karnaugh diagrams

- Karnaugh map of a non-standard sum of products
  - A non-standard term lacks one or more variables to its expression, which must be completed.

AB \ C	0	1
00	1	1
01	1	1
11	1	
10	1	1

$$\overline{A} + A\overline{B} + AB\overline{C}$$

$\overline{A}$	$A\overline{B}$	$AB\overline{C}$
000	100	110
001	101	
010		
011		

U1.5. Karnaugh diagrams

- Karnaugh maps of 4 variables
  - A, B, C, D: Variables. Matrix of 16 cells
  - Binary values of A and B are located left, C and D ones on the top (this can be done inversely also)

AB \ CD	00	01	11	10
00	0	0	0	1
01	1	0	0	0
11	0	0	0	0
10	0	1	0	0

AB \ CD	00	01	11	10
00	$(\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D})$	$(\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot D)$	$(\overline{A}\cdot\overline{B}\cdot C\cdot D)$	$(\overline{A}\cdot\overline{B}\cdot C\cdot\overline{D})$
01	$(\overline{A}\cdot B\cdot\overline{C}\cdot\overline{D})$	$(\overline{A}\cdot B\cdot\overline{C}\cdot D)$	$(\overline{A}\cdot B\cdot C\cdot D)$	$(\overline{A}\cdot B\cdot C\cdot\overline{D})$
11	$(A\cdot B\cdot\overline{C}\cdot\overline{D})$	$(A\cdot B\cdot\overline{C}\cdot D)$	$(A\cdot B\cdot C\cdot D)$	$(A\cdot B\cdot C\cdot\overline{D})$
10	$(A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D})$	$(A\cdot\overline{B}\cdot\overline{C}\cdot D)$	$(A\cdot\overline{B}\cdot C\cdot D)$	$(A\cdot\overline{B}\cdot C\cdot\overline{D})$

Example: Function has a value of '1': on the top right cell where variables A, B, C and D are 0010 (/A./B.C./D), on the second row cell where they are 0100 (/A.B./C./D) and on the bottom row corresponding with a value of 1001 (/A./B./C.D).

U1.5. Karnaugh diagrams

- Karnaugh maps of 5 variables
  - A, B, C, D, E: Variables. Matrix of 32 cells
  - Take 2 maps of 4 variables where they correspond to a value of variable E equal to 0 and 1, respectively.
  - Binary values of B and C are located left, D and E ones on top.

BC \ DE	00	01	11	01	00	01	11	10
00								
01								
11								
10								
	A=0				A=1			

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Sum of products simplification
  - Minimization: Process that generates an expression cointaining the lowest possible number of terms with the minimum possible number variables.
  - After obtaining Karnaugh diagram , 3 steps should be followed to obtain the minimal expression of products:
    - One's grouping
    - Determination of each term for the SOP (one per Group).
    - Obtain the final equation (adding the terms).

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Sum of products simplification
  - One’s grouping
    - A group has to contain 1, 2, 4, 8 or 16 cells (power of 2). Diagram of 3 variables: máximum group of 8 cells.
    - Each cell of a group has to be adjacent to one or more cells of the same group, but not all cells of the group must be adjaccent to each other.
    - Maximize number of 1s in each group
    - Each ‘1’ of the diagram has to be included in, at least, 1 group. ‘1’s already in a group can be included into other groups given that the overlaping groups contains non common ‘1’s.

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Sum of products simplification
  - One's grouping

AB \ C	0	1
00	1	
01		1
11	1	1
10		

AB \ C	0	1
00	1	1
01	1	
11		1
10	1	1

AB \ CD	00	01	11	10
00	1	1		
01	1	1	1	1
11				
10		1	1	

AB \ CD	00	01	11	10
00	1			1
01	1	1		1
11	1	1		1
10	1		1	1

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Sum of products simplification
  - Determination of each term of the SOP.
    - Each group of cells containing ‘1’s gives one product term composed of all variables appering in the group in only one form (complemented or non complemented).
    - Variables complemented and non complemented inside the same group are deleted.
  - Sum of product terms obtained.
    - Once obtained all minimum terms from the Karnaugh diagram, they are added up to obtainthe minimal product expression.

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Sum of products simplification
  - Sum of products expression determination from the diagram. Sum of product terms obtained.

AB \ C	0	1
00	1	
01		1
11	1	1
10		

$$\overline{A}\,\overline{B}\,\overline{C} + AB + BC$$

AB \ C	0	1
00	1	1
01	1	
11		1
10	1	1

$$\overline{A}\,\overline{C} + AC + \overline{B}$$

AB \ CD	00	01	11	10
00	1	1		
01	1	1	1	1
11				
10		1	1	

$$A\overline{B}D + \overline{A}B + \overline{A}\,\overline{C}$$

AB \ CD	00	01	11	10
00	1			1
01	1	1		1
11	1	1		1
10	1		1	1

$$A\overline{B}C + B\overline{C} + \overline{D}$$

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Product of sums simplification
  - Product of sums expression determination from the diagram. Product of sum terms obtained.

AB \ C	0	1
00	0	
01		0
11	0	0
10		

$$(A+B+C)\cdot(\overline{A}+\overline{B})\cdot(\overline{B}+\overline{C})$$

AB \ C	0	1
00	0	0
01	0	
11		0
10	0	0

$$(A+C)\cdot(\overline{A}+\overline{C})\cdot B$$

AB \ CD	00	01	11	10
00	0	0		
01	0	0	0	0
11				
10		0	0	

$$(\overline{A}+B+\overline{D})\cdot(A+\overline{B})\cdot(A+C)$$

AB \ CD	00	01	11	10
00	0			0
01	0	0		0
11	0	0		0
10	0		0	0

$$(\overline{A}+B+\overline{C})\cdot(\overline{B}+C)\cdot D$$

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Karnaugh maps of 5 variables.

  Simplify $F(A,B,C,D,E)= \sum(2,3,5,6,7,8,9,10,12,13,14,16,18,20,21,22,23,25,26,30)$

  - Two maps of 4 variables, 5th variable allows selection between maps
  - Adjacency: Imagine that map A=0 is on top of map A=1; each cell of map A=0 is adjacent with the cell inmediately below of map A=1.

BC \ DE	00	01	11	10	00	01	11	10
00			1	1	1			1
01		1	1	1	1	1	1	1
11	1	1		1				1
10	1	1		1		1		1
		A=0				A=1		

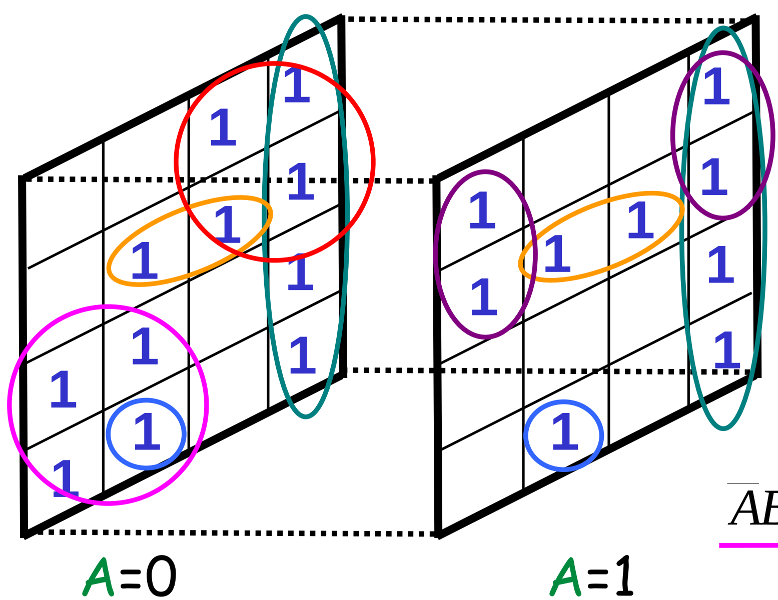
$$\bar{A}B\bar{D} + \bar{A}\bar{B}D + A\bar{B}\bar{E} + D\bar{E} + \bar{B}CE + B\bar{C}\bar{D}E$$

U1.5. Karnaugh diagrams

- Karnaugh maps of 5 variables.

  Simplify F(A,B,C,D,E)= Σ(2,3,5,6,7,8,9,10,12,13,14,16,18,20,21,22,23,25,26,30)

  - Two maps of 4 variables, one for the fifth variable equal to 0 and for it equal to 1.
  - Adjacency: Imagine that map A=0 is on top of map A=1; each cell of map A=0 is adjacent with the cell inmediately below of map A=1.



$$\bar{A}B\bar{D} + \bar{A}\bar{B}D + A\bar{B}\bar{E} + D\bar{E} + \bar{B}CE + B\bar{C}\bar{D}E$$

U1.5. Karnaugh diagrams

- Karnaugh diagrams: Product of sums simplification
  - The minimization process of a product of sums is basically the same as that for a sum of products although now the ‘0’s are to be grouped to créate the mínimum mumber of sum terms.
  - Rules applied to group ‘0’s are the same as those to group ‘1’s.

Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Obtaining a Karnaugh diagram from its truth table
  - Example:

Nº	A	B	C	D	F	Minterms	Maxterms
0	0	0	0	0	1	$\rightarrow (\bar{A}\cdot\bar{B}\cdot\bar{C}\cdot\bar{D})$	
1	0	0	0	1	1	$\rightarrow (\bar{A}\cdot\bar{B}\cdot\bar{C}\cdot D)$	
2	0	0	1	0	0		$\rightarrow (A+B+\bar{C}+D)$
3	0	0	1	1	1	$\rightarrow (\bar{A}\cdot\bar{B}\cdot C\cdot D)$	
4	0	1	0	0	0		$\rightarrow (A+\bar{B}+C+D)$
5	0	1	0	1	1	$\rightarrow (\bar{A}\cdot B\cdot\bar{C}\cdot D)$	
6	0	1	1	0	1	$\rightarrow (\bar{A}\cdot B\cdot C\cdot\bar{D})$	
7	0	1	1	1	0		$\rightarrow (A+\bar{B}+\bar{C}+\bar{D})$
8	1	0	0	0	0		$\rightarrow (\bar{A}+B+C+D)$
9	1	0	0	1	1	$\rightarrow (A\cdot\bar{B}\cdot\bar{C}\cdot D)$	
10	1	0	1	0	0		$\rightarrow (\bar{A}+B+\bar{C}+D)$
11	1	0	1	1	1	$\rightarrow (A\cdot\bar{B}\cdot C\cdot D)$	
12	1	1	0	0	1	$\rightarrow (A\cdot B\cdot\bar{C}\cdot\bar{D})$	
13	1	1	0	1	1	$\rightarrow (A\cdot B\cdot\bar{C}\cdot D)$	
14	1	1	1	0	0		$\rightarrow (\bar{A}+\bar{B}+\bar{C}+D)$
15	1	1	1	1	1	$\rightarrow (A\cdot B\cdot C\cdot D)$	

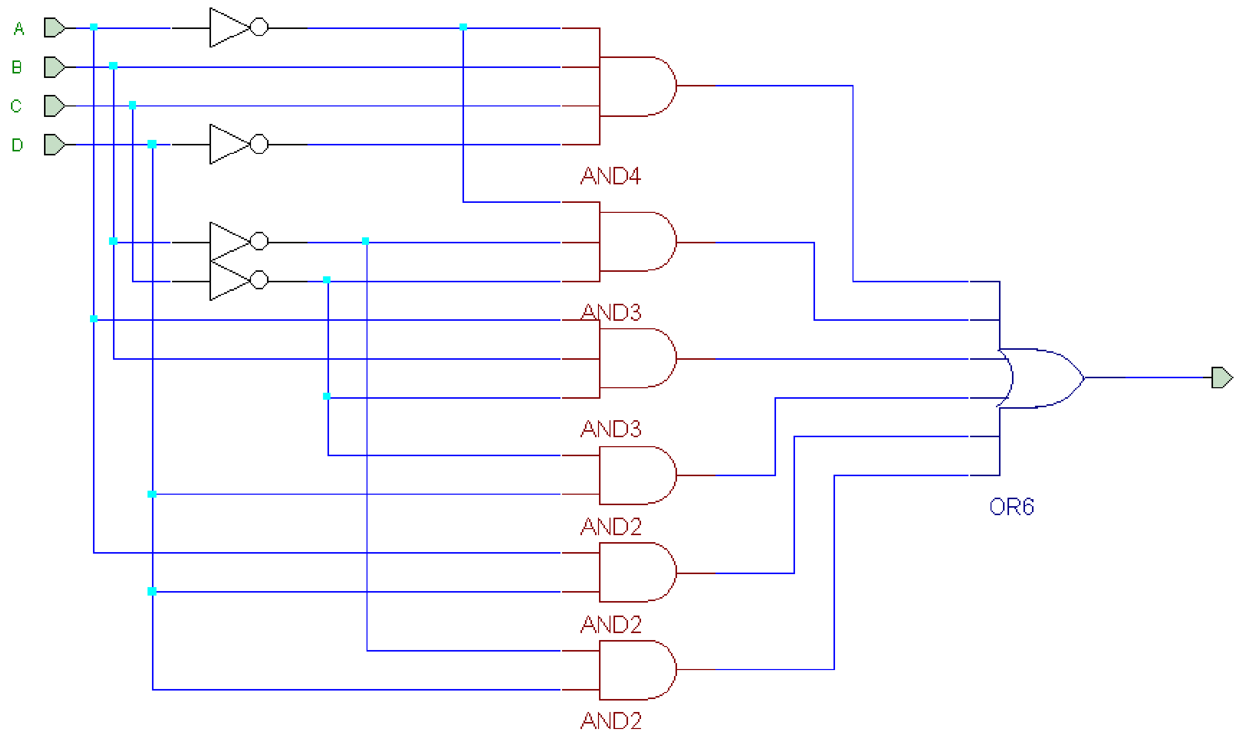
Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Obtaining a Karnaugh diagram from its truth table
  - Example: Development by minterms

AB \ CD	00	01	11	10
00	1	1	1	
01		1		1
11	1	1	1	
10		1	1	

$$F = \bar{A}BC\bar{D} + \bar{A}\bar{B}\bar{C} + AB\bar{C} + \bar{C}D + AD + \bar{B}D$$



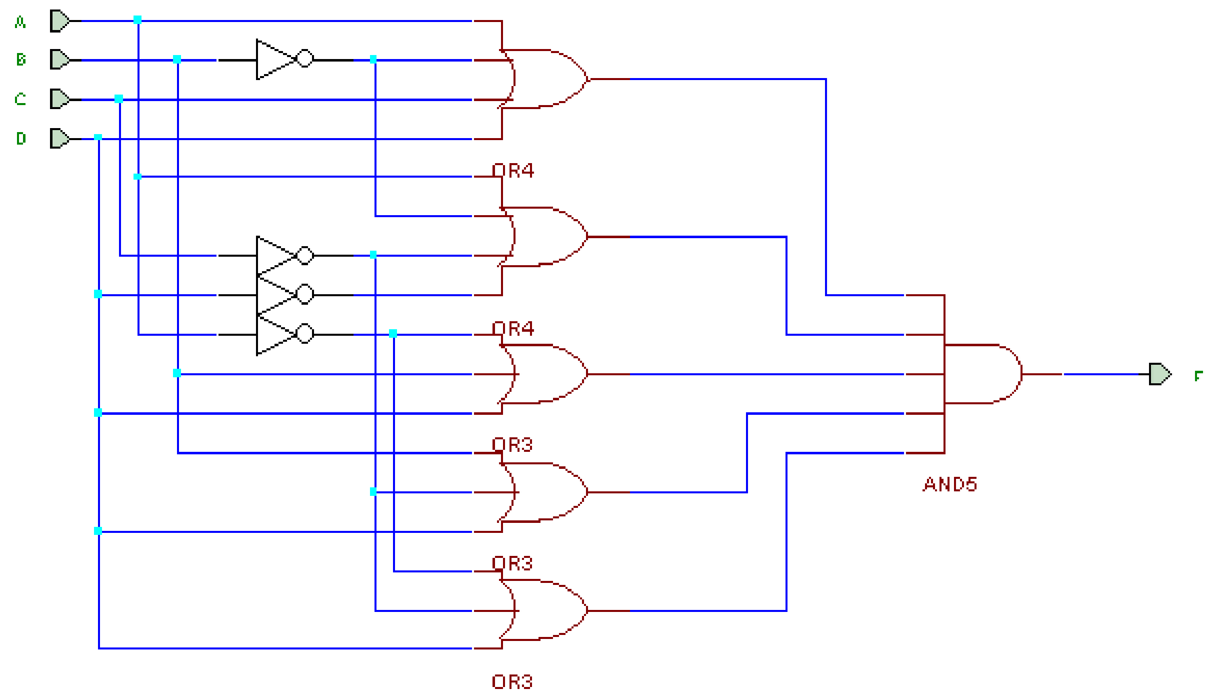
Escuela Politécnica Superior

U1.5. Karnaugh diagrams

- Obtaining a Karnaugh diagram from its truth table
  - Example: Development by maxterms

$$F=\underline{(A+\overline{B}+C+D)}\cdot\underline{(A+\overline{B}+\overline{C}+\overline{D})}\cdot\underline{(\overline{A}+B+D)}\cdot\underline{(B+\overline{C}+D)}\cdot\underline{(\overline{A}+\overline{C}+D)}$$

AB \ CD	00	01	11	10
00				0
01	0		0	
11				0
10	0			0



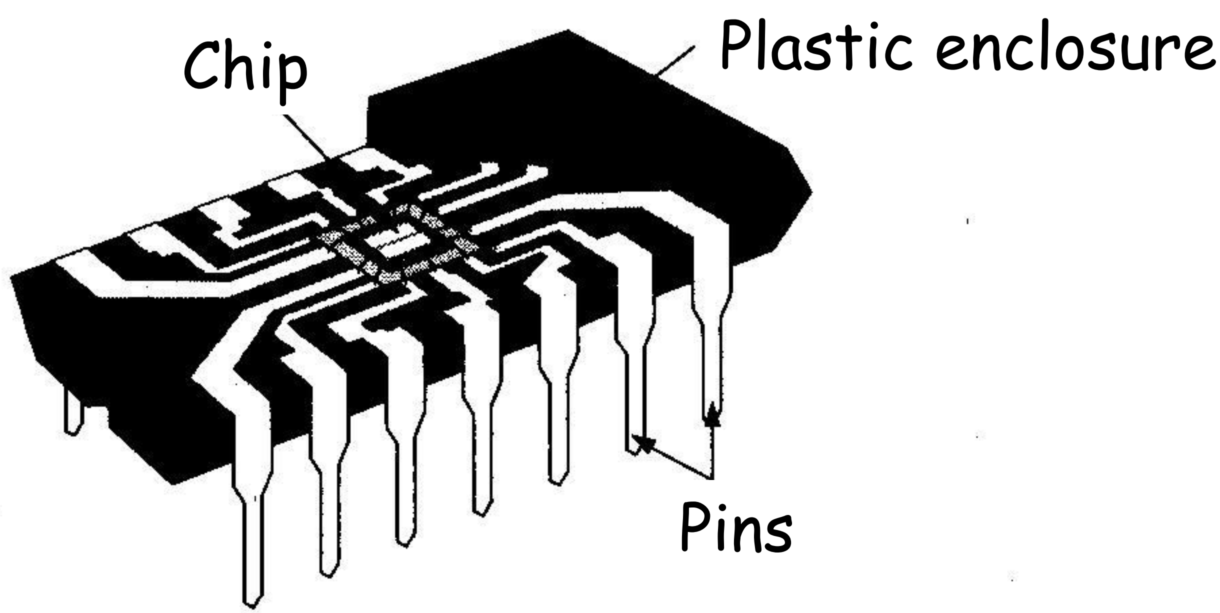
Escuela Politécnica Superior

Annex. Integrated digital circuits

- Element and logical functions seen are available as integrated circuits (ICs).
- A monolitic IC is an electronic circuit all built onto a small silicon chip.
- All circuit components (transistors, diodes, resistors and capacitors) are inside of the chip.

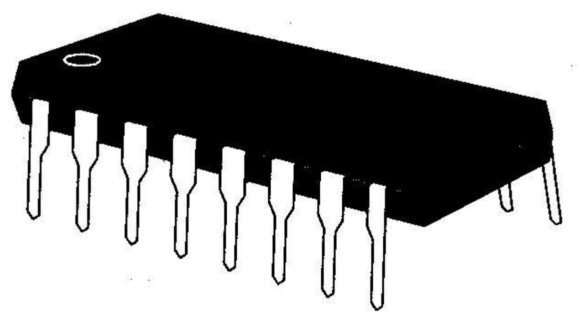
Escuela Politécnica Superior

Annex. Integrated digital circuits



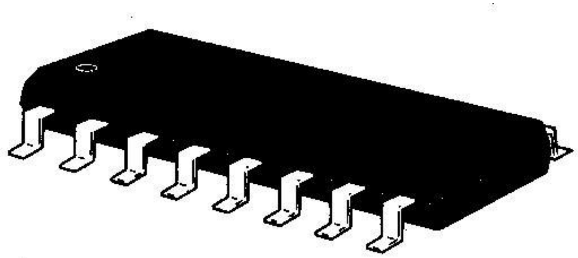
Annex. Integrated digital circuits

- IC encapsulation
  - They are classified as the way in which they have been mounted on the PCB (Printed Circuit –Through hole or SMD)
  - Insertion capsules / Through-hole components:
    - The IC pins are inserted in the holes of the PCB and the solder tracks are soldered from the other face of the PCB.
    - Most typical: DIP (Dual In-line Package)



Annex. Integrated digital circuits

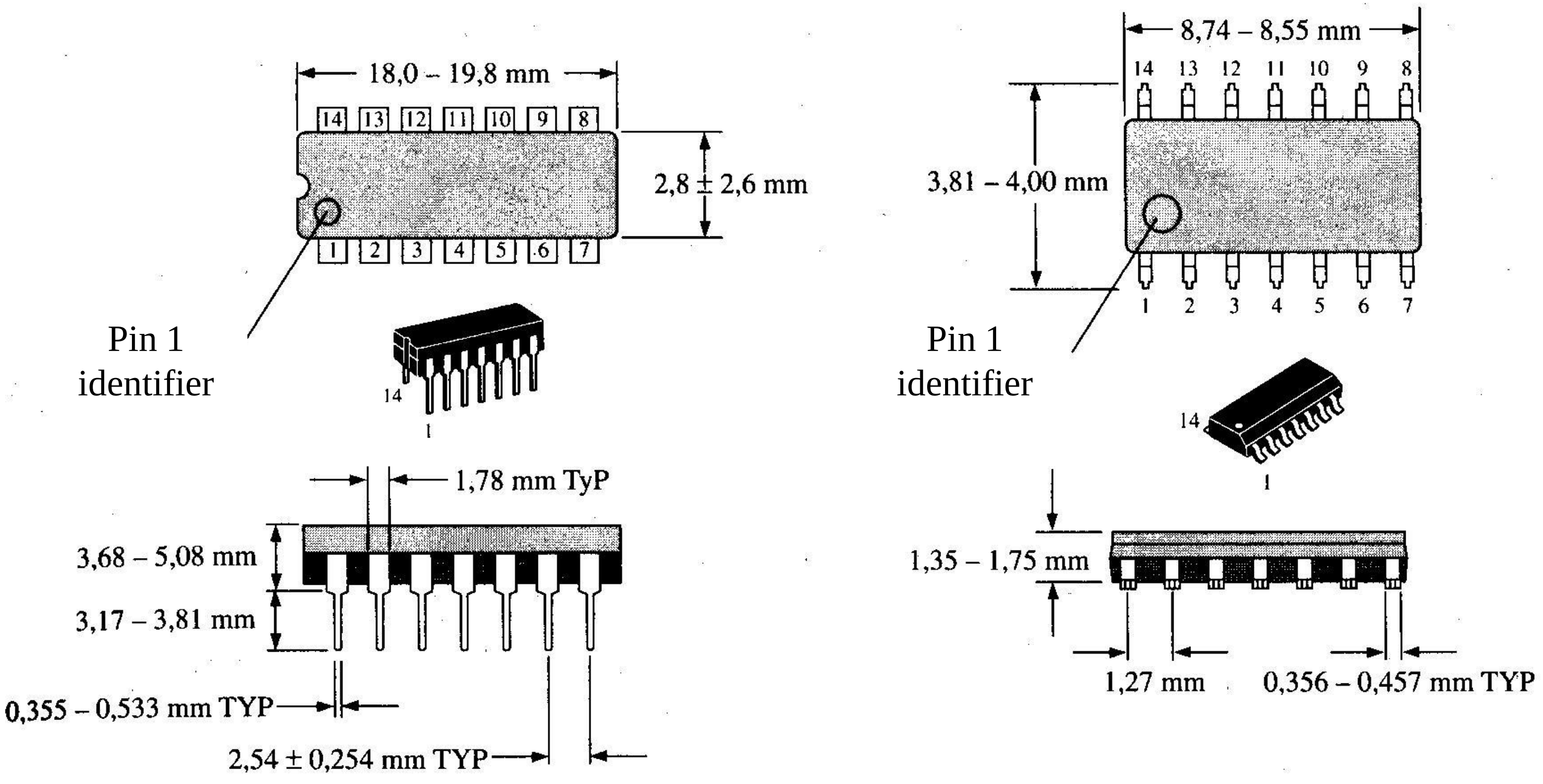
- IC encapsulation
  - SMC : Surface Mount Component
    - Most modern method, less space
    - No need of holes on the PCBs, pins are directly soldered to the pads available on one side of the PCB, leaving the other side for additional circuitry.
    - Smaller than DIP, pins are closer to each other.
    - Most typical: SOIC (Small-Outline IC)



Escuela Politécnica Superior

Annex. Integrated digital circuits

- IC encapsulation
  - Typical DIP and SOIC encapsulation: typical dimensions and pin breakout.



Annex. Integrated digital circuits

- Pinout configuration diagrams for most common logic gates