500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC

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***Abstract*—A 500-MS/s 5-bit ADC for UWB applications has been fabricated in a 65-nm CMOS technology using no analog-specific processing options. The time-interleaved successive approximation register (SAR) architecture has been chosen due to its simplicity versus flash and its amenability to scaled technologies versus pipelined, which relies on operational amplifiers. Six time-interleaved channels are used, sharing a single clock operating at the composite sampling rate. Each channel has a split capacitor array that reduces switching energy, increases speed, and has similar INL and decreased DNL, as compared to a conventional binary-weighted array. A variable delay line adjusts the instant of latch strobing to reduce preamplifier currents. The ADC achieves Nyquist performance, with an SNDR of 27.8 and 26.1 dB for 3.3 and 239 MHz inputs, respectively. The total active area is 0.9 mm^2, and the ADC consumes 6 mW from a 1.2-V supply.**

***Index Terms*—ADC, analog-to-digital conversion, deep-submicron CMOS, successive approximation register, ultra-wideband radio.**

I. Introduction

ULTRA-WIDEBAND (UWB) radio is an emerging technology for very-high-data-rate, short distance wireless communications. Both OFDM [1] and pulse-based [2] solutions are being developed to achieve data rates in excess of 480 Mb/s. UWB receivers require high-speed but low-resolution analog-to-digital converters (ADCs), in the range of 4–5 bits [3]–[5]. The ADC in this work is targeted for specifications (5 bit, 500 MS/s) compatible with a custom pulse-based UWB transceiver [6], [7], where 100 Mb/s communication is achieved using BPSK-modulated 500-MHz-wide Gaussian pulses transmitted in one of 14 bands between 3.1–10.6 GHz.

The flash topology, along with its interpolating and folding variants, has been the conventional choice for high-speed, low-resolution ADCs [8]–[12]. While flash can maintain the highest throughput, it requires an exponential growth in the number of comparisons with the resolution. The ensuing complexity motivates the use of other architectures.

Pipelined ADCs are used for high-speed, medium-resolution applications [13], [14]. They can provide one conversion per clock period throughput and only a linear scaling in complexity with resolution; however, they rely on operational amplifiers at the heart of the multiplying digital-to-analog converter (MDAC) in each pipelined stage. Because it must be closed loop stable, this amplifier typically uses one or two high gain stages. Unfortunately, in deep-submicron CMOS, the achievable gain per stage is limited because short-channel effects lower $g_m r_o$ for a single transistor, and reduced voltage supplies restrict circuit techniques such as cascoding. Thus, there are significant challenges for continued scaling of pipelined ADCs.

Very recently, for the high-speed, low resolution converters necessary for UWB, the time-interleaved successive approximation register (SAR) architecture has re-emerged[1] as a low-power alternative to flash and pipelined ADCs [17]. At the required speeds, their major limitation is digital power; a SAR converter includes digital feedback in the critical path. A full custom logic controller with dynamic registers can reduce digital power significantly, but it still remains a dominant source of power consumption in a 0.18-μm CMOS implementation [18]. Another approach uses dynamic registers with asynchronous operation to reduce clock power, and combined with a non-binary successive approximation algorithm, has led to a very energy efficient design in 0.13-μm CMOS [19]. Fortunately, technology scaling improves the digital power and speed without many of the issues plaguing pipelined converters. The only active analog component in a SAR ADC, the comparator, still requires large gain and bandwidth, but because it does not have to be linear, this gain can be achieved through cascaded stages and positive feedback.

This paper presents a 500-MS/s 5-bit ADC fabricated in a 65-nm CMOS technology [20]. At the maximum sampling rate, the ADC consumes 6 mW from a 1.2-V supply. This low power consumption is achieved through proper architecture selection, a new capacitor array, and careful timing allocation between the digital and analog circuits. The ADC has six time-interleaved SAR channels synchronized to a common clock. The split capacitor array reduces switching energy, is robust to digital delay mismatches for overall improved settling time, and has a reduction in peak static differential nonlinearity (DNL). In the comparator, a variable delay line adjusts the instant of strobing for the regenerative latches, minimizing idle time during each bit-cycle without sacrificing bit error rate (BER) performance.

II. ADC Architecture

A SAR ADC requires one period for sampling and b periods to resolve the b digital output bits. To make the internal SAR clock synchronous to the overall sampling clock, six time-interleaved channels are used, as shown in Fig. 1. Thus, only a single 500 MHz clock is required in the prototype, easing clock generation and distribution. The channels synchronize by passing

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[1]Time-interleaved SAR was used as early as 1980 as a low area alternative to the flash ADC [15], and, more recently, for reduced comparator power in a medium resolution application [16].

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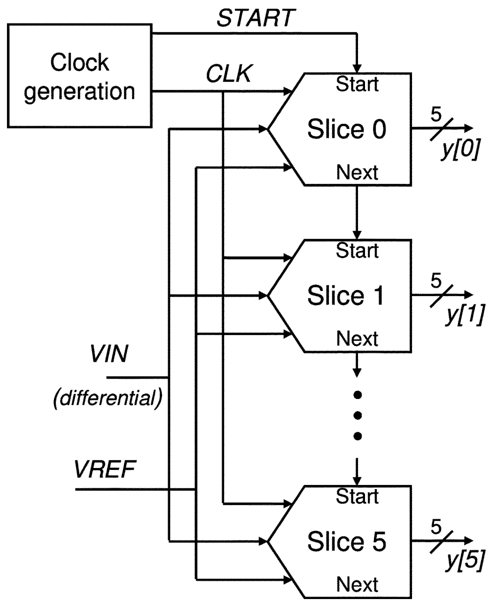

Fig. 1. Top-level block diagram of the 6-way time-interleaved ADC.

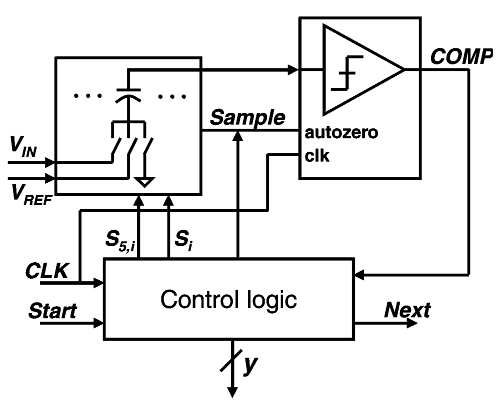

Fig. 2. Block diagram of the channel, which has a capacitive DAC, comparator, and digital logic.

a token to cue their start of sampling, and all critical sampling edges are aligned to the same shared clock [18]. Timing skew between channels is thus limited to routing variations to the channels and the delay mismatch through a single register in each channel; both of these error sources can be kept sufficiently small such that digital timing correction (a complex, power hungry process [21]) is not necessary.

The channel, shown in Fig. 2, consists of a capacitive digital-to-analog converter (DAC), a comparator, and control logic (itself called the SAR). The control logic switches the DAC using a binary search algorithm to minimize the error between the digital output and the analog input. The split capacitor array and comparator, the two analog blocks, are discussed in Section III, followed by some of the considerations used in designing circuits for 65-nm CMOS.

III. Circuit Design

A. Split Capacitor Array

The DAC serves two purposes in a SAR converter: it samples the input charge, and it generates an error voltage between the input and current digital estimate. The conventional DAC choice is a binary-weighted capacitor array [22], as shown in Fig. 3, which is insensitive to stray capacitance. As shown in [23], however, the conventional capacitor array uses charge inefficiently during a conversion. To demonstrate this, a conversion of a 2-bit capacitor array is presented here. During the first bit decision after sampling, the MSB capacitor is connected to $V_{\rm REF}$ with the remaining capacitors connected to ground (left circuit in Fig. 4). The output of the capacitor array, V_X, is

$$V_X = -V_{\rm IN} + \frac{1}{2}V_{\rm REF} \tag{1}$$

where $V_{\rm IN}$ is the input voltage sampled on the capacitor array and $V_{\rm REF}$ is the reference voltage. During the second bit-cycle, the SAR does one of two transitions. If $V_X < 0$, an "up" transition is performed, where C_1 is switched from ground up to $V_{\rm REF}$, drawing

$$E_{\rm up} = \frac{C_0 V_{\rm REF}^2}{4} \tag{2}$$

from the reference voltage supply. Inversely, if $V_X > 0$, a "down" transition is performed (Fig. 4); C_1 and C_2 switch places. If they switch at the same time, the energy required is

$$E_{\rm down,conv} = \frac{5}{4}C_0 V_{\rm REF}^2. \tag{3}$$

It takes 5 times more energy to lower V_X than to raise it; this occurs because all of the charge initially on C_2 is discharged to ground, and all the charge that ends up on C_1 must be delivered from the reference voltage supply.

Ref. [23] analyzes three alternatives to the conventional capacitor array and switching procedure. Of these alternatives, this work implements the split capacitor array because it has both the lowest switching energy and does not require an extra clock phase that would limit high speed operation. A b-bit split capacitor array is shown in Fig. 5; the MSB capacitor of the conventional array has been split into an identical copy (MSB subarray) of the rest of the array (main subarray). These arrays are placed in parallel (common top plate), not to be confused with the series connected capacitor arrays used in the sub-DAC approach.[2] The total capacitance of the split capacitor array is $2^b C_0$, identical to the conventional case, and the area requirements are unchanged.

The split capacitor switching algorithm is presented in Fig. 6. Here, the two-bit example from above is repeated for the split capacitor array to demonstrate the switching method and energy savings. During the first bit-cycle (left side of Fig. 7), the MSB subarray, $C_{2,1}$ and $C_{2,0}$, is connected to $V_{\rm REF}$, and the main subarray is connected to ground. Since $C_2 = C_{2,1} + C_{2,0}$, (1) also represents the output of the split array. In the case of an "up" transition, the array transitions in the same method as above, with C_1 switching to $V_{\rm REF}$, consuming the same energy calculated in (2). In the "down" transition (Fig. 7), half of the MSB subarray, $C_{2,1}$ is lowered to ground, leaving both C_1 and $C_{2,0}$ unchanged. By only switching one capacitor the energy

[2]Historically, the combination of capacitive main- and sub-DACs had been called a "split array" [15], but this has not become common usage, and we have co-opted the term for the new structure.

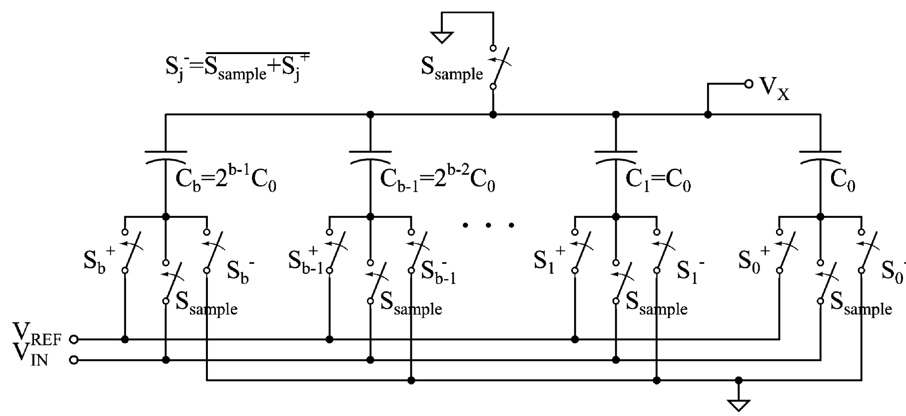

Fig. 3. Conventional b-bit binary weighted capacitor array.

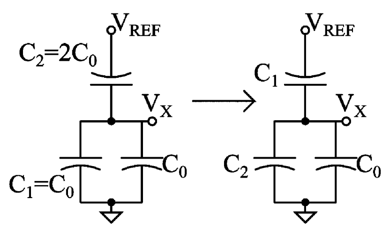

Fig. 4. "Down" transition of the conventional capacitor array.

consumed is

$$E_{\text{down,split}} = \frac{C_0 V_{\text{REF}}^2}{4} \tag{4}$$

identical to the "up" transition.

The overall energy savings of the split capacitor array is input voltage (or output digital code) dependent. Where the relative frequency of "down" transitions is greater, the savings for the split capacitor array is enhanced, as seen in Fig. 8. Assuming a full swing sinusoidal input distribution, the split capacitor array is expected to have 37% lower switching energy than the conventional array.

For this high-speed implementation, an additional advantage of considerable significance is related to the array's settling time. During a "down" transition, two capacitors are required to switch for the conventional capacitor array; any mismatch, whether random or deterministic, in the digital logic driving these switches can cause the capacitor array to initially transition in the wrong direction, potentially exacerbating an overdrive condition for the preamplifiers. Only one capacitor in the split capacitor array transitions during any bit-cycle, providing inherent immunity to the skew of the switch signals. Simulation results comparing the settling times of the two arrays is shown in Fig. 9. For the simulation, the total width of the switches is identical for the split and conventional arrays. The split capacitor array settles up to 10% faster, which is used to reduce the bias currents in the preamplifiers by a similar amount.

1) Linearity Performance: To compare the theoretical static linearity of the binary-weighted and split DACs, each of the capacitors is modeled as the sum of the nominal capacitance value and some error term:

$$\begin{aligned} C_n &= 2^{n-1}C_0 + \delta_n \\ C_{b,n} &= 2^{n-1}C_0 + \delta_{b,n}. \end{aligned} \tag{5}$$

Initially, consider only the case where all the errors are in the unit capacitors, whose values are independent identically-distributed (i.i.d.) Gaussian random variables; later in this section, other non-idealities will be considered. Then the error terms δ_n and $\delta_{b,n}$ have zero mean, are independent, and have variance

$$E\left[\delta_n^2\right] = E\left[\delta_{b,n}^2\right] = 2^{n-1}\sigma_0^2 \tag{6}$$

where σ_0 is the standard deviation of the unit capacitor.

The linearity of a SAR ADC is limited by the accuracy of the DAC outputs, which are calculated here for the case of no initial charge on the array ($V_{\text{IN}} = 0$). For a given DAC digital input $y = \sum_{n=1}^{b} S_n 2^{n-1}$, with S_n equals 0 or 1 represents the ADC decision for bit n, the analog output for the conventional binary-weighted array is

$$V_{X,conv}(y) = \frac{\sum_{n=1}^{b} \left(2^{n-1}C_0 + \delta_n\right) S_n}{2^b C_0 + \Delta C} V_{\text{REF}}. \tag{7}$$

The second term in the denominator $\Delta C = \sum_{n=0}^{b} \delta_n$ will be neglected for this discussion. This will make the analysis simpler but will prevent a complete closed form solution for the integral nonlinearity (INL). Subtracting the nominal value yields the error term

$$V_{\text{err}}(y) \approx \frac{\sum_{n=1}^{b} \delta_n S_n}{2^b C_0} V_{\text{REF}} \tag{8}$$

with variance

$$\begin{aligned} E\left[V_{\text{err}}^2(y)\right] &= \frac{\sum_{n=1}^{b} 2^{n-1}\sigma_0^2 S_n}{2^{2b} C_0^2} V_{\text{REF}}^2 \\ &= \frac{y}{2^{2b}} \frac{\sigma_0^2}{C_0^2} V_{\text{REF}}^2. \end{aligned} \tag{9}$$

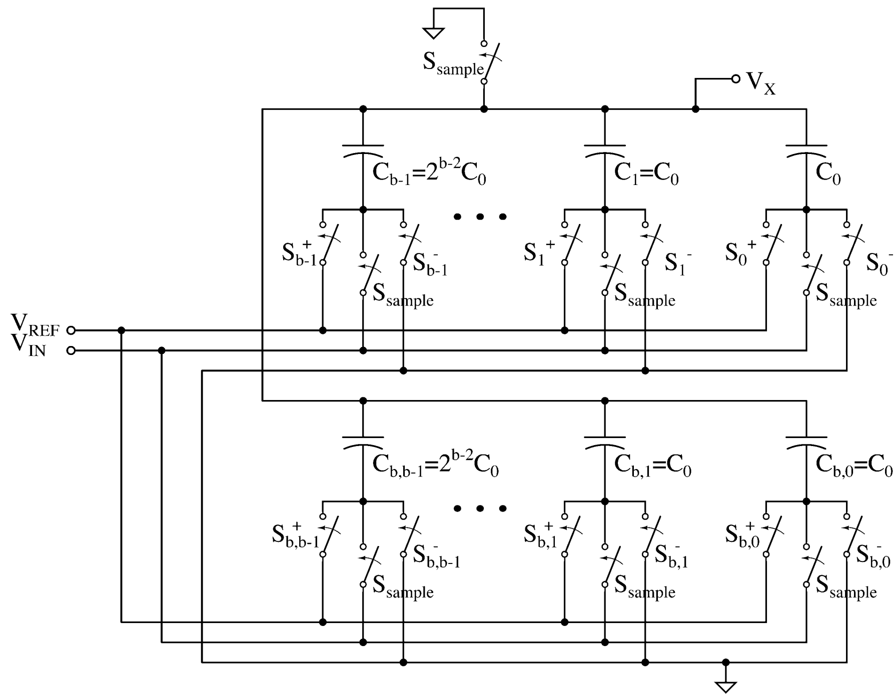

Fig. 5. The b-bit split capacitor array, with the main subarray on top and the MSB subarray below.

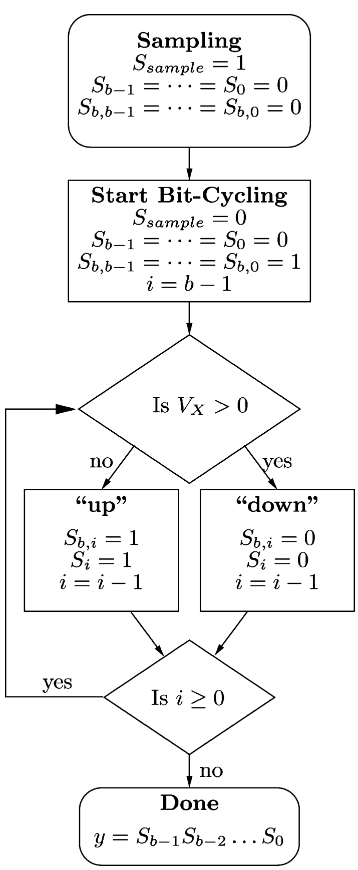

Fig. 6. Switching procedure for split capacitor array. i represents the bit currently being decided.

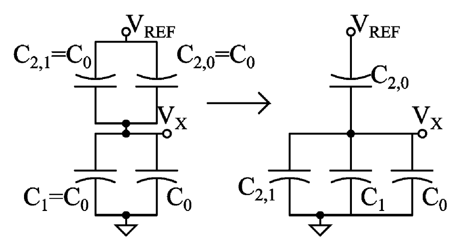

Fig. 7. "Down" transition of the split capacitor array. The "up" transition entails switching C_1 to $V_{\rm REF}$.

This voltage error is simply the sum of the errors from y unit capacitors connected to $V_{\rm REF}$. Because the errors in the unit capacitors are assumed to be i.i.d., it does not matter which unit capacitors are connected to $V_{\rm REF}$ but only the total number. Thus, (9) holds for the case of the split capacitor array as well. This error is also directly related to the INL of the ADC, and thus there should be no difference between the maximum INLs of the two arrays.

The DNL of the capacitive DAC is, neglecting gain errors, the difference between the voltage errors at two consecutive DAC outputs, as in

$$\mathrm{DNL}(y) \approx \Delta V_{\rm err}(y) = V_{\rm err}(y) - V_{\rm err}(y-1). \tag{10}$$

The worst case DNL for the binary weighted capacitor array is expected to occur at the step below the MSB transition, where its variance is

$$E\left[\Delta V_{\rm err}^2\left(2^{b-1}\right)\right] = E\left[\left(\frac{\delta_b - \sum_{n=1}^{b-1}\delta_n}{2^b C_0} V_{\rm REF}\right)^2\right] \approx \frac{\sigma_0^2}{2^b C_0^2} V_{\rm REF}^2. \tag{11}$$

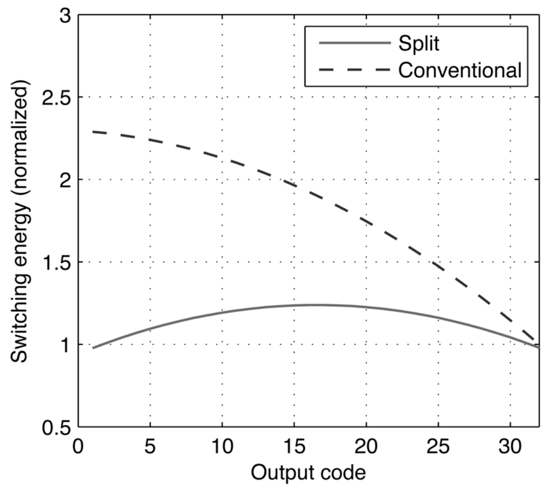

Fig. 8. Normalized switching energies of the conventional and split capacitor arrays versus output code. The number of "down" transitions is greater on the left side of the plot.

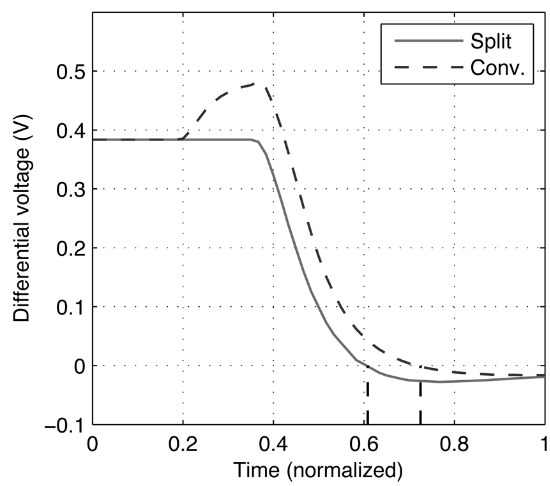

Fig. 9. Simulation of the settling time of the split and conventional capacitor arrays under the presence of digital timing skew.

For the split capacitor array, the worst case DNL also occurs at the step below the MSB transition, but its value is

$$\begin{aligned}\Delta V_{\mathrm{err}}\left(2^{b-1}\right) &= \frac{\sum_{n=0}^{b-1}\delta_{b,n}-\left(\sum_{n=0}^{b-2}\delta_{b,n}+\sum_{n=1}^{b-2}\delta_n\right)}{2^bC_0}V_{\mathrm{REF}} \\ &= \frac{\delta_{b,b-1}-\sum_{n=1}^{b-2}\delta_n}{2^bC_0}V_{\mathrm{REF}}. \qquad (12)\end{aligned}$$

This error has a variance of

$$E\left[\Delta V_{\mathrm{err}}^2\left(2^{b-1}\right)\right]\approx\frac{1}{2}\frac{\sigma_0^2}{2^bC_0^2}V_{\mathrm{REF}}^2. \qquad (13)$$

Comparing (11) and (13) shows that the standard deviation of the worst case DNL is $\sqrt{2}$ lower for the split capacitor array. Conceptually, this occurs because the errors at $y=2^{b-1}$ and $y=2^{b-1}-1$ are partially correlated for the split capacitor array,

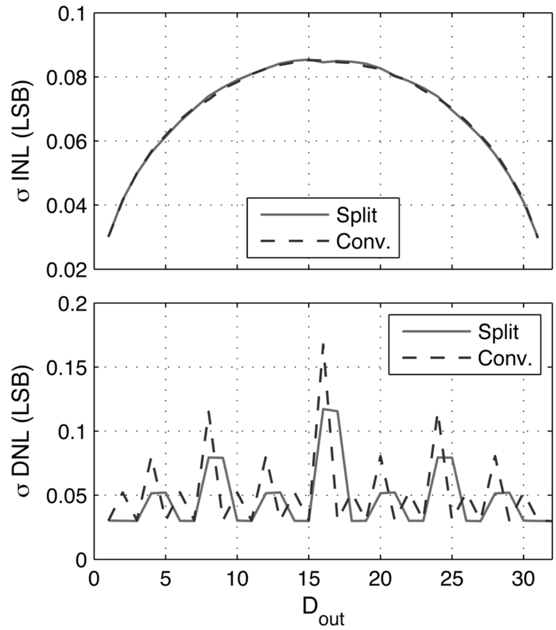

Fig. 10. Behavioral simulation comparing the linearity of the split and conventional capacitor arrays. 10 000 Monte Carlo runs were performed, with i.i.d. Gaussian errors in the unit capacitors ($\sigma_0/C_0=3\%$). The standard deviation of the INL and DNL are plotted.

causing the cancellation of $\delta_{b,0},\ldots,\delta_{b,b-2}$ in (12). This can be also be seen in the energy example above. In Fig. 4, the errors of the top capacitors are completely uncorrelated for the two bit decisions; however, in Fig. 7, the error of $C_{2,0}$ contributes equally to both bit decisions.

A behavioral simulation of the SAR ADC, with both the binary weighted and split capacitor arrays, was performed. The values of the unit capacitors are taken to be Gaussian random variables with standard deviation of 3% ($\sigma_0/C_0=0.03$), and the ADC is otherwise ideal. Fig. 10 shows the results of 10 000 Monte Carlo runs, where the standard deviation of the INL and DNL are plotted versus output code at the 5-bit level. As expected, the conventional and split arrays have identical INL characteristics, and the split capacitor array has $\sqrt{2}$ better DNL. This improvement in DNL is similar to that conferred at the MSB transition from using 1-bit of unary decoding in a segmented DAC [24].

The above discussion assumes that the errors in the unit capacitors are due to an i.i.d. random process. In practice, care must be taken during layout to ensure absence of systematic nonidealities. The unit capacitors are arranged in a common centroid configuration to eliminate the effect of first order gradients. Fringing effects at the edge of the array are reduced by using 32 dummy capacitors around the 32 active unit capacitors. The largest capacitors in the main subarray and MSB subarray are distributed so as to have equal numbers of edges next to the dummy capacitors to further reduce fringing errors. The split capacitor array does have twice as many bottom plate signals that must be routed within the array. Coupling from these routes to the top plate routing can cause linearity errors and was avoided by routing the top and bottom plate signals distant from each other, which was sufficient at 5-bit resolution. For higher resolutions, electrostatic shielding may be necessary where the bottom

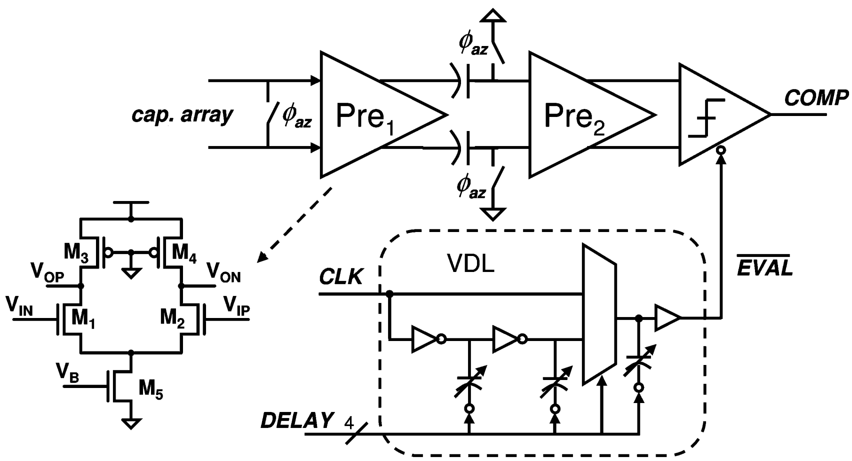

Fig. 11. Comparator schematic showing preamplifier chain, latch, and VDL inserted in series with the latch strobe signal.

plate routing is separated from the capacitors by grounded metal [25]. Shielding can also improve immunity to noise coupling from the substrate.

B. Comparator With Adjustable Strobing

The comparator, shown in Fig. 11, has a regenerative latch preceded by two stages of autozeroed preamplifiers, used to reduce the input referred offset of the latch to below one quarter of the LSB voltage. The preamplifiers are linear amplifiers with an input NFET differential pair M_1-M_2 and resistive loads, formed by PFETs M_3-M_4 operating in the linear region. The gain per stage is selected to be 3–4 for ease of integration at both low voltages and with very short channel devices. The offset of the first preamplifier is cancelled using output offset storage. The sizing of the preamplifiers, autozeroing capacitors, and latch follows the offset/matching-limited optimization procedure described in [26].

During bit-cycling, the clock period is divided into one phase for the settling of the DAC and preamplifiers and one phase for regeneration of the latch. The latch typically resolves, even for small inputs, in much less than the 1ns that is allocated assuming an even division of the period. The ADC sits idle after the latch settles until the start of the next bit-cycle. Self-timed bit-cycling uses this idle time to start the next bit-cycle early [18], [27]. This approach relaxes the preamplifier settling time requirement for all but the first bit-cycle (determining the MSB), as it has no prior bit-cycle from which to borrow. Instead, here a variable delay line (VDL) has been inserted in series with the latch strobe signal to extend analog settling time in the first half of every bit-cycle, including the first, "pre-borrowing" time from that bit-cycle's own latch phase. The beginning of every bit period is synchronous with the sampling clock, and the latch strobing is determined by the setting of the VDL, which is tuned externally to see tradeoffs between extended settling time and ADC performance.

C. Technology Considerations

The SAR architecture's digital complexity directly benefits from the reduced feature sizes. Even though this ADC uses a fully static CMOS logic style, it still consumes less power than the highly customized logic, including dynamic registers, used in [18]. Care was taken throughout the digital logic to provide the maximum robustness in presence of delay variations.

The two analog blocks are well suited for integration in 65-nm CMOS with the following design considerations. For the same absolute device size, transistor matching improves in successive technology generations, allowing smaller total device area and capacitance in the comparators [28]; however, the matching is not improved for minimum size devices. Also, due to the reduced power supplies and decreased $g_m r_o$ of the short channel devices, it is difficult to get high gain in a single analog stage. The preamplifiers and latch use non-minimum length transistors to improve both the matching and output impedance. While this does increase device capacitance for the same g_m, there is minimal power impact because wiring parasitics dominate the total capacitance in the comparator.

The capacitor array is entirely passive, and its switching speed is improved with the shorter gate lengths. Because no analog-specific processing steps (e.g., a thin oxide for high density MiM capacitors) were used in fabrication the capacitors are formed using interdigitated metal comb capacitors. The capacitance is determined by fringing between adjacent metal lines, structures that have been shown to achieve similar densities to MiM capacitors with matching limits at greater than the 7-bit level [29]. The capacitance size is chosen according to the matching requirements discussed in Section III-A. The input voltage is constrained to between 0 and 400mV to allow sampling with a single standard-V_T NFET transistor without exceeding the process voltage limit of 1.2 V.

IV. Measurements

The ADC has been fabricated in a 65-nm CMOS technology; a die photograph is shown in Fig. 12. With a 91-kHz input sampled at 500 MS/s, the INL and DNL are $-0.16/0.15$ and $-0.20/0.26$ LSBs, respectively (Fig. 13). The split capacitor array suffers no linearity degradation as compared to a separate on-chip test channel with the conventional array. The split array uses 31% less power from the 400 mV reference voltage supply; the difference in energy savings from the theory presented above is due to the increased bottom-plate routing.

The delay line was tested using an on-chip delay detection circuit and varying the input differential voltage. Due to an un-

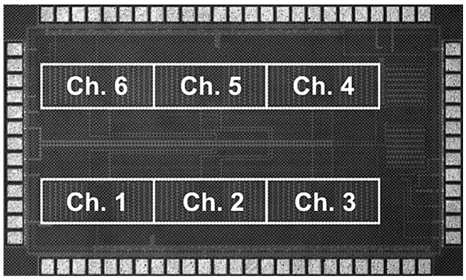

Fig. 12. Photograph of 1.9 × 1.4 mm die.

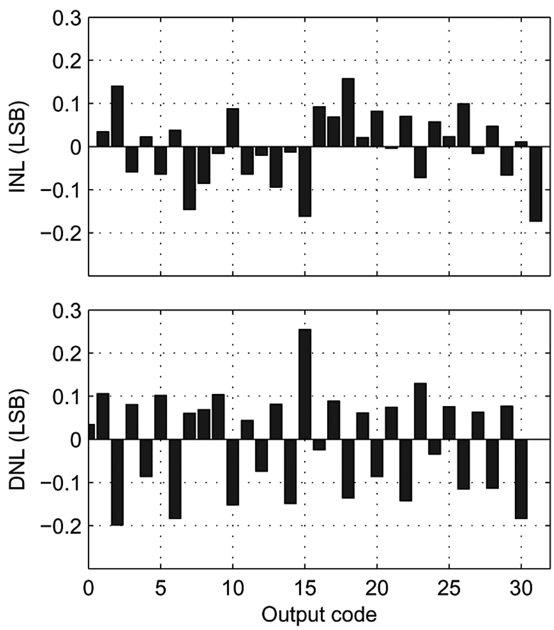

Fig. 13. Static linearity of ADC versus output code.

derestimation of parasitics in the delay line, only the first two delay steps out of 16 provided sufficient time for latch regeneration, and these extended the period available to the preamplifiers by about 10%. At 250 MS/s, a 0.5–1 dB improvement in SNDR was achieved by properly tuning the delay.

The dynamic performance of the ADC is shown in Fig. 14 with the input frequency swept from DC to beyond Nyquist. The signal-to-noise-plus-distortion ratio (SNDR) does not drop by 3 dB until past the Nyquist frequency. A fast Fourier transform (FFT) of a 239.04-MHz input is shown in Fig. 15. Spurs (a)–(d) result from gain errors and skew between channels, and spurs (e)–(f) are due to offset mismatch. All of these spurs are below −39 dBFS, and their combined power is still less than the total noise power (excluding the spurs) at this near-Nyquist input. The gain mismatch between channels is 0.9%. The individual channels have an effective number of bits (ENOB) between 4.65 and 4.75 with low-frequency inputs, dropping by 0.4 bits at Nyquist.

The ADC consumes 2.86 mW and 3.06 mW, respectively, from 1.2-V analog and digital supplies at the maximum sampling frequency. The ADC was also tested at lower sampling frequencies. At 250 MS/s, the ADC consumes a total of 1.58 mW from a 1 V digital and 0.8 V analog supply, while still maintaining Nyquist performance. A summary of the ADC is listed in Table I.

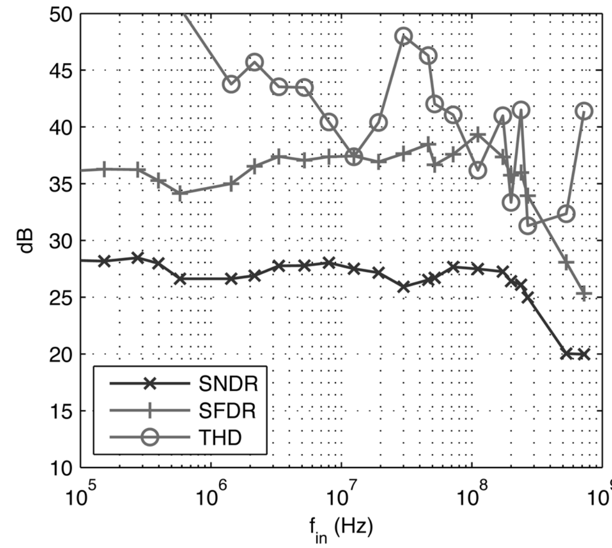

Fig. 14. Dynamic performance versus input frequency.

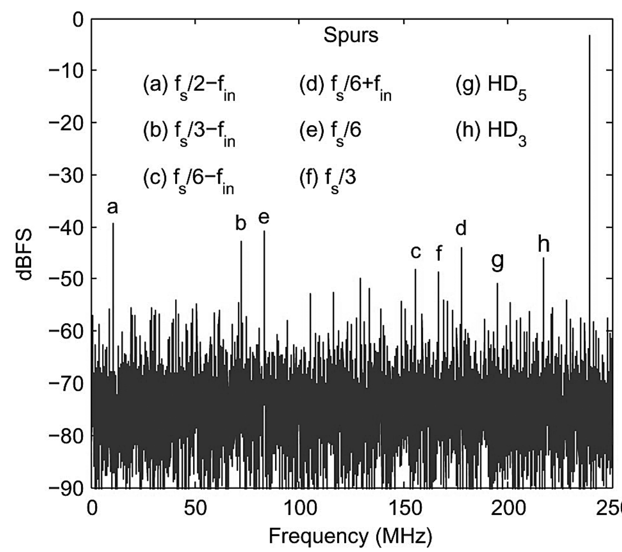

Fig. 15. FFT of 239.04-MHz sine wave sampled at 500 MS/s; dominant spurs are labeled.

TABLE I
SUMMARY OF PERFORMANCE

Technology	65-nm CMOS 1P6M
Supply Voltage	1.2 V
Sampling Rate	500 MS/s
Resolution	5 bit
Input Range	800 mV$_{pp}$ Differential
SNDR (f_{in}=3.3 MHz)	27.8 dB
SNDR (f_{in}=239 MHz)	26.1 dB
SFDR (f_{in}=239 MHz)	36.0 dB
THD (f_{in}=239 MHz)	-41.5 dB
DNL (channel)	0.26 LSB
INL (channel)	0.16 LSB
Analog Power	2.86 mW
Digital Power	3.06 mW
Total Power	5.93 mW
Active Area	0.65 mm × 1.4 mm

TABLE II
COMPARISON OF STATE-OF-THE-ART ADCS

Work	Architecture	Feature Size	Power (mW)	f_S (MHz)	Resolution (bits)	f_{in} (MHz)	ENOB	FOM (pJ/conv. step)
[17]	SAR	90 nm	10	600	6	300	5.1	0.5
[19]	SAR	0.13 μm	5.3	600	6	300	5.02	0.27
[30]	Subranging	0.13 μm	21	125	8	62.5	7.5	0.96
[13]	Pipelined	0.18 μm	30	200	8	99	7.68	0.74
[31]	Subranging	90 nm	55	1000	6	500	5.3	1.37
[32]	Flash	90 nm	2.5	1250	4	625	3.66	0.16
This work	SAR	65 nm	5.9	500	5	239	4.04	0.75
	SAR	65 nm	1.8	250	5	120	4.10	0.44
	SAR	65 nm	0.9	125	5	60	3.95	0.51

V. COMPARISON AND DISCUSSION

To enable a comparison to other ADCs operating at different speeds and resolutions, the figure of merit

$$\mathrm{FOM} = \frac{P}{2^{\mathrm{ENOB}} \cdot 2 \cdot f_{\mathrm{in}}} \tag{14}$$

is used [17], where P is the power consumption, and ENOB is measured for input frequency f_{in}, not to exceed Nyquist input. Table II compares state-of-the-art ADCs with sampling rates in excess of 100 MS/s and resolutions of 8 bits or less. From the results, this ADC has one of the best energy efficiencies of published work. In addition, as three out of the four best designs demonstrate, the time-interleaved SAR architecture can achieve very low power for these specifications. This work requires no linearity calibration or digital post-processing of the samples.

VI. CONCLUSION

An ADC targeted for UWB specifications has been presented. The time-interleaved SAR architecture provides superior energy efficiency to a flash converter because of its linear growth in complexity with the resolution. Two new techniques have enabled high-speed, low-power SAR operation. The split capacitor array offers both lower switching energy and improved settling speed as compared to the conventional array. Joint timing design of the analog and digital portions of the chip, as demonstrated with the adjustable latch strobing instant, can ease settling time requirements and use otherwise wasted idle time during bit-cycling. State-of-the-art energy efficiency and performance have been demonstrated with robust operation in deep-submicron CMOS.

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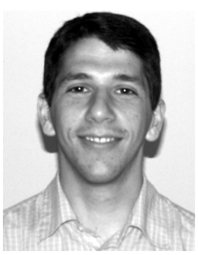

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