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Ch.7 Basic PLL Architectures

PD (7.1)

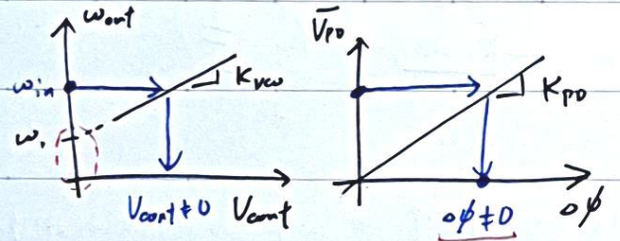
$\overline{V_{out}} = K_{PD} \cdot \phi_e$ XOR Gate: $K_{PD} = \frac{V_o}{\pi}$, Mixer: $\overline{V_{out}}(t) = \frac{kV_o^2}{2}\cos\phi_e$

PLL Analysis (7.3)

$$\phi = \int \omega dt = \int \omega_o + K_{VCO} V_{cont}\, dt = \omega_o t + K_{VCO} \int V_{cont}\, dt$$

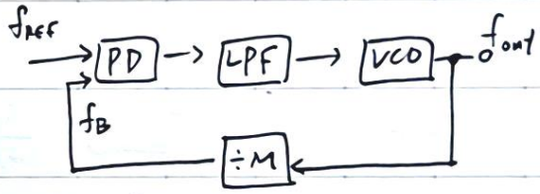
For Lock: $\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0 \Rightarrow f_{out} = f_{in}$

* Static Phase Offset For $\omega_{out} = \omega_{in}$, $V_{cont} \neq 0 \Rightarrow \Delta\phi \neq 0$



↓Static Phase Offset

⇒ Reduced by K_{VCO}↑



* Frequency Multiplication

For $\Delta\phi = \text{Const}$, $f_{REF} = f_B = \frac{f_{out}}{M} \Rightarrow f_{out} = M \times f_{REF}$

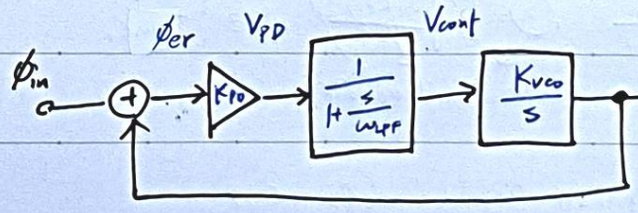
* Acquisition

⇒ PLL needs time to make $f_{out} = f_{in}$

⇒ Both frequency & phase acquisition are required

Transfer Function

Small-Signal Model :



$$A(s) \equiv \frac{\phi_{out}}{\phi_{er}} = K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}, \quad H(s) \equiv \frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \underbrace{\omega_{LPF}}_{2\zeta\omega_n} s + \underbrace{K_{PD}K_{VCO}\omega_{LPF}}_{\omega_n^2}}$$

$$H(s) = \frac{A(s)}{1+A(s)}$$

① ② $\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$, $\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}}$

Tradeoffs:

① PD Makes Noise ⇒ ω_{LPF}↓ ⇒ ζ↓ ⇒ Stability↓

② VCO creates static ϕ_{er} ⇒ K_{PD}↑ ⇒ ζ↓ ⇒ Stability↓

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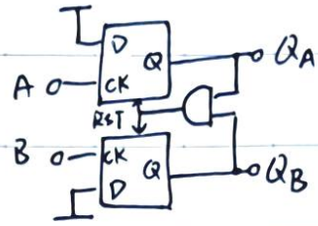
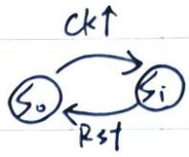
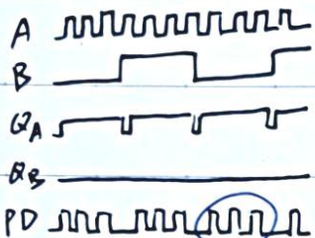
PFD (7.4)

Acquisition : (PFD Vs. PD)



$\Rightarrow$





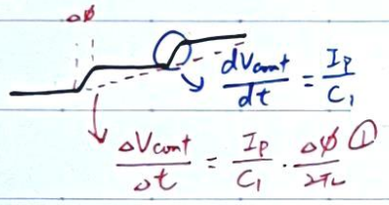
→ Meaningful Output

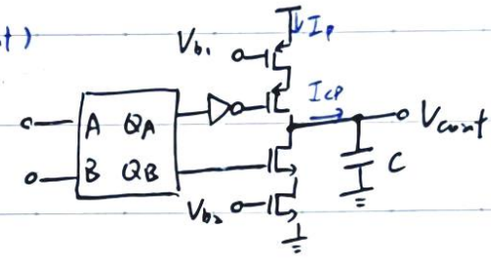
$\Rightarrow$ Useless

Same output as $\Delta\phi = \frac{\pi}{2}$ (Constant)

CPPLL (7.5)

I_{CP} :





$\Rightarrow$ No static phase error ($\because \Delta\phi \rightarrow I_{CP} \neq 0 \rightarrow V_{cont} \uparrow \rightarrow \omega \uparrow \rightarrow \omega_{in} \neq \omega_{out}$)

* Transfer Function

$$\frac{V_{cont}}{\Delta\phi}(s) \overset{①}{=} \frac{I_P}{2\pi C_1 s} \quad I_{CP} = C\frac{dV}{dt} \Longrightarrow \quad \frac{I_{CP}}{\Delta\phi}(s) = \frac{I_P}{2\pi}$$

(Integrator $\Rightarrow$ Type-II PLL)

$$A(s) = \frac{I_P}{2\pi C_1 s} \frac{K_{VCO}}{s} \Rightarrow H(s) = \frac{I_P K_{VCO}}{2\pi C_1 s^2 + I_P K_{VCO}}$$

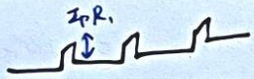
$\angle A(s) = 180^\circ \Rightarrow$ Unstable

$\zeta = 0 \Rightarrow$ Unstable

$\Rightarrow$ Add open-loop zero : $\frac{1}{T} C_1 \Rightarrow \frac{1}{T} C_1$ $\{R_1$

$$\Rightarrow H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO} R_1 s + \frac{I_P K_{VCO}}{2\pi C_1}}$$

Stability Jump :



$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}}, \quad \zeta = \frac{R_1}{2}\sqrt{\frac{I_P K_{VCO} C_1}{2\pi}}, \quad \omega_z = -\frac{1}{R_1 C_1}$$

No more tradeoff

* Added C_2 on CPPLL ($C_2 \ll C_1$)

Peak-to-Peak Ripple : $\frac{I_P}{C_2} T_{sk}$

* CP Topologies

$\Rightarrow$ Source-Switched : Clock Feedthrough ↓, Rout ↑ ($R_{sat} > R_{triode}$)

$\Rightarrow$ Gate-Switched : Larger Voltage Swing

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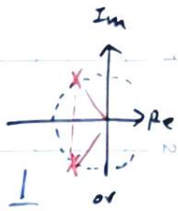
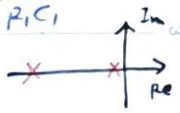
Ch.8 PLL Design Considerations

Bandwidth (8.1)

$$A(s)=\frac{2\omega_n\zeta s+\omega_n^2}{s^2} \Rightarrow H(s)=\frac{2\omega_n\zeta s+\omega_n^2}{s^2+2\omega_n\zeta s+\omega_n^2} \Rightarrow \omega_{1,2}=(-\zeta\pm\sqrt{\zeta^2-1})\omega_n$$



For $\zeta^2 \gg 1$: $\omega_{p1}\doteq -\frac{\omega_n}{2\zeta}=-\frac{1}{R_1C_1}$, $\omega_{p2}\doteq -2\zeta\omega_n=-\frac{R_1I_DK_{VCO}}{2\pi}$, $\omega_z\doteq -\frac{\omega_n}{2\zeta}=-\frac{1}{R_1C_1}$ or

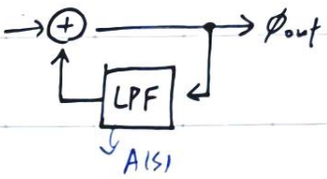


$\omega_{-3dB}\doteq 2\zeta\omega_n\doteq\omega_{p2} \Rightarrow \omega_{p1}\doteq\omega_z \Rightarrow$ Cancel, $\omega_{-3dB}\doteq\omega_n \Rightarrow$ One Pole

$\omega_u\doteq 2\zeta\omega_n\doteq\omega_{3dB}$

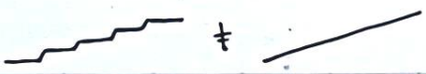
* Noise Suppression Noise : VCO > CP > PFD > divider

$$\frac{\phi_{out,vco}}{\phi_n}(s)=\frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2},\ \omega_{HP}=\left[2\zeta^2-1+\sqrt{(2\zeta^2-1)^2+1}\right]\omega_n^2$$



For $2\zeta^2 \gg 1$: $\omega_{HP}\doteq 2\zeta\omega_n\doteq\omega_u\doteq\omega_{3dB}$

* Limitations of CT Approximation



$\neq$ $\Rightarrow$ Bigger C : Slower Ramp $\Rightarrow$ DT $\approx$ CT

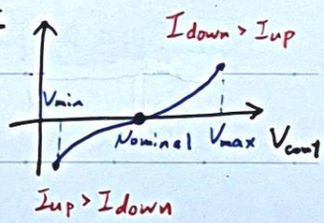
Charge Pump Issues (8.3)

Skew :  delay $\Rightarrow$ Still has skew due to temperature / corner issues

Voltage Compliance : Input Voltage Range of VCO

Tradeoff

Channel Length Modulation : V_{cont} Swing $\Rightarrow I_1 \neq I_2$



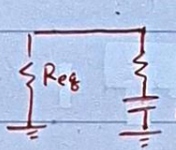
↳ Use long transistors for  $\Rightarrow V_A \uparrow$

Random Mismatches : Enlarge CP transistors

Clock Feedthrough : $|\Delta V_{cont}|=\left|V_{DD}\frac{C_{GD5}-C_{GD4}}{C_2+C_{GD3}+C_{GD4}}\right|$] $\Rightarrow$ big transistors ×

Charge Injection : $Q_{inject}=WLC_{ox}(V_{GS}-V_{TH})$

↳ Increase C_1 to smoothen the ripples

Effect of Rout : $R_{eq}=R_{out}\frac{T_{REF}}{T_{res}}$ $\Rightarrow$ pole : 

$\tau=(R_1+R_{eq})C_1$

Leakage Current : Causes $V_{cont} \to V_{cont}-\frac{I_{leak}}{C_1}T_{REF}$ $\Rightarrow$ Phase offset $\frac{I_{leak}}{I_p}T_{REF}$

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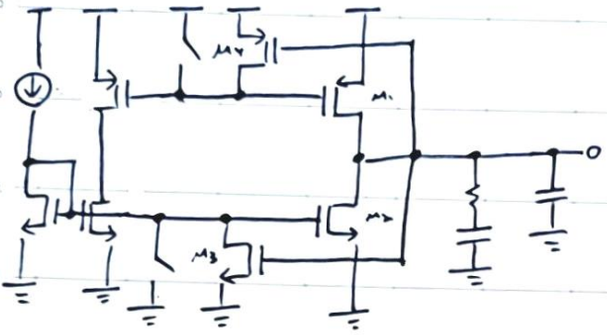
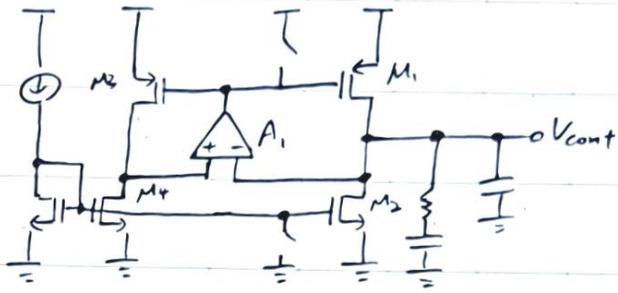
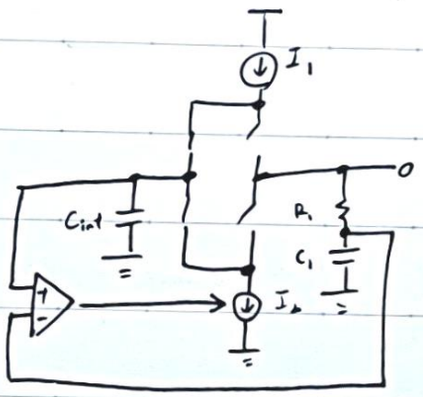
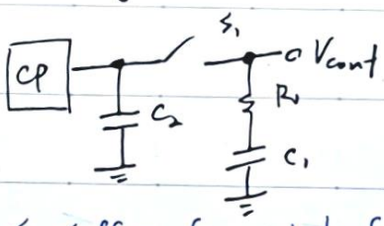
Improved charge Pumps (8.4)







* Sampling loop filter



=> S_1 suffers from clock feedthrough

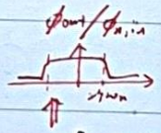
* Cap leakage => thick-oxide or metal Caps

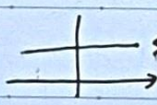
Filter Capacitor Reduction (8.8)

For $I_{p1} = \alpha I_{p2}$, $C_1 \to \frac{1}{\alpha - 1}$ Stabilizing jump is still $I_{p1}R_1$

↳ Suffers from two noise currents in CP1 and CP2

Phase Noise (8.10)



* $\phi_{n,in}$:  => Shaped by the HIsI of PLL => $\sigma_{t_{rms}} = \frac{1}{2\pi f_0}\sqrt{\pi M^2 S_{\phi,in} f_{3dB}} \cdot T_{out}$

* $\phi_{n,vco}$: $S_{\phi,vco}(\omega) = \frac{\alpha}{\omega^3} + \frac{\beta}{\omega^2}$, $\left|\frac{\phi_{out}}{\phi_{n,vco}}\right|^2 = \frac{\omega^4}{(\omega_n^2 - \omega^2)^2 + 4\zeta^2\omega_n^2\omega^2}$ (HP)

=> $S_{\phi n}(\omega) = S_{\phi,vco}(\omega) \cdot \left|\frac{\phi_{out}}{\phi_{n,vco}}\right|^2 \Rightarrow \sim \frac{\alpha\omega}{\omega_n^4}\ (\omega \ll \omega_c = \frac{\alpha}{\beta})$, $\sim \frac{\beta}{\omega^2}\ (\omega \gg \omega_c)$

Caused by HP response of $\phi_{n,vco}$; Caused by VCO T(s)

↳ Trade off: $S_\phi \downarrow \Rightarrow \omega_n \uparrow \Rightarrow C \downarrow \Rightarrow$ Ripple↑

↳ Integration of $S_{\phi,n} \Rightarrow \phi_{out,rms} = 4\pi\zeta f_{BW} \Rightarrow$ Optimize $S_{\phi,in} + S_{\phi,vco} \Rightarrow f_{BW} = \sqrt{\frac{4\beta}{\pi M^2 S_0}}$.

* $\phi_{n,CP}$: For |s| small, $S_{\phi n,white} = 2\overline{I_{1,n}^2} \times \frac{T_{res}}{T_{in}} \times \frac{4\pi^2 M^2}{I_p^2}$↑, $S_{\phi n,\frac{1}{f}} = 2\overline{I_{nf}^2}(1) \times \frac{T_{res}^2}{T_{in}^2} \times \frac{4\pi^2 M^2}{I_p}$ (negligible)

* $\phi_{n,LF}$: $S_{\phi n,p} = \frac{16kT\pi^2 M^2}{R_1 I_p^2}$↑

* $\phi_{n,supply}$: $\left|\frac{\phi_{out}}{V_n}\right| = \frac{K_{VCO}\, s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \Rightarrow \left|\frac{\phi_{out}}{V_n}\right|_{max} = \frac{K_{VCO}}{2\zeta\omega_n}$↑