

## Homework 6

Please clearly organize and present your solutions.

Due: Dec. 13

\* If  $V_{DD}$  is not specified,  $V_{DD}$  is set to 1 V. You should use real components in your simulation. For DC voltage source, please use “vdc” in analoglib.

\*Please attach your schematic and simulation results, and ensure that the background is inverted to white.

\* Plagiarism is strictly prohibited. If you are found guilty, you will receive a score of 0.

1. Problems 9.18 in the textbook.

**9.18.** In this problem, we design a two-stage op amp based on the topology shown in Fig. 9.90. Assume a power budget of 6 mW, a required output swing of 2.5 V, and  $L_{eff} = 0.5 \mu\text{m}$  for all devices.

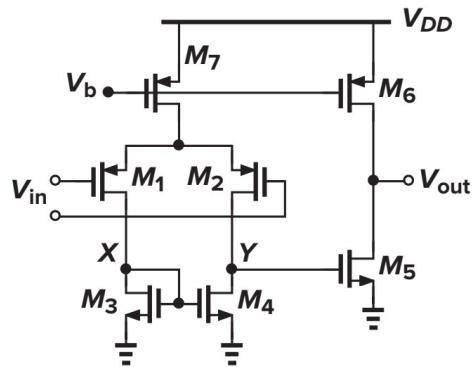


Figure 9.90

- Allocating a current of 1 mA to the output stage and roughly equal overdrive voltages to  $M_5$  and  $M_6$ , determine  $(W/L)_5$  and  $(W/L)_6$ . Note that the gate-source capacitance of  $M_5$  is in the signal path, whereas that of  $M_6$  is not. Thus,  $M_6$  can be quite a lot larger than  $M_5$ .
- Calculate the small-signal gain of the output stage.
- With the remaining 1 mA flowing through  $M_7$ , determine the aspect ratio of  $M_3$  (and  $M_4$ ) such that  $V_{GS3} = V_{GS5}$ . This is to guarantee that if  $V_{in} = 0$  and hence  $V_X = V_Y$ , then  $M_5$  carries the expected current.
- Calculate the aspect ratios of  $M_1$  and  $M_2$  such that the overall voltage gain of the op amp is equal to 500.

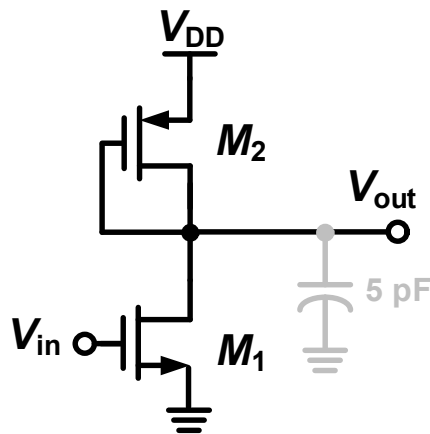


Fig. 1

| Transistor                         | $M_1$ | $M_2$  |
|------------------------------------|-------|--------|
| Finger number                      | 10    |        |
| Fin number (multiplier)            | 20    |        |
| Length                             | 16 nm | 240 nm |
| Source M1 width/<br>Drain M1 width | 50 nm |        |

Table 1

2. In this problem, consider a CS amplifier with a diode connected load as shown in Fig. 1. Transistors parameters are provided in Table 1.  $V_{in}$  is realized by “vsin” in analoglib with 10 mV<sub>p-p</sub> and a DC voltage of 500 mV to ensure the bias conditions of  $M_1$  and  $M_2$  unchanged. Perform “noise” simulation and answer the following questions.
- (1) Specify the frequency range to be 1 kHz~1 THz. Plot output noise ( $V^2/\text{Hz}$ ) in dB versus frequency in log scale.
  - (2) The plot above can be divided into several regions based on the slope of the plot. Look into “Noise Summary...” and specify the dominating noise contributor (including the name of the component and the type of noise) at each region.
  - (3) Specify the temperature as 60°C and repeat (1), (2).  
(Hint: Temperature setting can be found somewhere in ADE.)