1. DISPLAY GUIDELINES

Sample Test Case:

```
4000 MOVC R0, #0
4004 MOVC R1, #1
4008 MOVC R2, #2
4012 MOVC R4, #4
4016 MOVC R5, #1
4020 MOVC R6, #1000
4024 MOVC R7, #4028
4028 BZ #28                    /* goes to HALT when loop ends */
4032 MUL R3, R2, R2
4036 STR R3, R6, R0
4040 ADD R6, R6, R4
4044 ADD R2, R2, R1
4048 SUB R5, R5, R1            /*sets Z flag if result is zero */
4052 JUMP R7, #0
4056 HALT
```

Expected Output:

Below output is manually created, so verify the output with required functionalities and if you find any discrepancies then do let us know.

```
#--#--#--#--#--#--#--#--#--#--#--#--#--#-- SIMULATION START #--#--#--#--#--#--#--#--#--#--#--#--#-
^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 1 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I0) MOVC R0, #0
Instruction at DECODE_RF_STAGE ---> EMPTY
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Details of RAT State --
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Details of R-RAT State --
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Details of Unified Physical Register File State --
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Details of BTB State --
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Details of IQ (Issue Queue) State --
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Details of ROB (Reorder Buffer) State –
(H) (T)
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Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
```

Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
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Details of ROB Retired Instructions State –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 2 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I1) MOVC R1, #1
Instruction at DECODE_RF_STAGE ---> (I0) MOVC R0, #0
~~~~~~

Details of RAT State --
~~~~~~

Details of R-RAT State --
~~~~~~

Details of Unified Physical Register File State --
~~~~~~

Details of BTB State --
~~~~~~

Details of IQ (Issue Queue) State --
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) (T)
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 3 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I2) MOVC R2, #2
Instruction at DECODE_RF_STAGE ---> (I1) MOVC R1, #1
~~~~~~

Details of RAT State –
R[00] -> P0
~~~~~~

Details of R-RAT State –
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	0	-1
1	0	0	-1

2	0	0	-1
3	0	0	-1
4	0	0	-1
5	0	0	-1
6	0	0	-1

~~~~~~

Details of BTB State --

~~~~~~

Details of IQ (Issue Queue) State –
(I0) MOVC P0, #0 [MOVC R0, #0]

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I0) MOVC P0, #0 [MOVC R0, #0]
(T) ->

~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY

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Details of ROB Retired Instructions State –

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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 4 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I3) MOVC R4, #4
Instruction at DECODE_RF_STAGE ---> (I2) MOVC R2, #2

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Details of RAT State –
R[00] -> P0
R[01] -> P1

~~~~~~

Details of R-RAT State –

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Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	0	-1
1	1	0	-1
2	0	0	-1
3	0	0	-1
4	0	0	-1
5	0	0	-1
6	0	0	-1

~~~~~~

Details of BTB State --

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Details of IQ (Issue Queue) State –
(I1) MOVC P1, #1 [MOVC R1, #1]
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I0) MOVC P0, #0 [MOVC R0, #0]
(I1) MOVC P1, #1 [MOVC R1, #1]
(T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I0) MOVC P0, #0 [MOVC R0, #0]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 5 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I4) MOVC R5, #1
Instruction at DECODE_RF_STAGE ---> (I3) MOVC R4, #4
~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
~~~~~~

Details of R-RAT State –
R[0] -> P0
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	0	-1
2	1	0	-1
3	0	0	-1
4	0	0	-1
5	0	0	-1
6	0	0	-1

~~~~~~

Details of BTB State --
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Details of IQ (Issue Queue) State –
(I2) MOVC P2, #2 [MOVC R2, #2]
~~~~~~
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I1) MOVC P1, #1 [MOVC R1, #1]
(I2) MOVC P2, #2 [MOVC R2, #2]
(T) ->
~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I1) MOVC P1, #1 [MOVC R1, #1]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
(I0) MOVC P0, #0 [MOVC R0, #0]
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 6 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I5) MOVC R6, #1000
Instruction at DECODE_RF_STAGE ---> (I4) MOVC R5, #1
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	0	-1
3	1	0	-1
4	0	0	-1
5	0	0	-1
6	0	0	-1

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Details of BTB State --
~~~~~~
Details of IQ (Issue Queue) State –
(I3) MOVC P3, #4 [MOVC R4, #4]
~~~~~~
Details of ROB (Reorder Buffer) State –
~~~~~~

(H) -> (I2) MOVC P2, #2 [MOVC R2, #2]
(I3) MOVC P3, #4 [MOVC R4, #4]
(T) ->
~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I2) MOVC P2, #2 [MOVC R2, #2]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
(I1) MOVC P1, #1 [MOVC R1, #1]
~~~~~~
^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 7 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I6) MOVC R7, #4028
Instruction at DECODE_RF_STAGE ---> (I5) MOVC R6, #1000
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	0	-1
4	1	0	-1
5	0	0	-1
6	0	0	-1

~~~~~~
Details of BTB State --
~~~~~~
Details of IQ (Issue Queue) State –
(I4) MOVC P4, #1 [MOVC R5, #1]
~~~~~~
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I3) MOVC P3, #4 [MOVC R4, #4]
(I4) MOVC P4, #1 [MOVC R5, #1]
(T) ->
~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I3) MOVC P3, #4 [MOVC R4, #4]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
(I2) MOVC P2, #2 [MOVC R2, #2]
~~~~~~
^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 8 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I7) BZ #24
Instruction at DECODE_RF_STAGE ---> (I6) MOVC R7, #4028
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	0	-1
5	1	0	-1
6	0	0	-1

~~~~~~
Details of BTB State --
~~~~~~

Details of IQ (Issue Queue) State –
(I5) MOVC P5, #1000 [MOVC R6, #1000]
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I4) MOVC P4, #1 [MOVC R5, #1]
(I5) MOVC P5, #1000 [MOVC R6, #1000]
(T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I4) MOVC P4, #1 [MOVC R5, #1]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
(I3) MOVC P3, #4 [MOVC R4, #4]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 9 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I8) MUL R3, R2, R2
Instruction at DECODE_RF_STAGE ---> (I7) BZ #24
~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
~~~~~~

5	1	0	-1
6	1	0	-1

~~~~~~

Details of BTB State --

~~~~~~

Details of IQ (Issue Queue) State –
(I6) MOVC P6, #4028 [MOVC R7, #4028]

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I5) MOVC P5, #1000 [MOVC R6, #1000]
(I6) MOVC P6, #4028 [MOVC R7, #4028]
(T) ->

~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I5) MOVC P5, #1000 [MOVC R6, #1000]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY

~~~~~~

Details of ROB Retired Instructions State –
(I4) MOVC P4, #1 [MOVC R5, #1]

~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 10 ^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I9) STR R3, R6, R0
Instruction at DECODE_RF_STAGE ---> (I8) MUL R3, R2, R2

~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6

~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5

~~~~~~

Details of Unified Physical Register File State –
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#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	Invalid

~~~~~~

Details of IQ (Issue Queue) State –
(I7) BZ #24
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I6) MOVC P6, #4028 [MOVC R7, #4028]
(I7) BZ #24
(T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I6) MOVC P6, #4028 [MOVC R7, #4028]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
(I5) MOVC P5, #1000 [MOVC R6, #1000]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 11 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I9) ADD R6, R6, R4
Instruction at DECODE_RF_STAGE ---> (I9) STR R3, R6, R0
~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
R[3] -> P7
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	1	4028
7	0	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	Invalid

~~~~~~

Details of IQ (Issue Queue) State –
(I8) MUL R3, R2, R2 [MUL P7, P2, P2]
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I7) BZ #24
(I8) MUL R3, R2, R2 [MUL P7, P2, P2]
(T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> (I7) BZ #24
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
(I6) MOVC P6, #4028 [MOVC R7, #4028]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 12 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I11) ADD R2, R2, R1
~~~~~~

Instruction at DECODE_RF_STAGE ---> (I10) ADD R6, R6, R4

~~~~~~

Details of RAT State –

R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
R[3] -> P7

~~~~~~

Details of R-RAT State –

R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6

~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	1	4028
7	1	0	-1
8	0	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –

(I9) STR R3, R6, R0 [STR P7, P5, P0]

~~~~~~

Details of ROB (Reorder Buffer) State –

(H) -> (I7) BZ #24
        (I8) MUL R3, R2, R2 [MUL P7, P2, P2]
        (I9) STR R3, R6, R0 [STR P7, P5, P0]
(T) ->

~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> (I7) BZ #24
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> (I8) MUL R3, R2, R2 [MUL P7, P2, P2] (CYCLE 1)
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
(I6) MOVC P6, #4028 [MOVC R7, #4028]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 13 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I12) SUB R5, R5, R1
Instruction at DECODE_RF_STAGE ---> (I11) ADD R2, R2, R1
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	1	4028
7	1	0	-1

8	1	0	-1
9	0	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
(I9) STR R3, R6, R0 [STR P7, P5, P0]
(I10) ADD R6, R6, R4 [ADD P8, P5, P3]
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I8) MUL R3, R2, R2 [MUL P7, P2, P2]
(I9) STR R3, R6, R0 [STR P7, P5, P0]
(I10) ADD R6, R6, R4 [ADD P8, P5, P3]
(T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> (I8) MUL R3, R2, R2 [MUL P7, P2, P2] (CYCLE 2)
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
(I7) BZ #24
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 14 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I13) JUMP R7, #0
Instruction at DECODE_RF_STAGE ---> (I12) SUB R5, R5, R1
~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P4
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1

R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	1	4028
7	1	0	-1
8	1	0	-1
9	1	0	-1
10	0	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

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Details of IQ (Issue Queue) State –
(I9) STR R3, R6, R0 [STR P7, P5, P0]
(I11) ADD R2, R2, R1 [ADD P9, P2, P1]
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I8) MUL R3, R2, R2 [MUL P7, P2, P2]
(I9) STR R3, R6, R0 [STR P7, P5, P0]
(I10) ADD R6, R6, R4 [ADD P8, P5, P3]
(I11) ADD R2, R2, R1 [ADD P9, P2, P1]
(T) ->
~~~~~~

Instruction at JBU1_FU_STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I10) ADD R6, R6, R4 [ADD P8, P5, P3]
Instruction at MUL_FU_STAGE ---> (I8) MUL R3, R2, R2 [MUL P7, P2, P2] (CYCLE 3)
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
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^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 15 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I14) HALT

Instruction at DECODE_RF_STAGE ---> (I13) JUMP R7, #0

~~~~~~

Details of RAT State –

R[0] -> P0

R[1] -> P1

R[2] -> P9

R[4] -> P3

R[5] -> P10

R[6] -> P8

R[7] -> P6

R[3] -> P7

~~~~~~

Details of R-RAT State –

R[0] -> P0

R[1] -> P1

R[2] -> P2

R[4] -> P3

R[5] -> P4

R[6] -> P5

R[7] -> P6

R[3] -> P7

~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	0	-1
10	1	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –

(I12) SUB R5, R5, R1 [SUB P10, P4, P1]

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I9) STR R3, R6, R0 [STR P7, P5, P0]
(I10) ADD R6, R6, R4 [ADD P8, P5, P3]
(I11) ADD R2, R2, R1 [ADD P9, P2, P1]
(I12) SUB R5, R5, R1 [SUB P10, P4, P1]
(T) ->
~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I11) ADD R2, R2, R1 [ADD P9, P2, P1]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> (I9) STR R3, R6, R0 [STR P7, P5, P0]
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
(I8) MUL R3, R2, R2 [MUL P7, P2, P2]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 16 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> (I14) HALT
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P2
R[4] -> P3
R[5] -> P4
R[6] -> P5
R[7] -> P6
R[3] -> P7
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1

2	1	1	2
3	1	1	4
4	1	1	1
5	1	1	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	0	-1

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
(I13) JUMP R7, #0 [JUMP P6, #0]

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I9) STR R3, R6, R0 [STR P7, P5, P0]
    (I10) ADD R6, R6, R4 [ADD P8, P5, P3]
    (I11) ADD R2, R2, R1 [ADD P9, P2, P1]
    (I12) SUB R5, R5, R1 [SUB P10, P4, P1]
    (I13) JUMP R7, #0 [JUMP P6, #0]
(T) ->

~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> (I12) SUB R5, R5, R1 [SUB P10, P4, P1]
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> (I9) STR R3, R6, R0 [STR P7, P5, P0]

~~~~~~

Details of ROB Retired Instructions State –

~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 17 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> EMPTY

~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
~~~~~~

R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0

Z = 1
~~~~~~

Details of Data Memory State –
D[1000] = 4
~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I13) JUMP R7, #0 [JUMP P6, #0]
        (I14) HALT
(T) ->
~~~~~~

Instruction at JBU1_FU_STAGE ---> (I13) JUMP R7, #0 [JUMP P6, #0]
Instruction at JBU2_FU_STAGE ---> EMPTY
~~~~~~

Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
(I9) STR R3, R6, R0 [STR P7, P5, P0]
(I10) ADD R6, R6, R4 [ADD P8, P5, P3]
(I11) ADD R2, R2, R1 [ADD P9, P2, P1]
(I12) SUB R5, R5, R1 [SUB P10, P4, P1]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 18 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I7) BZ #24
Instruction at DECODE_RF_STAGE ---> EMPTY
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
~~~~~~

7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0

~~~~~~

Details of Data Memory State –
D[1000] = 4

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I13) JUMP R7, #0 [JUMP P6, #0]
(T) ->

~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> (I13) JUMP R7, #0 [JUMP P6, #0]
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY

~~~~~~

Details of ROB Retired Instructions State –

~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 19 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I8) MUL R3, R2, R2
Instruction at DECODE_RF_STAGE ---> (I7) BZ #24

~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7

~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
~~~~~~

R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0

~~~~~~

Details of Data Memory State –
D[1000] = 4
~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) (T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
(I13) JUMP R7, #0 [JUMP P6, #0]
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 20 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I9) STR R3, R6, R0
Instruction at DECODE_RF_STAGE ---> (I8) MUL R3, R2, R2
~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0
11	0	0	-1

~~~~~~

Details of Data Memory State –
D[1000] = 4
~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
(I7) BZ #24
~~~~~~
Details of ROB (Reorder Buffer) State –
(H) -> (I7) BZ #24
(T) ->
~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 21 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I10) ADD R6, R6, R4
Instruction at DECODE_RF_STAGE ---> (I9) STR R3, R6, R0
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P2
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
~~~~~~

2	1	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0
11	0	0	-1

~~~~~~

Details of Data Memory State –
D[1000] = 4

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
(I8) MUL R3, R2, R2 [MUL P2, P9, P9]

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I7) BZ #24
        (I8) MUL R3, R2, R2 [MUL P2, P9, P9]
(T) ->

~~~~~~

Instruction at JBU1_FU _STAGE ---> (I7) BZ #24
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY

~~~~~~

Details of ROB Retired Instructions State –

~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 22 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> (I10) ADD R6, R6, R4
Instruction at DECODE_RF_STAGE ---> (I9) STR R3, R6, R0

~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3

R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P2
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	1	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0
11	0	0	-1

~~~~~~

Details of Data Memory State –
D[1000] = 4
~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	00	4052

~~~~~~

Details of IQ (Issue Queue) State –
(I8) MUL R3, R2, R2 [MUL P2, P9, P9]
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I7) BZ #24
(I8) MUL R3, R2, R2 [MUL P2, P9, P9]
(T) ->
~~~~~~
~~~~~~

Instruction at JBU1_FU _STAGE ---> (I7) BZ #24
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 23 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
Instruction at FETCH_STAGE ---> (I14) HALT
Instruction at DECODE_RF_STAGE ---> EMPTY
~~~~~~
Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~
Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
~~~~~~

9	1	1	3
10	1	1	0

~~~~~~

Details of Data Memory State –
D[1000] = 4

~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	01	4052

~~~~~~

Details of IQ (Issue Queue) State –

~~~~~~

Details of ROB (Reorder Buffer) State –
(H) -> (I7) BZ #24
(T) ->

~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> (I7) BZ #24
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY

~~~~~~

Details of ROB Retired Instructions State –

~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 24 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE ---> (I14) HALT

~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7

~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
~~~~~~

R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0

~~~~~~

Details of Data Memory State –
D[1000] = 4
~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	01	4052

~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
(H) (T) ->
~~~~~~

Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~

Details of ROB Retired Instructions State –
(I7) BZ #24
~~~~~~

^^^^^^^^^^^^^^^^^^^^^^^^^^^^ CLOCK CYCLE 25 ^^^^^^^^^^^^^^^^^^^^^^^^^^^^

Instruction at FETCH_STAGE ---> EMPTY
Instruction at DECODE_RF_STAGE --->

~~~~~~

Details of RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of R-RAT State –
R[0] -> P0
R[1] -> P1
R[2] -> P9
R[4] -> P3
R[5] -> P10
R[6] -> P8
R[7] -> P6
R[3] -> P7
~~~~~~

Details of Unified Physical Register File State –

#	Allocated	Valid	Content
0	1	1	0
1	1	1	1
2	0	0	2
3	1	1	4
4	0	0	1
5	0	0	1000
6	1	1	4028
7	1	1	4
8	1	1	1004
9	1	1	3
10	1	1	0

~~~~~~

Details of Data Memory State –
D[1000] = 4
~~~~~~

Details of BTB State –

Branch	History bits	Computed target address
(I7) BZ #24	01	4052

~~~~~~

Details of IQ (Issue Queue) State –
~~~~~~

Details of ROB (Reorder Buffer) State –
~~~~~~

(H) -> (I14) HALT
(T) ->
~~~~~~
Instruction at JBU1_FU _STAGE ---> EMPTY
Instruction at JBU2_FU_STAGE ---> EMPTY
Instruction at INTU_FU_STAGE ---> EMPTY
Instruction at MUL_FU_STAGE ---> EMPTY
Instruction at M1_FU_STAGE ---> EMPTY
Instruction at M2_FU_STAGE ---> EMPTY
~~~~~~
Details of ROB Retired Instructions State –
~~~~~~

2. SIMULATOR METHODS

1. There are three functions – simulate(), display() and single_step() which needs to be implemented as a part of project.
2. There should be second command line argument (simulate/display/single_step) to distinguish these three functions:
    a. Second command line argument is "simulate" only show State of Unified Physical Register File and Data Memory.
    b. Second command line argument is "display" show Instruction Flow with all the states shown above, but **DO NOT** display State of Unified Physical Register File and Data Memory in each cycle (**Note:** Display State of Unified Physical Register File and Data Memory only at the end).
    c. Second command line argument is "single_step" simulation by one cycle and show Instruction Flow with all the states shown above, but **DO NOT** display State of Unified Physical Register File and Data Memory in each cycle (**Note:** Display State of Unified Physical Register File and Data Memory only at the end).
3. There should be third command line argument as "number of cycles" means up to this number of cycles simulation should run and produce output.
4. Example with three command line arguments while running the program:
    a. make
    b. ./apex_sim input.asm simulate 50
        i. Simulate for 50 cycles and then show State of Unified Physical Register File and Data Memory at the end of 50 cycles or at the end of program (whichever comes first).
    c. make
    d. ./apex_sim input.asm display 10
        i. Simulate for 10 cycles and then show Instruction Flow as well as State of Unified Physical Register File and Data Memory at the end of 10 cycles or at the end of program (whichever comes first).
    e. Make
~~~~~~

f. ./apex_sim input.asm single_step
    i. Proceed one cycle and display all the states shown above, but **DO NOT** display State of Unified Physical Register File and Data Memory in each cycle (**Note:** Display State of Unified Physical Register File and Data Memory only at the end)

3. SUBMISSION GUIDELINES

In order get your grades as soon as possible and with more feedback, follow these instructions, otherwise points will be deducted:

1. (-2 points) Check not to upload a corrupted file (you can download it and test it).
2. (-2 points) Submit a .tar.gz file (not a .tar nor .zip nor .rar) which should follow the following naming convention: **<lastname>_<firstname>_<bnumber>.**tar.gz, after unpacking this .tar.gz it should have a directory named **<lastname>_<firstname>_<bnumber>**. Inside of this folder, you should have two folders: **1_version** and **2_version** where corresponding simulators are located.
3. (-2 points) Check your code compile/run on bingsuns2.cc.binghamton.edu.
4. (-4 points) Your submission folder should contain README file where you should list your team members.