Traffic Light Controller with Simultaneous Red Lights

Implementation of an Intelligent traffic light controller using the ISE WebPack and Nexys 3 board. Design and implement a smart traffic light controller system using VHDL and FPGA. The system should model a Mealy based Finite state machine whereas the outputs depend on the inputs and the current state. The system should control an intersection with turning lanes and a prioritized busy lane.

Specifications:
- give green light to (busy) highway as much as possible (higher priority).
- give green to (not busy) farm road momentarily when needed.
- must always have at least one red light.
- sensor on farm road indicates when cars are waiting for green light.
- must obey required (time) lengths for green, yellow, red lights.

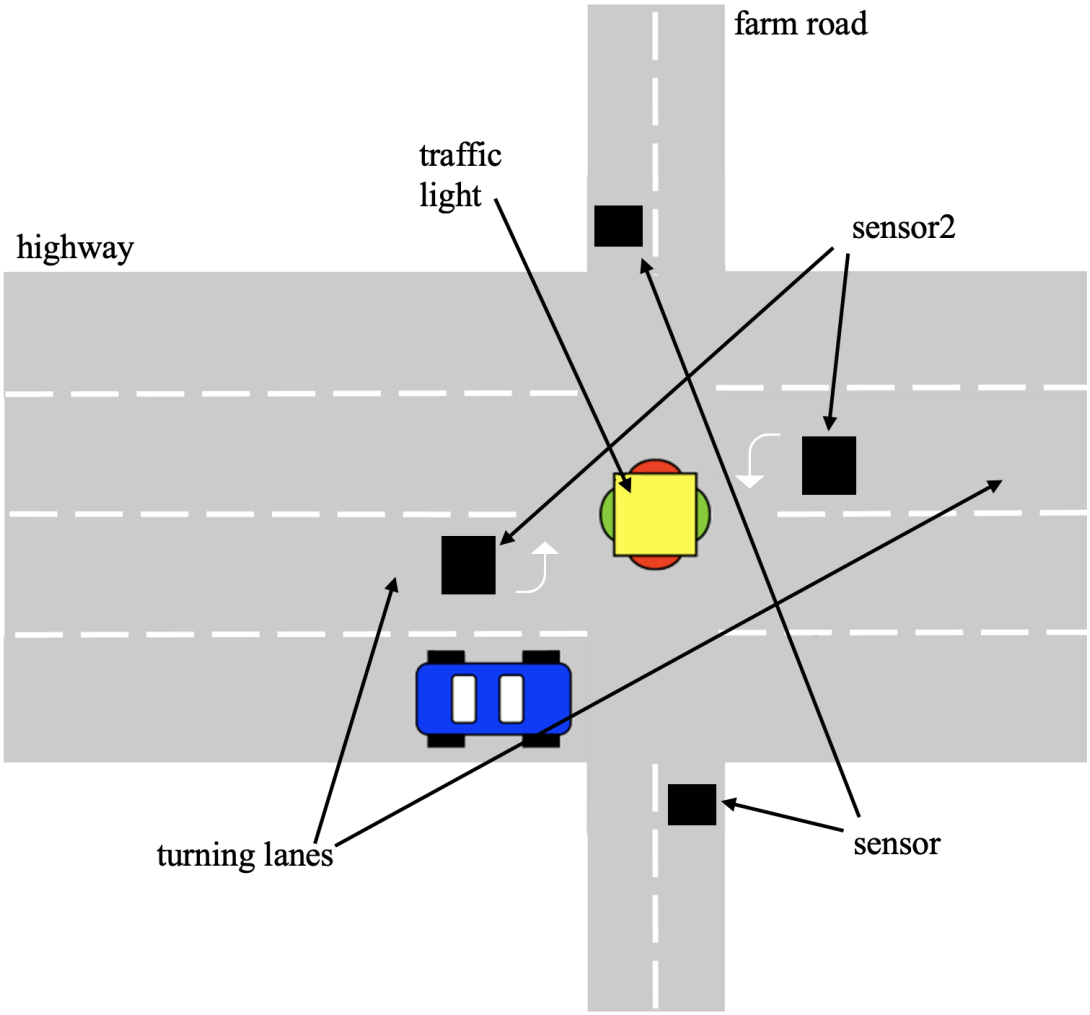
Cases to Consider:
1. no car waiting at farm road -> highway green and farm road red.
2. car(s) waiting at farm road AND highway green for some minimum time (called LONG) -> highway turns yellow for some minimum time (called SHORT) -> highway turns red and farm road stays red.
3. Both highway and farm road stay red for some minimum time (called SHORT) -> farm road turns green.
4. no car waiting at farm road anymore OR farm road green for some minimum time (LONG) -> farm road turns yellow for some minimum time (SHORT) -> farm road turns red and highway turns green.
5. repeat #1.

Design Approach:
Build the traffic light controller out of two modules:
- a state machine: sets colors of lights, etc
- two counters: control durations of lights

Basic Design

clear=1 resets the two counters
long=1 when long counter expires
short=1 when short counter expires
sensor=1 when car(s) on farm road
sensor2=1 when car(s) in turning

Modeled Intersection



State Machine