CS 271 Computer Architecture and Assembly Language
Self-Check for Lecture #2 **Solutions**

1. Terms / Definitions
   a. "caching" is **moving information from slower storage to faster storage, where it can be accessed more quickly.**
   b. A "bus" is **a set of parallel "wires" for transferring a set of electrical signals simultaneously.**
   c. "vonNeumann architecture" refers to computer architectures that **store programs in memory, and execute them under the control of the instruction execution cycle.**

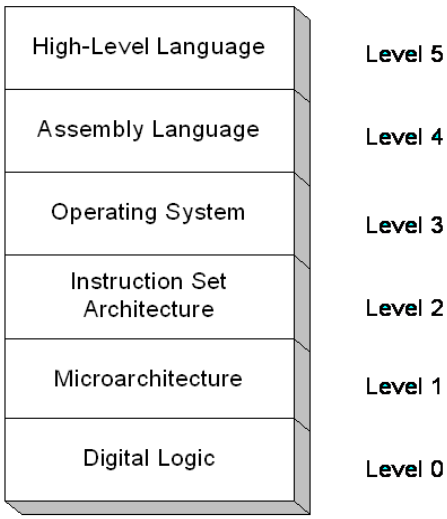
2. Inside the computer, machine instructions, memory addresses, numbers, characters, etc., are all represented as **electrical signals.**

3. In the simple CISC architecture discussed in Lecture #2, which register holds
   a. the current machine instruction? **The Instruction Register (IR).**
   b. the current micro-instruction? **The Control Register.**

4. Number the order of steps in the instruction execution cycle.

   3 Decode the instruction in the Instruction Register.
   4 If the instruction requires memory access, determine the memory address, and fetch the operand from memory into a CPU register, or send the operand from a CPU register to memory.
   2 Increment the Instruction Pointer to point to next instruction.
   5 Execute the instruction.
   1 Fetch the instruction at the address in the Instruction Pointer into the Instruction Register.
   6 Repeat from step 1.

5. Consider the virtual machine levels in the diagram at the right. At each level (except 0 and 5), an interpreter accepts an instruction from the level above, converts the instruction to its own language, and passes the resulting instructions to the level below. Note that Level-0 has no interpreter; the instructions from the Micro-architecture level are sent directly to the hardware.



   Suppose that the interpreters at each level (levels 1 - 4) generate *n* instructions in order to represent one instruction from the level above. Suppose also that each Level-0 instruction executes in *c* nanoseconds.
   a. How long does it take to execute a Level-3 instruction?
      cn^2 ns. **Going from level-3 to level-2 creates n instructions. For each of those n instructions, going from level-2 to level-1 creates n instructions, so there will be n^2 micro-instructions, each of which requires c nano-seconds to execute.**
   b. How long does it take to execute a Level-5 instruction? **cn^4** ns.