Architecture: DE10-Nano based RL Emulator

USER interface + LEDs

RAM
1 GB

MICRO
SD-card

Serial
I/O
Debug
console

Internet

ARM Cortex-A9 CPU

Interface , RL I/O bus , 12 differential signals

Command
Sequencer

PORT #2

**Dual Ported RAM(DPR)
5760 words = 1 RL track**

PORT #1

MFM
DECODER

Data-Sequencer
+
Clock Manager
+
Sector-Puls-
generator

MFM
ENCODER