

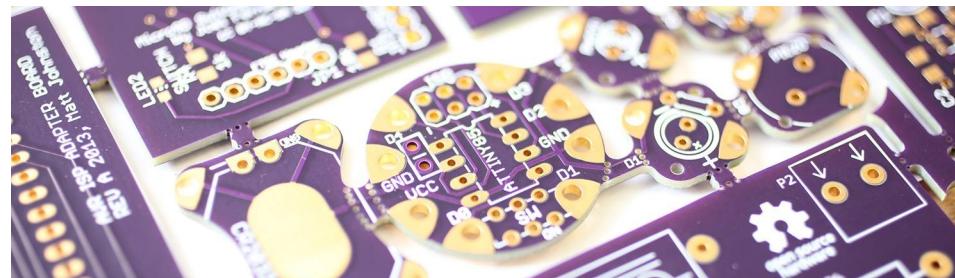
Slides: <https://github.com/pdp7/talks/blob/master/lug-riscv.pdf>

# Linux on RISC-V

*Chicago GNU/Linux User Group (2020-01-25)*



**Drew Fustini**  
**OSH Park**  
[drew@oshpark.com](mailto:drew@oshpark.com)  
[@oshpark / @pdp7](https://twitter.com/@oshpark)



- Open Source Hardware designer at OSH Park
  - PCB manufacturing service in the USA
  - [drew@oshpark.com](mailto:drew@oshpark.com) / Twitter: [@oshpark](https://twitter.com/@oshpark)
- Volunteer Member of Board of Directors of BeagleBoard.org Foundation
  - [drew@beagleboard.org](mailto:drew@beagleboard.org)
- Volunteer Member of the Board of Directors of the Open Source Hardware Association (OSHWA)
  - [drew@pdp7.com](mailto:drew@pdp7.com)

Slides: <https://github.com/pdp7/talks/blob/master/lug-riscv.pdf>



*Section:*  
Open Source FPGA tools

# Open Source and FPGAs

- Hackspace Magazine column about how open source FPGA tools developed by [Claire Wolf \(oe1cxw\)](#), [David Shah](#) and others have made FPGAs more accessible than ever before to makers and hackers:
  - [hackspace.raspberrypi.org/issues/26/](https://hackspace.raspberrypi.org/issues/26/)

MAKE | BUILD | HACK | CREATE **132 PAGES** OF MAKING

# HackSpace

TECHNOLOGY IN YOUR HANDS

hsmag.cc | January 2020 | Issue #26

WHAT 3D PRINTER?

Find the ultimate replicator for 2020

CIRCUIT PYTHON

SOLDERING WITH GAS

PICKING AN IMPACT DRIVER

SEWING MACHINES

Building a kiln

Melting glass with a Raspberry Pi

Drew Fustini

@pdpf

Drew Fustini is a hardware designer and embedded Linux developer. He is the Vice President of the Open Source Hardware Association, and a board member of the BeagleBoard Foundation. Drew designs circuit boards for OSH Park, a PCB manufacturing service, and maintains the Adafruit BeagleBone Python library.

FPGA

FPGAs have been the talk of the town at many of this year's hacker conferences. But what exactly is an FPGA, and why are they so hot right now?

FPGA stands for Field Programmable Gate Array, a digital logic chip that can be programmed to reconfigure the internal hardware. An FPGA does not run software – it physically changes the configuration of its gate arrays to adapt to the task at hand. Is an FPGA an incredibly versatile tool? Need 25 PWM pins for a project? No problem. Want to replicate the functionality of a vintage CPU? Your FPGA has you covered. Not only is an FPGA versatile, but it is also better at handling timing-critical tasks than a microcontroller. You can filter high-speed sensor data before it's read by your processor, or offload repetitive tasks like debouncing buttons from the burden on your microcontroller.

FPGAs are hot right now but they're not a new technology – they've been used in industry for decades

The Lattice ECP5 FPGA is capable of more advanced features than the iCE40, and it's easier to get started with too, thanks to Project Trellis led by David Shah. This enabled the ECP5-powered Supercon badge to have cool features like HDMI video, while still being open for anyone to hack on without requiring proprietary tools.

FPGAs are a fascinating technology with lots of awesome applications. If you want to find out more, start off by reading Luke Valenty's *The Hobbyists Guide to FPGAs on Hackaday.io*. ([hsmag.cc/GOAQnR](https://hsmag.cc/GOAQnR)), and watch Tim Ansell's Supercon talk to learn about the exciting future of open-source FPGA tools ([hsmag.cc/kY5IPD](https://hsmag.cc/kY5IPD)). □

The rise of the FPGA

Reconfigure your chips to suit your project

This opened the door for low-cost, open hardware boards such as mystorm Blackice, TinyFPGA, iCEBreaker, and Fomu, which are great tools for teaching workshops and building projects.

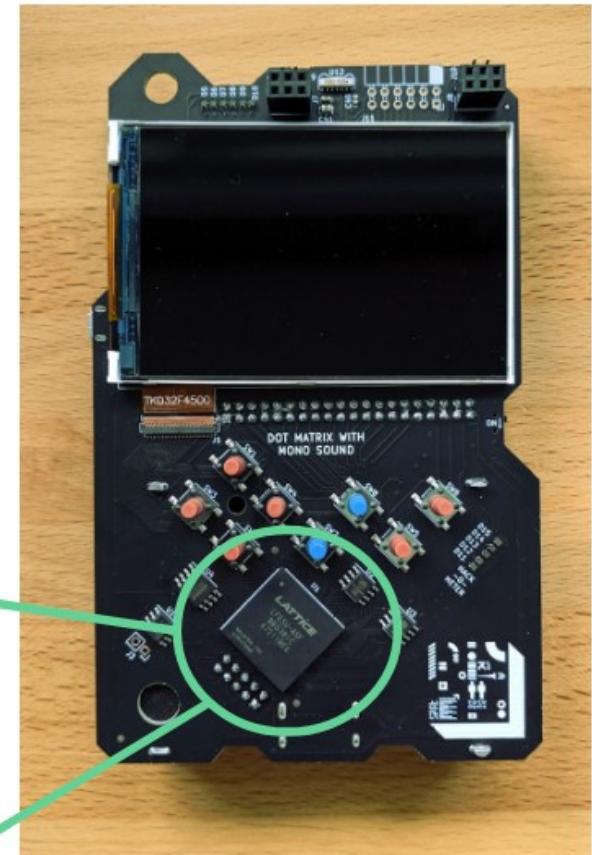
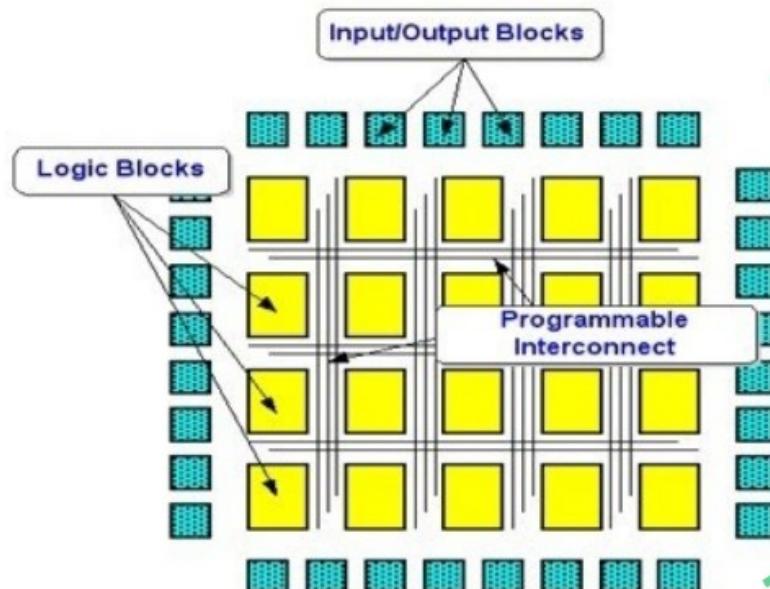
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- Keynote at Hackday Supercon 2019 by Dr. Megan Wachs of SiFive
- **“RISC-V and FPGAs: Open Source Hardware Hacking”**
  - [https://www.youtube.com/watch?v=vCG5\\_nxm2G4](https://www.youtube.com/watch?v=vCG5_nxm2G4)

# Where do FPGAs Come In?

- Field Programmable Gate Array
- Change a chip's HARDWARE in a few minutes
- Make it act like a new chip!



# Open Source and FPGAs

- Open Source toolchains for FPGAs!
  - Project IceStorm for Lattice iCE40
    - “A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs”  
by [Claire Wolf \(oe1cxw\)](#) at 32c3

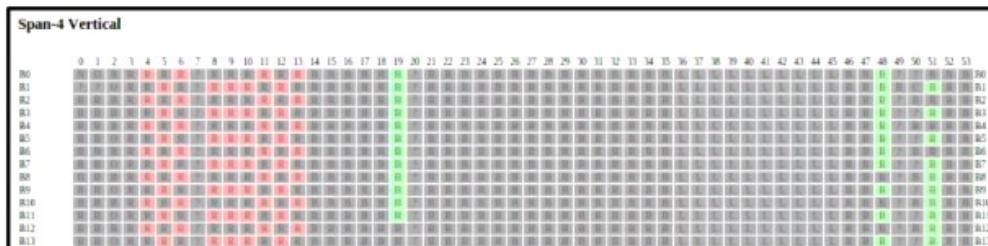


## A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs



by [Clifford](#)

Some screenshots from IceStrom Docs:



(2 17)	(3 17)	(4 17)	(5 17)	(6 17)
LOGIC Tile (2 16)	RAMT Tile (3 16)	LOGIC Tile (4 16)	LOGIC Tile (5 16)	LOGIC Tile (6 16)
LOGIC Tile (2 15)	RAMB Tile (3 15)	LOGIC Tile (4 15)	LOGIC Tile (5 15)	LOGIC Tile (6 15)
LOGIC Tile (2 14)	RAMT Tile (3 14)	LOGIC Tile (4 14)	LOGIC Tile (5 14)	LOGIC Tile (6 14)

### Configuration Bitmap

A LOGIC Tile has 64x config bits in 16 groups of 54 bits each:

B0[53:0], B1[53:0], B2[53:0], B3[53:0], B4[53:0], B5[53:0], B6[53:0], B7[53:0],  
B8[53:0], B9[53:0], B10[53:0], B11[53:0], B12[53:0], B13[53:0], B14[53:0], B15[53:0]



# Open Source and FPGAs

- Open Source toolchains for FPGAs!
  - Project Trellis for Lattice ECP5
  - “Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5”
    - David Shah (@fpga\_dave)
    - [youtube.com/watch?v=0se7kNes3EU](https://youtube.com/watch?v=0se7kNes3EU)

Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5

## **Project Trellis & nextpnr**

FOSS Tools for ECP5 FPGAs

David Shah  
@fpga\_dave

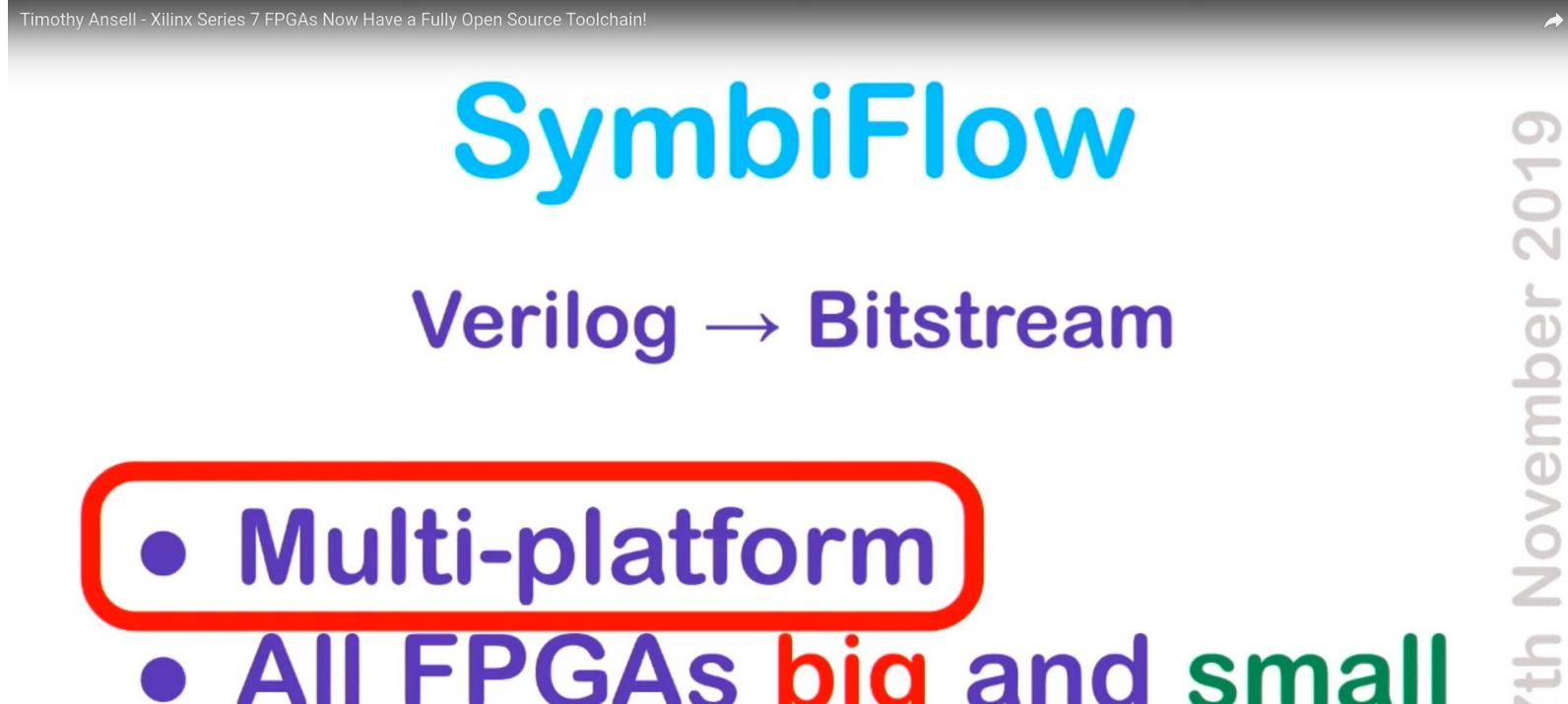
Symbiotic EDA || Imperial College London

FOSDEM 19  
org



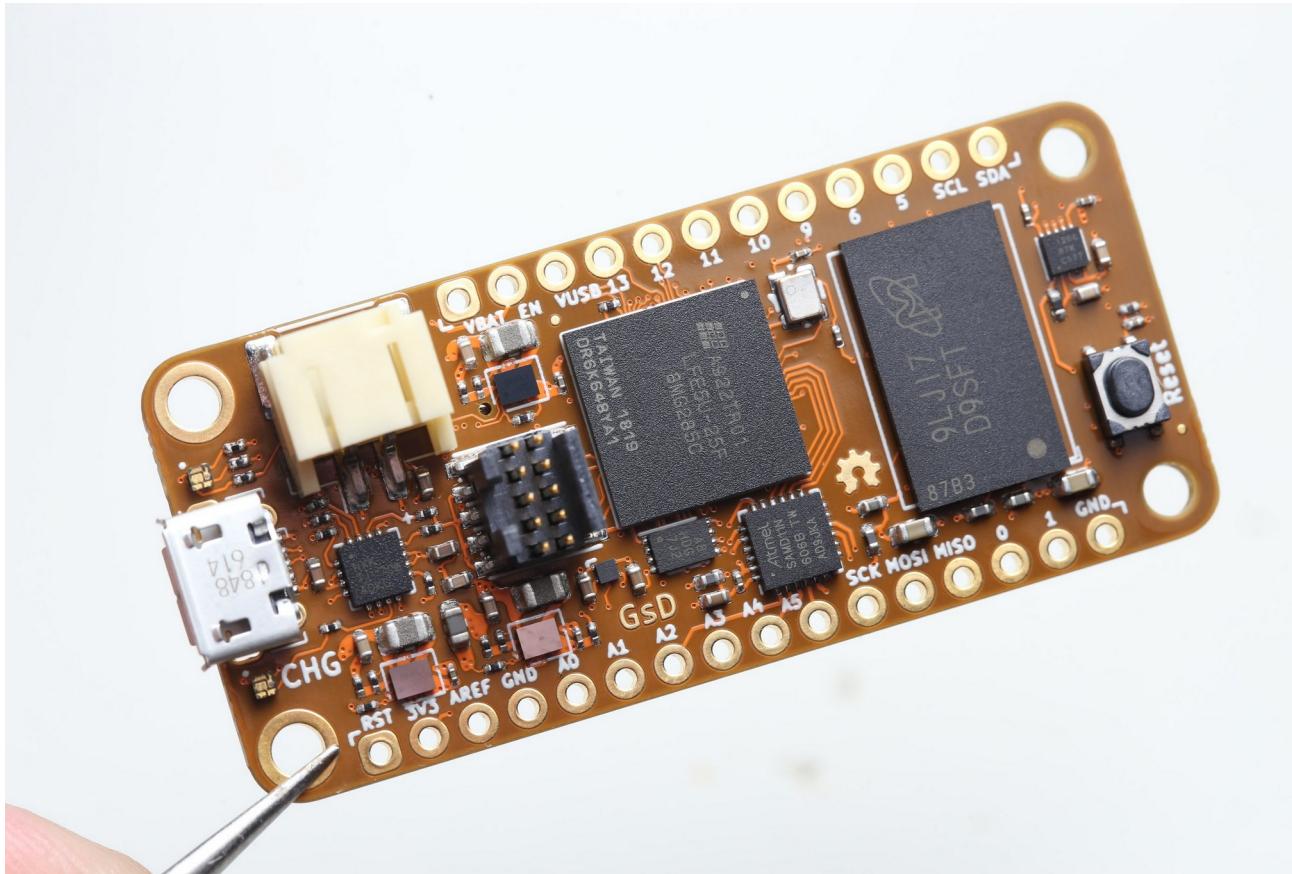
# Open Source and FPGAs

- Open Source toolchains for FPGAs!
  - Project X-Ray and SymbiFlow for Xilinx Series 7
  - [Timothy 'mithro' Ansell](#): “Xilinx Series 7 FPGAs Now Have a Fully Open Source Toolchain!” (*almost*)
    - [youtube.com/watch?v=EHePto95qoE](https://www.youtube.com/watch?v=EHePto95qoE)



# Open Source and FPGAs

- Open Source Hardware boards with Lattice ECP5 FPGA with open RISC-V “soft” CPU:
    - Orange Crab by Greg Davill
      - <https://github.com/gregdavill/OrangeCrab>





Greg @ #36c3  
@GregDavill



Replying to @mithro @pdp7 and 2 others

Done. 😊

```
File Edit View Terminal Tabs Help
SRAM:      4KB
L2:        8KB
MAIN-RAM: 131072KB

----- Initialization -----
Initializing SDRAM...
SDRAM now under software control
Read leveling:
m0, b0: |11100000| delays: 01+-01
best: m0, b0 delays: 01+-01
m1, b0: |11100000| delays: 01+-01
best: m1, b0 delays: 01+-01
SDRAM now under hardware control
Memtest OK

----- Boot -----
Booting from serial...
Press Q or ESC to abort boot completely.
sL5DdSMmkekro
[LXTERM] Received firmware download request from the device.
[LXTERM] Uploading buildroot/Image to 0xc0000000 (4545524 bytes)...
[LXTERM] Upload complete (85.6KB/s).
[LXTERM] Uploading buildroot/rootfs.cpio to 0xc0800000 (8029184 bytes)...
[ 0:43 ] 1.2K views => | 98%
```



# Open Source and FPGAs

- Radiona.org ULX3S
    - <https://www.crowdsupply.com/radiona/ulx3s>

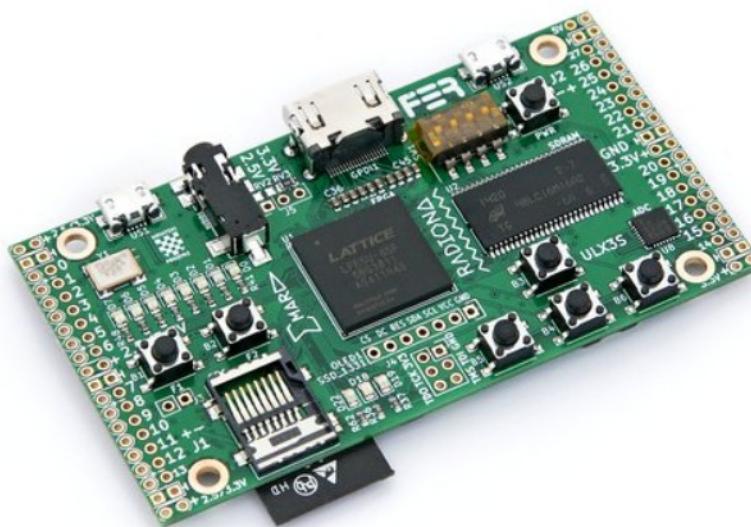
ULX3S

# A powerful, open hardware ECP5 FPGA dev board

This project is coming soon. Sign up to receive updates and be notified when this project launches.

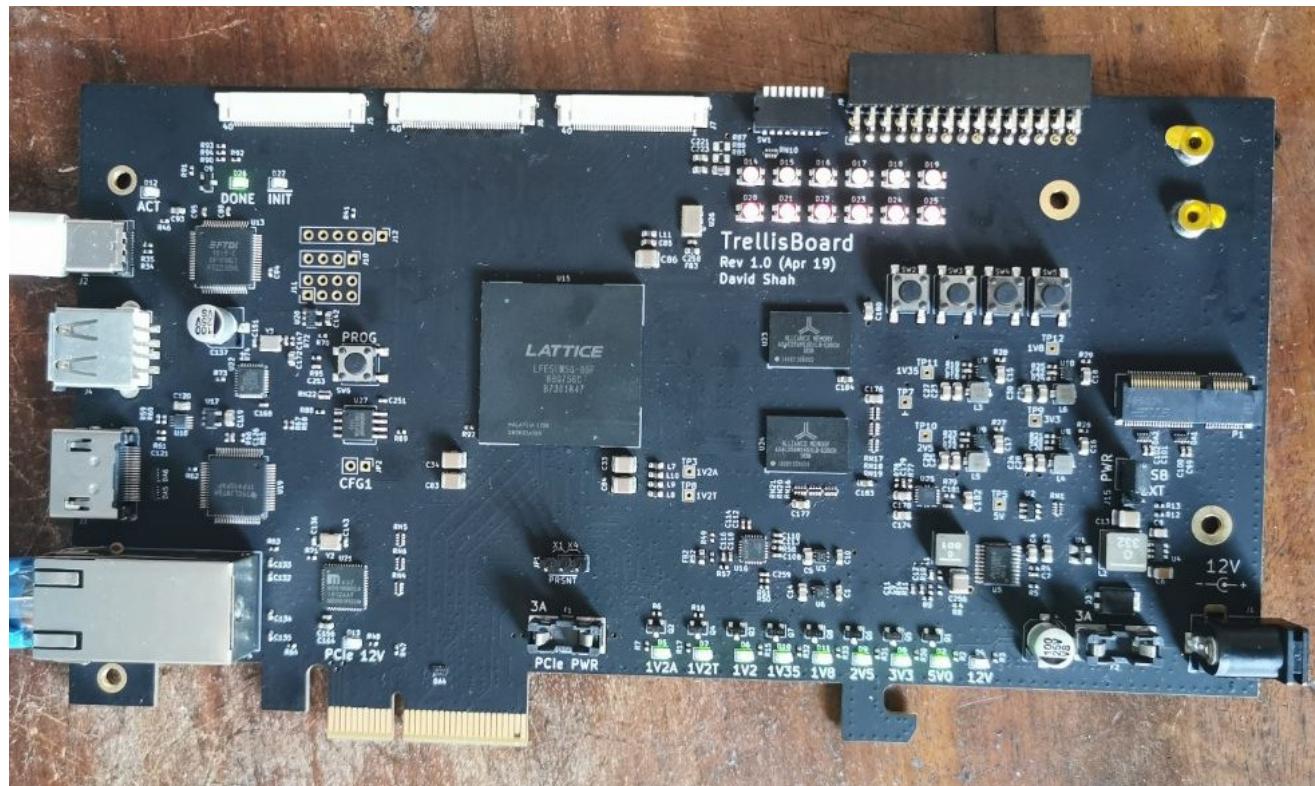
me@example.com

[Subscribe](#)



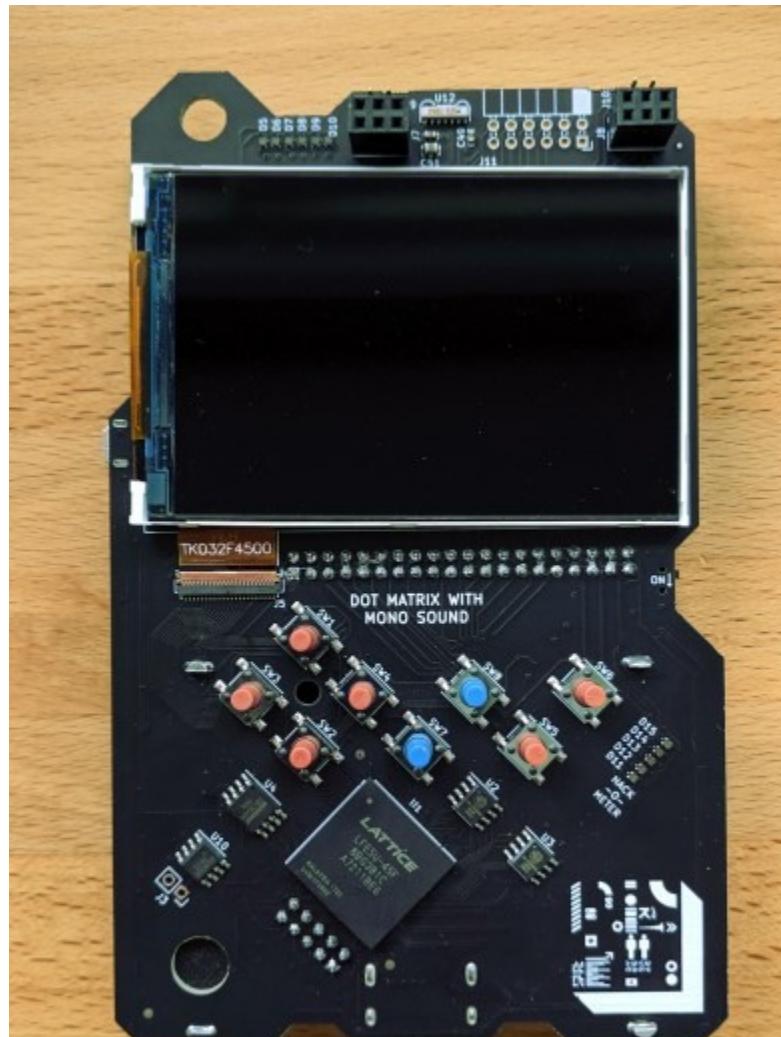
# Open Source and FPGAs

- Open Source Hardware boards with Lattice ECP5 FPGA with open RISC-V “soft” CPU:
  - David Shah's Trellis board (Ultimate ECP5 Board)
  - <https://github.com/daveshah1/TrellisBoard>



# Hackaday 2019 Supercon badge

- RISC-V “soft” core on ECP5 FPGA
- Gigantic FPGA In A Game Boy Form Factor

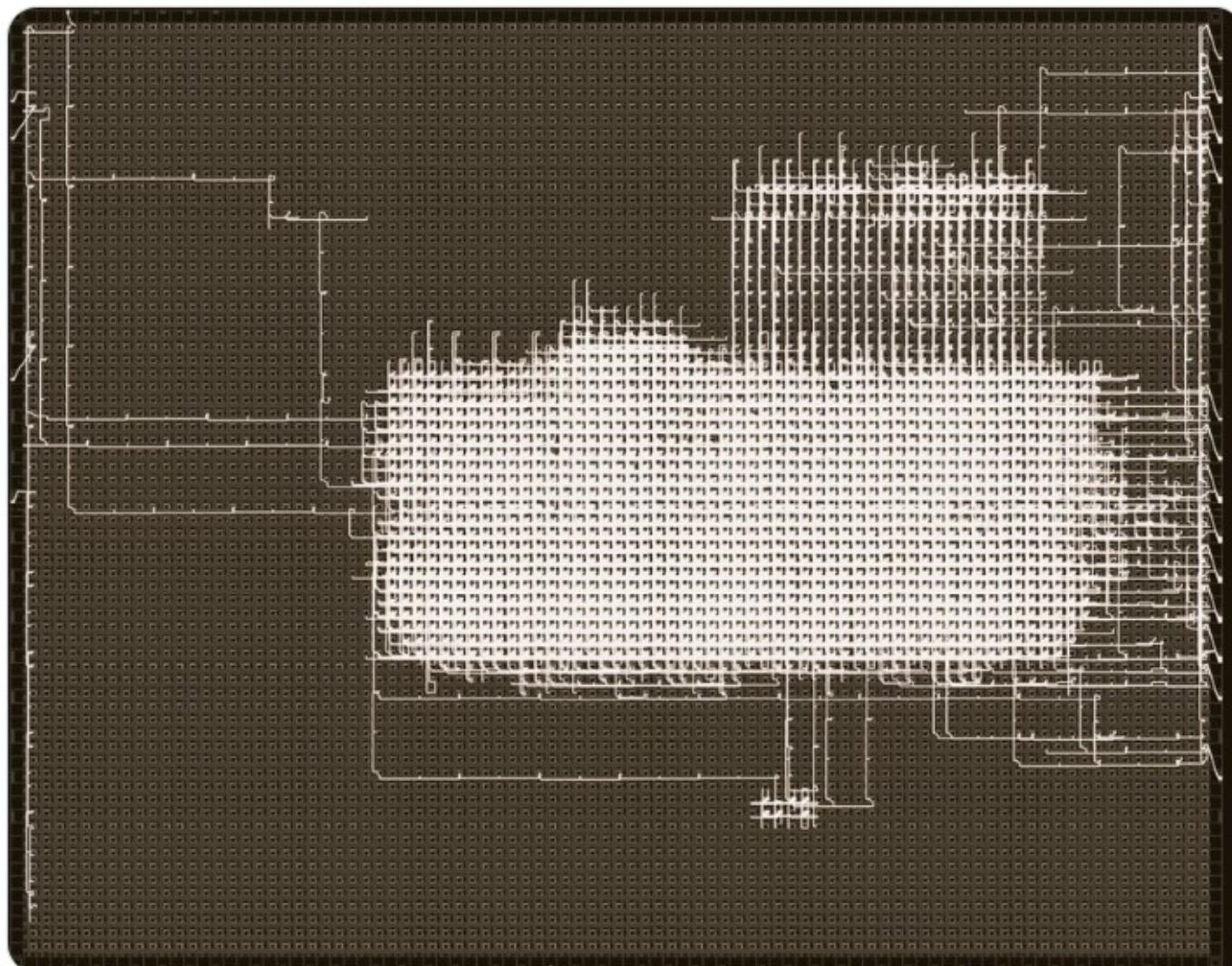


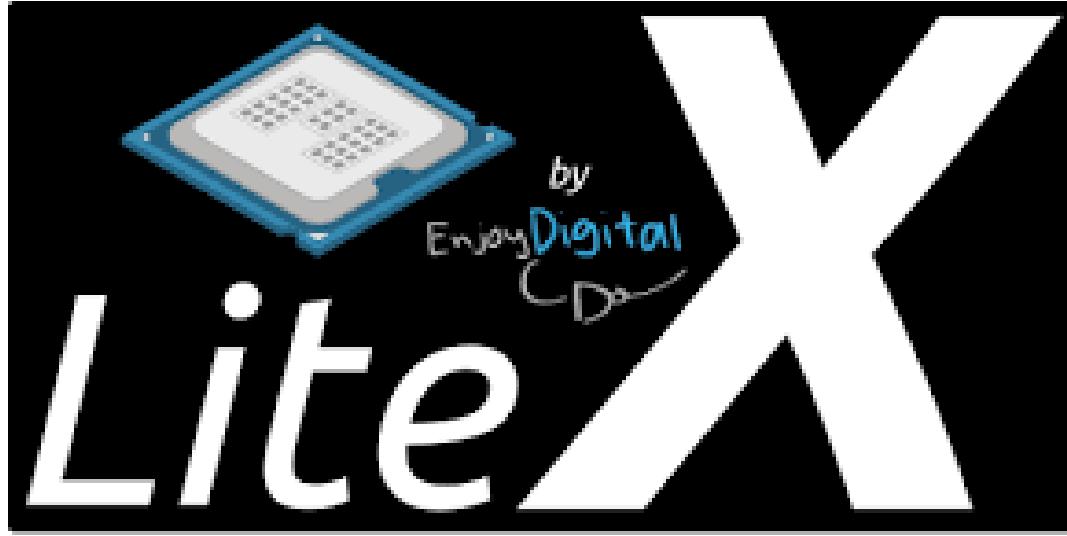


OSS FPGA & EDA tools  
@ico\_TC



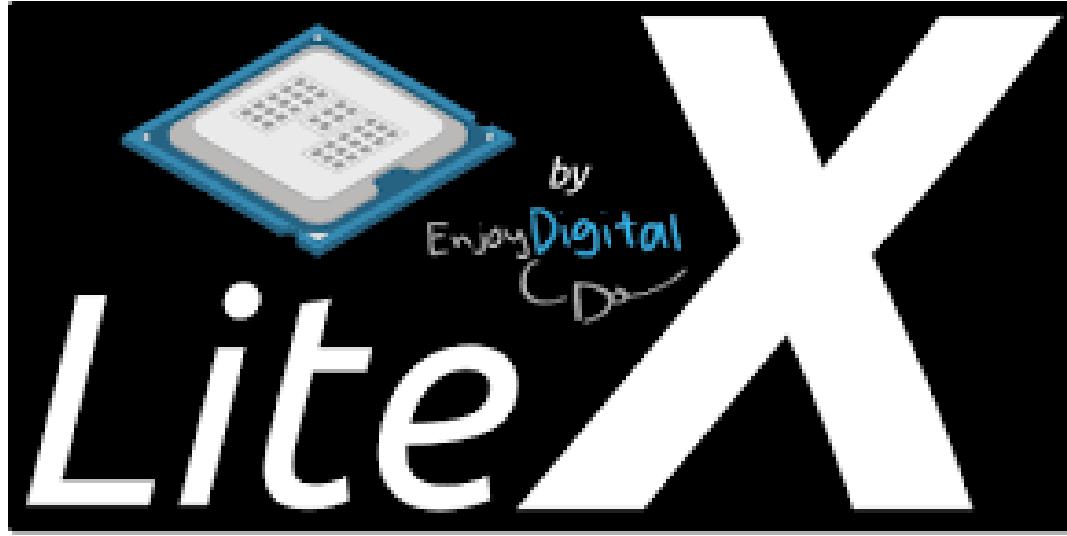
This is how a Linux capable core looks like on an  
FPGA. [#nextpnratwork](#)





Build your hardware, easily!

- LiteX is a FPGA design/SoC builder that can be used to build cores, create SoCs and full FPGA designs.
- LiteX is based on Migen and provides specific building/ debugging tools for a higher level of abstraction and compatibility with the LiteX core ecosystem.
- Think of Migen as a toolbox to create FPGA designs in Python and LiteX as a SoC builder to create/develop/debug FPGA SoCs in Python
- <https://github.com/enjoy-digital/litex>

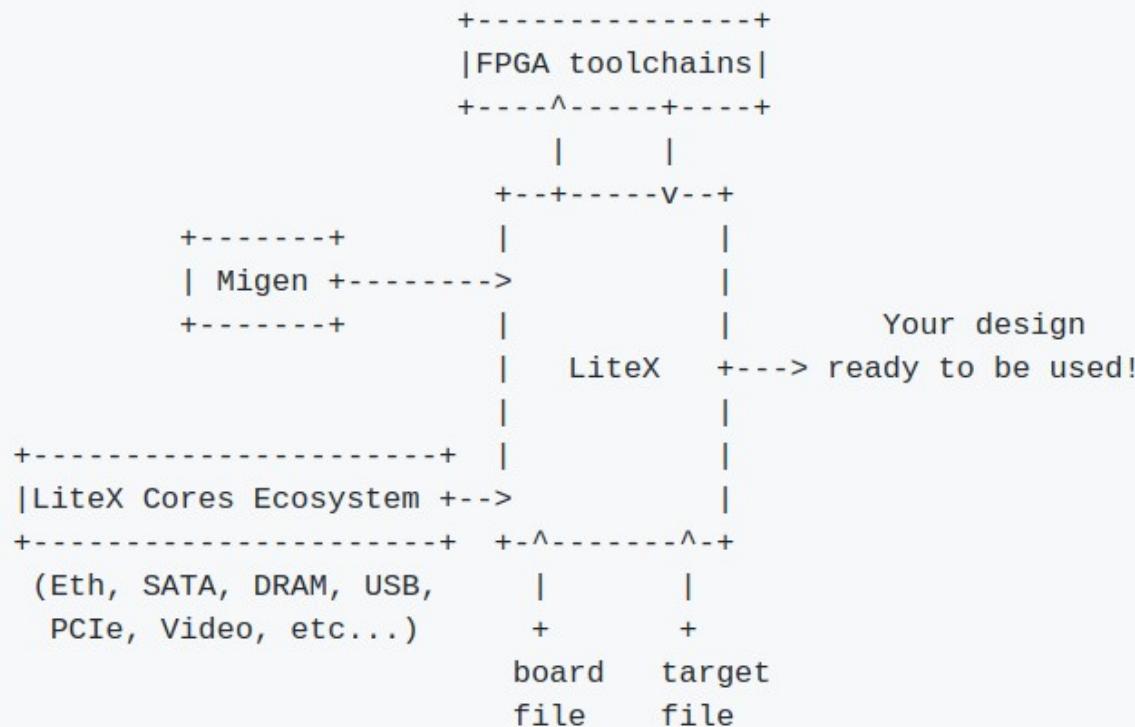


Build your hardware, easily!

- Bunnie:  
LiteX vs. Vivado: First Impressions

<https://www.bunniestudios.com/blog/?p=5018>

# Typical LiteX design flow:



LiteX already supports various softcores CPUs: LM32, Mor1kx, PicoRV32, VexRiscv and is compatible with the LiteX's Cores Ecosystem:

Name	Build Status	Description
LiteDRAM	<span>build</span> <span>passing</span>	DRAM
LiteEth	<span>build</span> <span>passing</span>	Ethernet
LitePCIe	<span>build</span> <span>passing</span>	PCIe
LiteSATA	<span>build</span> <span>passing</span>	SATA

# Linux on LiteX-VexRiscv

- Linux with VexRiscv CPU, a 32-bits Linux Capable RISC-V CPU written in Spinal HDL
- SoC around the VexRiscv CPU is created using LiteX as the SoC builder and LiteX's cores written in Migen Python DSL (LiteDRAM, LiteEth, LiteSDCard)
- [github.com/litex-hub/linux-on-litex-vexriscv](https://github.com/litex-hub/linux-on-litex-vexriscv)

```
michael@reactor: ~/projects/litex/lin...
```

```
michael@reactor: ~/projects/litex/lin...
```

```
Welcome to Buildroot  
buildroot login: root
```



```
32-bit VexRiscv CPU with MMU integrated in a LiteX SoC
```

```
login[55]: root login on 'console'
```

```
root@buildroot:~# ps
```

PID	USER	COMMAND
1	root	init
2	root	[kthreadd]
3	root	[kworker/0:0-eve]
4	root	[kworker/0:0H]
5	root	[kworker/u2:0-ev]
6	root	[mm_percpu_wq]
7	root	[ksoftirqd/0]
8	root	[kdevtmpfs]
9	root	[oom_reaper]
10	root	[writeback]
11	root	[kcompactd0]
12	root	[kblockd]
13	root	[kworker/0:1]
14	root	[kswapd0]
34	root	/sbin/klogd -n
55	root	-sh
56	root	[kworker/u2:1]
58	root	ps

```
root@buildroot:~# uname -a
```

Slides: <https://github.com/pdp7/talks/blob/master/lug-riscv.pdf>



*Section:*  
Open Source and Chip Design



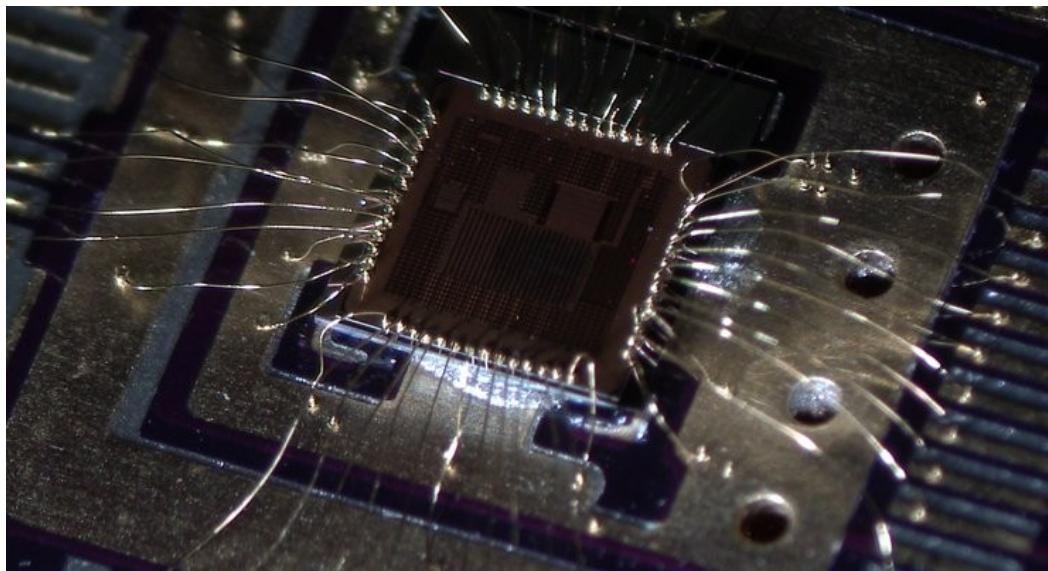
- **RISC-V: Free and Open RISC Instruction Set Arch**
  - “new instruction set architecture (ISA) that was originally designed to support computer architecture research and education and is now set to become a standard open architecture for industry”
  - Video: [Instruction Sets Want To Be Free: A Case for RISC-V](#)
  - Video: [Krste Asanovic presents](#) at RISC-V and Open Source Silicon Event in Munich on March 23, 2017

# *What about open source chips?*



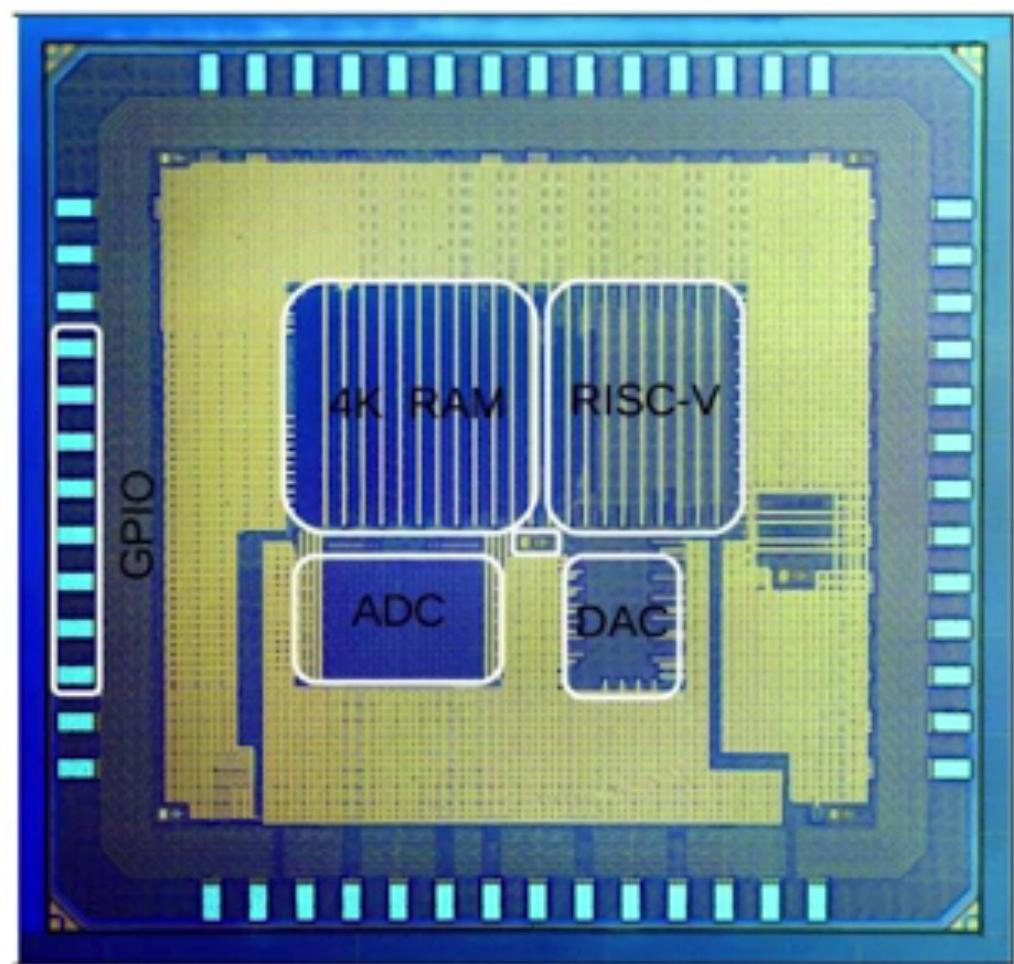
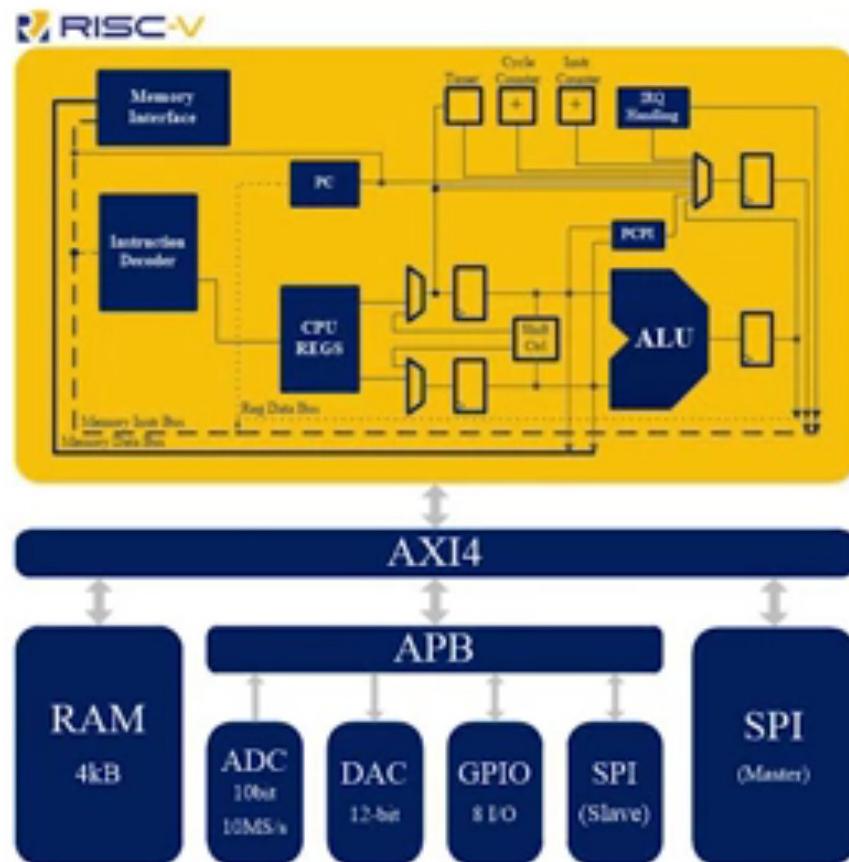
- [OnChip Open-V](#)

“completely free (as in freedom) and open source 32-bit microcontroller based on the RISC-V architecture”



# OnChip Open-V

A 32-bit RISC-V based Microcontroller



# OnChip Open-V

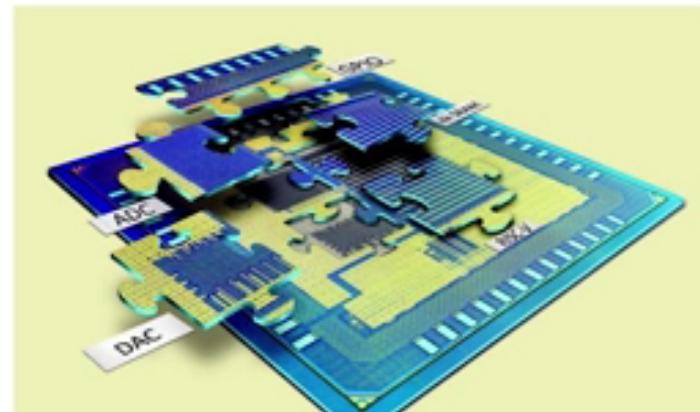


- Crowd Supply update: [A Taste of Chip Design](#)
- Video: [YoPuzzle: mRISC V development platform](#)
- Video: [RISC-V Community needs Peripheral Cores](#)

**Good to have an Open ISA. What about Peripheral?**



- IP vendors have IP based on previous customer. **Hard to get** a glue-and-play that works for your SoC. → \$\$\$
- There are some std, such as PHYs: USB, LPDDR, PCIe, AMBA  
**BUT**  
no for clocking circuitry, biasing, GPIO  
For instance a simple Power-on-Reset can hit your pocket, just because!
- Buses IP are out there but expensive.

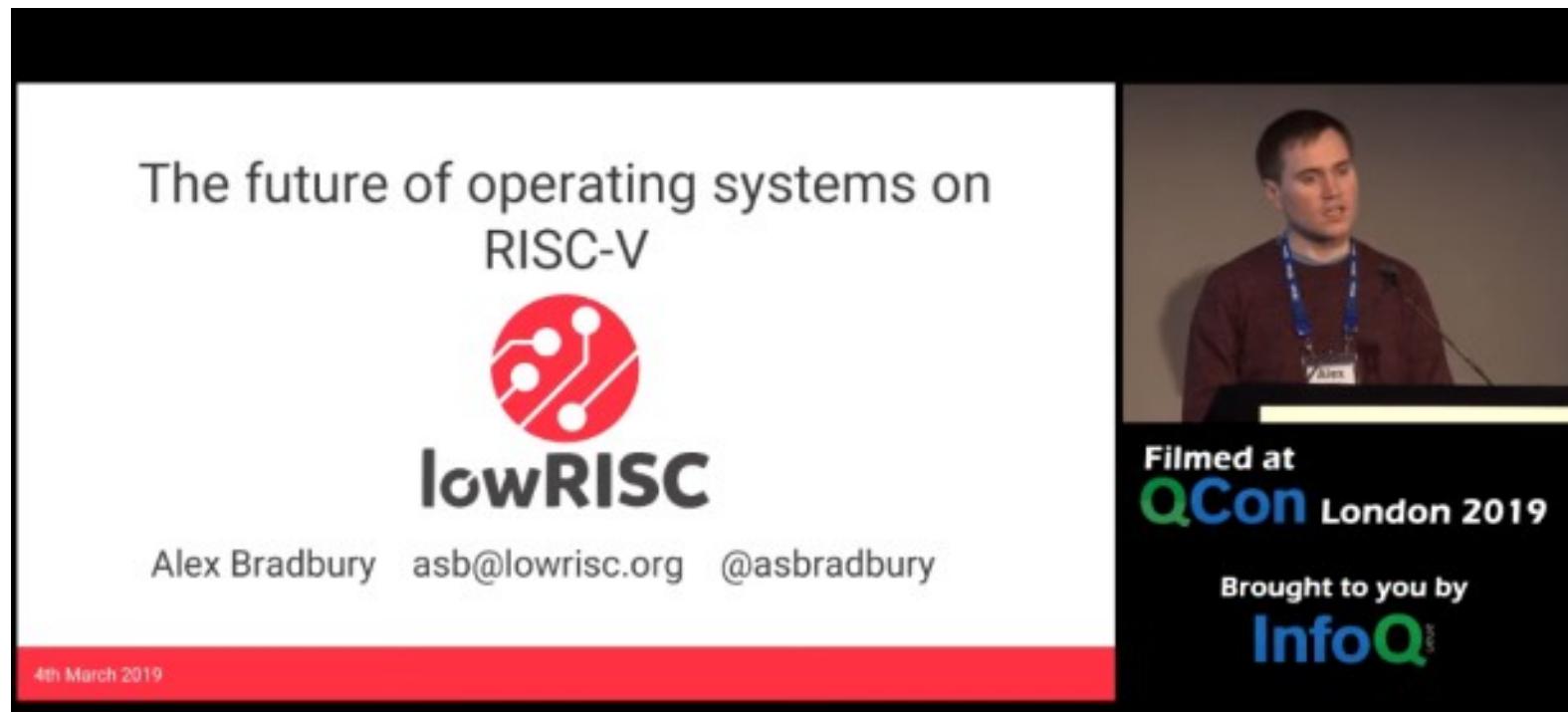


# Open Source chip design

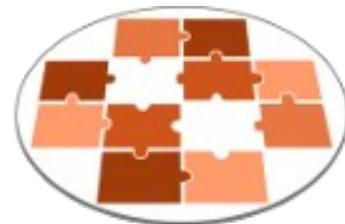


- lowRISC:  
“creating a fully open-sourced, Linux-capable, RISC-V-based SoC, that can be used either directly or as the basis for a custom design”
- Video: Rob Mullins talking about lowRISC  
(RISC-V & Open Source Silicon Event in Munich on March 23, 2017)
- Laura James from lowRISC is here!

- The Future of Operating Systems on RISC-V
  - Alex Bradbury gives an overview of the status and development of RISC-V as it relates to modern operating systems, highlighting major research strands, controversies, and opportunities to get involved.
  - <https://www.youtube.com/watch?v=emnN9p4vhzk>



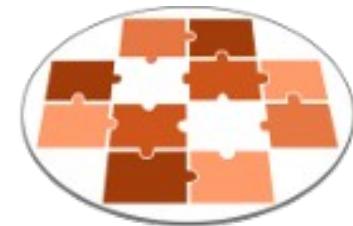
# Open Source chip design



**FOSSi**  
Foundation

- **FOSSi Foundation**
  - The **F**ree and **O**pen **S**ource **S**ilicon **F**oundation
  - “non-profit foundation with the mission to promote and assist free and open digital hardware designs”
  - “FOSSi Foundation operates as an open, inclusive, vendor-independent group.”

# Open Source chip design

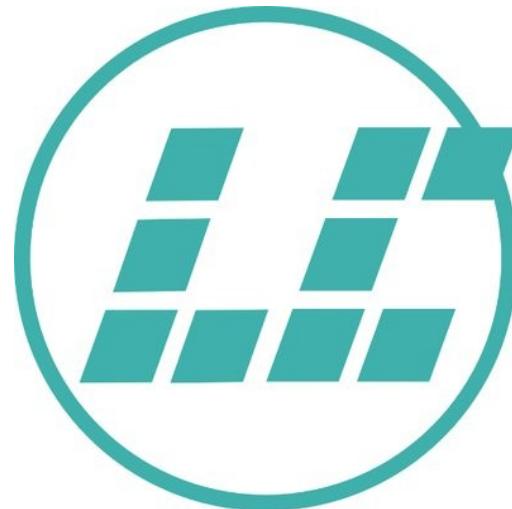


**FOSSi**  
Foundation

- Open Source Silicon Design Ecosystem
  - Talk by FOSSi co-founder Julius Baxter



# Open Source chip design



- **LibreCores**
  - Project of the FOSSi Foundation
  - “**gateway to free and open source digital designs** and other components that you can use and **re-use in your digital designs**”
  - “advances the idea of OpenCores.org”

# Latch-Up Conf 2019 videos



*Latch-Up 2020 will be*

*April 11-12 Cambridge MA, USA, at MIT*

# Week of Open Source Hardware

The video player displays a slide with the following content:

**History**

- March 2011: CERN OHL 1.0
- July 2011: CERN OHL 1.1
- September 2013: CERN OHL 1.2
- 2017: CERN OHL 2, beta 1
- 2019 : CERN OHL 2, beta 2

Below the slide, the video player interface shows:

CERN Open Hardware Licence 2.0  
80 views

Like 3 | Dislike 0 | Share | Save | ...

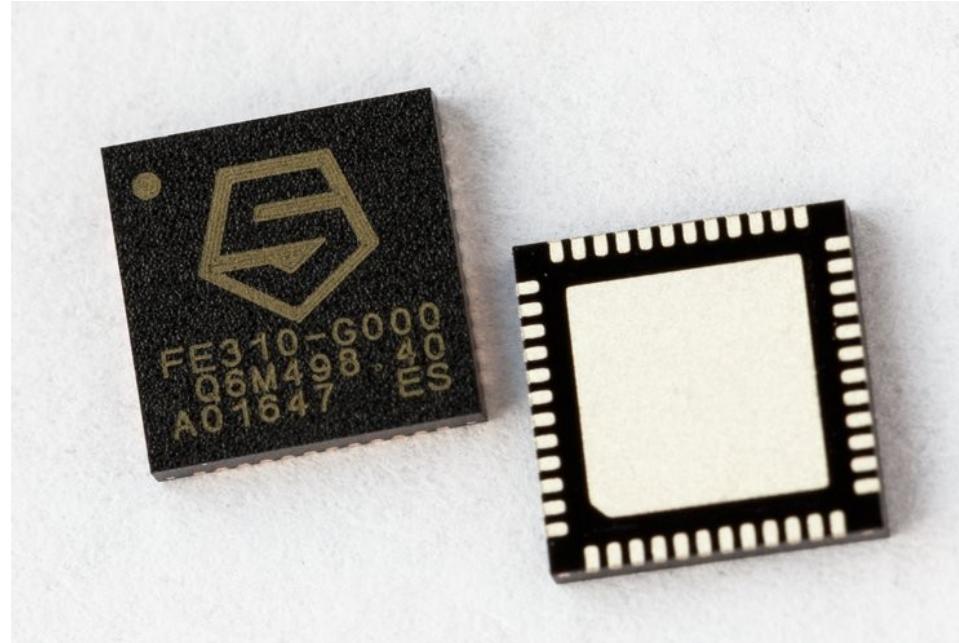


FOSSI Foundation

Published on Jun 20, 2019

SUBSCRIBE 654

# SiFive



- “founded by the creators of the free and open RISC-V architecture as a reaction to the end of conventional transistor scaling and escalating chip design costs”

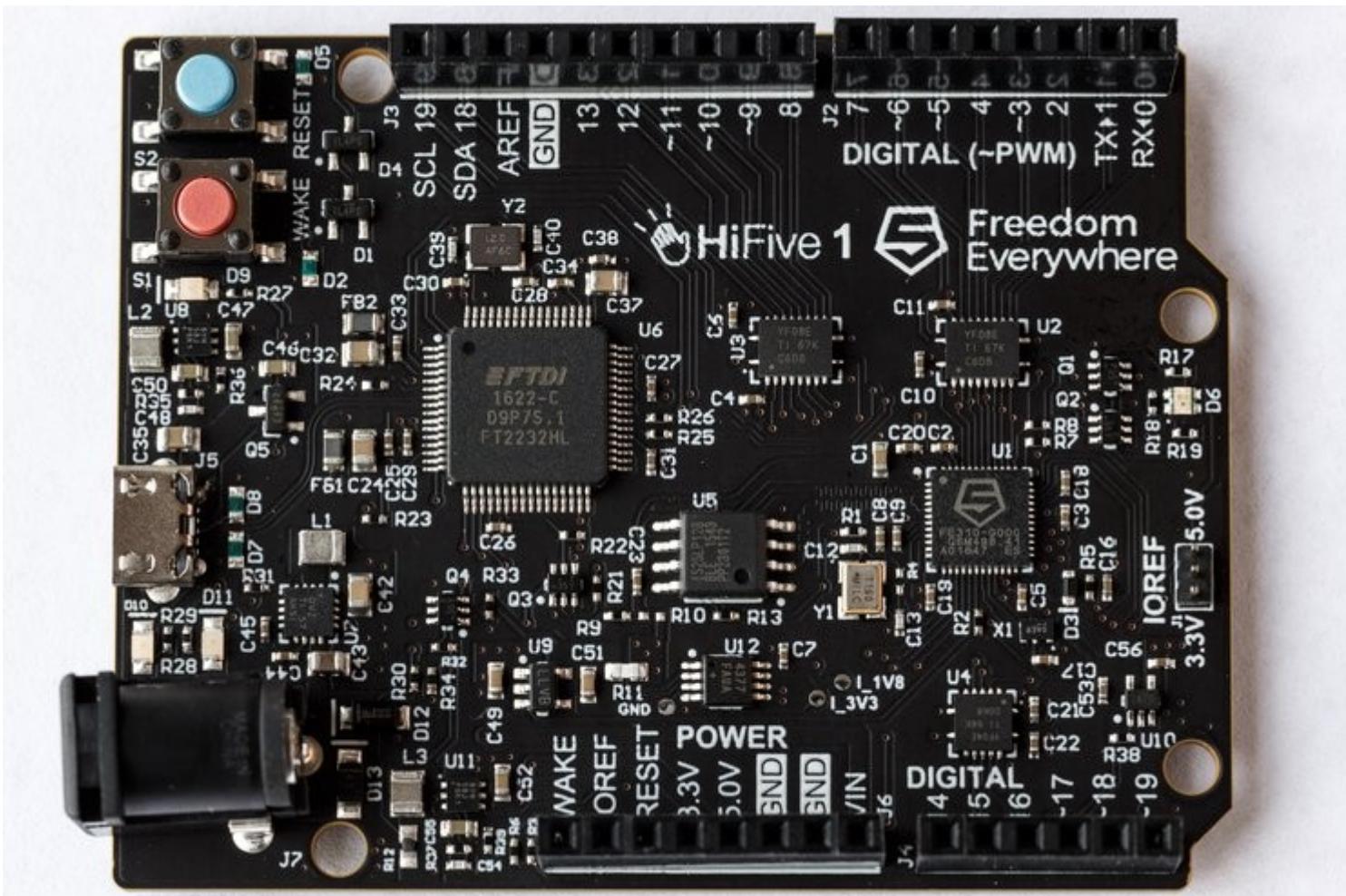
# RISC-V ecosystem

- RISC-V Keynote at Embedded Linux Conf
  - March 12<sup>th</sup>, 2018
  - Yunsup Lee, Co-Founder and CTO, SiFive
  - Designing the Next Billion Chips: How RISC-V is Revolutionizing Hardware



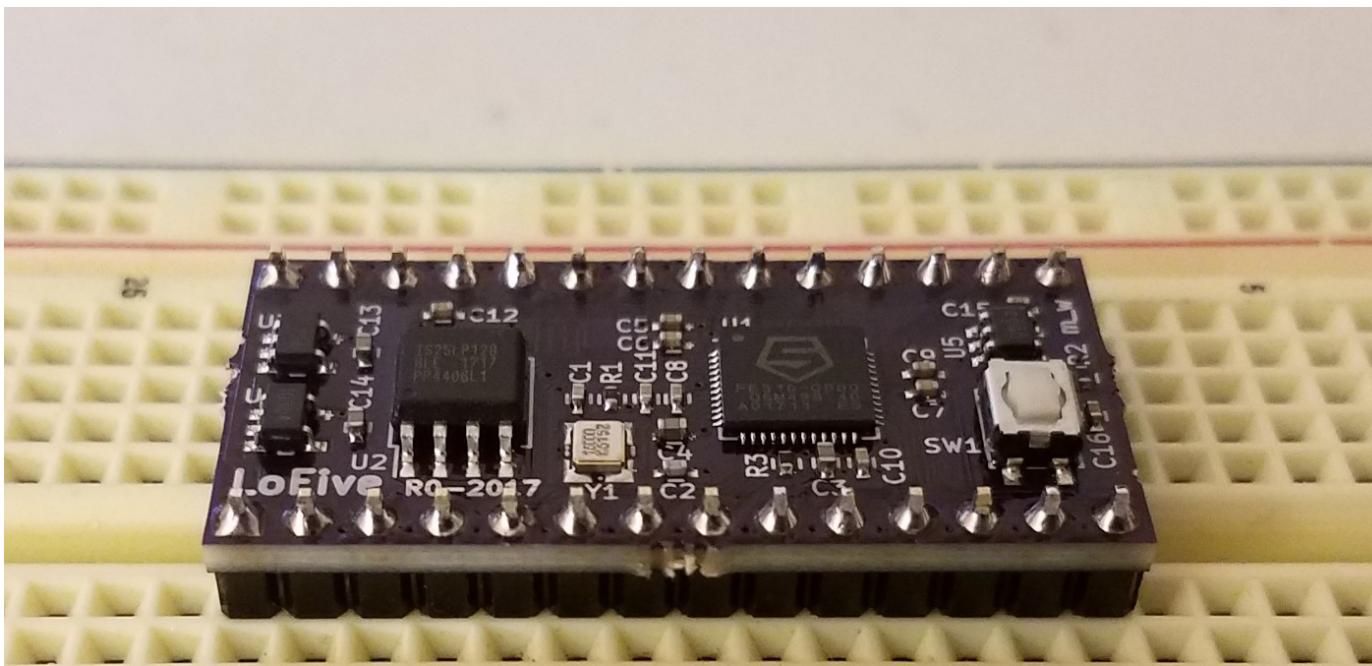
# SiFive FE310 microcontroller

- HiFive1: Arduino-Compatible RISC-V Dev Kit



# SiFive FE310 microcontroller

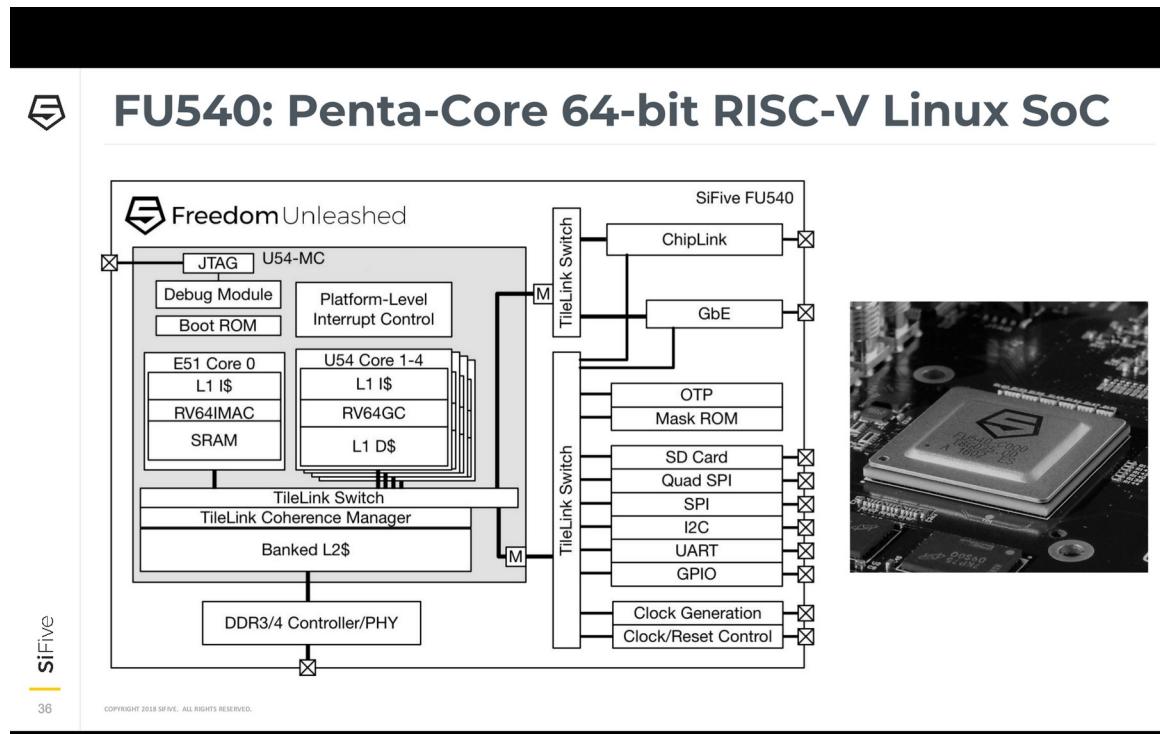
- [LoFive](#) designed by [Michael Welling](#)  
*(QWERTY Embedded Design)*
- Lower cost eval board for SiFive FE310.
- Open Source Hardware design files
- Sold as group buy on [GroupGets](#)



# SiFive: Linux on RISC-V

- FOSDEM 2018 talk

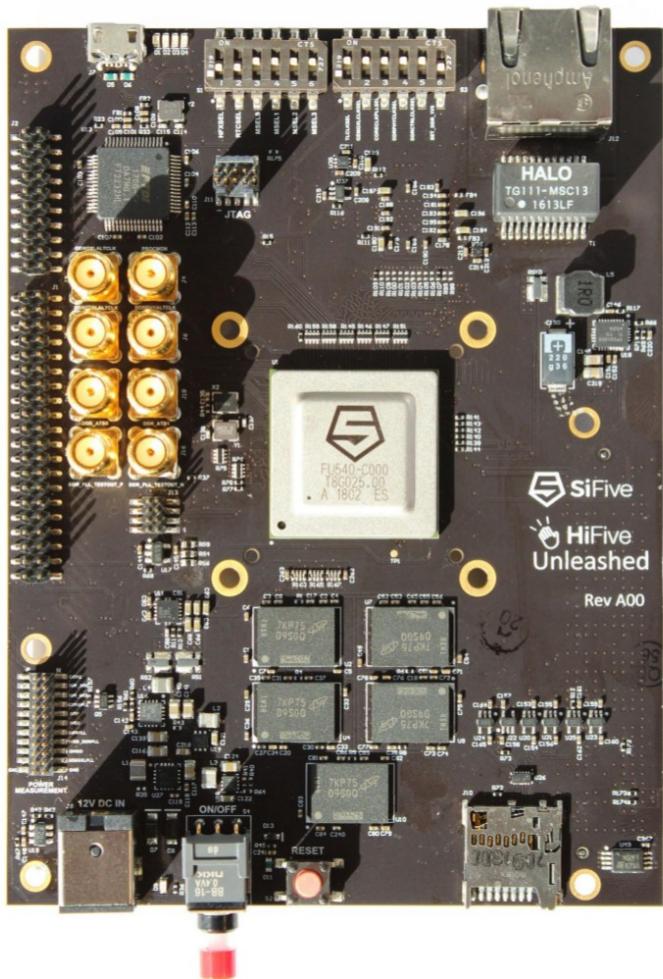
- YouTube: “Igniting the Open Hardware Ecosystem with RISC-V: SiFive's Freedom U500 is the World's First Linux-capable Open Source SoC Platform”
- Interview with Palmer Dabbelt of SiFive



# SiFive: Linux on RISC-V



## HiFive Unleashed



- World's First Multi-Core RISC-V Linux Development Board
  - SiFive FU540-C000 (built in 28nm)
    - 4+1 Multi-Core Coherent Configuration, up to 1.5 GHz
    - 4x U54 RV64GC Application Cores with Sv39 Virtual Memory Support
    - 1x E51 RV64IMAC Management Core
    - Coherent 2MB L2 Cache
    - 64-bit DDR4 with ECC
    - 1x Gigabit Ethernet
  - 8 GB 64-bit DDR4 with ECC
  - Gigabit Ethernet Port
  - 32 MB Quad SPI Flash
  - MicroSD card for removable storage
  - FMC connector for future expansion with add-in cards



# RISC-V NOMMU and M-Mode Linux

Damien Le Moal, Western Digital

Linux Plumbers Conference, September 9<sup>th</sup>, 2019

- PDF: RISC-V NOMMU and M-mode Linux
- <https://www.youtube.com/watch?v=ycG592N9EMA&t=10394>
- jump to 2h 53m
- Many RISC-V Improvements Ready For Linux 5.5: M-Mode, SECCOMP, Other Features

- HOT CHIPS 2019: Linux RISC-V tutorial
- <https://youtu.be/nPXdbm9lc3A?t=6139>
- 1 hour 42 minutes
- Overview of RISC-V SW Ecosystem Bunnaroath Sou, SiFive



# Getting Started

- Freedom Studio from [SiFive.com](https://sifive.com)

- or Freedom E SDK & Metal

- RISC-V on Qemu

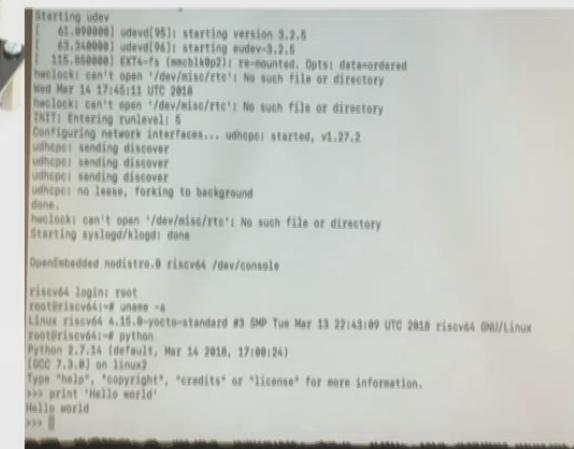
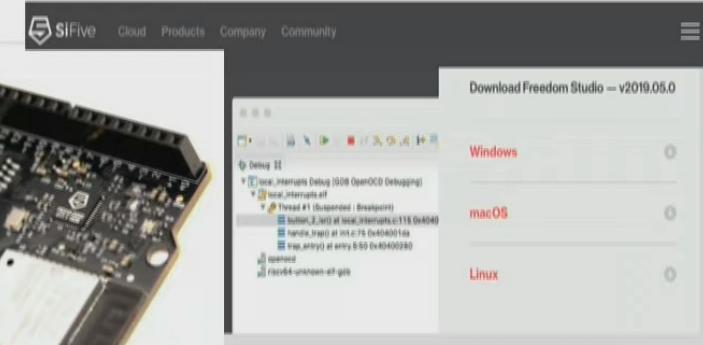
- <https://risc-v-getting-started-guide.readthedocs.io/en/latest/index.html>

- [sw-dev@groups.riscv.org](mailto:sw-dev@groups.riscv.org)

To download and build QEMU from git:

- #riscv on freenode

```
git clone https://git.qemu.org/git/qemu.git
cd qemu
git submodule init
./configure --target-list=riscv64-softmmu
./configure
make
```





# Fedora on RISC-V

Through the works of David Abdurachmanov

- ~20% of Fedora packages built for RISC-V
- Pre-build images available for Qemu and HiFive Unleashed
  - Build farm running, producing nightly images
- No signed RPM yet
- No images for Fedora Workstation/Server

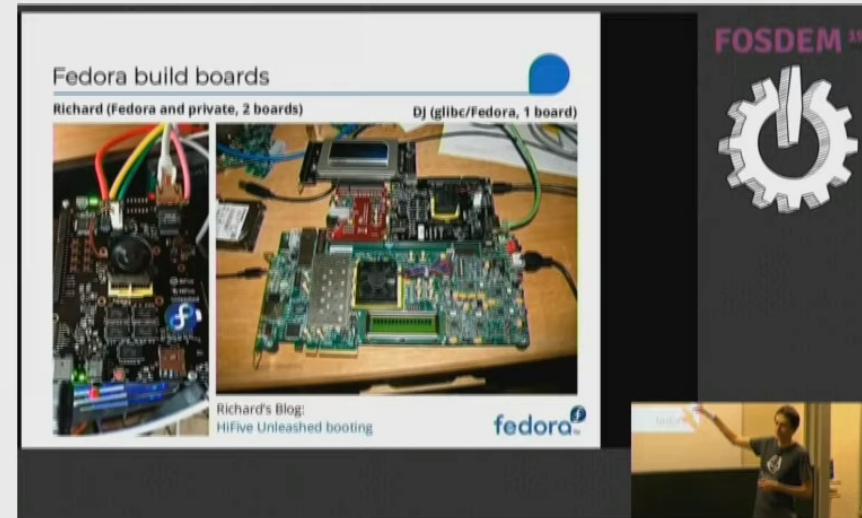


Want to know more/get involve, see

- <https://fedoraproject.org/wiki/Architectures/RISC-V>

Interest to try it out,

- Self Hosting images available
- <https://fedoraproject.org/wiki/Architectures/RISC-V/Installing>





# RISC-V Linux Early Boot

**Linux boots expects the system to be in the following state**

- a0 contains a unique per-hart id
- a1 contains a pointer to device tree, as a binary flattened device tree (DTB)
- Memory is identity mapped
- The kernel's ELF image has been loaded correctly
- Handle impedance mismatch between RISC-V spec and what Linux expects
- Perform "hart lottery," which is a very short AMO-based sequence that picks the first hart to boot, while the rest spin, until they can proceed

**Proceed with a fairly standard Linux early boot process:**

- A linear mapping of all physical memory is set up, with PAGE\_OFFSET as the offset
- Paging structures are initialized and then used (BBL boots with paging enabled)
- The C runtime is set up, which includes the stack and global pointers
- A spin-only trap vector is set up that catches any errors early in the boot process
- `start_kernel` is called to enter the standard Linux boot process

# Coming in 2020?

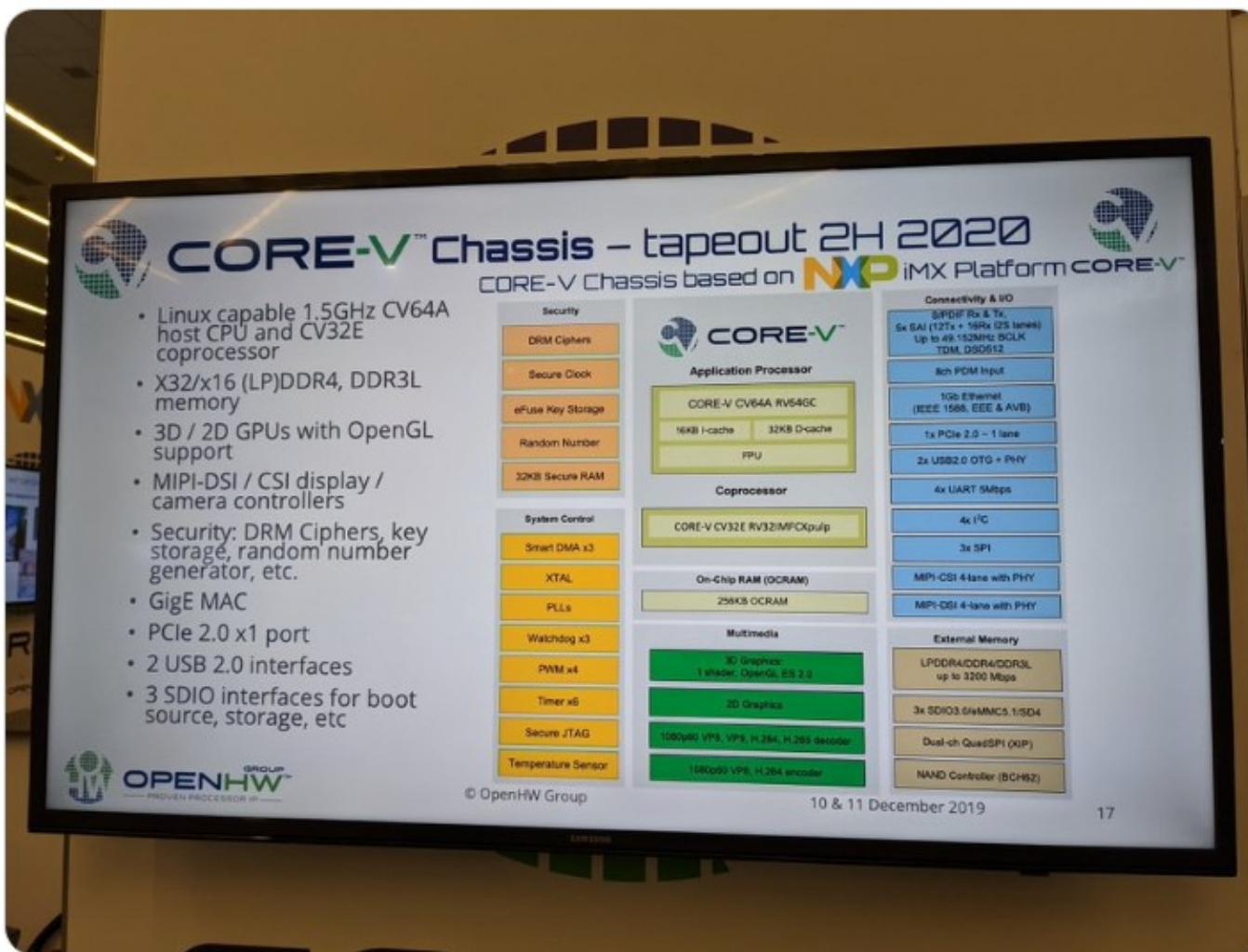
- OpenHW Group Unveils CORE-V Chassis SoC Project, Building on PULP Project IP
  - <https://abopen.com/news/openhw-group-unveils-core-v-chassis-soc-project-building-on-pulp-project-ip/>
  - “The design in question is based on the NXP i.MX platform, and features a CV64A 64-bit core running at up to 1.5GHz and built on the RV64GC RISC-V core IP from the PULP Platform; this is then partnered with a lower-power VC32E coprocessor, based on the PULP Platform’s RV32IMFCXpulp IP.”



Karim Yaghmour  
@karimyaghmour

▼

Spotted at RISC V summit: an iMX chip where the ARM core was ripped out and replaced with a RISC V/PULP - just wow



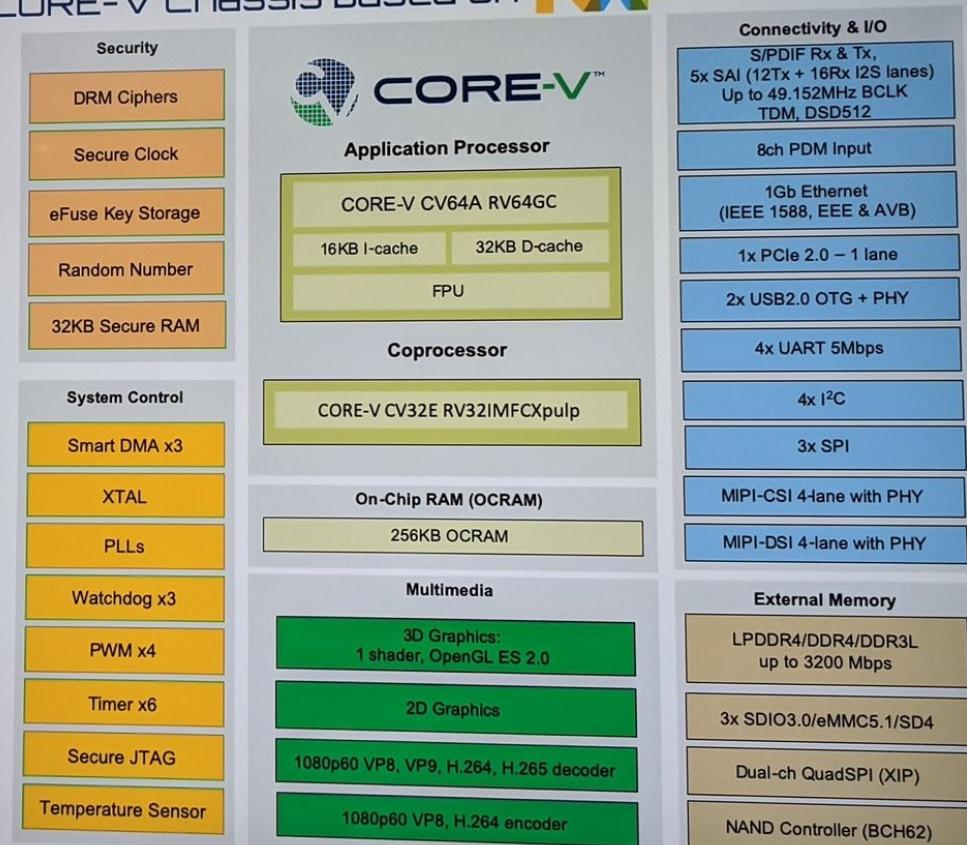


# CORE-V™ chassis – tapeout 2H 2020



CORE-V Chassis based on **NXP** iMX Platform **CORE-V**

- Linux capable 1.5GHz CV64A host CPU and CV32E coprocessor
- X32/x16 (LP)DDR4, DDR3L memory
- 3D / 2D GPUs with OpenGL support
- MIPI-DSI / CSI display / camera controllers
- Security: DRM Ciphers, key storage, random number generator, etc.
- GigE MAC
- PCIe 2.0 x1 port
- 2 USB 2.0 interfaces
- 3 SDIO interfaces for boot source, storage, etc



© OpenHW Group

10 & 11 December 2019

17

# OSHW RISC-V Linux board for less than \$100?

- Goal: Sub-\$100 Open Source Hardware board that can run Linux on RISC-V
- Possible by 2021?
- Interested in working together?
  - [drew@oshpark.com](mailto:drew@oshpark.com) / Twitter: [@pdp7](#)
  - create a mailing list?

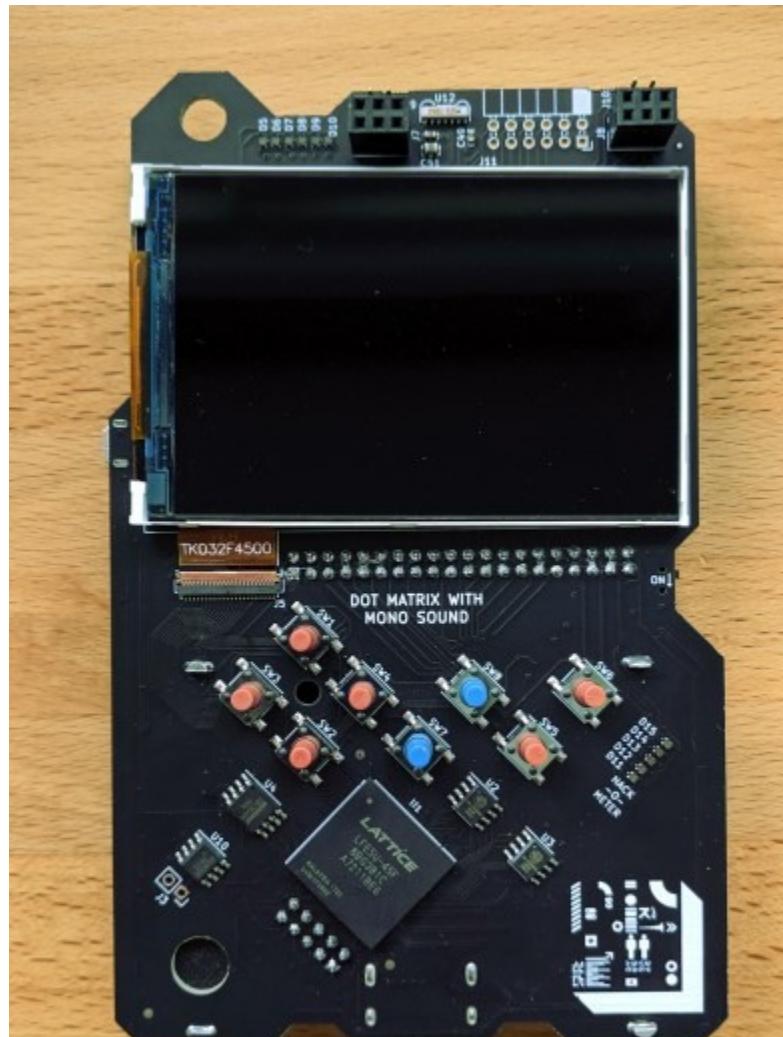
Slides: <https://github.com/pdp7/talks/blob/master/lug-riscv.pdf>



*Section:*  
Linux on the Hackaday Badge

# Hackaday 2019 Supercon badge

- RISC-V “soft” core on ECP5 FPGA
- Gigantic FPGA In A Game Boy Form Factor



# “Team Linux on Badge”

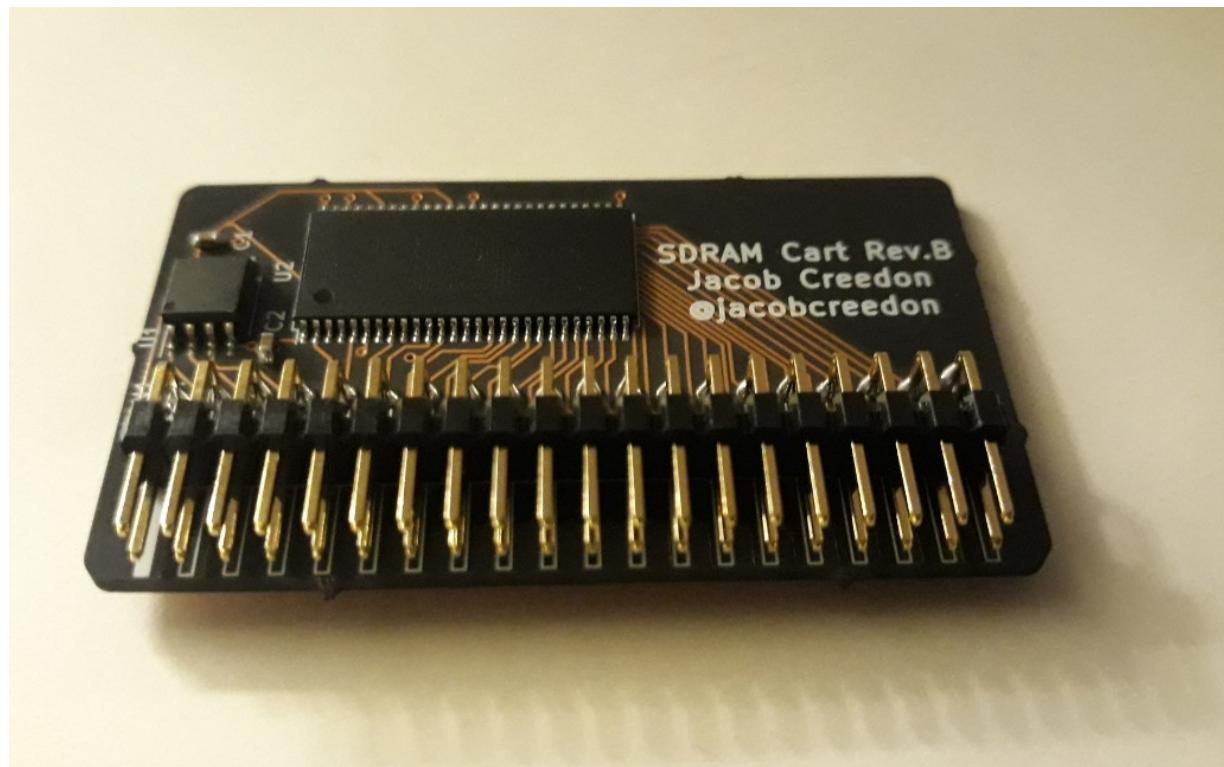


# “Team Linux on Badge”

- Blog post: Hackaday Supercon badge boots Linux using SDRAM cartridge
  - <https://blog.oshpark.com/2019/12/20/boot-linux-on-this-hackaday-supercon-badge-with-this-sdram-cartridge/>
- Michael Welling (@QwertyEmdedded), Tim Ansell (@mithro), Sean Cross (@xobs), Jacob Creedon (@jacobcreedon)
- First attempt: use the built-in 16MB SRAM... no luck :(
  - (*though xobs now might have a way to do it*)

# “Team Linux on Badge”

- Second attempt:
  - Jacob Creedon designed an a cartridge board that adds 32MB of SDRAM to the Hackaday Supercon badge... before the event!



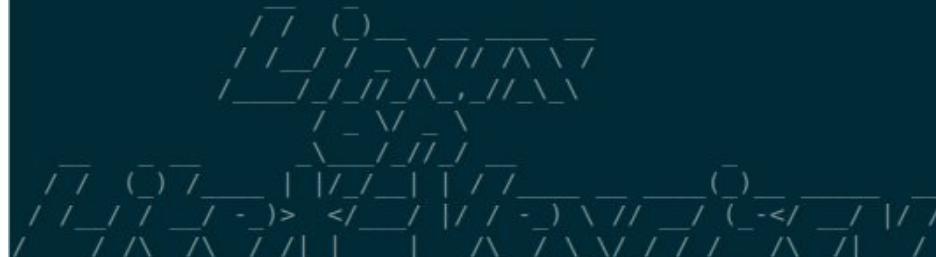


michael@reactor: ~/projects/litex/lin... X

michael@reactor: ~/projects/litex/lin... X

+ ▾

```
Welcome to Buildroot  
buildroot login: root
```



```
32-bit VexRiscv CPU with MMU integrated in a LiteX SoC
```

```
login[55]: root login on 'console'
```

```
root@buildroot:~# ps
```

PID	USER	COMMAND
1	root	init
2	root	[kthreadd]
3	root	[kworker/0:0-eve]
4	root	[kworker/0:0H]
5	root	[kworker/u2:0-ev]
6	root	[mm_percpu_wq]
7	root	[ksoftirqd/0]
8	root	[kdevtmpfs]
9	root	[oom_reaper]
10	root	[writeback]
11	root	[kcompactd0]
12	root	[kblockd]
13	root	[kworker/0:1]
14	root	[kswapd0]
34	root	/sbin/klogd -n
55	root	-sh
56	root	[kworker/u2:1]
58	root	ps

```
root@buildroot:~# uname -a
```

```
Linux buildroot 5.0.13 #2 Sat Nov 16 14:10:21 PST 2019 riscv32 GNU/Linux
```

```
root@buildroot:~# cat /proc/cpuinfo
```

processor	:	0
hart	:	0
isa	:	rv32ima
mmu	:	sv32
uarch	:	spinalhdl,vexriscv

```
root@buildroot:~# free
```

	total	used	free	shared	buff/cache	available
Mem:	17288	2376	9620	0	5292	9120

# “Team Linux on Badge”

- [https://youtu.be/3se\\_L0tRZeg?t=1055](https://youtu.be/3se_L0tRZeg?t=1055)

Watch the demo during the Badge Hacking ceremony (jump to 17m 35s):



# Linux on LiteX-VexRiscv

- Linux with VexRiscv CPU, a 32-bits Linux Capable RISC-V CPU written in Spinal HDL
  - [github.com/litex-hub/linux-on-litex-vexriscv](https://github.com/litex-hub/linux-on-litex-vexriscv)
- NOW with upstream support for the Hackaday Supercon badge!
  - <https://github.com/litex-hub/litex-boards/pull/31>



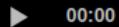
- Opened GitHub issue:
  - optimize performance on Hackaday Badge #35
    - <https://github.com/litex-hub/litex-boards/issues/35>
- Now 10x faster!
  - <https://asciinema.org/a/Pcm3vd1BEdEKY9srYX6MsNfCE>
  - Thanks to [enjoy-digital](#)



Asciicast updated.

```
[ 7.896093] Initramfs unpacking failed: junk in compressed archive
[ 7.953813] workingset: timestamp_bits=30 max_order=13 bucket_order=0
[ 9.236463] Block layer SCSI generic (bsg) driver version 0.4 loaded (major 253)
[ 9.239004] io scheduler mq-deadline registered
[ 9.240102] io scheduler kyber registered
[ 13.977920] f0001000.serial: MMIO 0xf0001000 (irq = 0, base_baud = 0) is a liteuart
[ 13.980290] printk: console [liteuart0] enabled
[ 13.980290] printk: console [liteuart0] enabled
[ 13.982965] printk: bootconsole [sbi0] disabled
[ 13.982965] printk: bootconsole [sbi0] disabled
[ 14.058778] libphy: Fixed MDIO Bus: probed
[ 14.074959] i2c /dev entries driver
[ 14.247461] NET: Registered protocol family 10
[ 14.307974] Segment Routing with IPv6
[ 14.315214] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[ 14.455698] Freeing unused kernel memory: 140K
[ 14.457905] This architecture does not have kernel memory protection.
[ 14.459170] Run /init as init process
mount: mounting tmpfs on /dev/shm failed: Invalid argument
mount: mounting tmpfs on /tmp failed: Invalid argument
mount: mounting tmpfs on /run failed: Invalid argument
Starting syslogd: OK
Starting klogd: OK
Running sysctl: OK
Initializing random number generator... [ 23.063050] random: dd: uninitialized urandom read (512 bytes read)
done.
Starting network: OK
Starting dropbear sshd: [ 27.336210] random: dropbear: uninitialized urandom read (32 bytes read)
OK
```

Welcome to Buildroot



00:00



Linux boots on Hackaday Supercon FPGA badge [10x faster!]

Slides:  
[github.com/pdp7/talks/blob/master/lug-riscv.pdf](https://github.com/pdp7/talks/blob/master/lug-riscv.pdf)

**Drew Fustini**  
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**@pdp7 / @oshpark**



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Slides: <https://github.com/pdp7/talks/blob/master/lug-riscv.pdf>



*bonus section:*  
Linux on OSHW laptops

# Novena laptop

- Created by Bunnie Huang & Sean Cross (xobs)
  - Chumby, “Hacking the Xbox”, [amazing reverse engineers](#)
- 100% Open Source Hardware laptop
- Quad-core 1.2GHz ARM, 4GB RAM, SSD, WiFi
- Xilinx FPGA for custom hardware design
- Software Defined Radio (SDR) module





# MNT Reform

## Open Source DIY Laptop for Hacking, Customization, and Privacy

This project is coming soon. Sign up to receive updates and be notified when this project launches.

me@example.com

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### Introducing the much more personal computer.

Modern laptops have secret schematics, glued-in batteries, and mystery components all over. But Reform is the opposite — it invites both curious makers and privacy aware users to take a look under the hood, customize the documented electronics, and 3D-print their own parts.