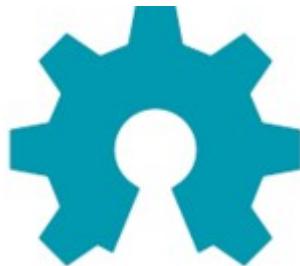


Slides: <https://github.com/pdp7/talks/blob/master/oshw-linux-36c3.pdf>

Linux on Open Source Hardware and Open Source Chip Design

Chaos Communication Congress (36c3)



Drew Fustini

OSH Park

drew@oshpark.com

[@oshpark](https://twitter.com/@oshpark) / [@pdp7](https://twitter.com/@pdp7)



- Open Source Hardware designer at OSH Park
 - PCB manufacturing service in the USA
 - drew@oshpark.com / Twitter: [@oshpark](https://twitter.com/@oshpark)
- Volunteer Member of Board of Directors of BeagleBoard.org Foundation
 - drew@beagleboard.org
- Volunteer Member of the Board of Directors of the Open Source Hardware Association (OSHWA)
 - serving as Vice President
 - drew@pdp7.com



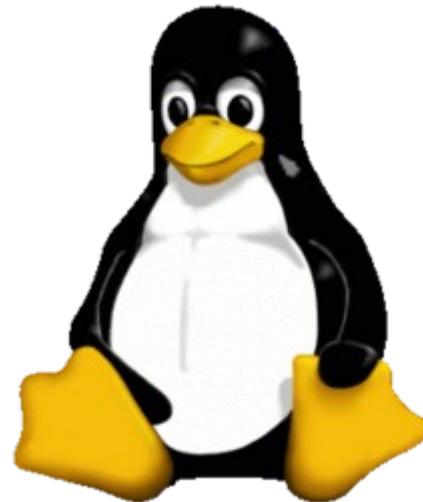
What is Open Source?



- Examples of popular Open Source projects



Apache



LibreOffice[®]



Firefox[®]



What is Open Source?

- The term "**open source**" refers to something people can **modify and share** because its design is **publicly accessible**
- **Open Source software** is software with source code that anyone can: **inspect, modify, and enhance**



Open Source Hardware



- **FLOSS** is a term to describe software that is Free, Libre, or Open Source Software
- In the context of hardware projects, I consider these terms equivalent:
 - Free Hardware
 - Libre Hardware
 - Open Hardware
 - Open Source Hardware

Slides: <https://github.com/pdp7/talks/blob/master/oshw-linux-36c3.pdf>



Statement of Principles:

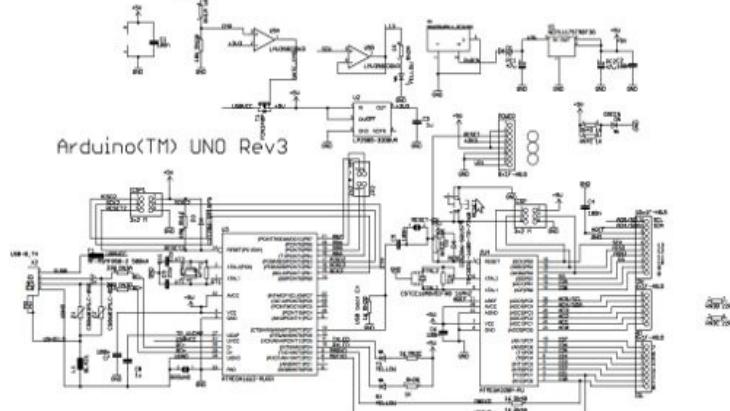
Hardware whose **design** is made **publicly available** so that anyone can **study**, **modify**, **distribute**, **make**, and **sell** the design or hardware based on that design

Slides: <https://github.com/pdp7/talks/blob/master/oshw-linux-36c3.pdf>

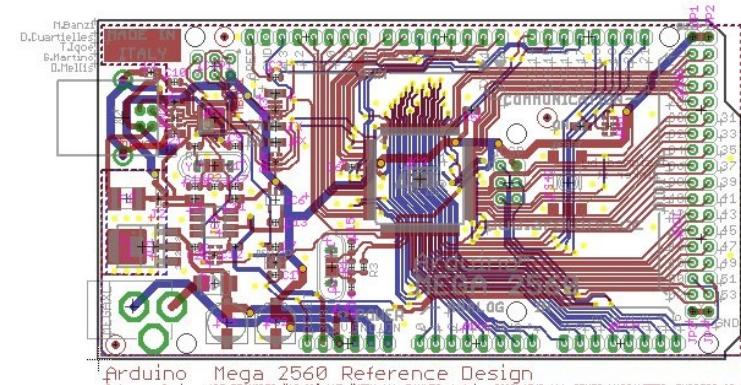
Open Source Hardware

Documentation required for electronics:

Schematics



Board Layout



Editable source files for CAD software such as KiCad or EAGLE

Bill of Materials (BoM)

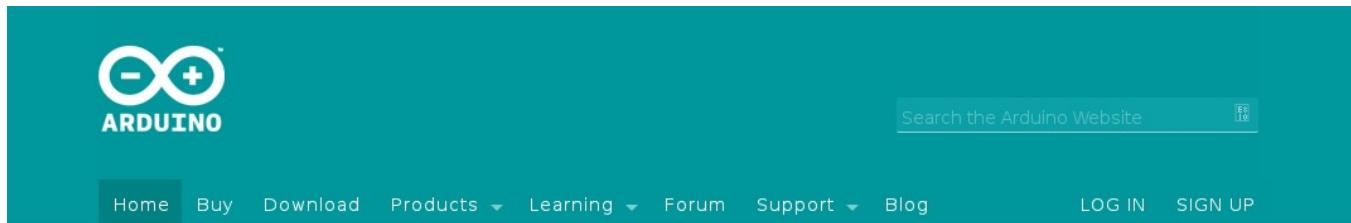
Not strict requirement, but best practice is for all components available from distributors in **low quantity**



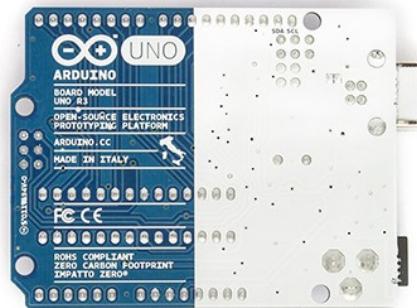
Open Source Hardware



Example: **Arduino** achieved critical mass by sharing their hardware designs and source code



Arduino Uno



Arduino: The Documentary describes the team's motivation



Open Source Hardware



✓ Example: [Arduino Uno](#) schematic and PCB layout design files for EAGLE CAD can be downloaded from [Arduino.cc](#)

The screenshot shows a web browser window with the Arduino website. The URL in the address bar is https://www.arduino.cc/en/Main/ArduinoBoardUno. The page title is "Arduino - ArduinoBoa...". The main content area is titled "Documentation" in orange. On the left, there's a sidebar with links: "Overview", "Get Inspired", "Related Items", "Technical Specs", and "Documentation" (which is highlighted in blue). Below the sidebar, there are two download buttons: one for "EAGLE FILES IN .ZIP" and another for "SCHEMATICS IN .PDF". The top navigation bar includes links for "Buy", "Software", "Products", "Learning", "Forum", "Support", and "Blog".

Documentation

Overview

Get Inspired

Related Items

Technical Specs

Documentation



EAGLE FILES
IN .ZIP



SCHEMATICS
IN .PDF

OSH: Schematics, Reference Design, Board size

Arduino / Genuino Uno is open-source hardware! You can build your own board using the following files:



Open Source Hardware



Publish documentation with an
Open Source license:

- Creative Commons Share-Alike: **CC-BY-SA**
 - Non-Commercial (NC) clause is NOT acceptable
- Copyleft: **GPLv2, GPLv3**
- Permissive: **Apache, BSD, MIT**
- OSHW inspired: **CERN OHL, TAPR, SolderPad**



CERN Open Hardware Licence

- Originally written for **CERN** designs hosted in the **Open Hardware Repository**
- Can be used by **any designer** wishing to **share design** information using a **license compliant** with the **OSHW definition criteria**.
- [CERN OHL version 1.2](#)
Contains the license itself and a guide to its usage



CERN Open Hardware Licence



- Video interview with [Javier Serrano](#)
- physicist and electronics engineer at CERN
- co-author of the **CERN Open Hardware License**
- creator of the **Open Hardware Repository**



Open Source Hardware



Licenses, Copyright and Patents
can get confusing!

Review of Popular OSHW Licenses

Video of Ari Douglas at OHS 2014

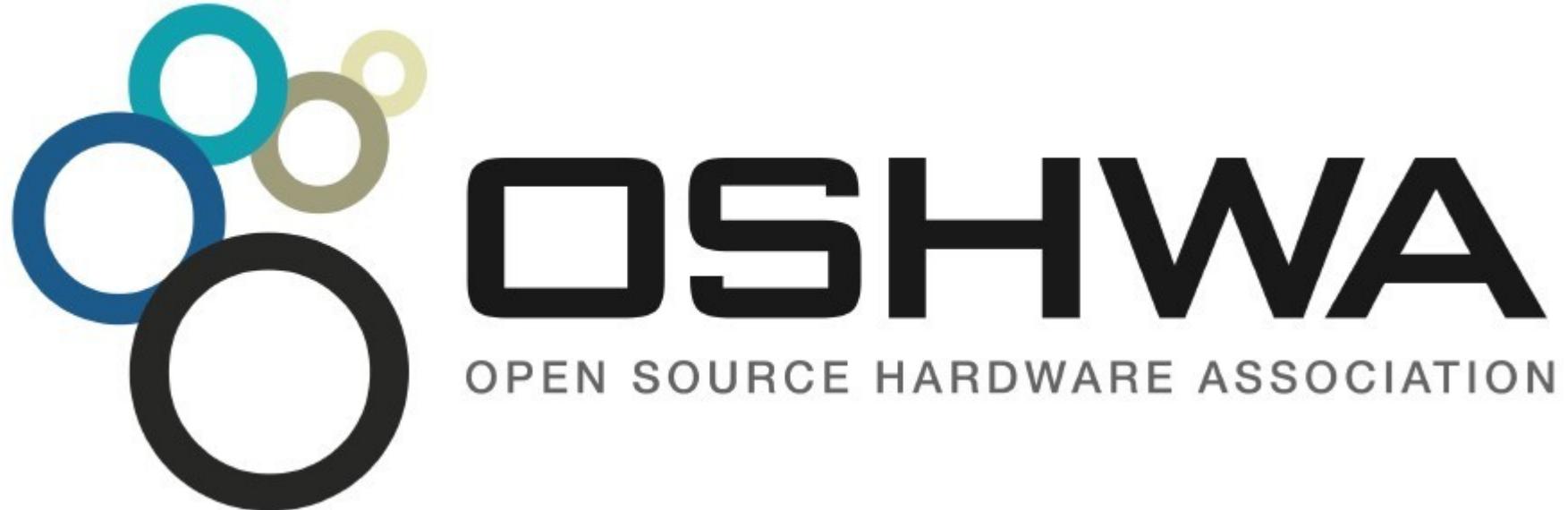


Open Source Hardware

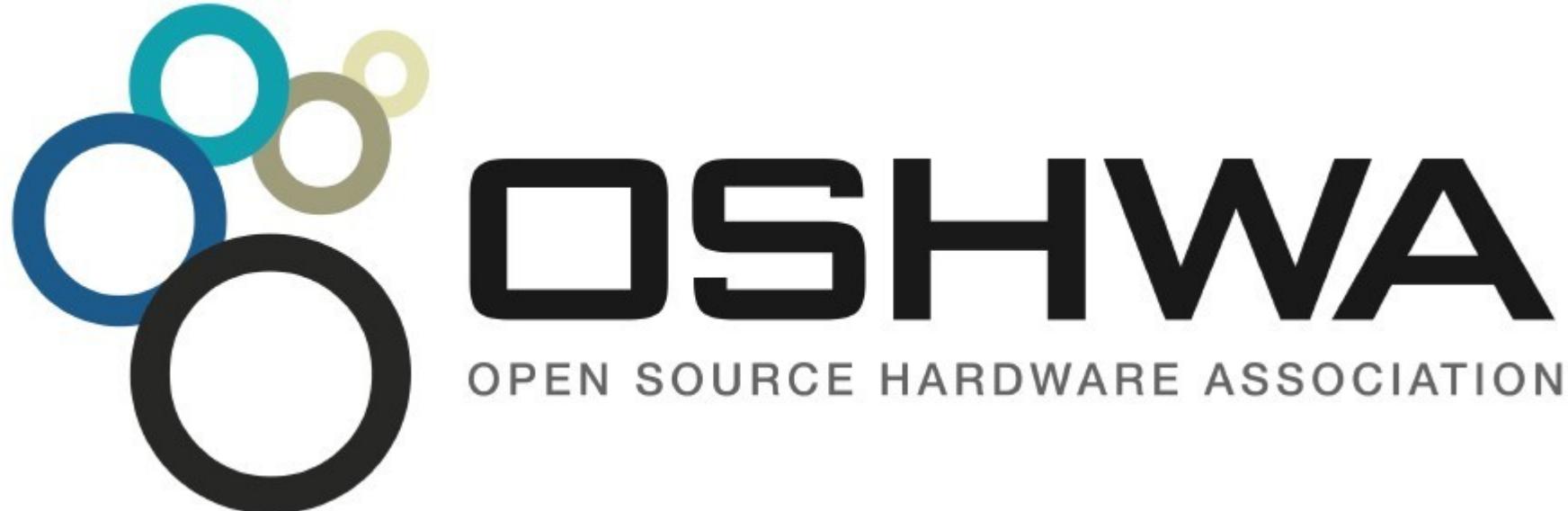


What is the spirit of Open Source?

- Publish everything that will:
enable collaborative development
- OSHW makes sense when you want to encourage other people to contribute to your project



- US-based 501(c)3 non-profit organization
- Hosts the **Open Source Hardware definition**
- “aims to be the **voice of the open hardware community**, ensuring that technological knowledge is accessible to everyone, and encouraging the collaborative development of technology”



- OSHW Best Practices
- Quick Reference Guide
- OSHW "May and Must" (PDF)
- OSHW Checklist (PDF)

Open Hardware Summit (OHS)

- OHS 2020: March 13 in NYC (USA)
 - <http://2020.oshwa.org/>
- *8 prior summits:*
 - **2010, 2011:** New York Hall of Science
 - **2012:** Eyebeam (*NYC*)
 - **2013:** MIT (*Boston area*)
 - **2014:** Roma, Italia!
 - **2015:** Philadelphia, USA
 - **2016:** Portland, Oregon, USA
 - **2017:** Denver, USA
 - **2018:** MIT (Cambridge, MA, USA)

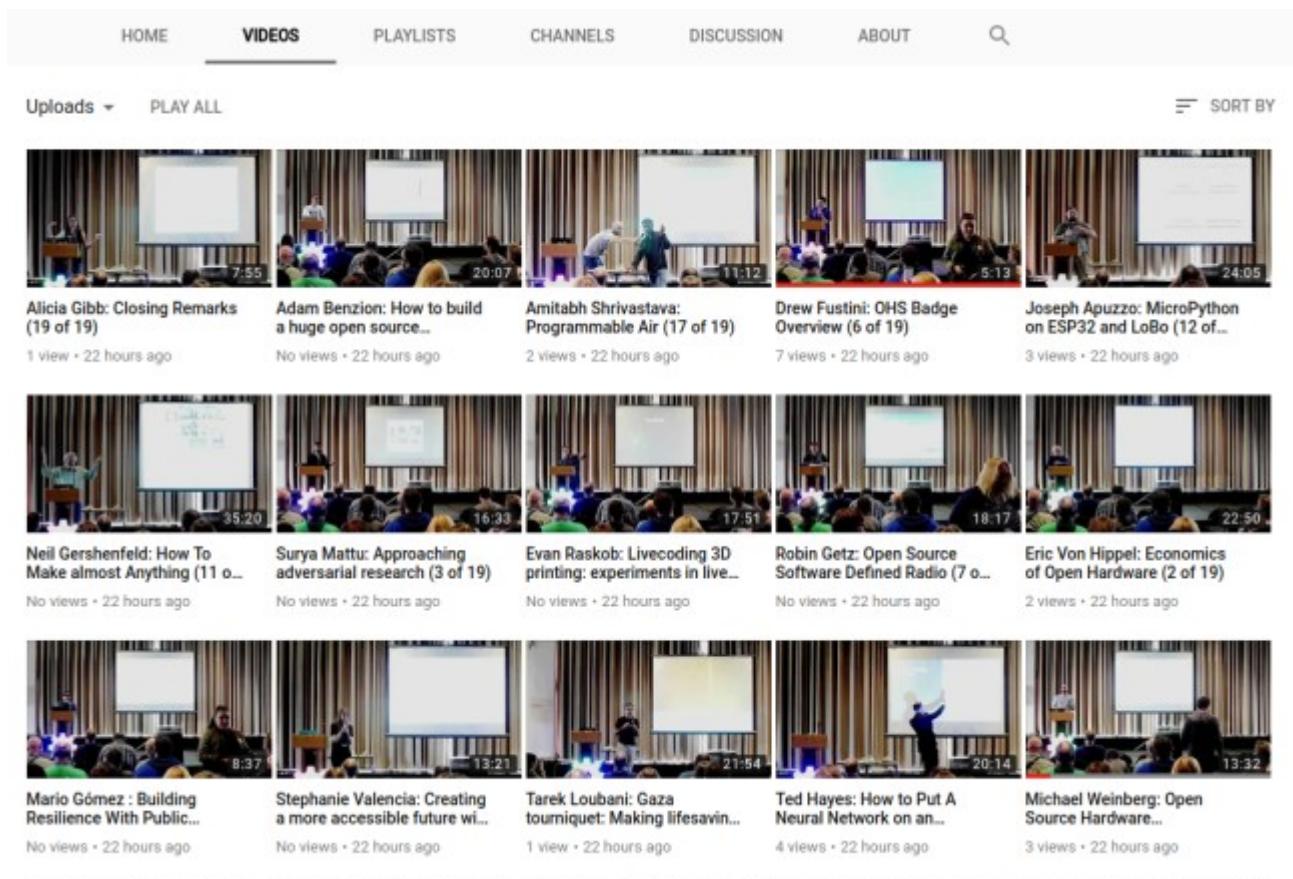
October is Open Hardware Month!



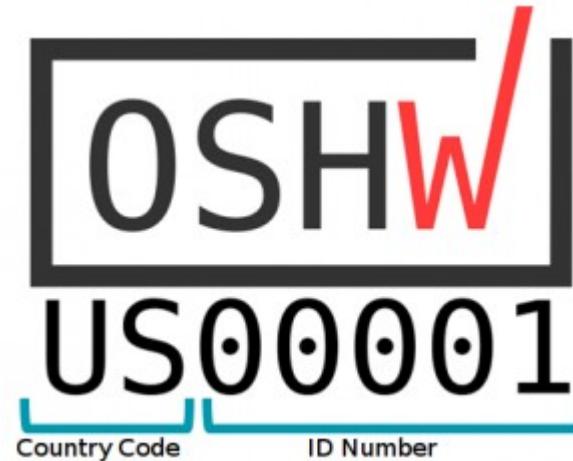
- People all over the world celebrated with meet-ups, talks and workshops
- Kicked off with events at RAIT in Vienna (Austria) and SparkFun in Colorado (USA), followed by gatherings in Poland, Panama, Thailand, Japan, Ghana and more!
- 40 events in 14 different countries across 5 continents

Open Hardware Summit (OHS)

- The Open Hardware Summit 2018 talks are available as individual videos on YouTube



Open Source Hardware Certification Program



- Allows hardware that complies with the community definition of Open Source Hardware to display a [certified OSHW logo](#)
- Make it easier for users of OSHW to track down documentation and information
- *More information:* [certificate.oshwa.org](#)

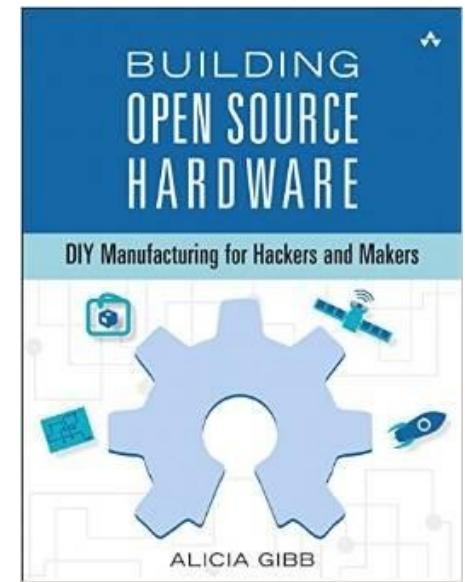


Open Source Hardware



Resources

- Join OSHWA, visit oshwa.org
- Subscribe to the mailing list
- Post in the OSHWA Forum
- Follow on Twitter:
 - [@OHSummit](https://twitter.com/OHSummit)
 - [@oshwassociation](https://twitter.com/oshwassociation)
- [Building Open Source Hardware](#)
by Alicia Gibb (*executive director of OSHWA*)



Slides: <https://github.com/pdp7/talks/blob/master/oshw-linux-36c3.pdf>



Section:
LINUX on OSHW
(my two favorite things!)

Novena laptop

- Created by Bunnie Huang & Sean Cross (xobs)
 - Chumby, “Hacking the Xbox”, [amazing reverse engineers](#)
- 100% Open Source Hardware laptop
- Quad-core 1.2GHz ARM, 4GB RAM, SSD, WiFi
- Xilinx FPGA for custom hardware design
- Software Defined Radio (SDR) module





MNT Reform

Open Source DIY Laptop for Hacking, Customization, and Privacy

This project is coming soon. Sign up to receive updates and be notified when this project launches.

me@example.com

Subscribe



Introducing the much more personal computer.

Modern laptops have secret schematics, glued-in batteries, and mystery components all over. But Reform is the opposite — it invites both curious makers and privacy aware users to take a look under the hood, customize the documented electronics, and 3D-print their own parts.

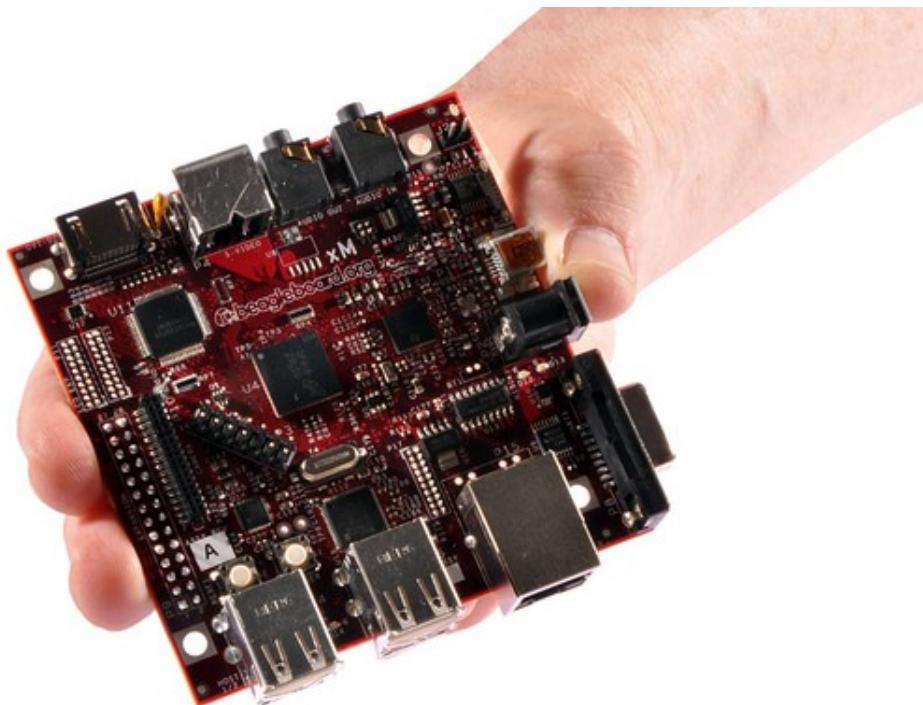


- Open Source Hardware computing for Makers, Educators & Professionals
- Developed by [BeagleBoard.org Foundation](#) and [BeagleBoard.org Community](#)
- Manufacturers: [element14](#), [GHI](#), [Seeed](#)



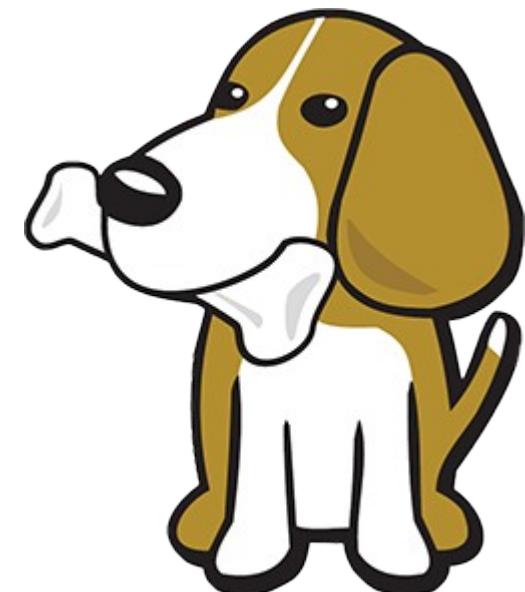


BeagleBoard.org released the first
BeagleBoard, an affordable, open
hardware ARM computer in **2008**





Maker focused, Altoids tin sized
BeagleBone introduced in **2011**





More affordable, more powerful
BeagleBone Black in 2013

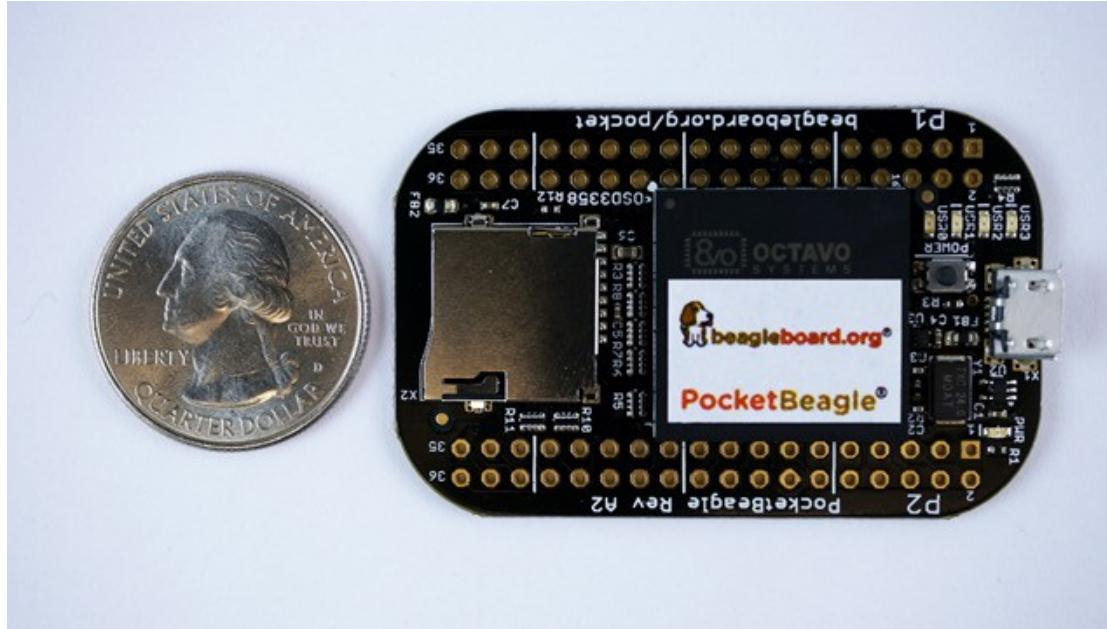




Open Source Hardware BeagleBone derivatives

	Capes	HDMI	Flash	Special
BeagleBoard.org BeagleBone	Y	N	N	JTAG
BeagleBoard.org BeagleBone Black	Y	Y	Y	-
Arrow BeagleBone Black Industrial	Y	Y	Y	Industrial
Element14 BeagleBone Black Industrial	Y	Y	Y	Industrial
SeeedStudio BeagleBone Green	Y	N	Y	Grove
SanCloud BeagleBone Enhanced	Y	Y	Y	1GB, 1Gbit, wireless
BeagleBoard.org BeagleBone Blue	N	N	Y	Robotics
BeagleBoard.org BeagleBoard-X15	N	Y	N	Big jump in CPUs and I/O

BeagleBoard.org PocketBeagle



- Michael Welling designed the “*PocketBone*” using the Octavo SiP and shared on Hackaday.io
- In response to online demand, BeagleBoard.org worked with GHI in Michigan to design and manufacture a new product: the PocketBeagle

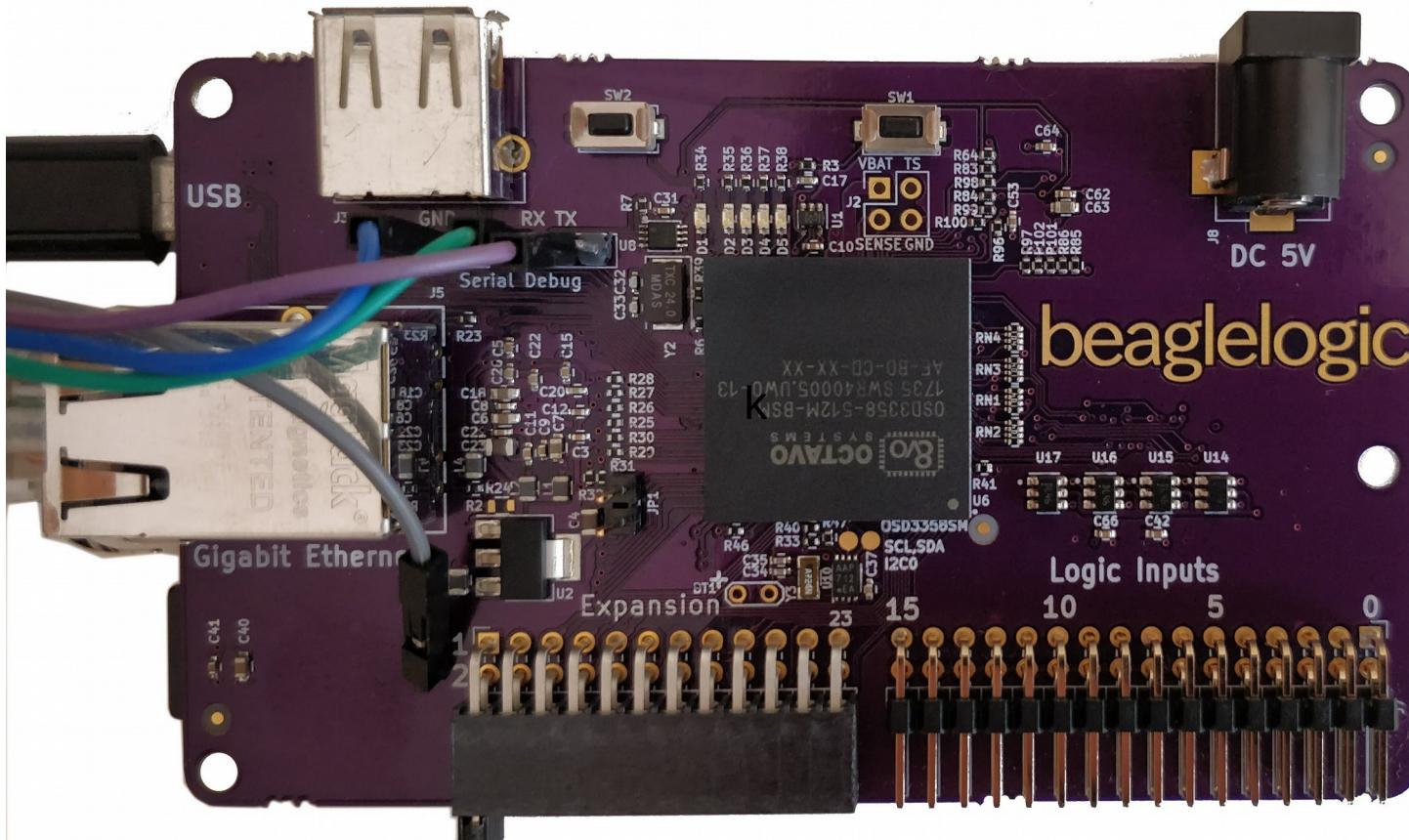
BeagleBoard.org PocketBeagle

- PocketBeagle design makes it feasible for individuals to create their own derivatives
- 4 layer PCB published for EAGLE and KiCad
- Low cost assembly is possible with solder paste stencil and toaster oven



BeagleLogic

- Kumar Abhishek created a derivative board intended to be used a logic analyzer
 - Finalist in the Best Product round of the Hackaday Prize



BeagleBone AI design files

README.md

BeagleBoard.org BeagleBone AI

Fast track to Embedded Artificial Intelligence

BeagleBone AI is built on the proven BeagleBoard.org® open source Linux platform for small SBCs and more powerful industrial computers. Based on the Texas Instruments® Sitara™ processor, it provides the power of the Sitara™ processor and the performance of the BeagleBoard.org® SoC in a compact package. It features the powerful SoC with the ease of BeagleBone® Black header and pinout compatibility. It is designed to explore how artificial intelligence (AI) can be used in everyday applications. The BeagleBone AI includes a neural network engine (NNE) and embedded-vision-engine (EVE) cores supported through the BeagleBoard.org® open source Linux distribution and installed tools. Focused on everyday automation in industrial, medical, and consumer applications.

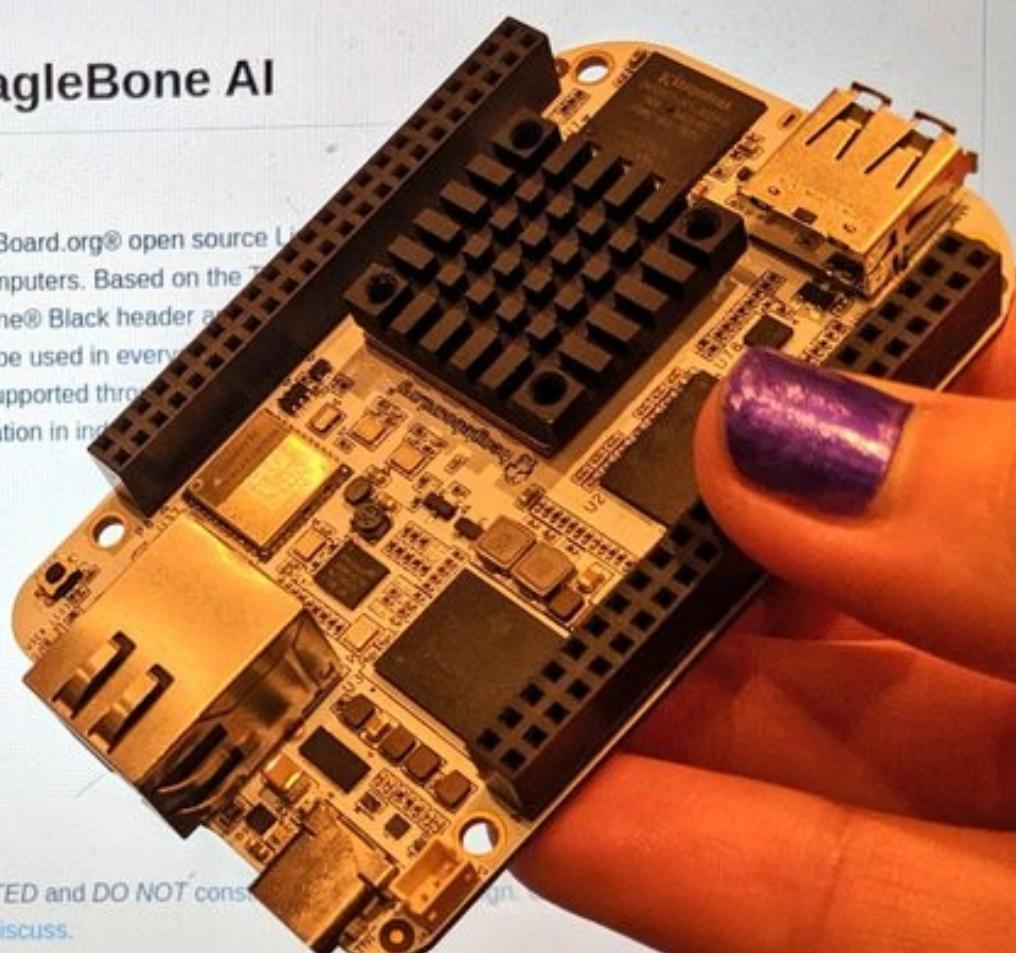
OSHW
US000169

Terms

These design materials are **NOT SUPPORTED** and **DO NOT** constitute a license under any intellectual property rights of BeagleBoard.org or its licensors. You may submit questions and comments to the support forums at [BeagleBoard.org/discuss](https://beagleboard.org/discuss).

THERE IS NO WARRANTY FOR THE DESIGN MATERIALS, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED.

CSV



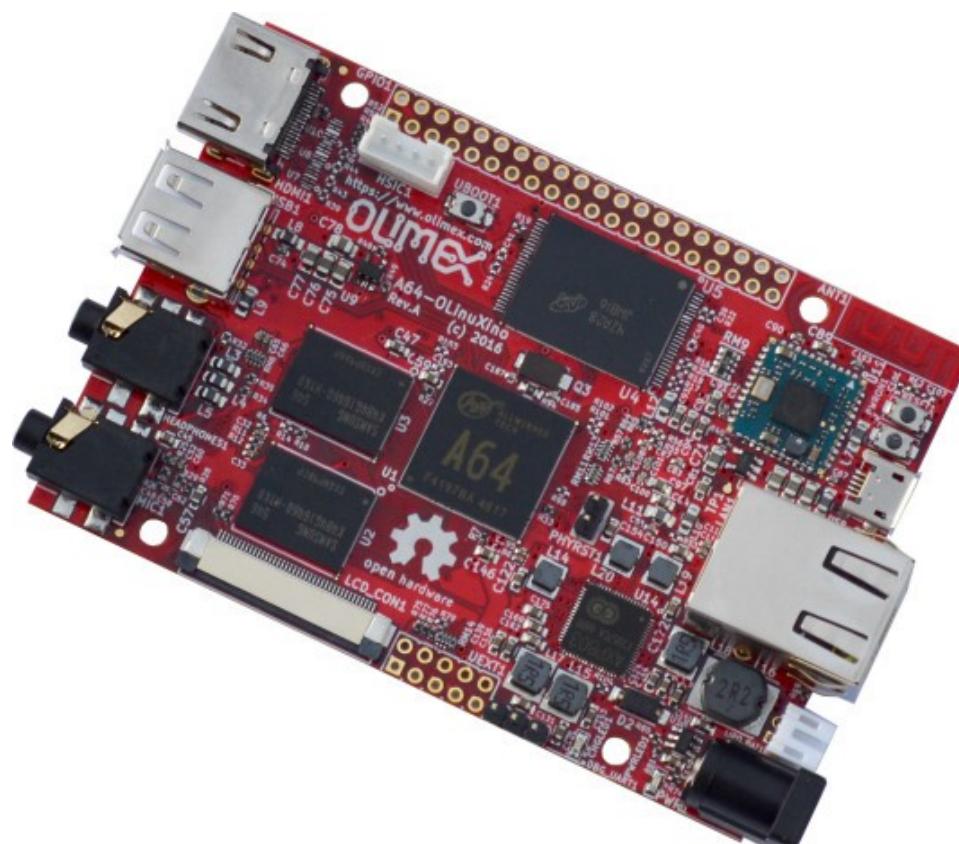


OLinuXino



- Low cost OSHW Linux computers
- Designed and manufactured by **Olimex** in **Bulgaria**
- Great blog post:
[Open Source Hardware, why it matters and what is pseudo OSHW](#)

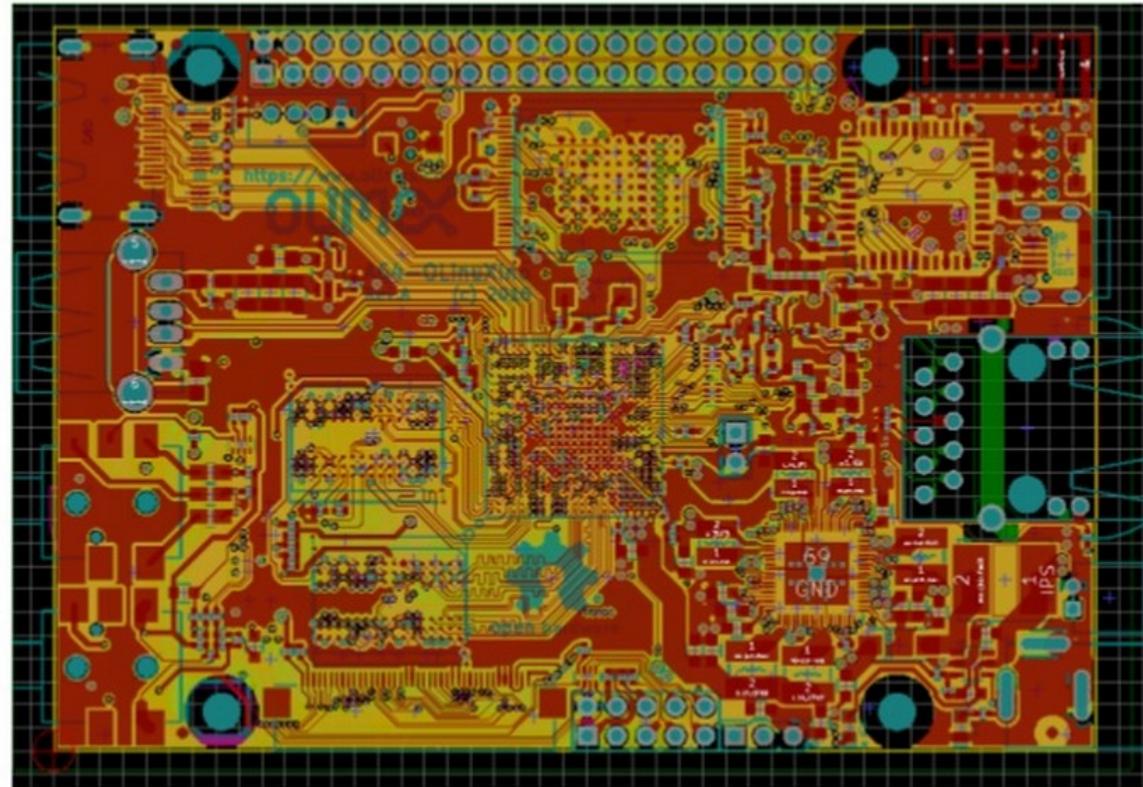
- Allwinner A64: Quad Core 64-bit ARM
 - Designed with Open Source [KiCad](#)
 - 1GB RAM, 4GB eMMC, WiFi+BLE4.0





Using FOSS tools for OSHW project

Designing with KiCAD of 64-bit ARM board



Tsvetan Usunov, OLIMEX Ltd

FOSDEM 2016

[Slides](#) / [Video](#)

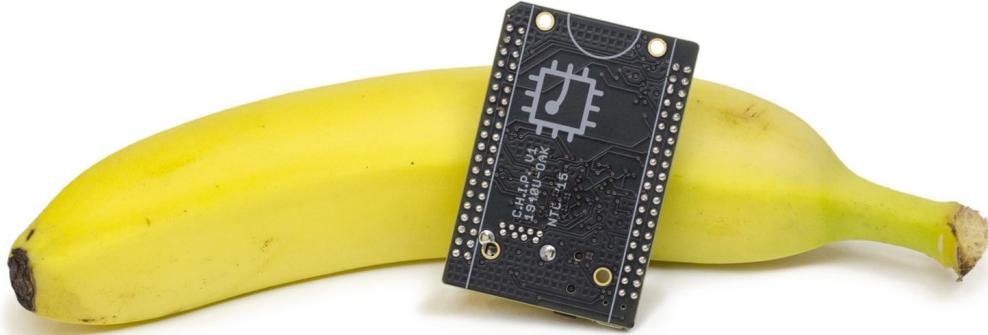


- **KiCad** is an Open Source EDA suite including Schematic Capture and PCB Layout
- Cross platform: **Windows**, **Mac OS** and **Linux**
- **CERN has contributed** professional CAD features for high-speed digital design
- Learn to design your own PCB in KiCad with: **Getting to Blinky**

- “DIY Open Source Hardware Software Hacker's friendly Modular Laptop”
- Developing an Open Source Laptop talk by Olimex founder Tsvetan Usunov at Hackaday Belgrade
- Design files on GitHub:
“everyone can download & learn, study, edit, modify”



C H I P



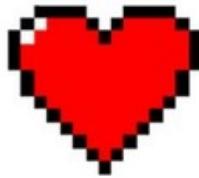
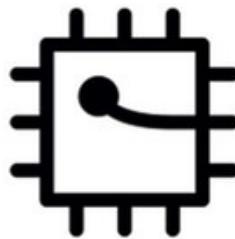
The World's First \$9 Computer

- getchip.com
- Next Thing Co. in Oakland
- Kickstarter in 2015
- Company ended in 2018

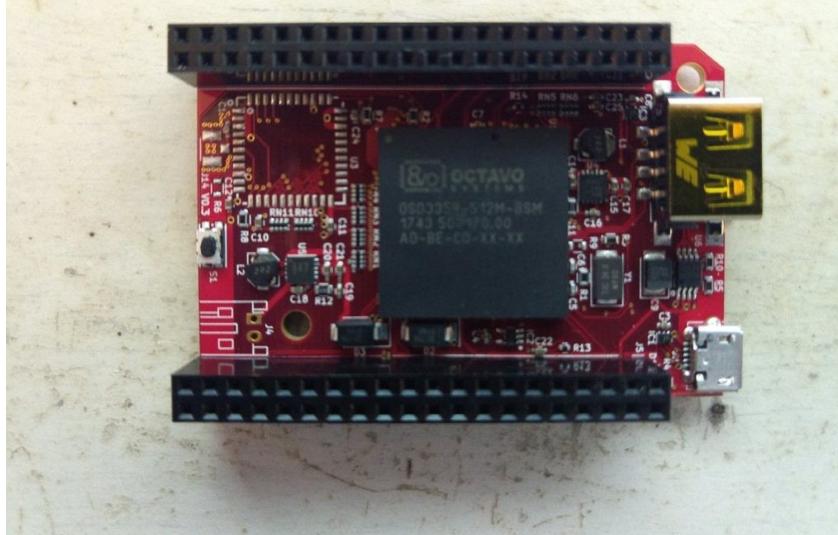


funded with
**KICK
STARTER**

C.H.I.P. is OSHW



- **GitHub:** [NextThingCo/CHIP-Hardware](#)
 - Schematics
 - PCB Layout
 - Bill of Materials (*BoM*)
- **License:**
 - Creative Commons Attribution-ShareAlike (CC-BY-SA)



- Nebula One created by Groguard to be compat
- PocketChip with Nebula One running DOOM!

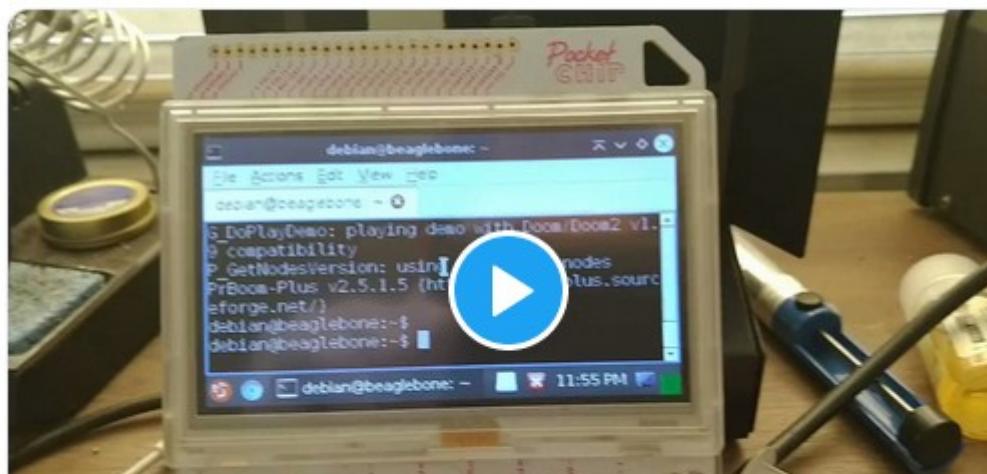


Groguard
@groguard

Follow ▾

Doom running on the NebulaOne board in the
PocketCHIP. Wifi and LCD are working! Just
need get the keyboard sorted next! @pdp7

@Jadon @dcschelt



Giant Board by groguard

- A single-board computer in the Adafruit Feather form factor
- Funded on Crowd Supply



Giant Board

by Groboards

Open Hardware
Computers & Networking
Development Kits

A single-board computer in the Adafruit Feather form factor

Part of
Microchip Get Launched
2019



\$13,670 raised
of \$12,250 goal

111% Funded!

Order Below

8 updates Aug 08 funded on 162 backers

Last update posted Aug 07, 2019

me@example.com

Subscribe to Updates



Open Source and FPGAs

- Hackspace Magazine column about how open source FPGA tools developed by [Claire Wolf \(oe1cxw\)](#), [David Shah](#) and others have made FPGAs more accessible than ever before to makers and hackers:
 - hackspace.raspberrypi.org/issues/26/

MAKE | BUILD | HACK | CREATE 132 PAGES OF MAKING

HackSpace

TECHNOLOGY IN YOUR HANDS

hsmag.cc | January 2020 | Issue #26

WHAT 3D PRINTER?

Find the ultimate replicator for 2020

CIRCUIT PYTHON

SOLDERING WITH GAS

PICKING AN IMPACT DRIVER

SEWING MACHINES

Building a kiln

Melting glass with a Raspberry Pi

Drew Fustini

@pdpf

Drew Fustini is a hardware designer and embedded Linux developer. He is the Vice President of the Open Source Hardware Association, and a board member of the BeagleBoard Foundation. Drew designs circuit boards for OSH Park, a PCB manufacturing service, and maintains the Adafruit BeagleBone Python library.

FPGA

FPGAs have been the talk of the town at many of this year's hacker conferences. But what exactly is an FPGA, and why are they so hot right now?

FPGA stands for Field Programmable Gate Array, a digital logic chip that can be programmed to reconfigure the internal hardware. An FPGA does not run software – it physically changes the configuration of its gate arrays to adapt to the task at hand. It's like an FPGA is an incredibly versatile tool! Need 25 PWM pins for a project? No problem. Want to replicate the functionality of a vintage CPU? Your FPGA has you covered. Not only is an FPGA versatile, but it is also better at handling timing-critical tasks than a microcontroller. You can filter high-speed sensor data before it's read by your processor, or offload repetitive tasks like debouncing buttons and moving the burden on your microcontroller.

FPGAs are hot right now but they're not a new technology – they've been used in industry for decades

The Lattice ECP5 FPGA is capable of more advanced features than the iCE40, and it's easier to learn how to use too, thanks to Project Trellis led by David Shah. This enabled the ECP5-powered Supercon badge to have cool features like HDMI video, while still being open for anyone to hack on without requiring proprietary tools.

FPGAs are a fascinating technology with lots of awesome applications. If you want to find out more, start off by reading Luke Valenty's *The Hobbyists Guide to FPGAs on Hackaday.io*. (hsmag.cc/GOAQwR), and watch Tim Ansell's Supercon talk to learn about the exciting future of open-source FPGA tools (hsmag.cc/kY5IPD). ☺

The rise of the FPGA

Reconfigure your chips to suit your project

This opened the door for low-cost, open hardware boards such as mystorm Blackice, TinyFPGA, iCEBreaker, and Fomu, which are great tools for teaching workshops and building projects.

Hobbyists Guide to FPGAs on Hackaday.io

(hsmag.cc/GOAQwR), and watch Tim Ansell's Supercon talk to learn about the exciting future of open-source FPGA tools (hsmag.cc/kY5IPD). ☺

Arduino

GNC

KIM

Open Source and FPGAs

- Open Source toolchains for FPGAs!
 - Project IceStorm for Lattice iCE40
 - “A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs”
by [Claire Wolf \(oe1cxw\)](#) at 32c3

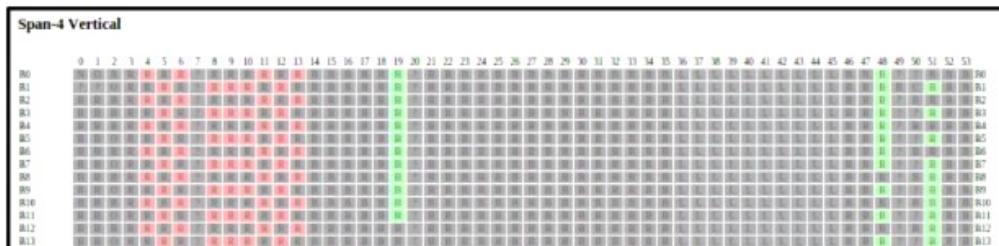


A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs



by [Clifford](#)

Some screenshots from IceStrom Docs:

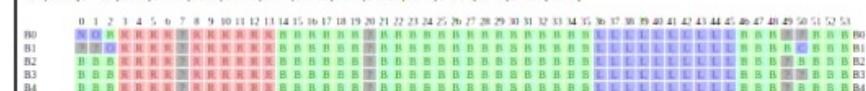


(2 17)	(3 17)	(4 17)	(5 17)	(6 17)
LOGIC Tile (2 16)	RAMT Tile (3 16)	LOGIC Tile (4 16)	LOGIC Tile (5 16)	LOGIC Tile (6 16)
LOGIC Tile (2 15)	RAMB Tile (3 15)	LOGIC Tile (4 15)	LOGIC Tile (5 15)	LOGIC Tile (6 15)
LOGIC Tile (2 14)	RAMT Tile (3 14)	LOGIC Tile (4 14)	LOGIC Tile (5 14)	LOGIC Tile (6 14)

Configuration Bitmap

A LOGIC Tile has 64x bits in 16 groups of 54 bits each:

B0[53:0], B1[53:0], B2[53:0], B3[53:0], B4[53:0], B5[53:0], B6[53:0], B7[53:0],
B8[53:0], B9[53:0], B10[53:0], B11[53:0], B12[53:0], B13[53:0], B14[53:0], B15[53:0]



Open Source and FPGAs

- Open Source toolchains for FPGAs!
 - Project Trellis for Lattice ECP5
 - “Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5”
 - David Shah (@fpga_dave)
 - youtube.com/watch?v=0se7kNes3EU

Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5

Project Trellis & nextpnr

FOSS Tools for ECP5 FPGAs

David Shah
@fpga_dave

Symbiotic EDA || Imperial College London

FOSDEM 19
org



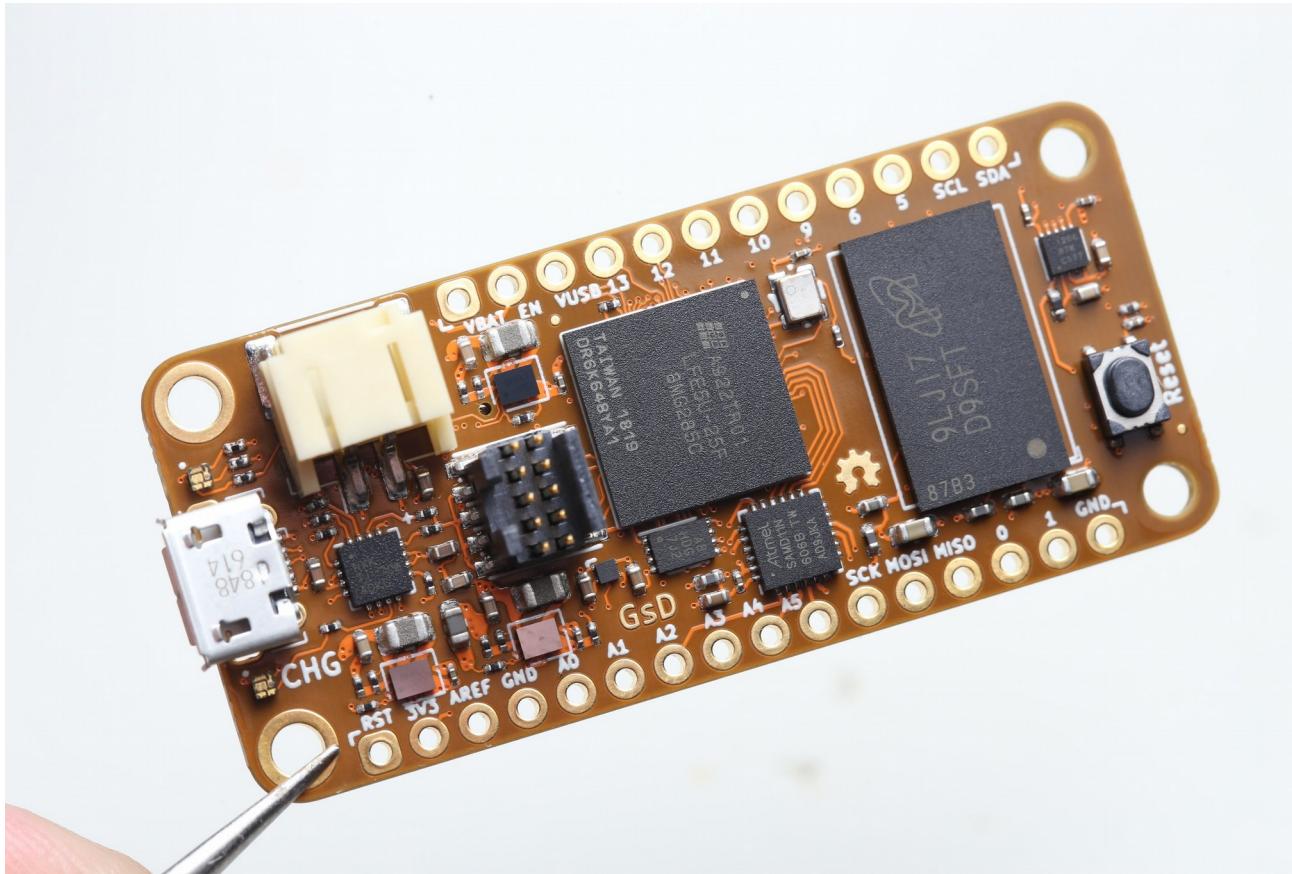
Open Source and FPGAs

- Open Source toolchains for FPGAs!
 - Project X-Ray and SymbiFlow for Xilinx Series 7
 - [Timothy 'mithro' Ansell](#): “Xilinx Series 7 FPGAs Now Have a Fully Open Source Toolchain!” (*almost*)
 - youtube.com/watch?v=EHePto95qoE



Open Source and FPGAs

- Open Source Hardware boards with Lattice ECP5 FPGA with open RISC-V “soft” CPU:
 - Orange Crab by Greg Davill
 - <https://github.com/gregdavill/OrangeCrab>





Greg @ #36c3
@GregDavill



Replying to @mithro @pdp7 and 2 others

Done. 😊

```
File Edit View Terminal Tabs Help
SRAM:      4KB
L2:        8KB
MAIN-RAM: 131072KB

----- Initialization -----
Initializing SDRAM...
SDRAM now under software control
Read leveling:
m0, b0: |11100000| delays: 01+-01
best: m0, b0 delays: 01+-01
m1, b0: |11100000| delays: 01+-01
best: m1, b0 delays: 01+-01
SDRAM now under hardware control
Memtest OK

----- Boot -----
Booting from serial...
Press Q or ESC to abort boot completely.
sL5DdSMmkekro
[LXTERM] Received firmware download request from the device.
[LXTERM] Uploading buildroot/Image to 0xc0000000 (4545524 bytes)...
[LXTERM] Upload complete (85.6KB/s).
[LXTERM] Uploading buildroot/rootfs.cpio to 0xc0800000 (8029184 bytes)...
[ 0:43 ] 1.2K views => | 98%
```



Open Source and FPGAs

- Radiona.org ULX3S
 - <https://www.crowdsupply.com/radiona/ulx3s>

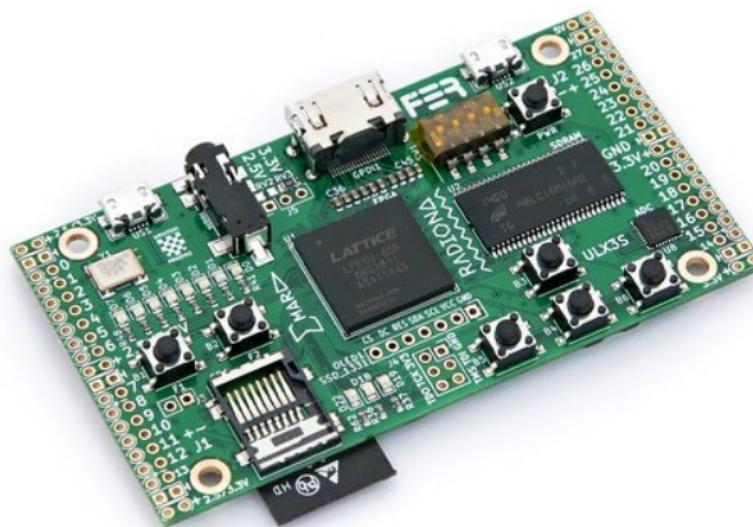
ULX3S

A powerful, open hardware ECP5 FPGA dev board

This project is coming soon. Sign up to receive updates and be notified when this project launches.

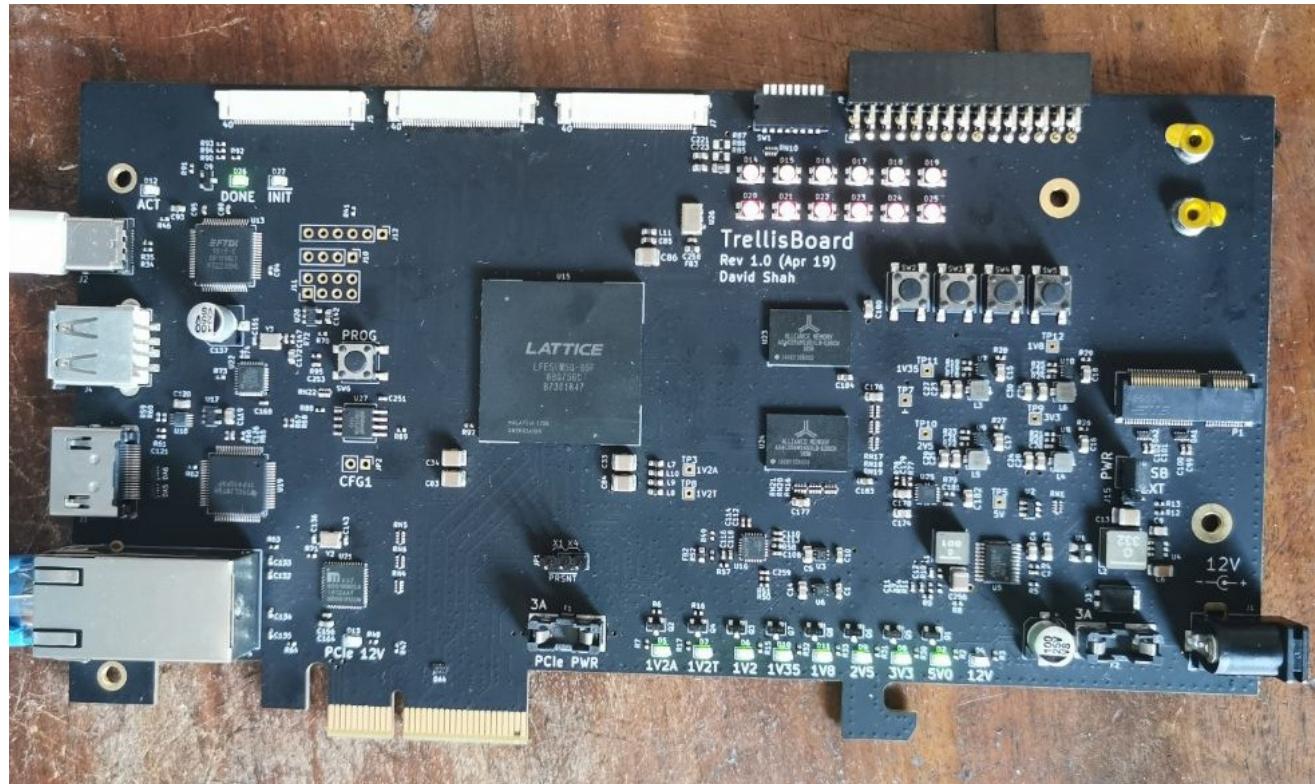
me@example.com

[Subscribe](#)



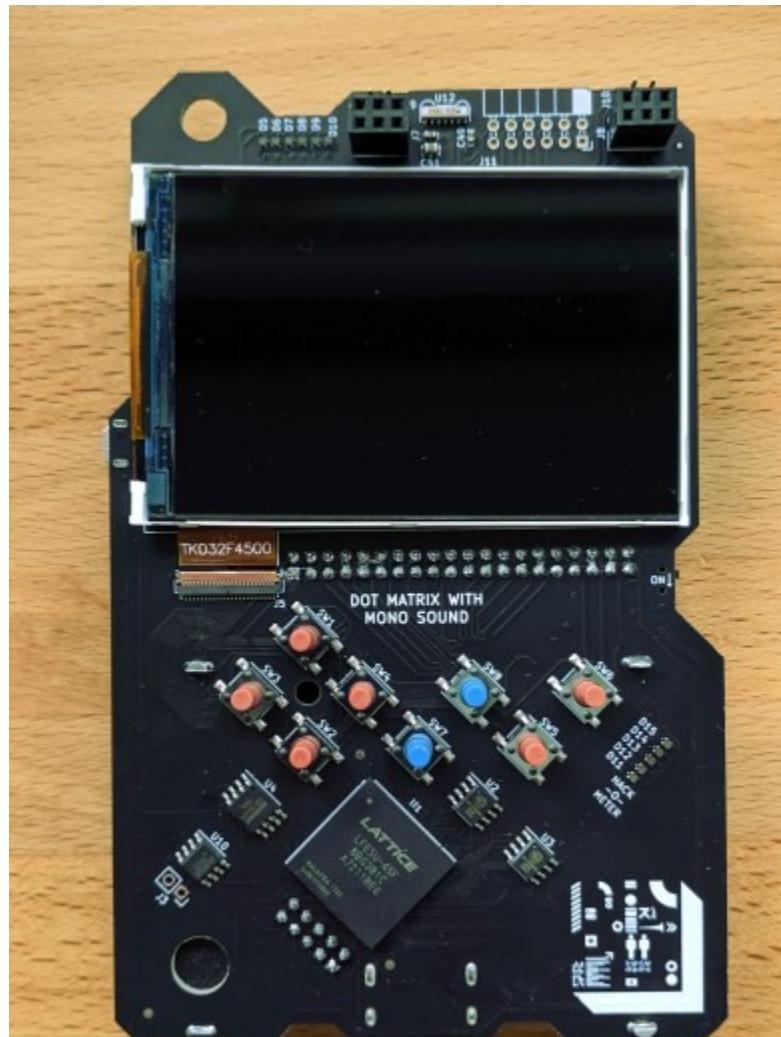
Open Source and FPGAs

- Open Source Hardware boards with Lattice ECP5 FPGA with open RISC-V “soft” CPU:
 - David Shah's Trellis board (Ultimate ECP5 Board)
 - <https://github.com/daveshah1/TrellisBoard>



Hackaday 2019 Supercon badge

- RISC-V “soft” core on ECP5 FPGA
- Gigantic FPGA In A Game Boy Form Factor

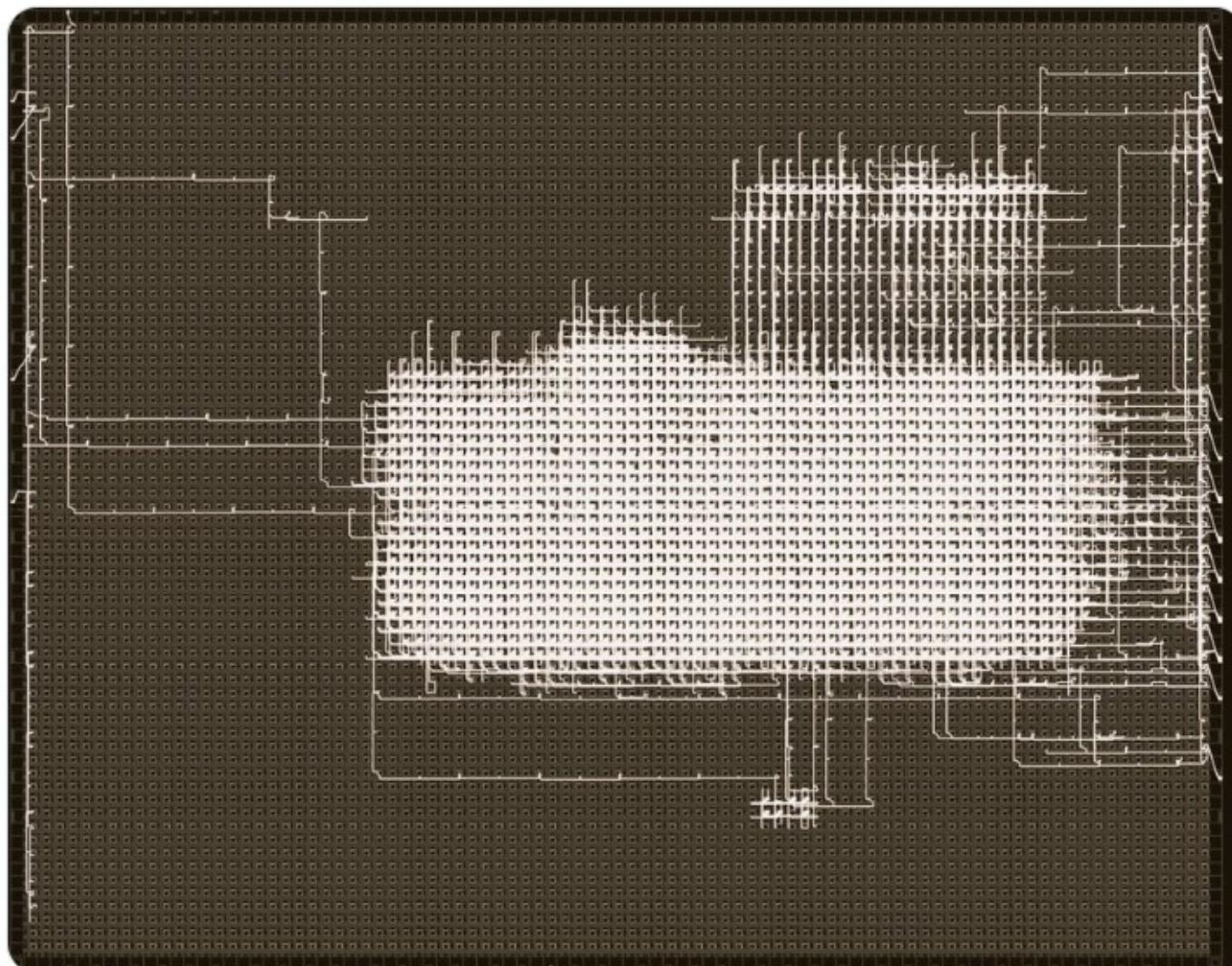


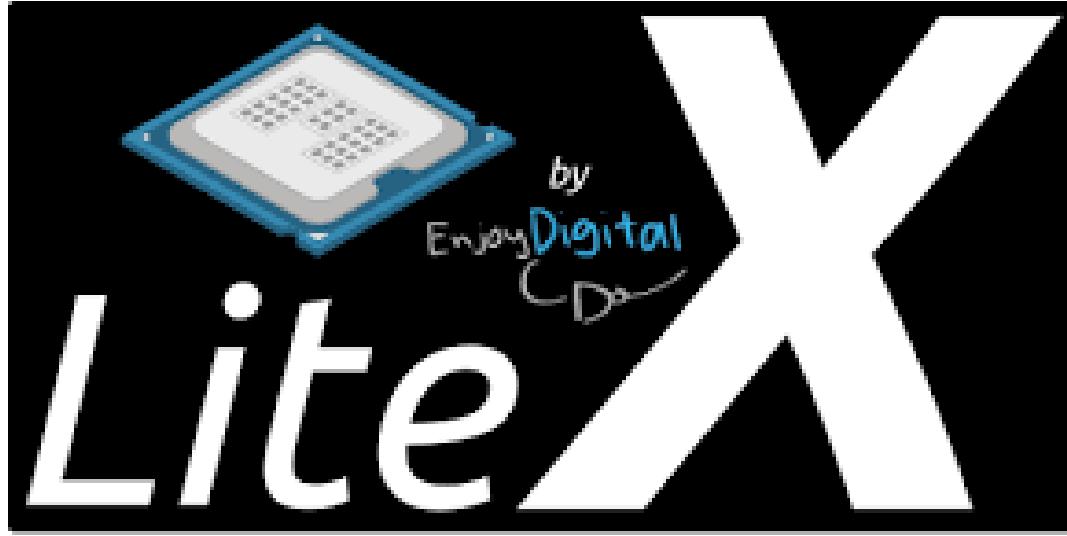


OSS FPGA & EDA tools
@ico_TC



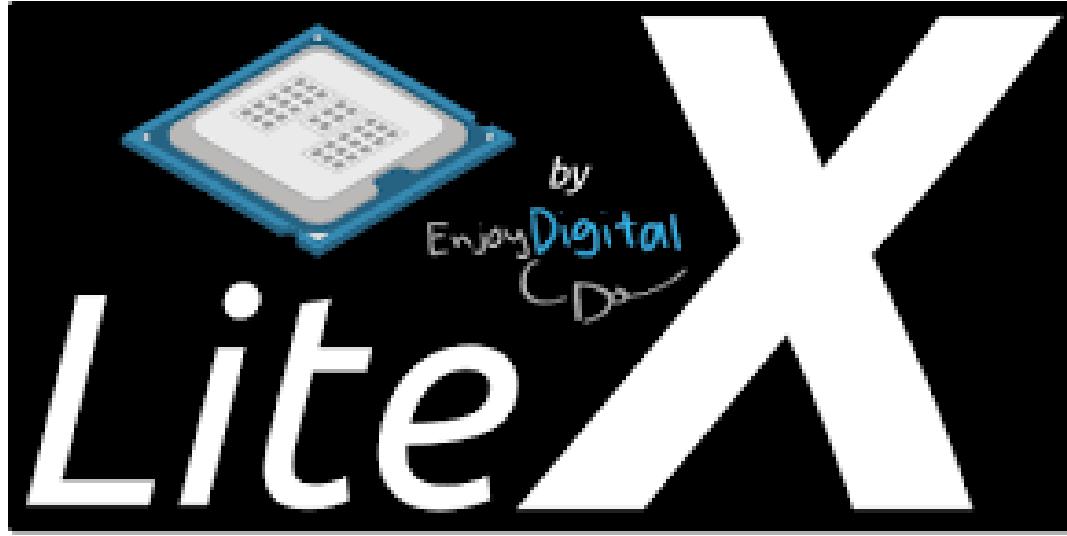
This is how a Linux capable core looks like on an
FPGA. [#nextpnratwork](#)





Build your hardware, easily!

- LiteX is a FPGA design/SoC builder that can be used to build cores, create SoCs and full FPGA designs.
- LiteX is based on Migen and provides specific building/ debugging tools for a higher level of abstraction and compatibility with the LiteX core ecosystem.
- Think of Migen as a toolbox to create FPGA designs in Python and LiteX as a SoC builder to create/develop/debug FPGA SoCs in Python
- <https://github.com/enjoy-digital/litex>

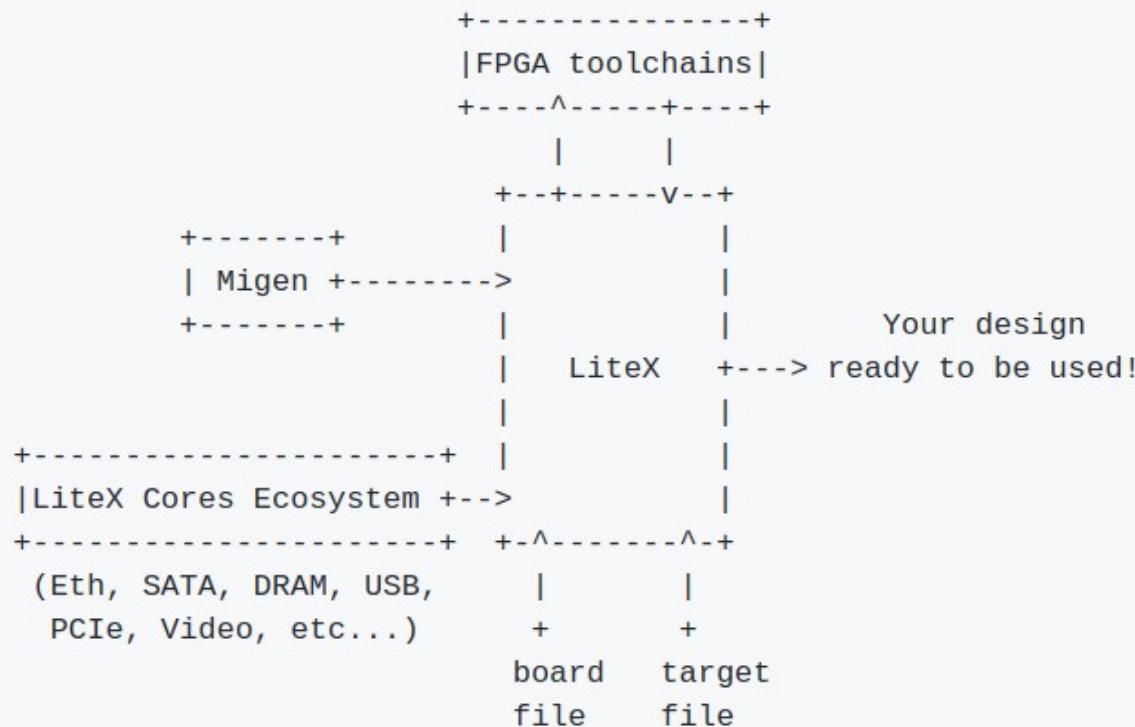


Build your hardware, easily!

- Bunnie:
LiteX vs. Vivado: First Impressions

<https://www.bunniestudios.com/blog/?p=5018>

Typical LiteX design flow:



LiteX already supports various softcores CPUs: LM32, Mor1kx, PicoRV32, VexRiscv and is compatible with the LiteX's Cores Ecosystem:

Name	Build Status	Description
LiteDRAM	build passing	DRAM
LiteEth	build passing	Ethernet
LitePCIe	build passing	PCIe
LiteSATA	build passing	SATA

Linux on LiteX-VexRiscv

- Linux with VexRiscv CPU, a 32-bits Linux Capable RISC-V CPU written in Spinal HDL
- SoC around the VexRiscv CPU is created using LiteX as the SoC builder and LiteX's cores written in Migen Python DSL (LiteDRAM, LiteEth, LiteSDCard)
- github.com/litex-hub/linux-on-litex-vexriscv

```
michael@reactor: ~/projects/litex/lin...
```

```
michael@reactor: ~/projects/litex/lin...
```

```
Welcome to Buildroot  
buildroot login: root
```



```
32-bit VexRiscv CPU with MMU integrated in a LiteX SoC
```

```
login[55]: root login on 'console'
```

```
root@buildroot:~# ps
```

PID	USER	COMMAND
1	root	init
2	root	[kthreadd]
3	root	[kworker/0:0-eve]
4	root	[kworker/0:0H]
5	root	[kworker/u2:0-ev]
6	root	[mm_percpu_wq]
7	root	[ksoftirqd/0]
8	root	[kdevtmpfs]
9	root	[oom_reaper]
10	root	[writeback]
11	root	[kcompactd0]
12	root	[kblockd]
13	root	[kworker/0:1]
14	root	[kswapd0]
34	root	/sbin/klogd -n
55	root	-sh
56	root	[kworker/u2:1]
58	root	ps

```
root@buildroot:~# uname -a
```

Slides: <https://github.com/pdp7/talks/blob/master/oshw-36c3.pdf>



Section:
Open Source and Chip Design

What about open source chips?



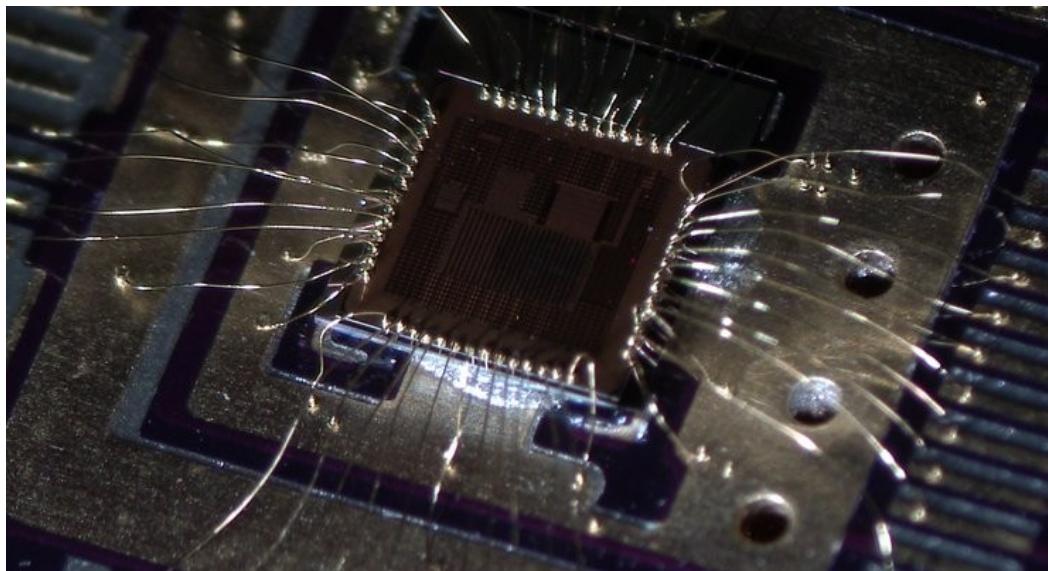
- **RISC-V: Free and Open RISC Instruction Set Arch**
 - “new instruction set architecture (ISA) that was originally designed to support computer architecture research and education and is now set to become a standard open architecture for industry”
 - Video: [Instruction Sets Want To Be Free: A Case for RISC-V](#)
 - Video: [Krste Asanovic presents](#) at RISC-V and Open Source Silicon Event in Munich on March 23, 2017

What about open source chips?



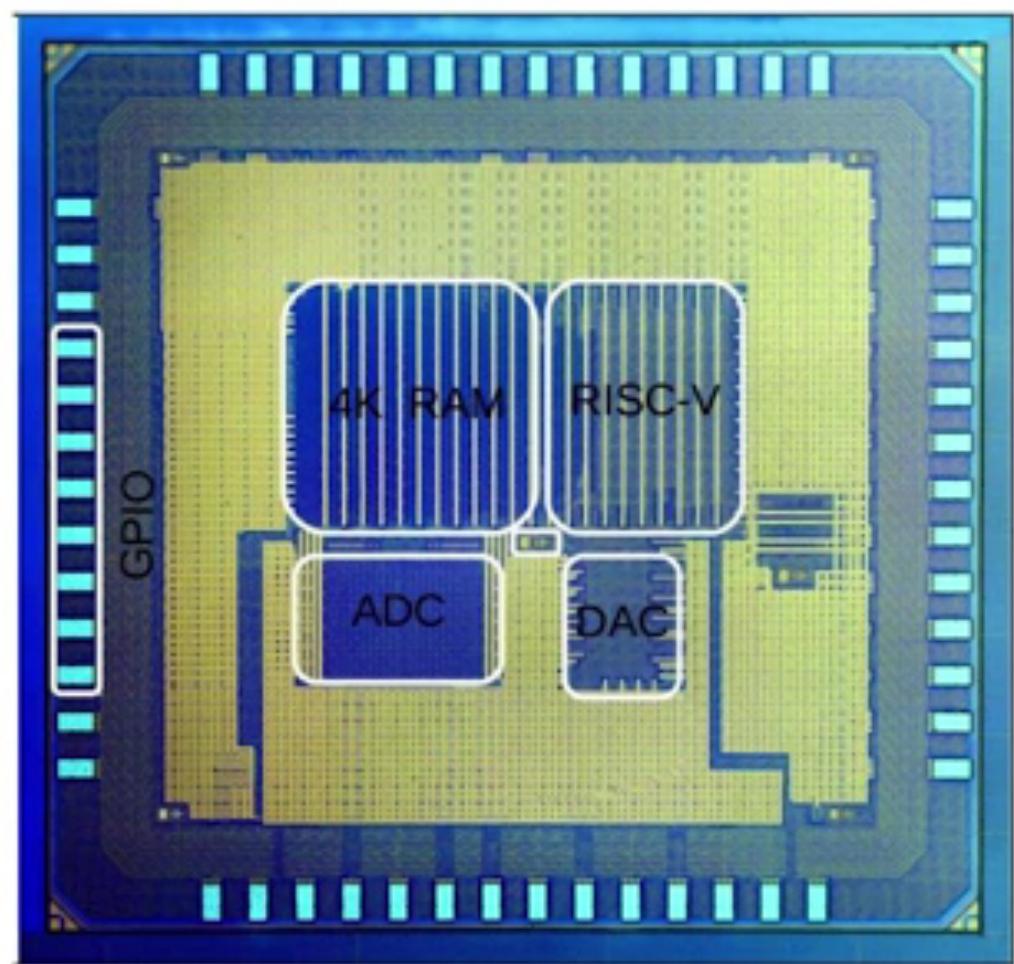
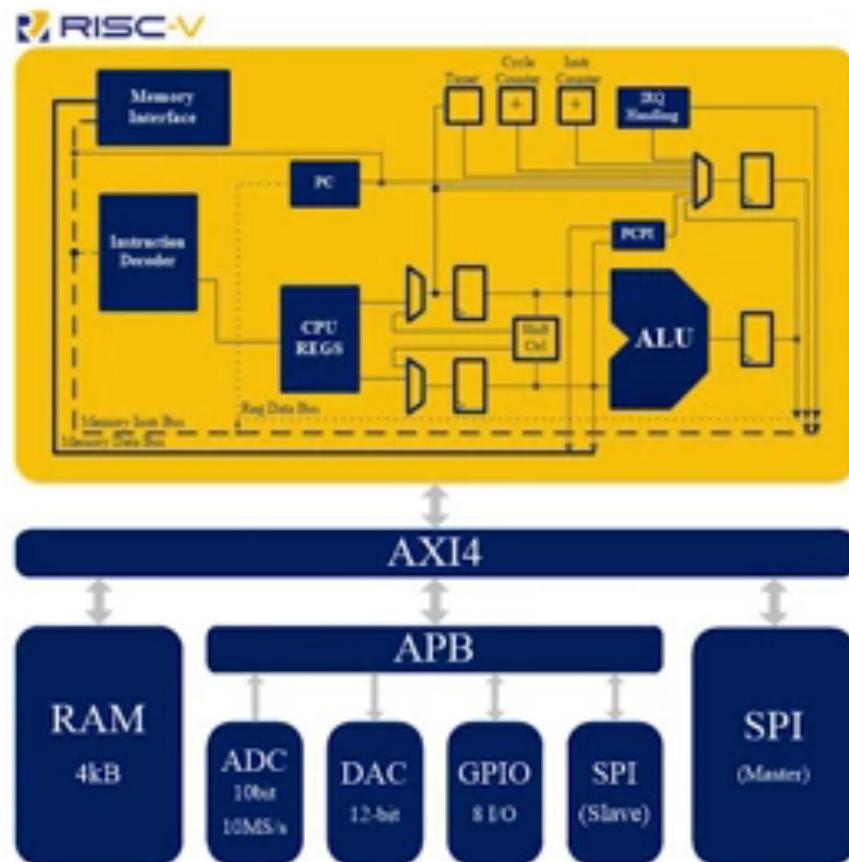
- [OnChip Open-V](#)

“completely free (as in freedom) and open source 32-bit microcontroller based on the RISC-V architecture”



OnChip Open-V

A 32-bit RISC-V based Microcontroller



OnChip Open-V

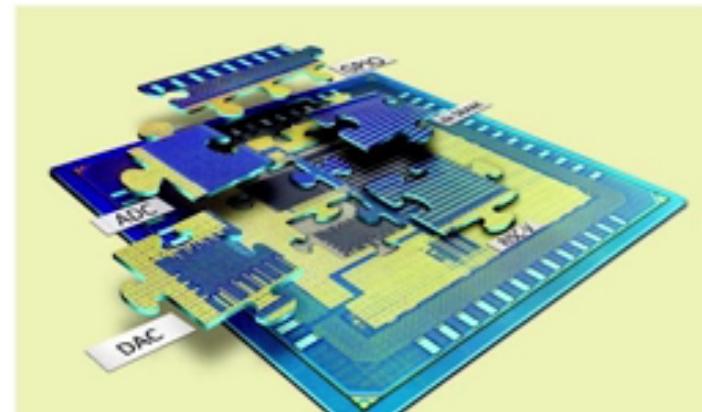


- Crowd Supply update: [A Taste of Chip Design](#)
- Video: [YoPuzzle: mRISC V development platform](#)
- Video: [RISC-V Community needs Peripheral Cores](#)

Good to have an Open ISA. What about Peripheral?



- IP vendors have IP based on previous customer. **Hard to get** a glue-and-play that works for your SoC. → \$\$\$
- There are some std, such as PHYs: USB, LPDDR, PCIe, AMBA
BUT
no for clocking circuitry, biasing, GPIO
For instance a simple Power-on-Reset can hit your pocket, just because!
- Buses IP are out there but expensive.

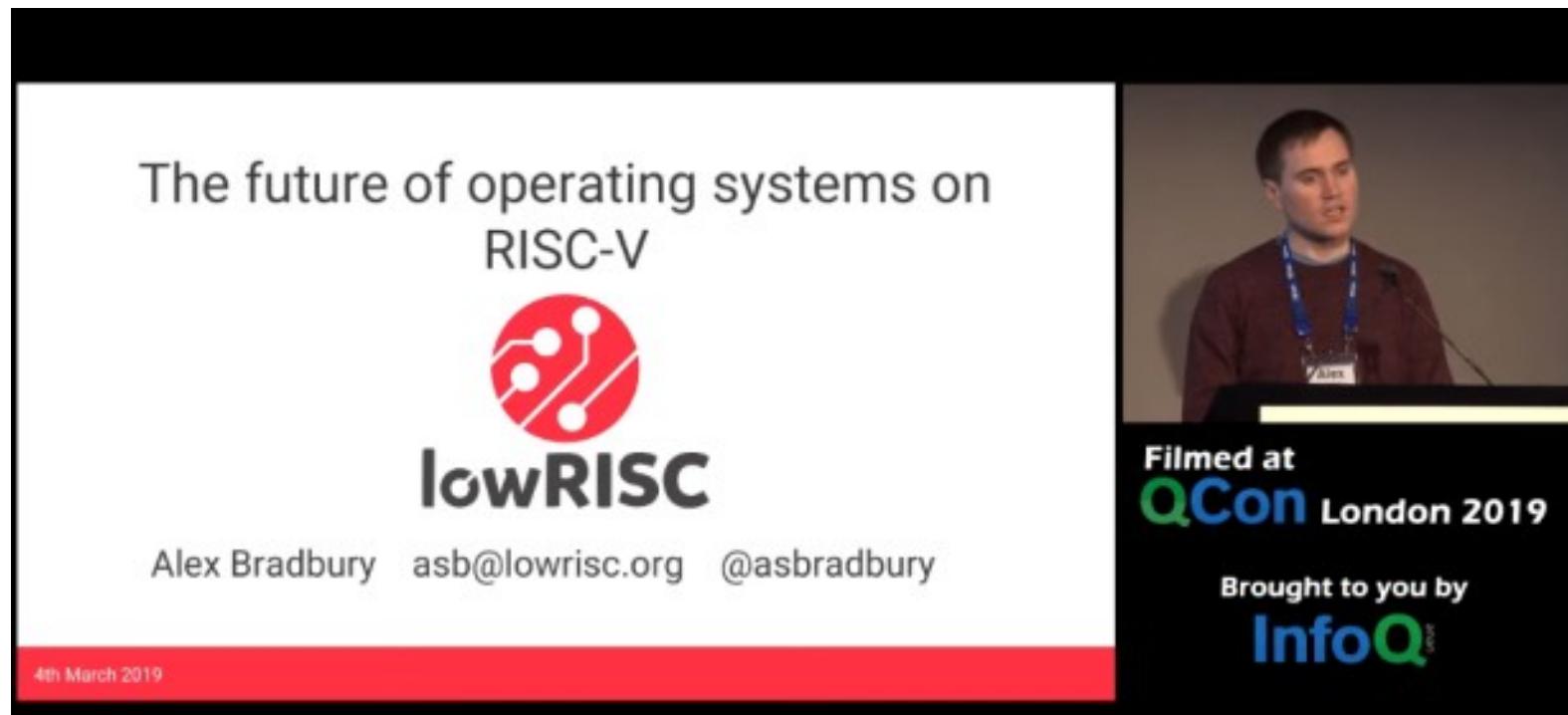


Open Source chip design

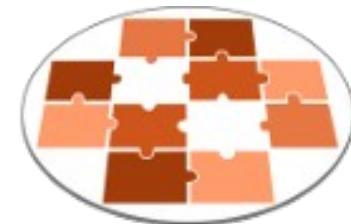


- lowRISC:
“creating a fully open-sourced, Linux-capable, RISC-V-based SoC, that can be used either directly or as the basis for a custom design”
- Video: [Rob Mullins talking about lowRISC](#)
(RISC-V & Open Source Silicon Event in Munich on March 23, 2017)
- [Laura James](#) from lowRISC is here!

- The Future of Operating Systems on RISC-V
 - Alex Bradbury gives an overview of the status and development of RISC-V as it relates to modern operating systems, highlighting major research strands, controversies, and opportunities to get involved.
 - <https://www.youtube.com/watch?v=emnN9p4vhzk>



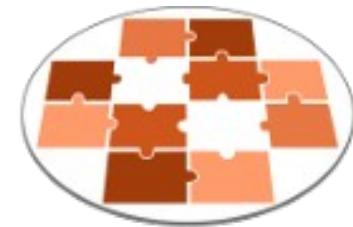
Open Source chip design



FOSSi
Foundation

- [FOSSi Foundation](#)
 - The Free and Open Source Silicon Foundation
 - “non-profit foundation with the mission to promote and assist free and open digital hardware designs”
 - “FOSSi Foundation operates as an open, inclusive, vendor-independent group.”

Open Source chip design

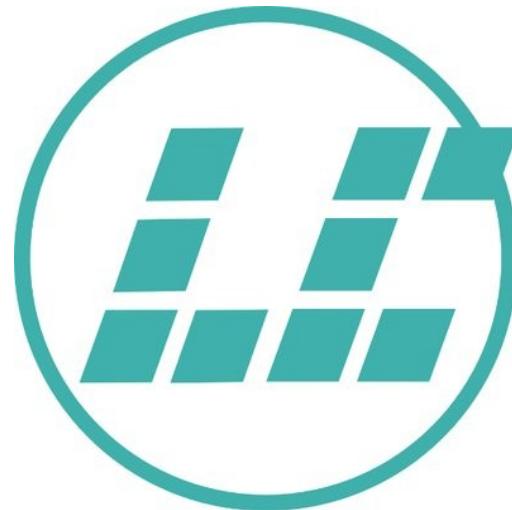


FOSSi
Foundation

- Open Source Silicon Design Ecosystem
 - Talk by FOSSi co-founder Julius Baxter



Open Source chip design



- **LibreCores**
 - Project of the FOSSi Foundation
 - “**gateway to free and open source digital designs** and other components that you can use and **re-use in your digital designs**”
 - “advances the idea of OpenCores.org”

Latch-Up Conf 2019 videos



Latch-Up 2020 will be

April 11-12 Cambridge MA, USA, at MIT

Week of Open Source Hardware

The video player displays a slide with the following content:

History

- March 2011: CERN OHL 1.0
- July 2011: CERN OHL 1.1
- September 2013: CERN OHL 1.2
- 2017: CERN OHL 2, beta 1
- 2019 : CERN OHL 2, beta 2

Below the slide, the video player interface shows:

CERN Open Hardware Licence 2.0
80 views

Like 3 | Dislike 0 | Share | Save | ...

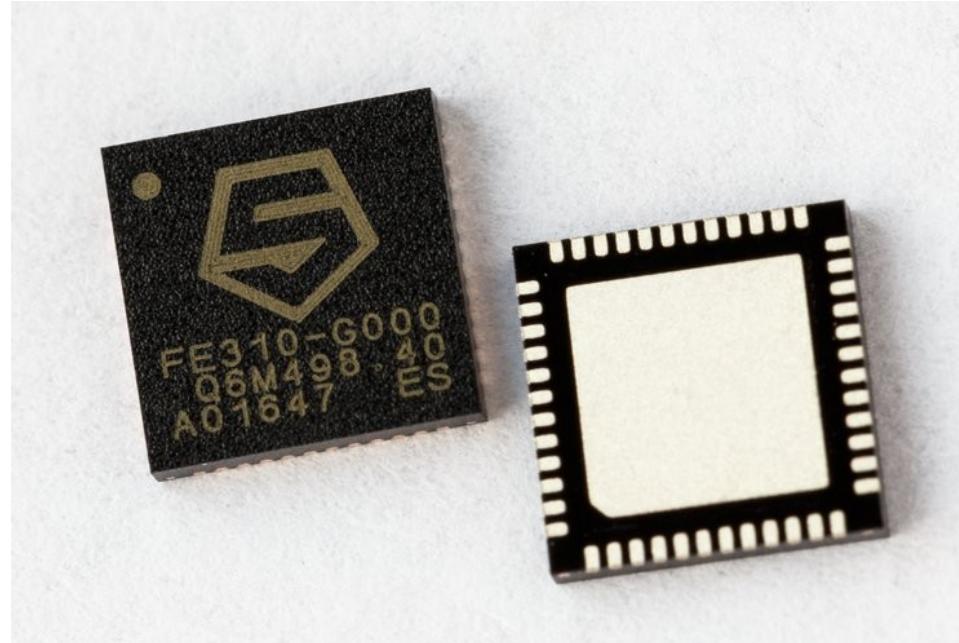


FOSSI Foundation

Published on Jun 20, 2019

SUBSCRIBE 654

SiFive



- “founded by the creators of the free and open RISC-V architecture as a reaction to the end of conventional transistor scaling and escalating chip design costs”

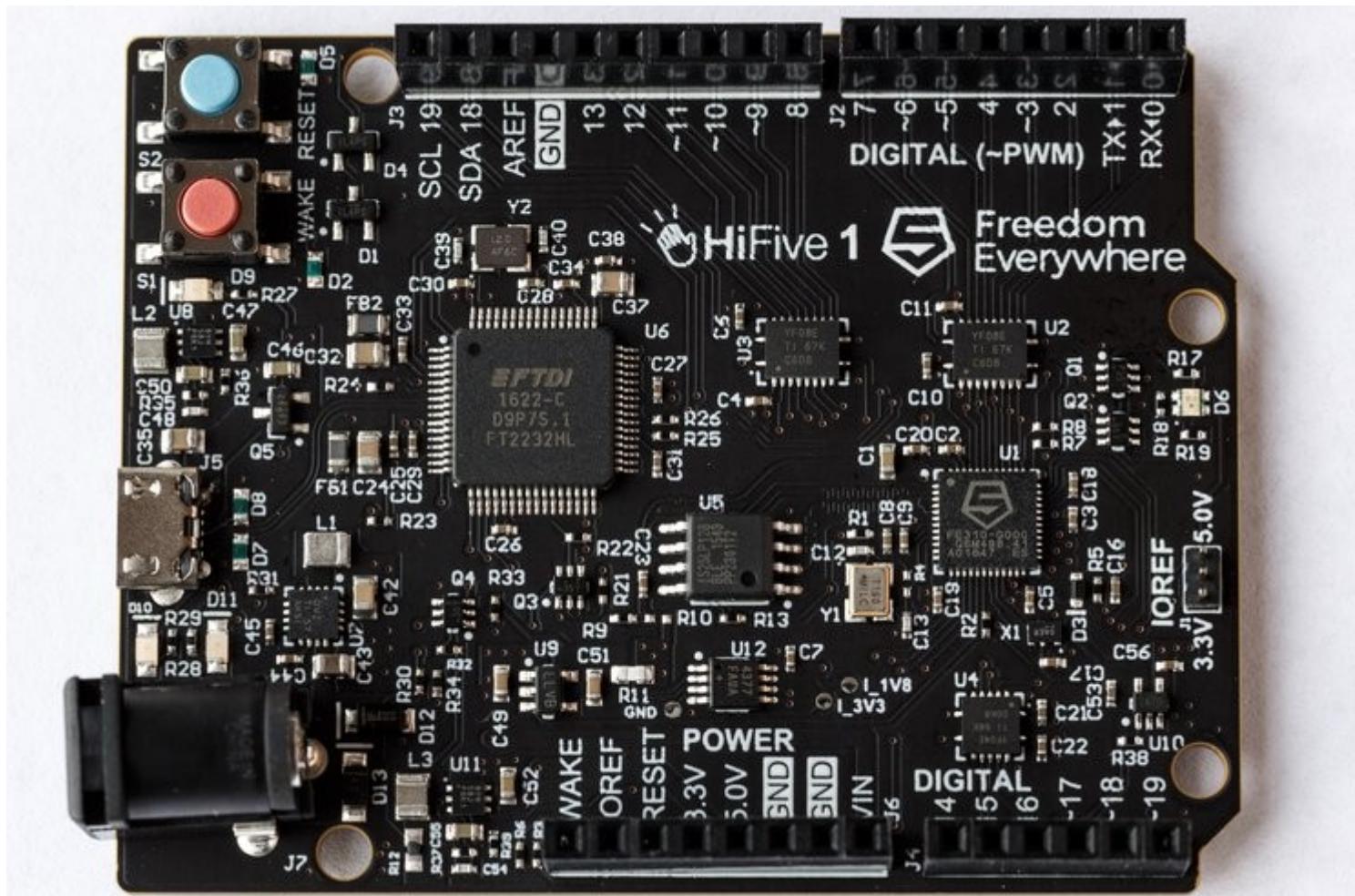
RISC-V ecosystem

- RISC-V Keynote at Embedded Linux Conf
 - March 12th, 2018
 - Yunsup Lee, Co-Founder and CTO, SiFive
 - Designing the Next Billion Chips: How RISC-V is Revolutionizing Hardware



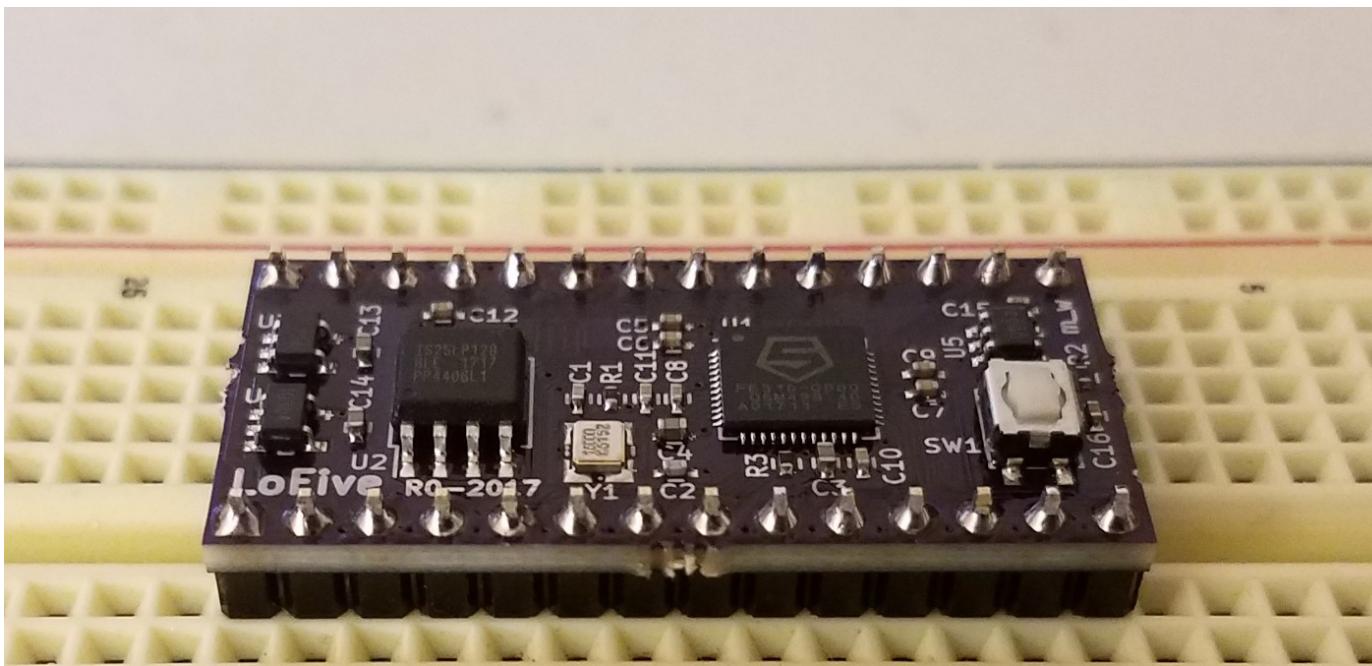
SiFive FE310 microcontroller

- **HiFive1**: Arduino-Compatible RISC-V Dev Kit



SiFive FE310 microcontroller

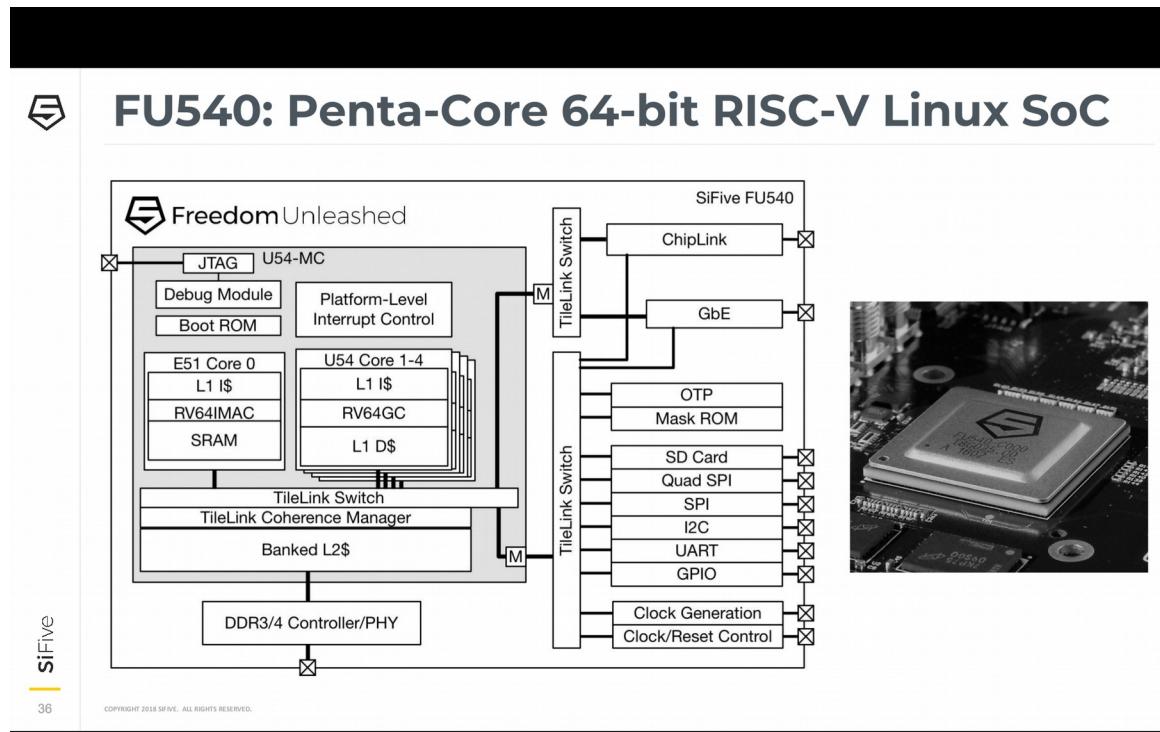
- [LoFive](#) designed by [Michael Welling](#)
(QWERTY Embedded Design)
- Lower cost eval board for SiFive FE310.
- [Open Source Hardware design files](#)
- Sold as group buy on [GroupGets](#)



SiFive: Linux on RISC-V

- FOSDEM 2018 talk

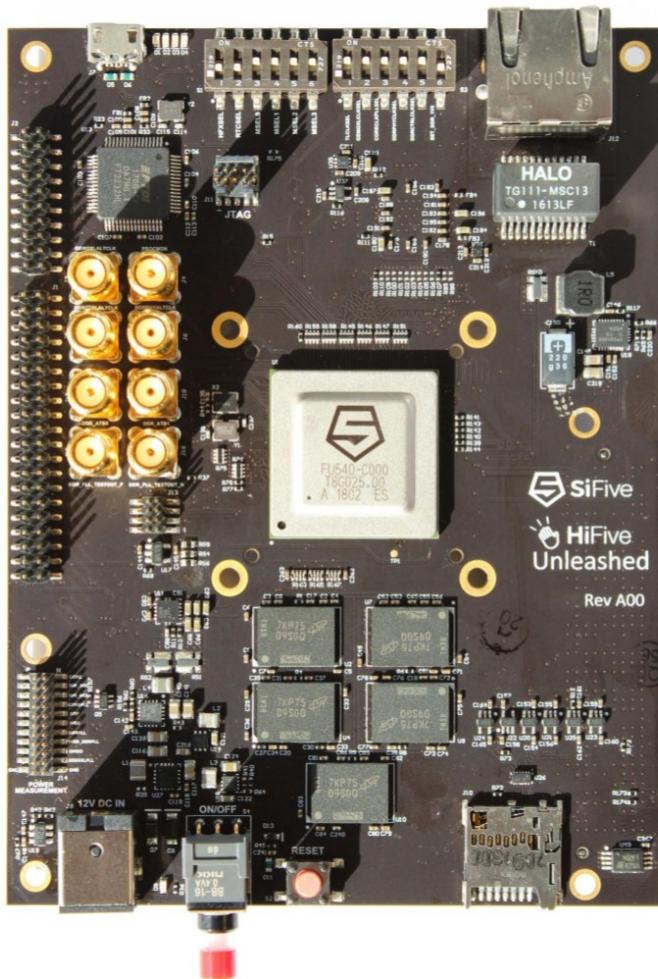
- YouTube: “Igniting the Open Hardware Ecosystem with RISC-V: SiFive's Freedom U500 is the World's First Linux-capable Open Source SoC Platform”
- Interview with Palmer Dabbelt of SiFive



SiFive: Linux on RISC-V



HiFive Unleashed



- World's First Multi-Core RISC-V Linux Development Board
 - SiFive FU540-C000 (built in 28nm)
 - 4+1 Multi-Core Coherent Configuration, up to 1.5 GHz
 - 4x U54 RV64GC Application Cores with Sv39 Virtual Memory Support
 - 1x E51 RV64IMAC Management Core
 - Coherent 2MB L2 Cache
 - 64-bit DDR4 with ECC
 - 1x Gigabit Ethernet
 - 8 GB 64-bit DDR4 with ECC
 - Gigabit Ethernet Port
 - 32 MB Quad SPI Flash
 - MicroSD card for removable storage
 - FMC connector for future expansion with add-in cards



RISC-V NOMMU and M-Mode Linux

Damien Le Moal, Western Digital

Linux Plumbers Conference, September 9th, 2019

- PDF: RISC-V NOMMU and M-mode Linux
- <https://www.youtube.com/watch?v=ycG592N9EMA&t=10394>
- jump to 2h 53m
- Many RISC-V Improvements Ready For Linux 5.5: M-Mode, SECCOMP, Other Features

- HOT CHIPS 2019: Linux RISC-V tutorial
- <https://youtu.be/nPXdbm9lc3A?t=6139>
- 1 hour 42 minutes
- Overview of RISC-V SW Ecosystem Bunnaroath Sou, SiFive



Getting Started

- Freedom Studio from [SiFive.com](https://sifive.com)

- or Freedom E SDK & Metal

- RISC-V on Qemu

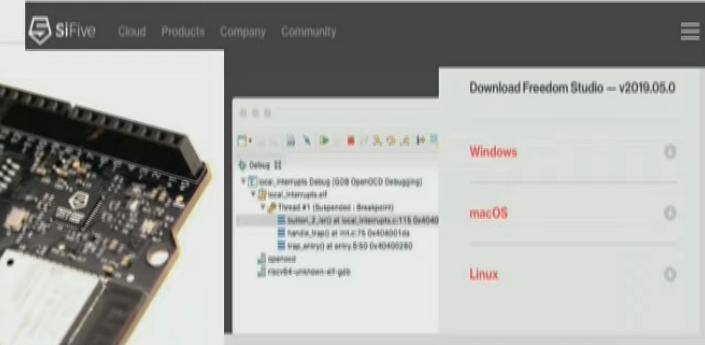
- <https://risc-v-getting-started-guide.readthedocs.io/en/latest/index.html>

- sw-dev@groups.riscv.org

To download and build QEMU from git:

- #riscv on freenode

```
git clone https://git.qemu.org/git/qemu.git
cd qemu
git submodule init
./configure --target-list=riscv64-softmmu
./configure
make
```



```
Starting udev
61.099000] udevd[95]: starting version 3.2.6
63.540000] udevd[96]: starting uudev-3.2.6
[115.688000] EXT4-fs (mochi0p2): re-mounted. Opts: data=ordered
hwclock: can't open '/dev/mmc rtc': No such file or directory
Wed Mar 14 27:45:11 UTC 2018
hwclock: can't open '/dev/mmc/rtc': No such file or directory
2NNI! Entering runlevel: 5
Configuring network interfaces... udhcpc: started, v1.27.2
udhcpc: sending discover
udhcpc: sending discover
udhcpc: sending discover
udhcpc: no lease, forking to background
done.
hwclock: can't open '/dev/mmc/rtc': No such file or directory
Starting syslogd/klogd: done

OpenEmbedded nodistro.0 riscv64 /dev/console

riscv64 login: root
root@riscv64:~# uname -a
Linux riscv64 4.15.0-yocto-standard #3 SMP Tue May 13 22:43:09 UTC 2018 riscv64 GNU/Linux
root@riscv64:~# python
Python 2.7.13 (default, Mar 14 2018, 17:00:24)
[GCC 7.3.0] on linux2
Type "help", "copyright", "credits" or "license" for more information.
>>> print 'Hello world'
Hello world
>>>
```



Fedora on RISC-V

Through the works of David Abdurachmanov

- ~20% of Fedora packages built for RISC-V
- Pre-build images available for Qemu and HiFive Unleashed
 - Build farm running, producing nightly images
- No signed RPM yet
- No images for Fedora Workstation/Server

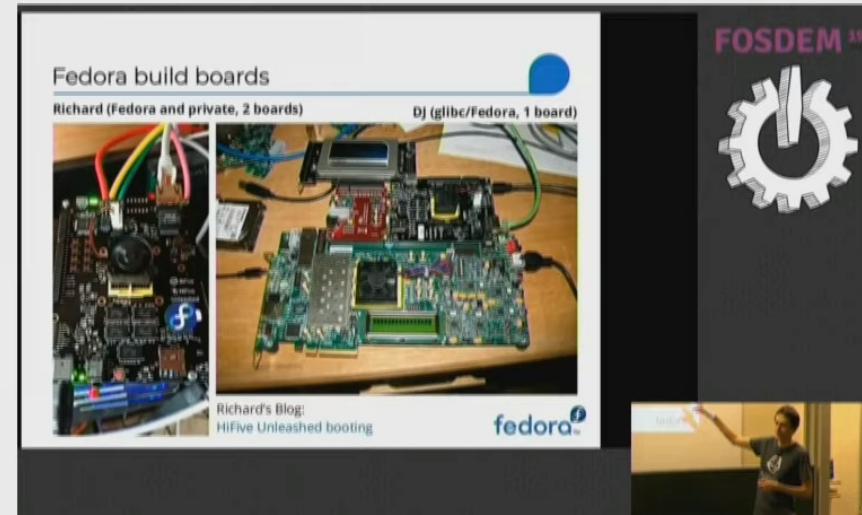


Want to know more/get involve, see

- <https://fedoraproject.org/wiki/Architectures/RISC-V>

Interest to try it out,

- Self Hosting images available
- <https://fedoraproject.org/wiki/Architectures/RISC-V/Installing>





RISC-V Linux Early Boot

Linux boots expects the system to be in the following state

- a0 contains a unique per-hart id
- a1 contains a pointer to device tree, as a binary flattened device tree (DTB)
- Memory is identity mapped
- The kernel's ELF image has been loaded correctly
- Handle impedance mismatch between RISC-V spec and what Linux expects
- Perform "hart lottery," which is a very short AMO-based sequence that picks the first hart to boot, while the rest spin, until they can proceed

Proceed with a fairly standard Linux early boot process:

- A linear mapping of all physical memory is set up, with PAGE_OFFSET as the offset
- Paging structures are initialized and then used (BBL boots with paging enabled)
- The C runtime is set up, which includes the stack and global pointers
- A spin-only trap vector is set up that catches any errors early in the boot process
- `start_kernel` is called to enter the standard Linux boot process

Coming in 2020?

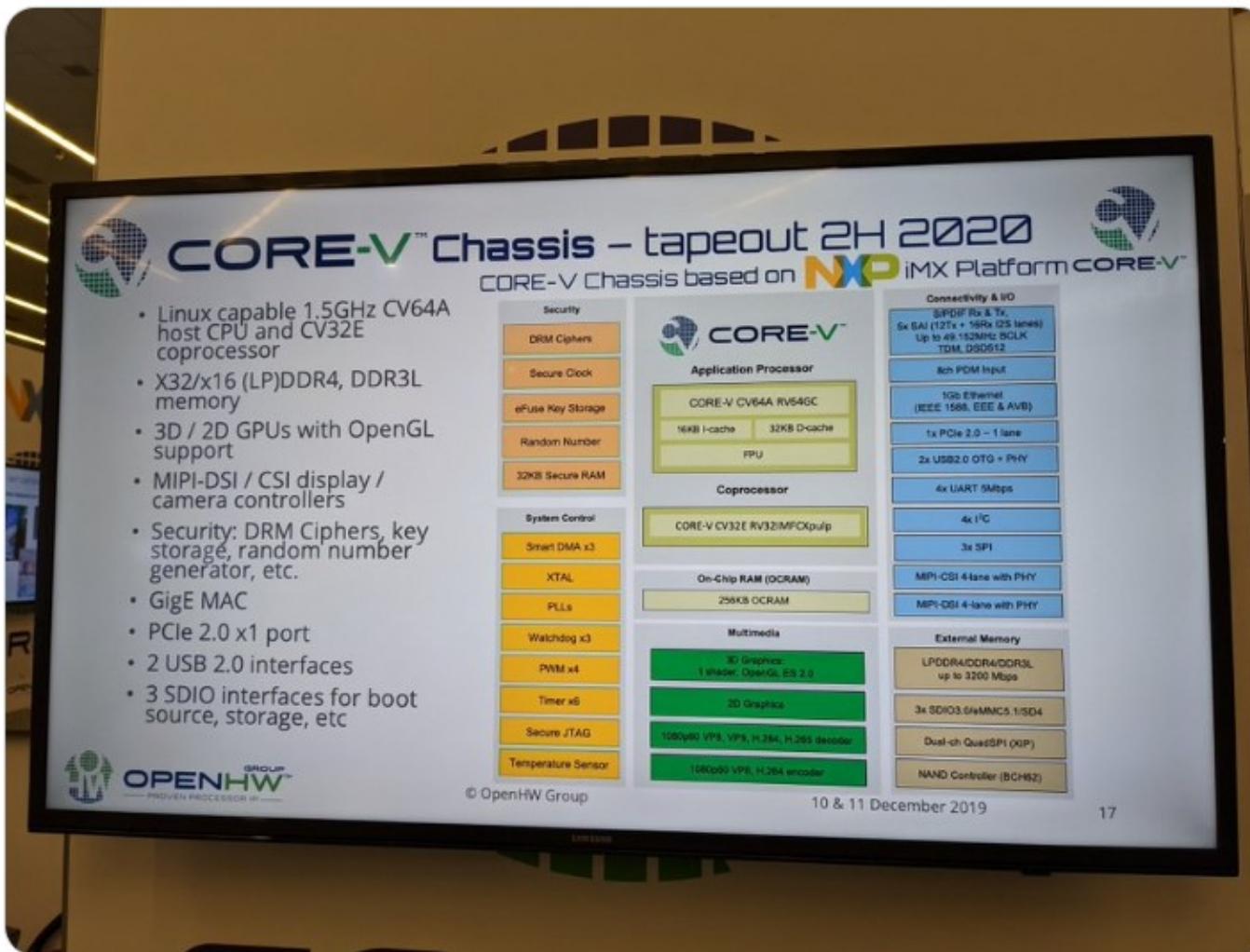
- OpenHW Group Unveils CORE-V Chassis SoC Project, Building on PULP Project IP
 - <https://abopen.com/news/openhw-group-unveils-core-v-chassis-soc-project-building-on-pulp-project-ip/>
 - “The design in question is based on the NXP i.MX platform, and features a CV64A 64-bit core running at up to 1.5GHz and built on the RV64GC RISC-V core IP from the PULP Platform; this is then partnered with a lower-power VC32E coprocessor, based on the PULP Platform’s RV32IMFCXpulp IP.”



Karim Yaghmour
@karimyaghmour

▼

Spotted at RISC V summit: an iMX chip where the ARM core was ripped out and replaced with a RISC V/PULP - just wow



17

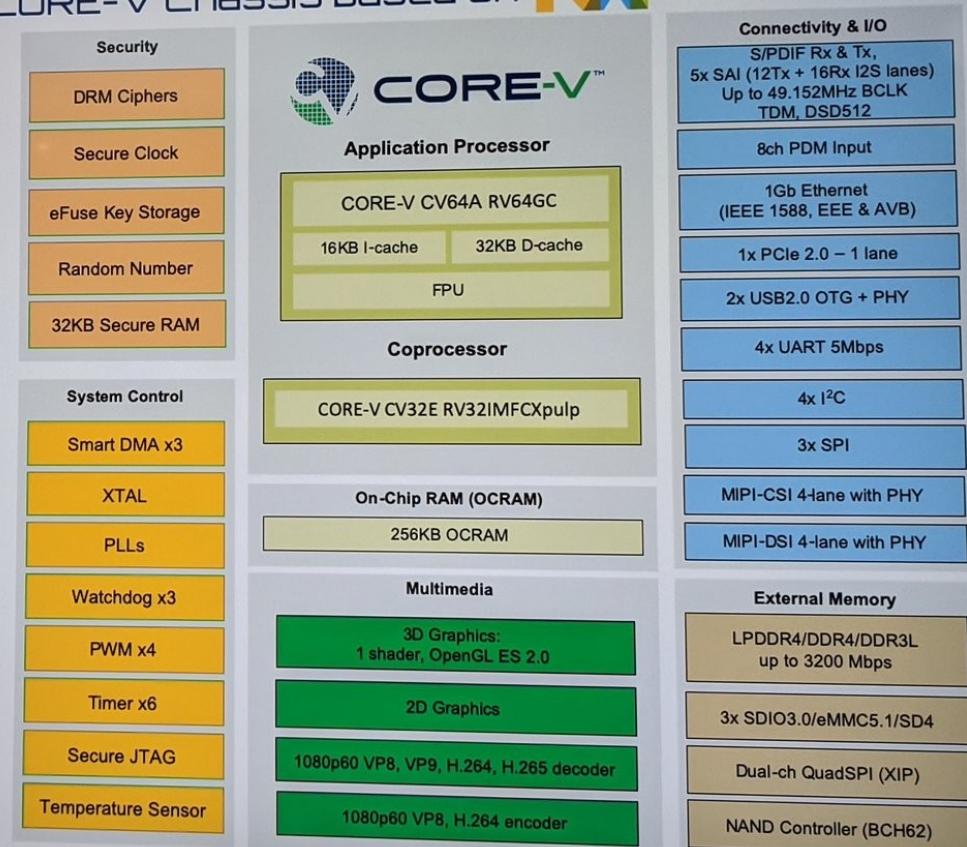


CORE-V™ chassis – tapeout 2H 2020



CORE-V Chassis based on **NXP** iMX Platform **CORE-V**

- Linux capable 1.5GHz CV64A host CPU and CV32E coprocessor
- X32/x16 (LP)DDR4, DDR3L memory
- 3D / 2D GPUs with OpenGL support
- MIPI-DSI / CSI display / camera controllers
- Security: DRM Ciphers, key storage, random number generator, etc.
- GigE MAC
- PCIe 2.0 x1 port
- 2 USB 2.0 interfaces
- 3 SDIO interfaces for boot source, storage, etc



© OpenHW Group

10 & 11 December 2019

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OSHW RISC-V Linux board for less than \$100?

- Goal: Sub-\$100 Open Source Hardware board that can run Linux on RISC-V
- Possible by 37c3?
- Interested in working together?
 - drew@oshpark.com / Twitter: [@pdp7](https://twitter.com/pdp7)
 - create a mailing list?

Slides:

github.com/pdp7/talks/blob/master/oshw-linux-36c3.pdf

Drew Fustini
drew@oshpark.com
@pdp7 / @oshpark



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