

Slides: <https://github.com/pdp7/talks/blob/master/fosdem20.pdf>

How to run Linux on RISC-V

with open hardware and open source FPGA tools

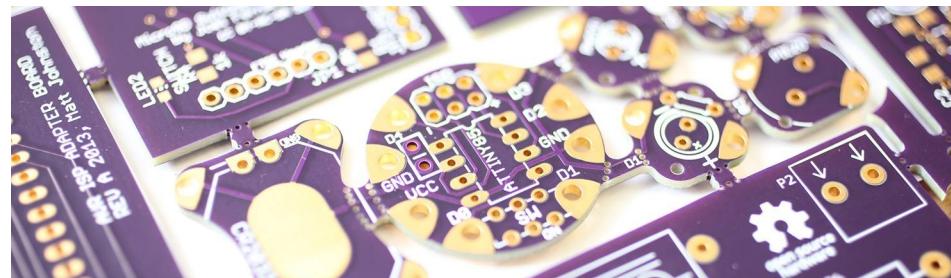
FOSDEM (2020-02-02)



Drew Fustini

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- Open Source Hardware designer at OSH Park
 - PCB manufacturing service in the USA
 - drew@oshpark.com / Twitter: [@oshpark](https://twitter.com/@oshpark)
- Volunteer Member of Board of Directors of BeagleBoard.org Foundation
 - small open source Linux boards
 - drew@beagleboard.org
- Volunteer Member of the Board of Directors of the Open Source Hardware Association (OSHWA)
 - Open Source Hardware Certification Program: <https://certification.oshwa.org/>

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You're going to this event!

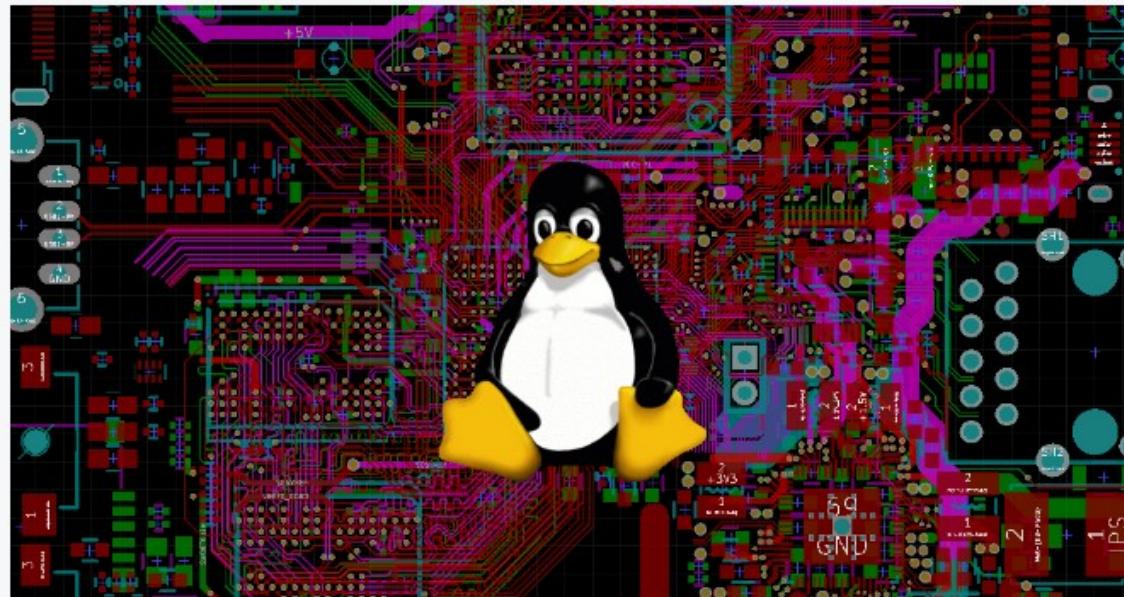
Wednesday, February 12, 2020

Berlin Embedded Linux Meetup



Hosted by

Drew Fustini and mntmn

[Share](#)[Organizer tools](#)**Berlin Embedded Linux
Meetup**Public group [?](#)

Wednesday, February 12, 2020
7:00 PM to 9:00 PM
[Add to calendar](#)

MNT Research GmbH
Fehlerstraße 8 · Berlin

Wed, Feb 12 · 7:00 PM
Berlin Embedded Linux Meetup

You're going!
[Edit RSVP](#)

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Open Hardware Summit 2020 in NYC (USA)
on March 13th (Friday)
<https://2020.oshwa.org/>

Special Edition:
10th Anniversary
of Open Hardware Summit





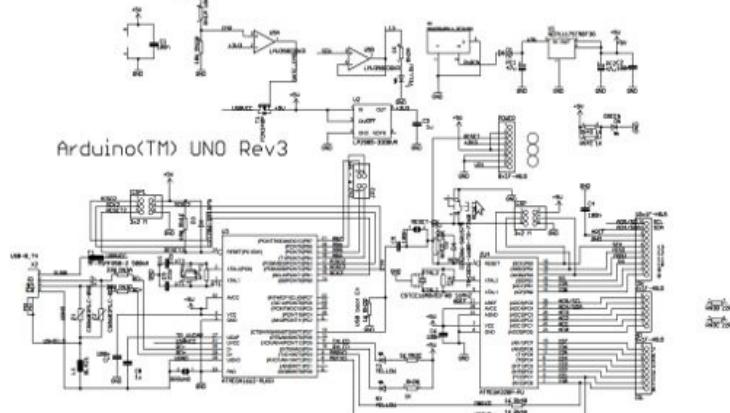
Statement of Principles:

Hardware whose **design** is made **publicly available** so that anyone can **study, modify, distribute, make,** and **sell** the design or hardware based on that design

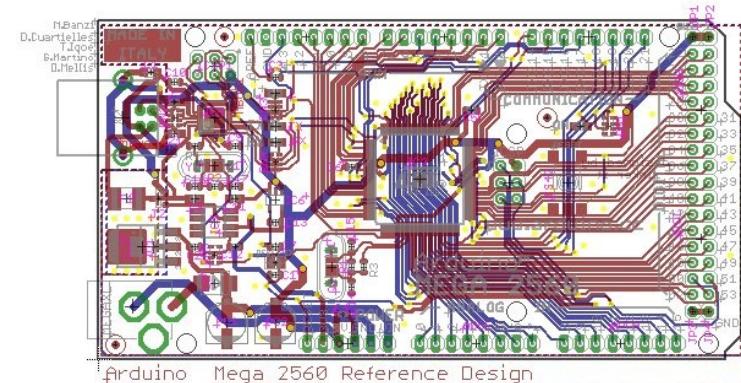


Documentation required for electronics:

Schematics



Board Layout



Editable source files for CAD software such as KiCad or EAGLE

Bill of Materials (BoM)

Not strict requirement, but best practice is for all components available from distributors in **low quantity**

36c3 talk: Linux on Open Source Hardware with Open Source chip design



CERN Open Hardware Licence

- Originally written for **CERN** designs hosted in the **Open Hardware Repository**
- Can be used by **any designer** wishing to **share design** information using a **license compliant** with the **OSHW definition criteria**.
- [**CERN OHL version 1.2**](#)
Contains the license itself and a guide to its usage



Slides: <https://github.com/pdp7/talks/blob/master/fosdem20.pdf>



Section:
RISC-V

the instruction set for everything?

- When you write a program in the Arduino IDE, it is compiled into instructions for the microcontroller to execute.
- How does the compiler know what instructions the chip understands?
 - defined by the **Instruction Set Architecture**
 - The **ISA** is a standard, a set of rules that define the tasks the processor can perform.
 - Examples: x86 (Intel/AMD) and ARM
 - Both are proprietary and need commercial licensing



- **RISC-V: Free and Open RISC Instruction Set Arch**
 - “new instruction set architecture (ISA) that was originally designed to support computer architecture research and education and is now set to become a standard open architecture for industry”



- **RISC-V: Free and Open RISC Instruction Set Arch**
 - Instruction Sets Want To Be Free: A Case for RISC-V
 - David Patterson, UC Berkeley – *co-creator of the original RISC!*
 - <https://www.youtube.com/watch?v=mD-njD2QKN0>
 - **RISC-V Summit 2019: State of the Union**
 - Krste Asanovic, UC Berkeley
 - https://www.youtube.com/watch?v=jdkFi9_Hw-c



State of the Union

Krste Asanovic

UC Berkeley, RISC-V Foundation, & SiFive Inc.

krste@berkeley.edu

RISC-V Summit
San Jose Convention Center, CA, USA
December 10, 2019

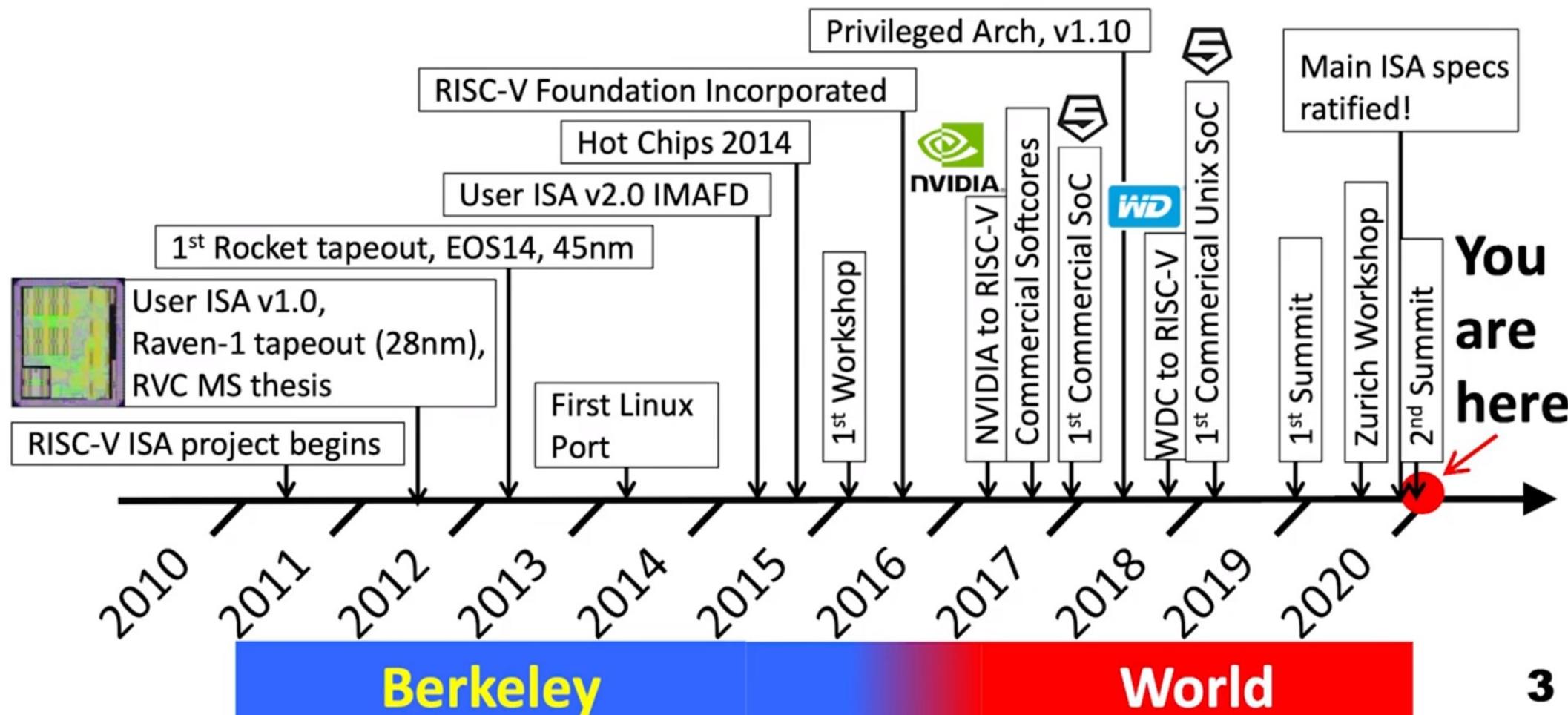


What's Different about RISC-V?

- ***Simple***
 - Far smaller than other commercial ISAs
- ***Clean-slate design***
 - Clear separation between user and privileged ISA
 - Avoids μarchitecture or technology-dependent features
- A ***modular*** ISA designed for ***extensibility/specialization***
 - Small standard base ISA, with multiple standard extensions
 - Sparse and variable-length instruction encoding for vast opcode space
- ***Stable***
 - Base and standard extensions are frozen
 - Additions via optional extensions, not new versions
- ***Community designed***
 - With leading industry/academic experts and software developers



RISC-V Timeline





RISC-V Ecosystem

Open-source software:

Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, ...

Commercial software:

Lauterbach, Segger, IAR, Micrium, ExpressLogic, Ashling, AntMicro, Imperas, UltraSoC ...

Software



ISA specification

Golden Model

Compliance

Hardware

Open-source cores:

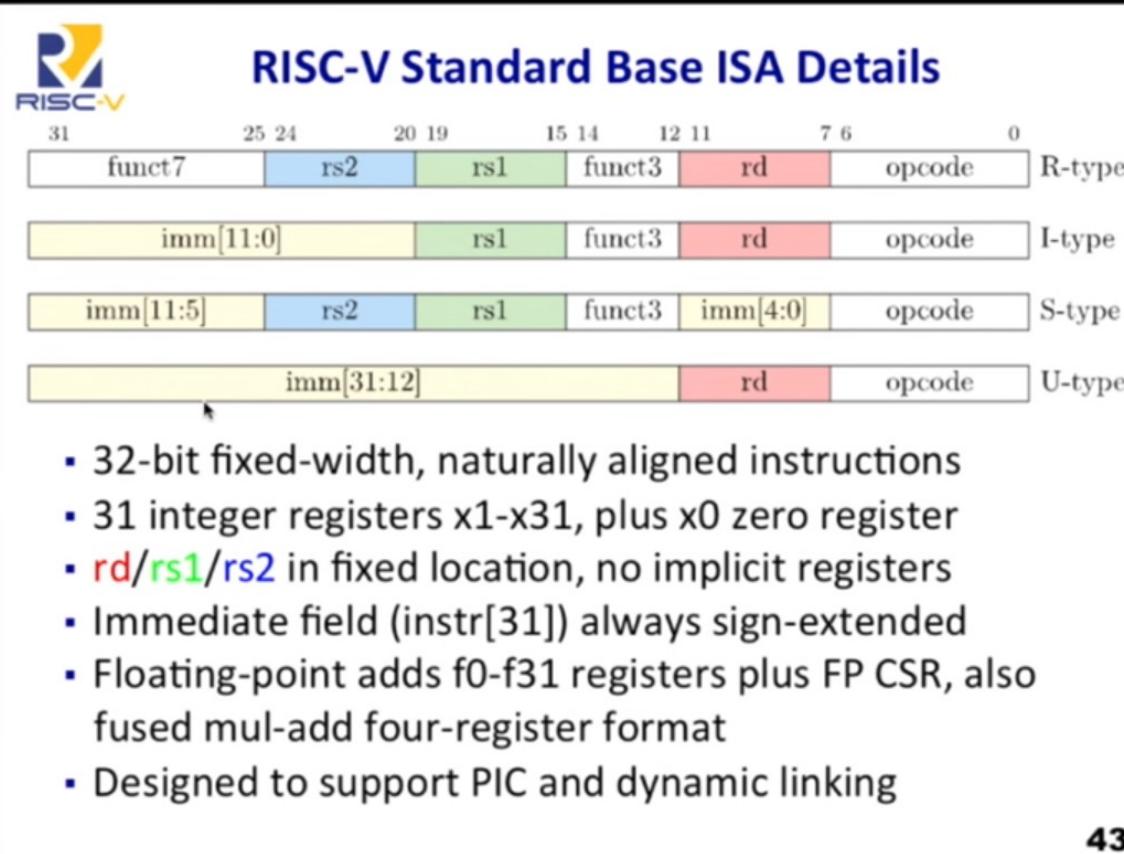
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Shakti, Serv, Swerv, Hummingbird, ...

Commercial core providers:

Alibaba, Andes, Bluespec, Cloudbear, Codasip, Cortus, InCore, Nuclei, SiFive, Syntacore, ...

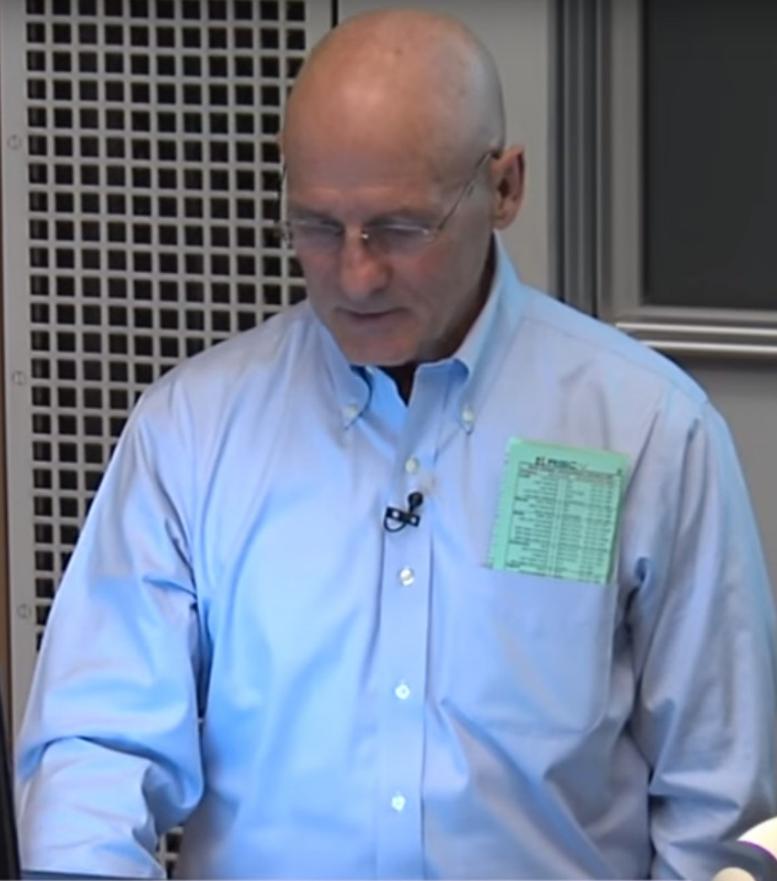
Inhouse cores:

Nvidia, WD, +others





RV32I			
① RISC-V Reference Card			
Base Integer Instructions (32-bit/64-bit/128-bit Base)			
Category Name Format RV32I/32(64)/128(128)			
Loads			
Load Byte	I	LB	r1,r2,r3,imm
Load Halfword	I	LH	r1,r2,r3,imm
Load Word	I	LW (D/I/Q)	r1,r2,r3,imm
Load Byte Unsigned	I	LBU	r1,r2,r3,imm
Load Half Unsigned	I	LHU (W/D/Q)	r1,r2,r3,imm
Stores			
Store Byte	S	SB	r1,r2,r3,imm
Store Halfword	S	SH	r1,r2,r3,imm
Store Word	S	SW (D/Q)	r1,r2,r3,imm
Shifts			
Shift Left	R	SLLI (W/D)	r1,r2,r3,r4
Shift Left Immediate	I	SLSLT (W/D)	r1,r2,r3,shamt
Shift Right	R	SLR (W/D)	r1,r2,r3,r4
Shift Right Immediate	I	SLSLT (W/D)	r1,r2,r3,shamt
Shift Right Arithmetic	R	SLRA (W/D)	r1,r2,r3,r4
Shift Right Arithmetic Immediate	I	SLSLT (W/D)	r1,r2,r3,shamt
Arithmetic			
ADD	R	ADD (I/W/D)	r1,r2,r3,r4
ADD Immediate	I	ADDI (I/W/D)	r1,r2,r3,imm
Subtract	R	DSUB (I/W/D)	r1,r2,r3,r4
Load Upper Imm.	U	LDU	r1,imm
Load Upper Imm. to DC	U	LDUDC	r1,imm
Logical			
XOR	R	XOR	r1,r2,r3,r4
XOR Immediate	I	XORI	r1,r2,r3,imm
OR	R	OR	r1,r2,r3,r4
OR Immediate	I	ORI	r1,r2,r3,imm
AND	R	AND	r1,r2,r3,r4
AND Immediate	I	ANDI	r1,r2,r3,imm
Compare			
Set <	R	SLT	r1,r2,r3,r4
Set < Immediate	I	SLTI	r1,r2,r3,imm
Set < Unsigned	R	SLTU	r1,r2,r3,r4
Set < Unsigned Immediate	I	SLTUI	r1,r2,r3,imm
Branches			
Branch =	S	BNE	r1,r2,r3,imm
Branch =	S	BNEQ	r1,r2,r3,imm
Branch =	S	BNEQZ	r1,r2,r3,imm
Branch =	S	BNEQNZ	r1,r2,r3,imm
Branch <	S	BLT	r1,r2,r3,imm
Branch < Unsigned	S	BLTU	r1,r2,r3,imm
Branch < Unsigned Immediate	S	BLTUI	r1,r2,r3,imm
Jump & Link			
Jump & Link	BL	BL	r1,imm
Jump & Link Register	BLR	BLR	r1,r2,r3,imm
Systm			
Sync Thread	I	FENCE	
Sync Inst & Data	I	FENCE.I	
System			
System CALL	I	ECALL	
System BREAK	I	EBREAK	
Counters			
Read CYCLE	I	RCYCLE	#0
Anti-CYCLE upper Half	I	RCYCLESU	#0
Anti-CYCLE lower Half	I	RCYCLESL	#0
Read TIME	I	RTIME	#0
Read TIME upper Half	I	RTIMESU	#0
Read TIME lower Half	I	RTIMESL	#0
Read INSTR Retired	I	RICNTRMT	#0
Read INSTR upper Half	I	RICNTRMTH	#0



Dave Patterson
UC BERKELEY



Instruction Sets Want To Be Free: A Case for RISC-V

RV32I / RV64I / RV128I + M, A, F, D, Q, C									
RISC-V "Green Card"									
RISC-V Reference Card									
Base Integer Instructions: RV32I(RV32I)					RV Privileged Instructions: RV32I(RV32I)				
Category Name Format RV32I(RV32I) Base					Category Name Format RV32I(RV32I)				
Loads									
Load	L	LB	0x0000_0000	rd,rw,lr	Load	L	0x0000_0000	rd,rw,lr	Load
Load Halfword	LH	LD	0x0000_0000	rd,rw,lr	Load Halfword	LH	0x0000_0000	rd,rw,lr	Load Halfword
Load Word	LW	LD	0x0000_0000	rd,rw,lr	Load Word	LW	0x0000_0000	rd,rw,lr	Load Word
Load Word Unaligned	LWU	LD	0x0000_0000	rd,rw,lr	Load Word Unaligned	LWU	0x0000_0000	rd,rw,lr	Load Word Unaligned
Load Word HUaligned	LWHU	LD	0x0000_0000	rd,rw,lr	Load Word HUaligned	LWHU	0x0000_0000	rd,rw,lr	Load Word HUaligned
Stores	SW	SD	0x0000_0000	rd,rw,ls	Stores	SW	0x0000_0000	rd,rw,ls	Stores
Store Halfword	SH	SD	0x0000_0000	rd,rw,ls	Store Halfword	SH	0x0000_0000	rd,rw,ls	Store Halfword
Store Word	SW	SD	0x0000_0000	rd,rw,ls	Store Word	SW	0x0000_0000	rd,rw,ls	Store Word
Store Word HUaligned	SWHU	SD	0x0000_0000	rd,rw,ls	Store Word HUaligned	SWHU	0x0000_0000	rd,rw,ls	Store Word HUaligned
Shifts	SHL	SL	0x0000_0000	rd,rw,rl	Shifts	SHL	0x0000_0000	rd,rw,rl	Shifts
Shift Left Immediate	SL	SL	0x0000_0000	rd,rw,rl	Shift Left Immediate	SL	0x0000_0000	rd,rw,rl	Shift Left Immediate
Shift Right Immediate	SR	SL	0x0000_0000	rd,rw,rl	Shift Right Immediate	SR	0x0000_0000	rd,rw,rl	Shift Right Immediate
Shift Right Immediate	SHR	SL	0x0000_0000	rd,rw,rl	Shift Right Immediate	SHR	0x0000_0000	rd,rw,rl	Shift Right Immediate
Shift Right Arithmetic	SRA	SL	0x0000_0000	rd,rw,rl	Shift Right Arithmetic	SRA	0x0000_0000	rd,rw,rl	Shift Right Arithmetic
Shift Right Arithmetic	SRAV	SL	0x0000_0000	rd,rw,rl	Shift Right Arithmetic	SRAV	0x0000_0000	rd,rw,rl	Shift Right Arithmetic
Arithmetic	ADD	AD	0x0000_0000	rd,rw,rc	Arithmetic	ADD	AD	0x0000_0000	rd,rw,rc
ADD Immediate	ADDI	AD	0x0000_0000	rd,rw,rc	ADD Immediate	ADDI	AD	0x0000_0000	rd,rw,rc
Subtract	SUB	AS	0x0000_0000	rd,rw,rc	Subtract	SUB	AS	0x0000_0000	rd,rw,rc
Load Upper Immediate	LDU	AD	0x0000_0000	rd,rw,rc	Load Upper Immediate	LDU	AD	0x0000_0000	rd,rw,rc
Load Upper Immediate	LDUI	AD	0x0000_0000	rd,rw,rc	Load Upper Immediate	LDUI	AD	0x0000_0000	rd,rw,rc
Logical	AND	AN	0x0000_0000	rd,rw,rc	Logical	AND	AN	0x0000_0000	rd,rw,rc
AND Immediate	ANDI	AN	0x0000_0000	rd,rw,rc	AND Immediate	ANDI	AN	0x0000_0000	rd,rw,rc
OR	OR	OR	0x0000_0000	rd,rw,rc	OR	OR	OR	0x0000_0000	rd,rw,rc
OR Immediate	ORI	OR	0x0000_0000	rd,rw,rc	OR Immediate	ORI	OR	0x0000_0000	rd,rw,rc
XOR	XOR	XN	0x0000_0000	rd,rw,rc	XOR	XOR	XN	0x0000_0000	rd,rw,rc
XOR Immediate	XORI	XN	0x0000_0000	rd,rw,rc	XOR Immediate	XORI	XN	0x0000_0000	rd,rw,rc
NOT	NOT	AN	0x0000_0000	rd,rw,rc	NOT	NOT	AN	0x0000_0000	rd,rw,rc
NOT Immediate	NOTI	AN	0x0000_0000	rd,rw,rc	NOT Immediate	NOTI	AN	0x0000_0000	rd,rw,rc
Branches	Branch	BR	0x0000_0000	rd,rw,rs	Branches	Branch	BR	0x0000_0000	rd,rw,rs
Set = Immediate	SET	BR	0x0000_0000	rd,rw,rs	Set = Immediate	SET	BR	0x0000_0000	rd,rw,rs
Set = Unaligned	SETU	BR	0x0000_0000	rd,rw,rs	Set = Unaligned	SETU	BR	0x0000_0000	rd,rw,rs
Set = Unaligned	SETUI	BR	0x0000_0000	rd,rw,rs	Set = Unaligned	SETUI	BR	0x0000_0000	rd,rw,rs
Branch & Unaligned	BRNU	BR	0x0000_0000	rd,rw,rs	Branch & Unaligned	BRNU	BR	0x0000_0000	rd,rw,rs
Branch & Unaligned	BRNUU	BR	0x0000_0000	rd,rw,rs	Branch & Unaligned	BRNUU	BR	0x0000_0000	rd,rw,rs
Jump & Link	JAL	JAL	0x0000_0000	rd,lr	Jump & Link	JAL	JAL	0x0000_0000	rd,lr
Jump & Link Register	JALR	JALR	0x0000_0000	rd,lr	Jump & Link Register	JALR	JALR	0x0000_0000	rd,lr
Syntax	Search Register	PERC	0x0000_0000		Syntax	Search Register	PERC	0x0000_0000	
Search Register	PERC	PERC	0x0000_0000		Search Register	PERC	PERC	0x0000_0000	
Search Register	PERCI	PERC	0x0000_0000		Search Register	PERCI	PERC	0x0000_0000	
System	System Call	SYSCALL	0x0000_0000		System	System Call	SYSCALL	0x0000_0000	
System	System Break	SYSEXIT	0x0000_0000		System	System Break	SYSEXIT	0x0000_0000	
Counters	Read CYCLE	RCYCLE	0x0000_0000		Counters	Read CYCLE	RCYCLE	0x0000_0000	
Read CYCLE upper half	RCYCLEH	RCYCLE	0x0000_0000		Read CYCLE upper half	RCYCLEH	RCYCLE	0x0000_0000	
Read TIME	RTIME	RTIME	0x0000_0000		Read TIME	RTIME	RTIME	0x0000_0000	
Read INSTR RETired	RINSTRRET	RINSTRRET	0x0000_0000		Read INSTR RETired	RINSTRRET	RINSTRRET	0x0000_0000	
Read INSTRET	RINSTRET	RINSTRET	0x0000_0000		Read INSTRET	RINSTRET	RINSTRET	0x0000_0000	
RV Privileged Instructions: RV32I(RV32I)									
Category Name Format RV32I(RV32I)					Category Name Format RV32I(RV32I)				
CSR Access									
Atomic Read & Set	RS	RS	0x0000_0000	rd,mc,rw,cs	Atomic Read & Set	RS	RS	0x0000_0000	rd,mc,rw,cs
Atomic Read & Clear	RC	RC	0x0000_0000	rd,mc,rw,cs	Atomic Read & Clear	RC	RC	0x0000_0000	rd,mc,rw,cs
Atomic RW	RW	RW	0x0000_0000	rd,mc,rw,cs	Atomic RW	RW	RW	0x0000_0000	rd,mc,rw,cs
Atomic Read & Set B	RSB	RSB	0x0000_0000	rd,mc,rw,cs	Atomic Read & Set B	RSB	RSB	0x0000_0000	rd,mc,rw,cs
Atomic Read & Clear B	RCB	RCB	0x0000_0000	rd,mc,rw,cs	Atomic Read & Clear B	RCB	RCB	0x0000_0000	rd,mc,rw,cs
Atomic Read & Set B Inv	RSBI	RSBI	0x0000_0000	rd,mc,rw,cs	Atomic Read & Set B Inv	RSBI	RSBI	0x0000_0000	rd,mc,rw,cs
Atomic Read & Set Inv	RSBI	RSBI	0x0000_0000	rd,mc,rw,cs	Atomic Read & Set Inv	RSBI	RSBI	0x0000_0000	rd,mc,rw,cs
Atomic Read & Clear Inv	RCBI	RCBI	0x0000_0000	rd,mc,rw,cs	Atomic Read & Clear Inv	RCBI	RCBI	0x0000_0000	rd,mc,rw,cs
Atomic Read & Clear B Inv	RCBBI	RCBBI	0x0000_0000	rd,mc,rw,cs	Atomic Read & Clear B Inv	RCBBI	RCBBI	0x0000_0000	rd,mc,rw,cs
Change Level	EL	EL	0x0000_0000	rd,mc,rw,cs	Change Level	EL	EL	0x0000_0000	rd,mc,rw,cs
Environment Breakpoint	EBREAK	EBREAK	0x0000_0000	rd,mc,rw,cs	Environment Breakpoint	EBREAK	EBREAK	0x0000_0000	rd,mc,rw,cs
Trap Redirect	TR	TR	0x0000_0000	rd,mc,rw,cs	Trap Redirect	TR	TR	0x0000_0000	rd,mc,rw,cs
Redirection Trap In Supervisor	TRT	TRT	0x0000_0000	rd,mc,rw,cs	Redirection Trap In Supervisor	TRT	TRT	0x0000_0000	rd,mc,rw,cs
Supervisor Trap In Supervisor	TRST	TRST	0x0000_0000	rd,mc,rw,cs	Supervisor Trap In Supervisor	TRST	TRST	0x0000_0000	rd,mc,rw,cs
Interrupt	RI	RI	0x0000_0000	rd,mc,rw,cs	Interrupt	RI	RI	0x0000_0000	rd,mc,rw,cs
MMEU	MMEU	MMEU	0x0000_0000	rd,mc,rw,cs	MMEU	MMEU	MMEU	0x0000_0000	rd,mc,rw,cs
Optional Multiply-Divide Extension: RV32M									
Category Name Format RV32M (Multi-Div)					Category Name Format RV32M (Multi-Div)				
Multiply									
Multiply	MUL	MUL	0x0000_0000	rd,rw,rc	Multiply	MUL	MUL	0x0000_0000	rd,rw,rc
Multiply upper half	MULH	MULH	0x0000_0000	rd,rw,rc	Multiply upper half	MULH	MULH	0x0000_0000	rd,rw,rc
Multiply lower half	MULL	MULL	0x0000_0000	rd,rw,rc	Multiply lower half	MULL	MULL	0x0000_0000	rd,rw,rc
Multiply upper half Inv	MULHI	MULHI	0x0000_0000	rd,rw,rc	Multiply upper half Inv	MULHI	MULHI	0x0000_0000	rd,rw,rc
Multiply lower half Inv	MULLI	MULLI	0x0000_0000	rd,rw,rc	Multiply lower half Inv	MULLI	MULLI	0x0000_0000	rd,rw,rc
Multiply upper half Inv Inv	MULHII	MULHII	0x0000_0000	rd,rw,rc	Multiply upper half Inv Inv	MULHII	MULHII	0x0000_0000	rd,rw,rc
Multiply lower half Inv Inv	MULLII	MULLII	0x0000_0000	rd,rw,rc	Multiply lower half Inv Inv	MULLII	MULLII	0x0000_0000	rd,rw,rc
Divide	DIV	DIV	0x0000_0000	rd,rw,rc	Divide	DIV	DIV	0x0000_0000	rd,rw,rc
Divide Unsigned	DIVU	DIVU	0x0000_0000	rd,rw,rc	Divide Unsigned	DIVU	DIVU	0x0000_0000	rd,rw,rc
Remainder	REM	REM	0x0000_0000	rd,rw,rc	Remainder	REM	REM	0x0000_0000	rd,rw,rc
Remainder Unsigned	REMU	REMU	0x0000_0000	rd,rw,rc	Remainder Unsigned	REMU	REMU	0x0000_0000	rd,rw,rc
Optional Atomic Instruction Extension: RVA									
Category Name Format RV32A (RV32A)					Category Name Format RV32A (RV32A)				
Load									
Load	LD	LD	0x0000_0000	rd,rw,ls	Load	LD	LD	0x0000_0000	rd,rw,ls
Load Double	LDD	LDD	0x0000_0000	rd,rw,ls	Load Double	LDD	LDD	0x0000_0000	rd,rw,ls
Load Double SP	LDDSP	LDDSP	0x0000_0000	rd,rw,ls	Load Double SP	LDDSP	LDDSP	0x0000_0000	rd,rw,ls
Load Quad	LQD	LQD	0x0000_0000	rd,rw,ls	Load Quad	LQD	LQD	0x0000_0000	rd,rw,ls
Load Quad SP	LQDSP	LQDSP	0x0000_0000	rd,rw,ls	Load Quad SP	LQDSP	LQDSP	0x0000_0000	rd,rw,ls
Load Quad Double	LQDQD	LQDQD	0x0000_0000	rd,rw,ls	Load Quad Double	LQDQD	LQDQD	0x0000_0000	rd,rw,ls
Load Quad Double SP	LQDQDSP	LQDQDSP	0x0000_0000	rd,rw,ls	Load Quad Double SP	LQDQDSP	LQDQDSP	0x0000_0000	rd,rw,ls
Store									
Store	SW	SW	0x0000_0000	rd,rw,ls	Store	SW	SW	0x0000_0000	rd,rw,ls
Store Word SP	SWSP	SWSP	0x0000_0000	rd,rw,ls	Store Word SP	SWSP	SWSP	0x0000_0000	rd,rw,ls
Store Double	SD	SD	0x0000_0000	rd,rw,ls	Store Double	SD	SD	0x0000_0000	rd,rw,ls
Store Double SP	SDSP	SDSP	0x0000_0000	rd,rw,ls	Store Double SP	SDSP	SDSP	0x0000_0000	rd,rw,ls
Store Quad	SQD	SQD	0x0000_0000	rd,rw,ls	Store Quad	SQD	SQD	0x0000_0000	rd,rw,ls
Store Quad SP	SQDSP	SQDSP	0x0000_0000	rd,rw,ls	Store Quad SP	SQDSP	SQDSP	0x0000_0000	rd,rw,ls
Store Quad Double	SQDQD	SQDQD	0x0000_0000	rd,rw,ls	Store Quad Double	SQDQD	SQDQD	0x0000_0000	rd,rw,ls
Store Quad Double SP	SQDQDSP	SQDQDSP	0x0000_0000	rd,rw,ls	Store Quad Double SP	SQDQDSP	SQDQDSP	0x0000_0000	rd,rw,ls
Optional FP Extensions: RV32P(RV1010)									
Category Name Format RV32P(RV1010)					Category Name Format RV32P(RV1010)				
Load									
Load	FLD	FLD	0x0000_0000	rd,rw,ls	Load	FLD	FLD	0x0000_0000	rd,rw,ls
Load Double	FLDD	FLDD	0x0000_0000	rd,rw,ls	Load Double	FLDD	FLDD	0x0000_0000	rd,rw,ls
Load Double SP	FLDDSP	FLDDSP	0x0000_0000	rd,rw,ls	Load Double SP	FLDDSP	FLDDSP	0x0000_0000	rd,rw,ls
Load Quad	FQD	FQD	0x0000_0000	rd,rw,ls	Load Quad	FQD	FQD	0x0000_0000	rd,rw,ls
Load Quad SP	FQDSP	FQDSP	0x0000_0000	rd,rw,ls	Load Quad SP	FQDSP	FQDSP	0x0000_0000	rd,rw,ls
Load Quad Double	FQDQD	FQDQD	0x0000_0000	rd,rw,ls	Load Quad Double	FQDQD	FQDQD	0x0000_0000	rd,rw,ls
Load Quad Double SP	FQDQDSP	FQDQDSP	0x0000_0000	rd,rw,ls	Load Quad Double SP	FQDQDSP	FQDQDSP	0x0000_0000	rd,rw,ls
Store									
Store	FST	FST	0x0000_0000	rd,rw,ls	Store	FST	FST	0x0000_0000	rd,rw,ls
Store Double	FSST	FSST	0x0000_0000	rd,rw,ls	Store Double	FSST	FSST	0x0000_0000	rd,rw,ls
Store Double SP	FSDSP	FSDSP	0x0000_0000	rd,rw					

RISC-V and Industry

- Created at UC Berkeley but useful beyond academia
- Designed to be extensible
 - Microcontroller to supercomputer
- RISC-V Foundation now controls standard: riscv.org
 - Over 400 members: companies, universities and more
 - [YouTube channel has hundreds of talks!](#)
 - <https://www.youtube.com/channel/UC5gLmcFuvdGbajs4VL-WU3g>
- Nvidia and Western Digital will ship millions of devices with RISC-V
 - freedom to leverage open source implementations
 - BOOM, Rocket, PULP, SweRV, and many more
 - avoiding ARM licensing fees

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RISC-V® Summit

THANKS FOR ATTENDING!

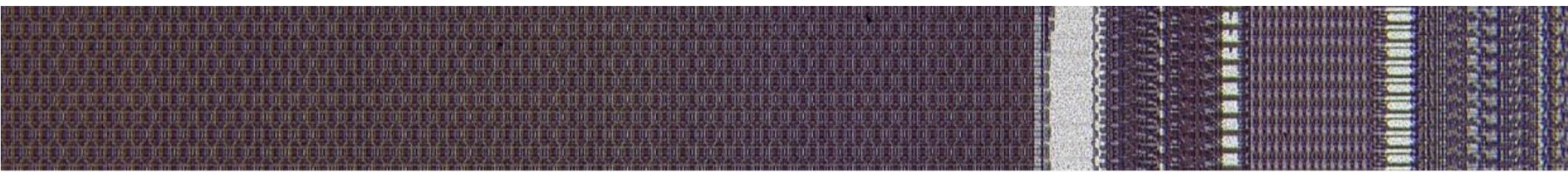
The **RISC-V Summit 2019** was held in San Jose, California on December 9-12. Slides are [now available](#), videos coming soon.



RISC-V: The Free and Open RISC Instruction Set Architecture

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

[NEW TO RISC-V? LEARN MORE](#)[Privacy - Terms](#)



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RISC-V and the world

- RISC-V Foundation moving from US to Switzerland
- Nations such as India have RISC-V initiatives
 - Desire for sovereign technology and avoid backdoors from other nations
- Strong interest from chipmakers in China
 - U.S. companies have been banned from doing business with Huawei... who's next?
 - ARM deemed UK-origin tech so ok to do business with Huawei, but what will brexit-govt bring?

- My column in the latest Hackspace Magazine is an introduction to RISC-V and how it is enabling open source chip design:
 - hackspace.raspberrypi.org/issues/27/



Drew Fustini

COLUMN

Open-source chips

Breaking free of chip design monopolies with RISC-V



Drew Fustini

When we think about what open-source hardware means, we usually think about the board design being freely available. But what about the processor? Is there a way to make hardware that is truly open source? This month's column is dedicated to an existing – and surprisingly political – development in chip design.

When you write a program in the Arduino IDE, it is compiled into instructions for the microcontroller to execute. How does the compiler know what instructions the chip understands? This is defined by the Instruction Set Architecture. The ISA is a standard, a set of rules that define the tasks the processor can perform.

Chances are that both your laptop and the data centre streaming your favourite movie are using an ISA owned by Intel or AMD. The processor in your smartphone is almost certainly using a proprietary ISA licensed from ARM. Proprietary standards can be overpriced, prevent innovation, or even disappear altogether when companies change strategy.

Enter RISC-V, a free and open ISA created by researchers at UC Berkeley, led by Krste Asanović and David Patterson. "We were always jealous that you could get industrial-strength software that was

open," Patterson explained to VentureBeat at the RISC-V Summit back in December. "But when it came to hardware, it was proprietary. Now, with RISC-V, we get the same kind of benefit. It helps education, and it helps competition."

This open standard proved to be useful outside of academia. Nvidia and Western Digital are now shipping millions of devices with RISC-V processors. These companies have the freedom to leverage open-source implementations while avoiding ARM licensing fees – which can really add up when shipping large volumes.

The ISA is a standard, a set of rules that define the tasks the processor can perform

Nations such as India see the importance of being able to create processors that are not under the control of a foreign corporation, who may be forced to build in backdoors for their own government. There is also strong interest from chipmakers in China, especially now that US companies have been banned from doing business with Huawei.

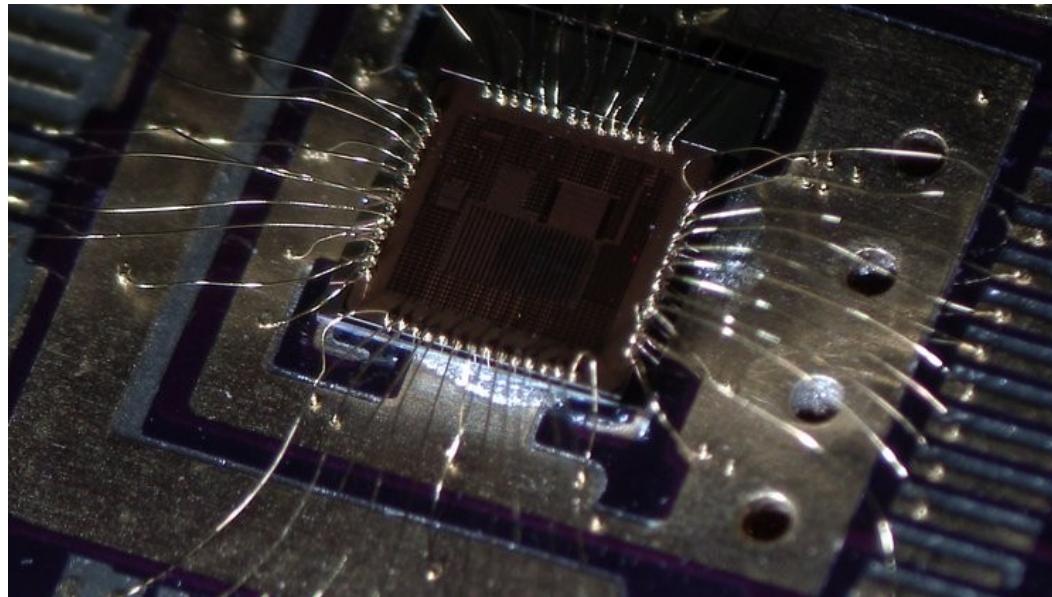
With these financial and political motivations, plus an increasingly mature software ecosystem, including Linux support, it won't be long before you have a device with a RISC-V processor in your home or pocket.

You can learn more about the exciting possibilities that RISC-V unleashes from Dr. Megan Wachs by pointing your web browser to hsmag.cc/qw-led.

- OnChip Open-V

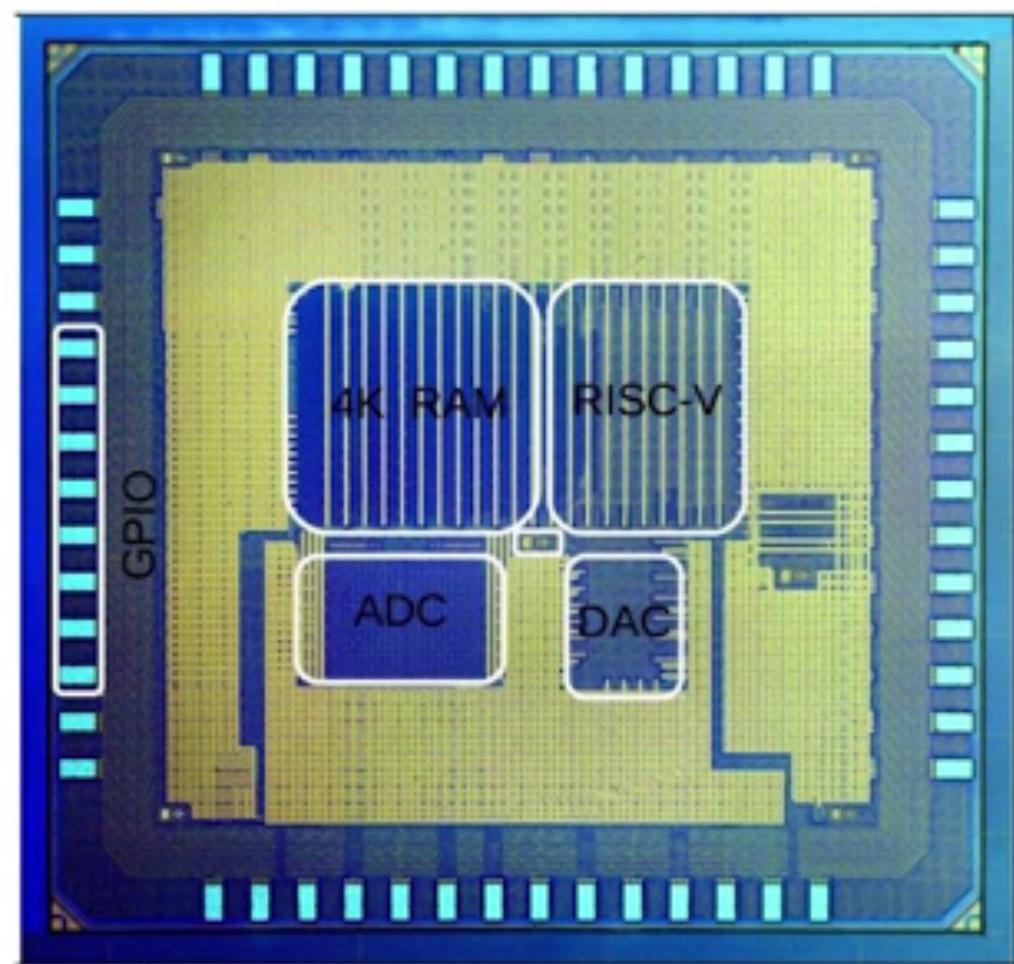
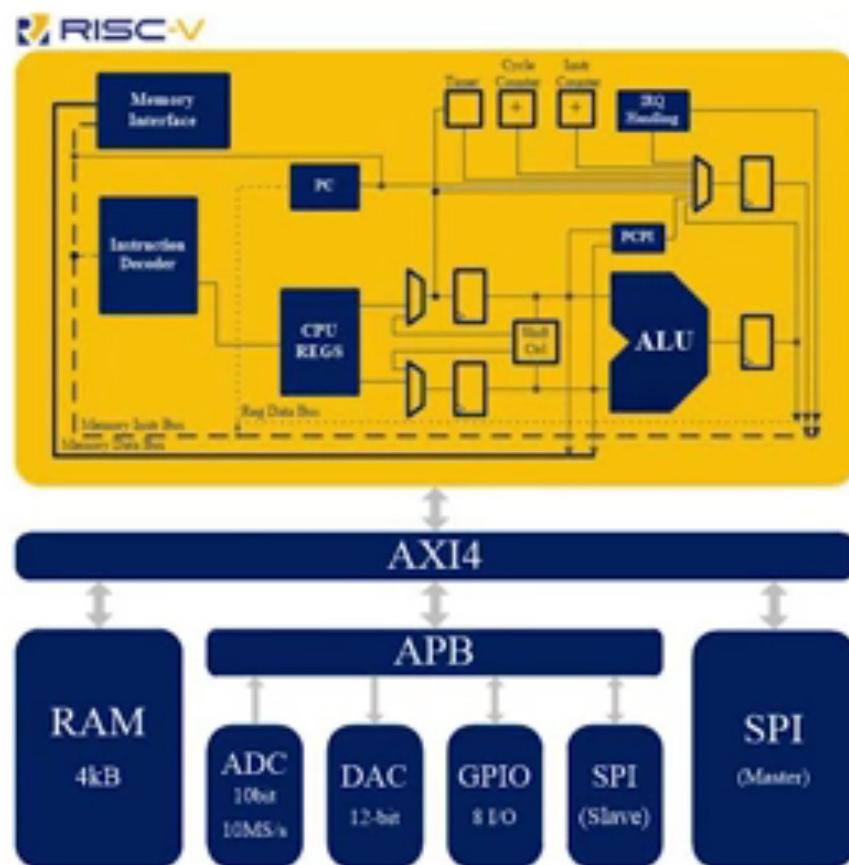


“completely free (as in freedom) and open source 32-bit microcontroller based on the RISC-V architecture”



OnChip Open-V

A 32-bit RISC-V based Microcontroller





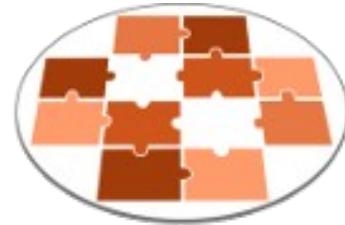
- lowRISC is a not-for-profit organisation whose goal is to produce a fully open source System-on-Chip (SoC) in volume
 - “We will produce a SoC design to populate a low-cost community development board and to act as an ideal starting point for derivative open-source and commercial designs”
- OpenTitan project with Google
 - Announcing OpenTitan, the First Transparent Silicon Root of Trust

- The Future of Operating Systems on RISC-V
 - Alex Bradbury gives an overview of the status and development of RISC-V as it relates to modern operating systems, highlighting major research strands, controversies, and opportunities to get involved.
 - <https://www.youtube.com/watch?v=emnN9p4vhzk>



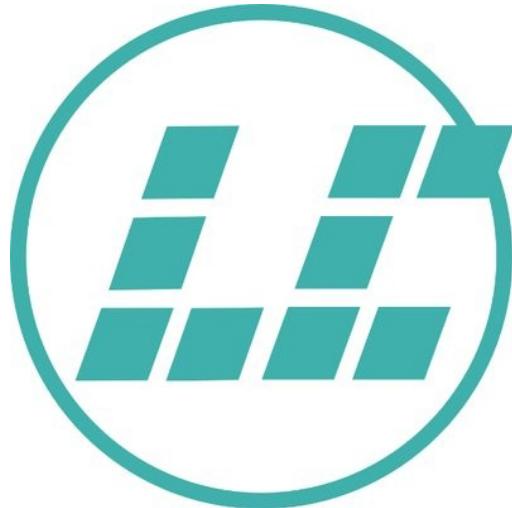


- Tutorial for the v0.7 lowRISC release
 - By Jonathan Kimmitt (lead developer), and Alex Bradbury (lead reviewer)
 - <https://www.cl.cam.ac.uk/~jrrk2/docs/ariane-v0.7/tutorial/>
 - Digilent Nexys A7-100T: \$265
 - This tutorial adds further functionality towards the final SoC design:
 - Graphical Colour Console with X-windows support incorporating mouse and keyboard events.
 - Choice of SD-Card, Quad-SPI or Ethernet TFTP boot-loader with DHCP support.
 - Linux 5.3.8 RISCV kernel and updated Debian userland with advanced package tool.
 - Choice of RV64-GC Rocket (Chisel) or Ariane (SystemVerilog) CPU



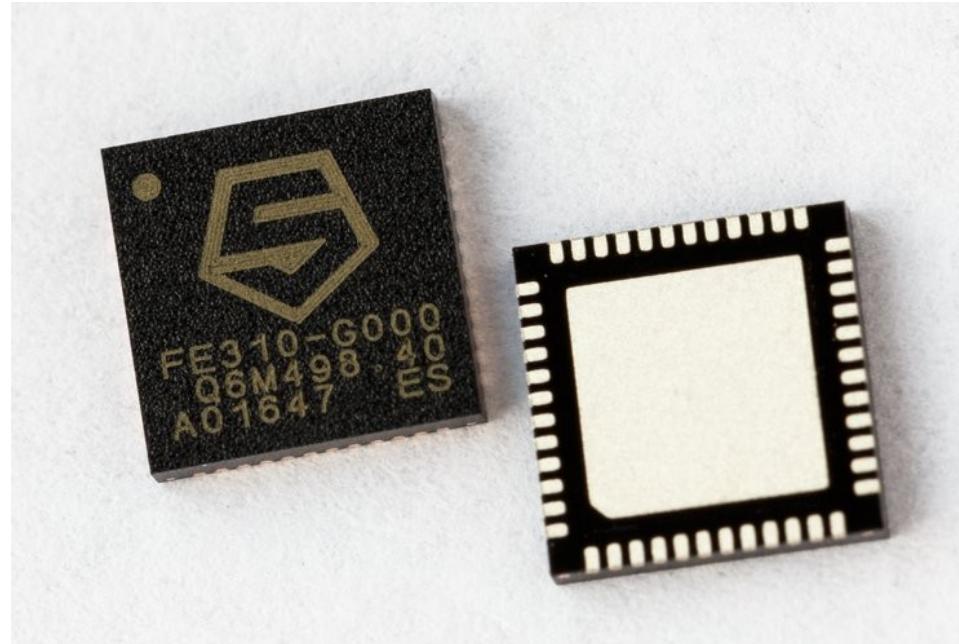
FOSSi
Foundation

- **FOSSi Foundation**
 - The Free and Open Source Silicon Foundation
 - “non-profit foundation with the mission to promote and assist free and open digital hardware designs”
 - Events: ORConf, Latch-up, Week of OSHW
 - **Open Source Silicon Design Ecosystem**
 - Talk by FOSSi co-founder Julius Baxter



- **LibreCores**
 - Project of the FOSSi Foundation
 - “**gateway to free and open source digital designs** and other components that you can use and **re-use in your digital designs**”
 - “advances the idea of OpenCores.org”

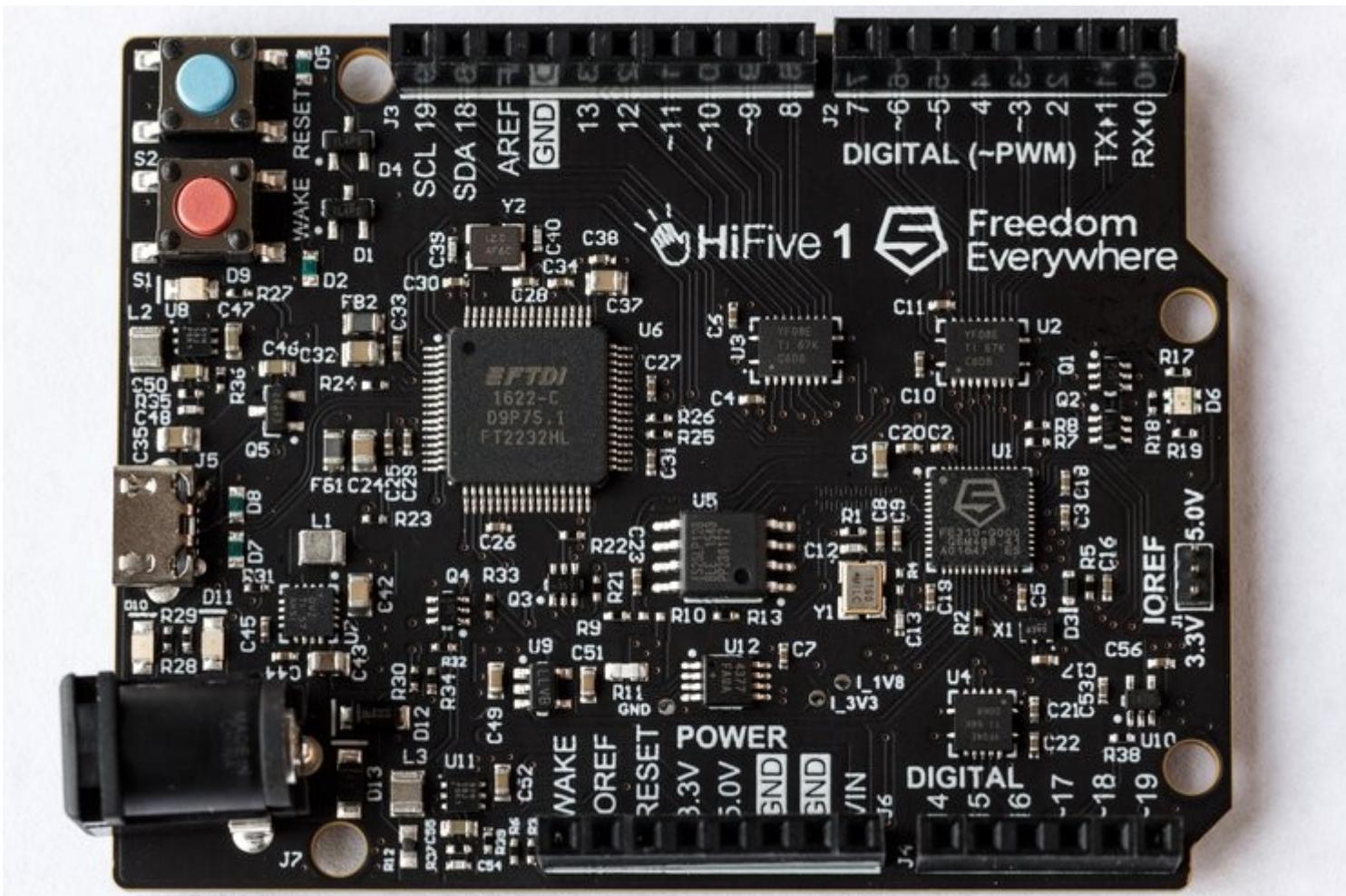
SiFive



- “founded by the creators of the free and open RISC-V architecture as a reaction to the end of conventional transistor scaling and escalating chip design costs”

SiFive FE310 microcontroller

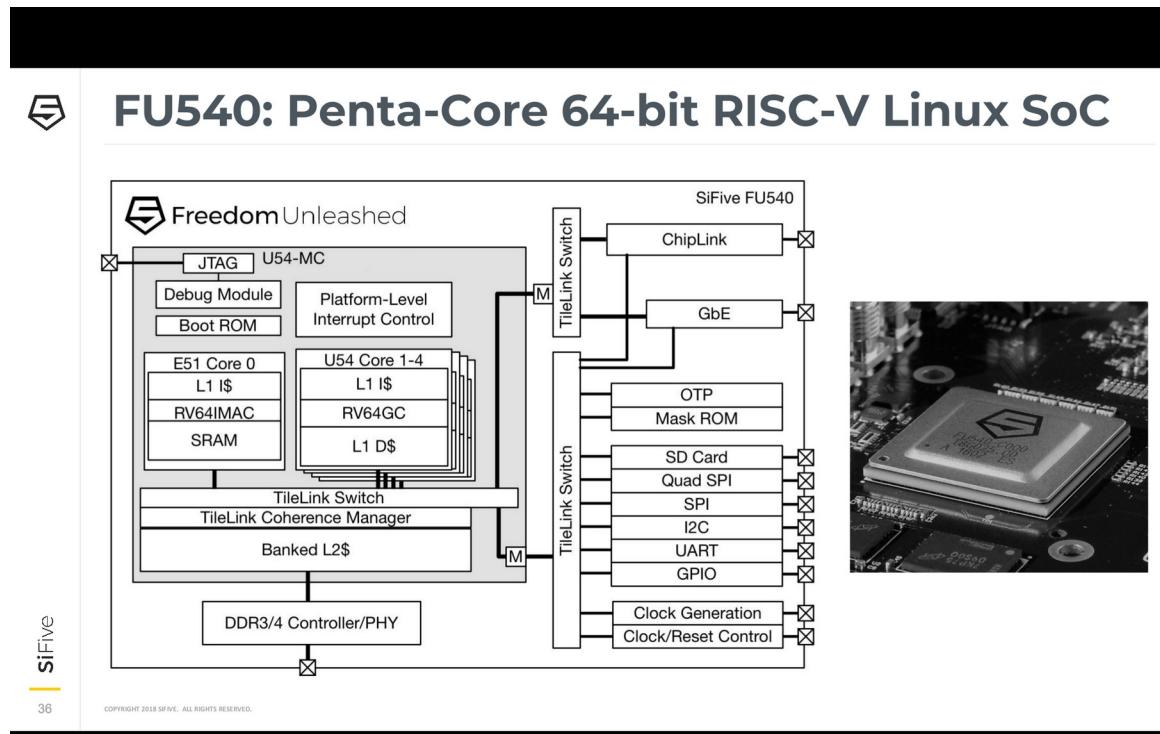
- HiFive1: Arduino-Compatible RISC-V Dev Kit



SiFive: Linux on RISC-V

- FOSDEM 2018 talk

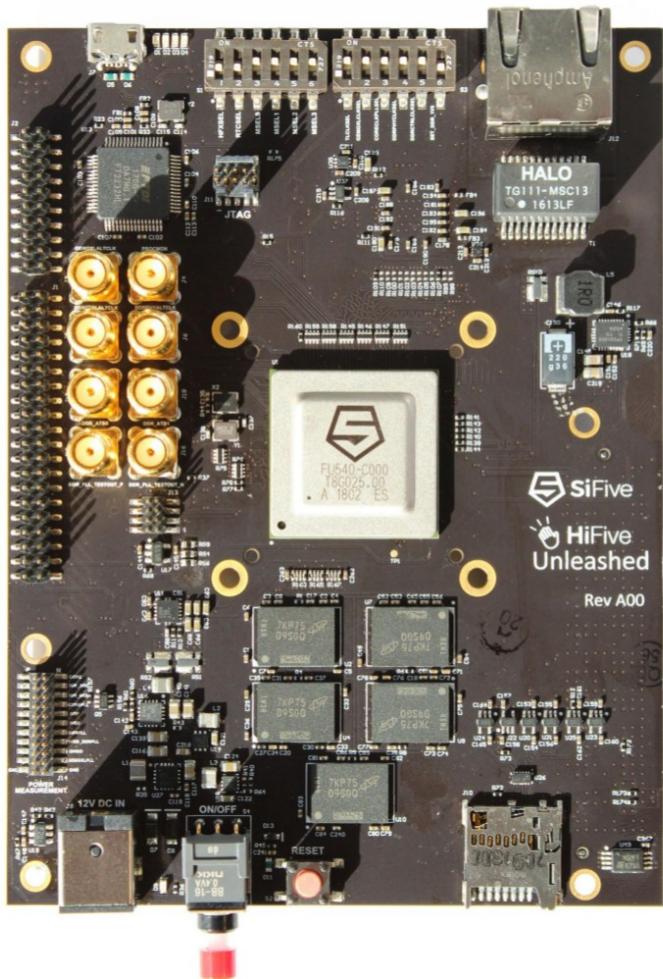
- YouTube: “Igniting the Open Hardware Ecosystem with RISC-V: SiFive's Freedom U500 is the World's First Linux-capable Open Source SoC Platform”
- Interview with Palmer Dabbelt of SiFive



SiFive: Linux on RISC-V



HiFive Unleashed



- World's First Multi-Core RISC-V Linux Development Board
 - SiFive FU540-C000 (built in 28nm)
 - 4+1 Multi-Core Coherent Configuration, up to 1.5 GHz
 - 4x U54 RV64GC Application Cores with Sv39 Virtual Memory Support
 - 1x E51 RV64IMAC Management Core
 - Coherent 2MB L2 Cache
 - 64-bit DDR4 with ECC
 - 1x Gigabit Ethernet
 - 8 GB 64-bit DDR4 with ECC
 - Gigabit Ethernet Port
 - 32 MB Quad SPI Flash
 - MicroSD card for removable storage
 - FMC connector for future expansion with add-in cards

RISC-V Summit 2019: Linux on RISC V Fedora and Firmware Status Update

- <https://www.youtube.com/watch?v=WC6e3g8uWdk>
- Wei Fu – Software Engineer, Red Hat

The slide features a central diagram with a green arrow pointing from a green box labeled 'Rich Software EcoSystem' to a blue box labeled 'RISC-V' and 'Instruction Sets Want to be Free!'. A blue arrow points from the blue box to another blue box labeled 'Rich Hardware EcoSystem'. To the right of the diagram is the 'Fedora always OPEN' logo with a penguin wearing a fedora hat. Below the diagram is a link 'From www.codasip.com'. At the bottom of the slide, there is a caption: 'We would like to support more targets based on standard RISC-V Spec.' The video player interface at the bottom includes a play button, a timestamp '9:56 / 18:37', a URL '#RISCVSUMMIT | tmt.knect365.com/risc-v-summit/', and a Red Hat logo.

Fedora on RISC-V

Rich Software EcoSystem

RISC-V
Instruction Sets Want to be Free!

Rich Hardware EcoSystem

From www.codasip.com

We would like to support more targets based on standard RISC-V Spec.

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RISC-V Summit 2019: 10 Linux on RISC V Fedora and Firmware Status Update

183 views • Jan 16, 2020

13 9:56 / 18:37

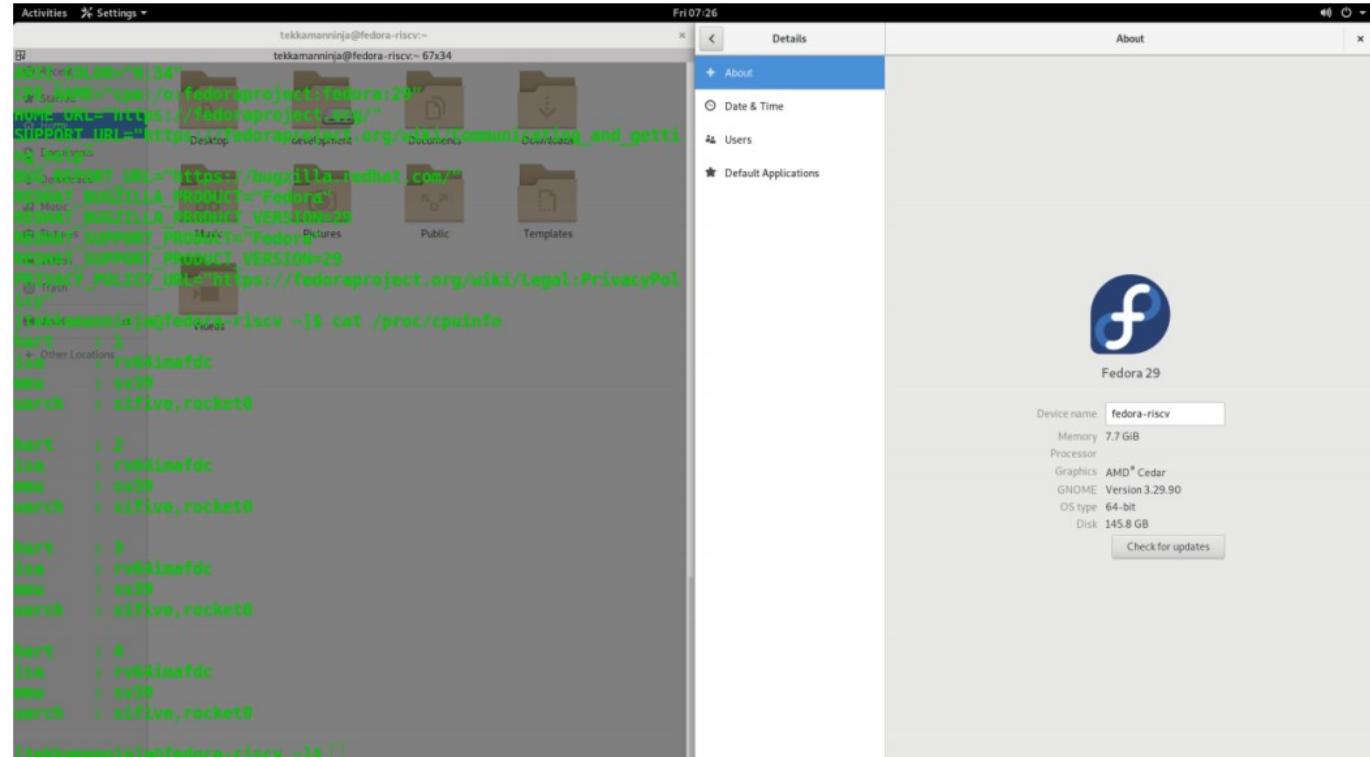
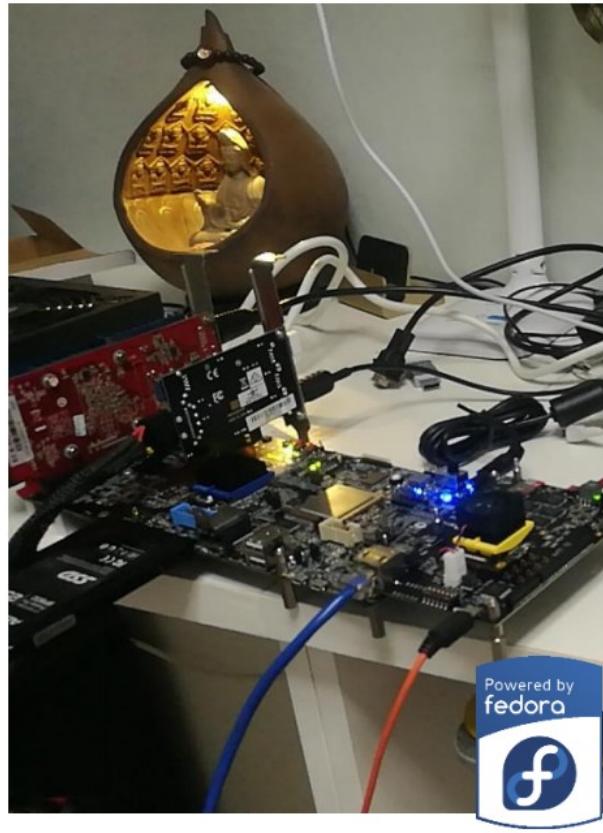
Red Hat

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RISC-V 7.91K subscribers

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Fedora GNOME Image on SiFive Unleashed



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Targets

Supported



Virtual: libvirt + QEMU

with graphics parameters (Spice).



Real Hardware: SiFive Unleashed

with Expansion Board, PCI-E graphic Card & SATA SSD

Tested



QEMU for AndeStar V5 && ADP-XC7KFF676

Andes QEMU and AndeShape **FPGA** board



中国科学院计算技术研究所
INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES



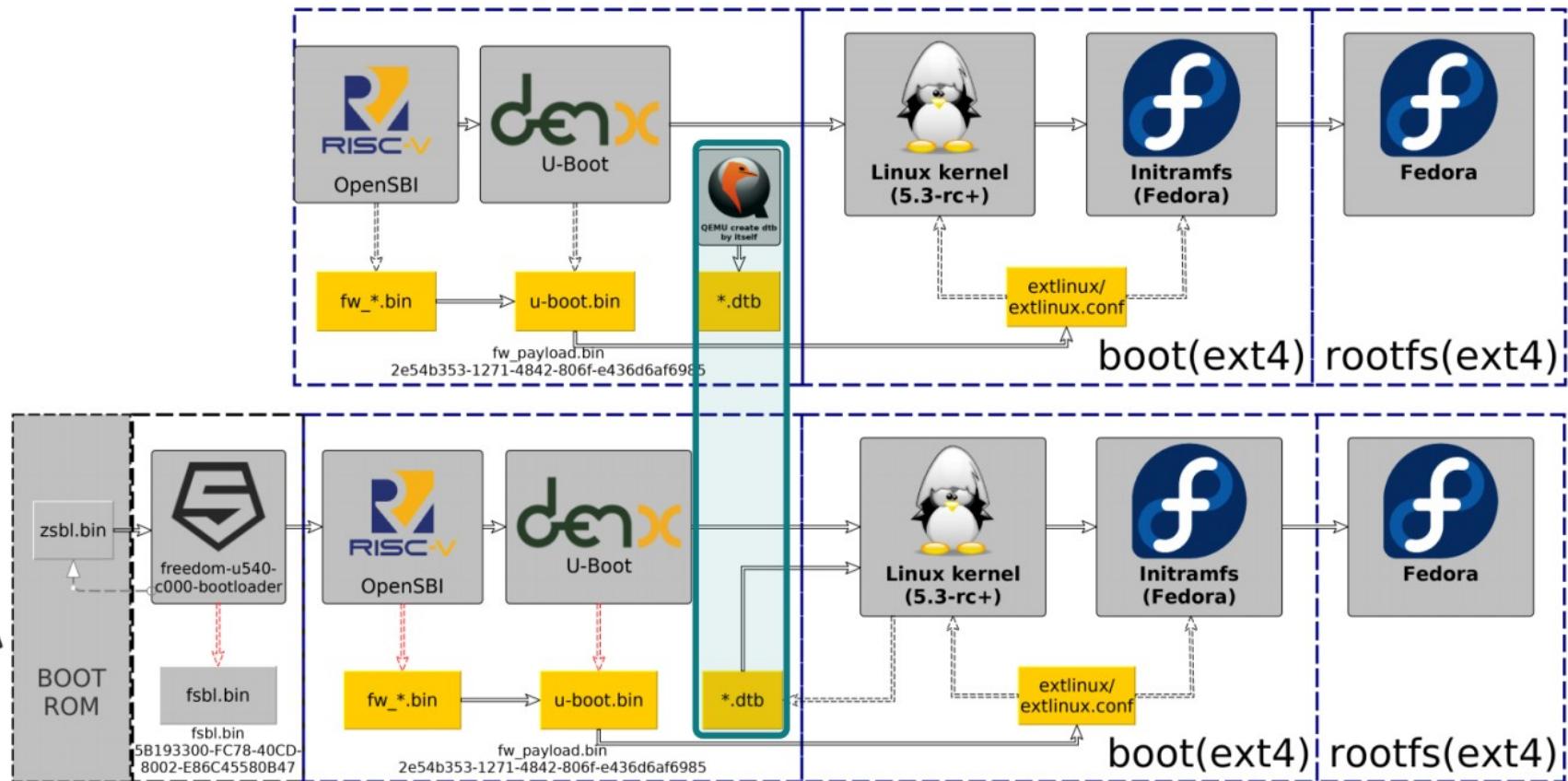
ICT SERVE Platform: FlameCluster

FPGA Cloud development platform (with PCI-E SSD and graphic Card)



#RISCVSUMMIT | tmt.knect365.com/risc-v-summit/

The current boot flow for Fedora on RISC-V





RISC-V

This page contains details about a port of Debian for the RISC-V architecture called **riscv64**.

Contents

[1. In a nutshell](#)

- [1. What is RISC-V?](#)
- [2. What is a Debian port?](#)
- [3. What are the goals of this project in particular?](#)
- [4. Progress](#)

[2. Upstream project / Architecture](#)

- [1. Upstream project / Community](#)
- [2. Architecture details](#)
- [3. Toolchain upstreaming status](#)

[3. Hardware](#)

- [1. ASIC implementations, i.e. "real" CPU chips](#)
 - [1. SiFive "Freedom U540" SoC \(quad-core RV64GC\) / "HiFive Unleashed"](#)
 - [2. Planned](#)
- [2. FPGA implementations](#)

- Experiment to get Linux on the low cost Kendryte K210 RISC-V microcontroller
 - dual core 64-bit RISC-V at 400MHz with 8MB SRAM
 - Sipeed MAix BiT for RISC-V \$13
 - PDF: RISC-V NOMMU and M-mode Linux
 - youtube.com/watch?v=ycG592N9EMA&t=10394
 - jump to 2h 53m
- Many RISC-V Improvements Ready For Linux 5.5: M-Mode, SECCOMP, Other Features



RISC-V NOMMU and M-Mode Linux

Damien Le Moal, Western Digital

Linux Plumbers Conference, September 9th, 2019

Kendryte K210 SoC + Busybox

Sipeed MAIX Go Board (6+2 MB SRAM)

```
[ 0.00000] Linux version 5.1.0-rc5-00314-g375c2321604f (damien@washi) (gcc version 8.2.0 (Buildroot 2018.11-rc2-00003-ga0787e9)) #221 SMP Fri May 10 15:17:17 JST 2019
[ 0.00000] earlycon: sbi0 at I/O port 0x0 (options '')
[ 0.00000] printk: bootconsole [sbi0] enabled
[ 0.00000] initrd not found or empty - disabling initrd
[ 0.00000] Zone ranges:
[ 0.00000]   DMA32    [mem 0x00000008000000-0x0000000807ffff]
[ 0.00000]   Normal    empty
[ 0.00000] Movable zone start for each node
[ 0.00000] Early memory node ranges
[ 0.00000]   node  0: [mem 0x00000008000000-0x0000000807ffff]
[ 0.00000] Initmem setup node 0 [mem 0x00000008000000-0x0000000807ffff]
[ 0.00000] elf_hwcap is 0x112d
[...]
[ 0.00000] Built 1 zonelists, mobility grouping off. Total pages: 2020
[ 0.00000] Kernel command line: console=hvc0 earlycon=sbi init=/bin/bash
[ 0.00000] Dentry cache hash table entries: 1024 (order: 1, 8192 bytes)
[ 0.00000] Inode-cache hash table entries: 512 (order: 0, 4096 bytes)
[ 0.00000] Sorting __ex_table...
[ 0.00000] Memory: 6284K/8192K available (920K kernel code, 101K rwdta, 158K rodata, 393K init, 95K bss, 1908K reserved, 0K cma-reserved)
[ 0.00000] SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=2, Nodes=1
[ 0.00000] rcu: Hierarchical RCU implementation.
[ 0.00000] rcu: RCU calculated value of scheduler-enlistment delay is 25 jiffies.
[ 0.00000] NR_IRQS: 0, nr_irqs: 0, preallocated irqs: 0
[...]
[ 0.251433] Freeing unused kernel memory: 392K
[ 0.254361] This architecture does not have kernel memory protection.
[ 0.259473] Run /bin/bash as init process
```

BusyBox v1.30.1 (2019-05-10 14:49:46 JST) hush - the humble shell

```
# mount -t proc none /proc
# cat /proc/cpuinfo
processor : 0
hart : 0
isa : rv64imafdc

processor : 1
hart : 1
isa : rv64imafdc
```

Coming in 2020?

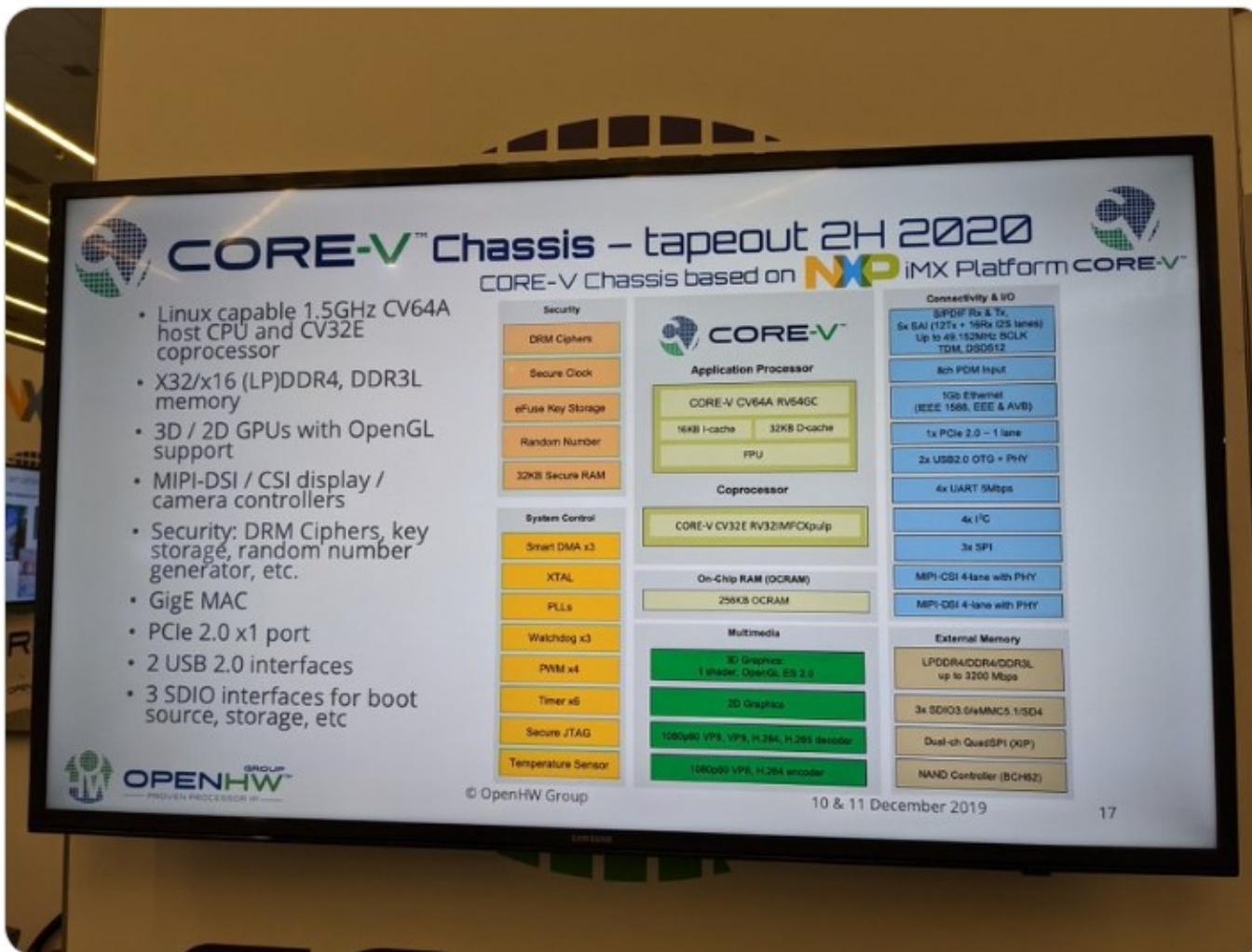
- Andes 27-series CPU
 - “32-bit A27 and 64-bit AX27 and NX27V cores, which will enter production in Q1 2020.”
 - [Andes’ RISC-V SoC debuts with AI-ready VPU as Microchip opens access to its PolarFire SoC](#)
- Microchip PolarFire SoC FPGA
 - Hard RISC-V with FPGA fabric... like the Xilinx Zync for ARM
- NXP iMX with RISC-V instead of ARM!
 - [OpenHW Group Unveils CORE-V Chassis SoC Project, Building on PULP Project IP](#)



Karim Yaghmour
@karimyaghmour



Spotted at RISC V summit: an iMX chip where the ARM core was ripped out and replaced with a RISC V/PULP - just wow



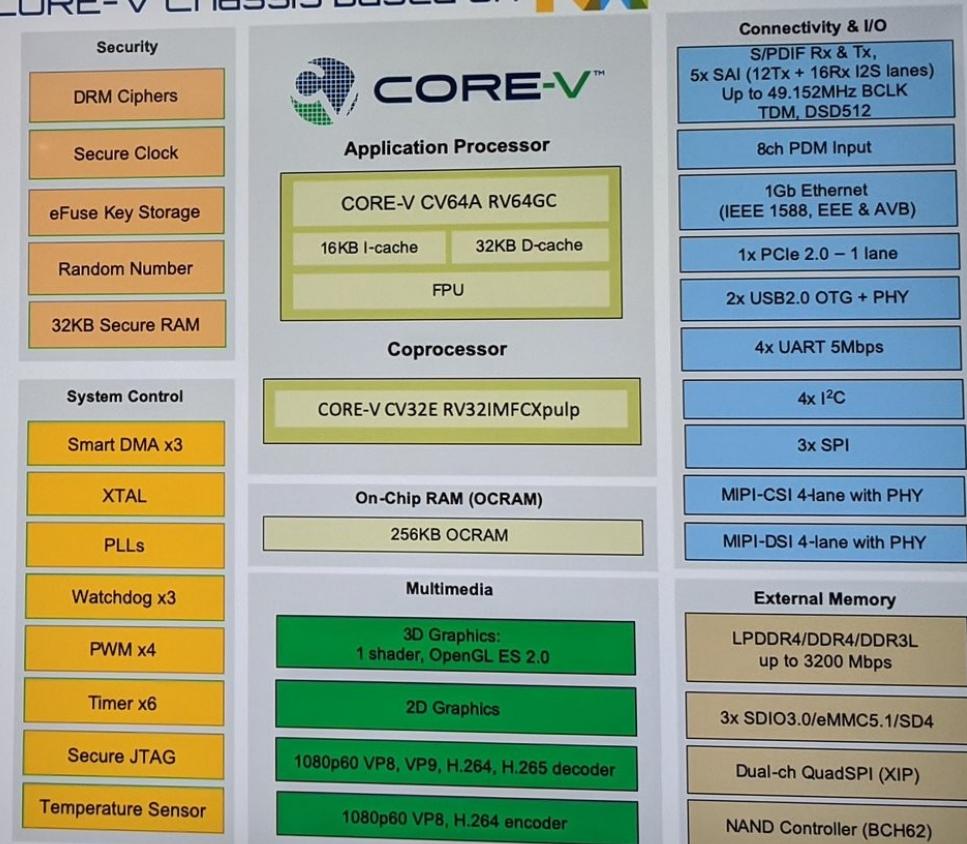


CORE-V™ chassis – tapeout 2H 2020



CORE-V Chassis based on **NXP** iMX Platform **CORE-V**

- Linux capable 1.5GHz CV64A host CPU and CV32E coprocessor
- X32/x16 (LP)DDR4, DDR3L memory
- 3D / 2D GPUs with OpenGL support
- MIPI-DSI / CSI display / camera controllers
- Security: DRM Ciphers, key storage, random number generator, etc.
- GigE MAC
- PCIe 2.0 x1 port
- 2 USB 2.0 interfaces
- 3 SDIO interfaces for boot source, storage, etc



© OpenHW Group

10 & 11 December 2019

17

OSHW RISC-V Linux board for less than \$100?

- Goal: Sub-\$100 Open Source Hardware board that can run Linux on RISC-V
- Possible by FOSDEM 2021?
- Interested in working together?
 - drew@oshpark.com / Twitter: [@pdp7](https://twitter.com/pdp7)
 - create a mailing list?

Slides: <https://github.com/pdp7/talks/blob/master/fosdem20.pdf>



Section:
Open Source FPGA tools

Open Source and FPGAs

- Hackspace Magazine column about how open source FPGA tools developed by [Claire Wolf \(oe1cxw\)](#), [David Shah](#) and others have made FPGAs more accessible than ever before to makers and hackers:
 - hackspace.raspberrypi.org/issues/26/

MAKE | BUILD | HACK | CREATE **132 PAGES** OF MAKING

HackSpace

TECHNOLOGY IN YOUR HANDS

hsmag.cc | January 2020 | Issue #26

WHAT 3D PRINTER?

Find the ultimate replicator for 2020

CIRCUIT PYTHON

SOLDERING WITH GAS

PICKING AN IMPACT DRIVER

SEWING MACHINES

Building a kiln

Melting glass with a Raspberry Pi

Drew Fustini

@pdpf

Drew Fustini is a hardware designer and embedded Linux developer. He is the Vice President of the Open Source Hardware Association, and a board member of the BeagleBoard Foundation. Drew designs circuit boards for OSH Park, a PCB manufacturing service, and maintains the Adafruit BeagleBone Python library.

FPGA

FPGAs have been the talk of the town at many of this year's hacker conferences. But what exactly is an FPGA, and why are they so hot right now?

FPGA stands for Field Programmable Gate Array, a digital logic chip that can be programmed to reconfigure the internal hardware. An FPGA does not run software – it physically changes the configuration of its gate arrays to adapt to the task at hand. Is an FPGA an incredibly versatile tool? Need 25 PWM pins for a project? No problem. Want to replicate the functionality of a vintage CPU? Your FPGA has you covered. Not only is an FPGA versatile, but it is also better at handling timing-critical tasks than a microcontroller. You can filter high-speed sensor data before it's read by your processor, or offload repetitive tasks like debouncing buttons and moving the burden on your microcontroller.

FPGAs are hot right now but they're not a new technology – they've been used in industry for decades

The Lattice ECP5 FPGA is capable of more advanced features than the iCE40, and it's easier to get started with it too, thanks to Project Trellis led by David Shah. This enabled the ECP5-powered Supercon badge to have cool features like HDMI video, while still being open for anyone to hack on without requiring proprietary tools.

FPGAs are a fascinating technology with lots of awesome applications. If you want to find out more, start off by reading Luke Valenty's *The Hobbyists Guide to FPGAs on Hackaday.io*. (hsmag.cc/GOAQnR), and watch Tim Ansell's Supercon talk to learn about the exciting future of open-source FPGA tools (hsmag.cc/kY5IPD). □

The rise of the FPGA

Reconfigure your chips to suit your project

FPGAs are hot right now but they're not a new technology – they've been used in industry for decades

This opened the door for low-cost, open hardware boards such as mystorm Blackice, TinyFPGA, iCEBreaker, and Fomu, which are great tools for teaching workshops and building projects.

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HackSpace

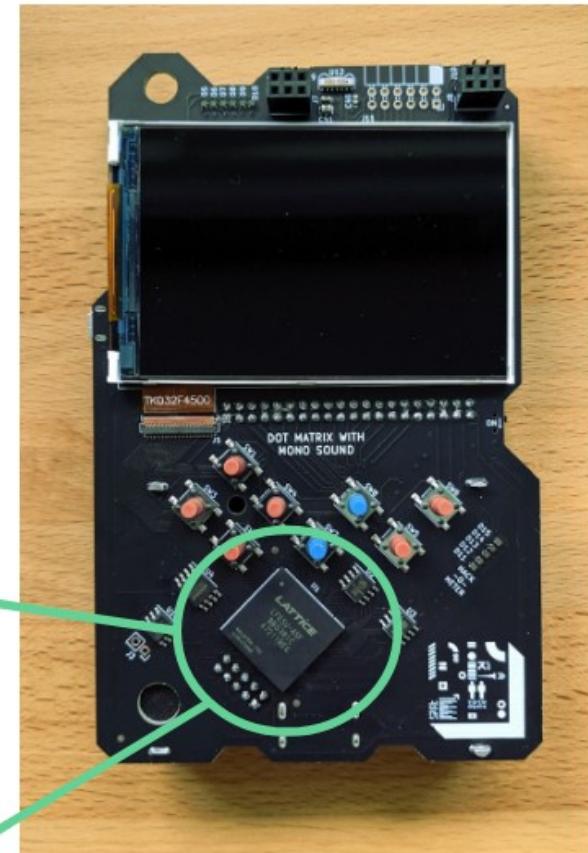
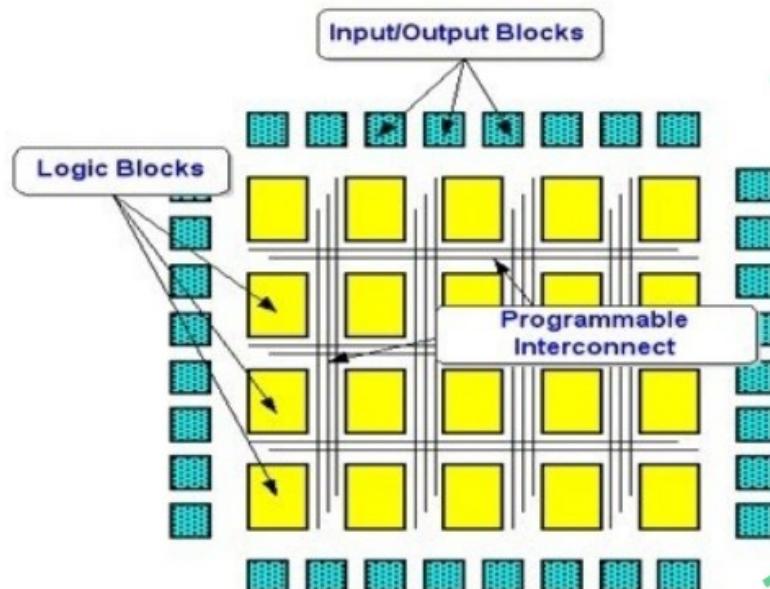
23



- Keynote at Hackday Supercon 2019 by Dr. Megan Wachs of SiFive
- **“RISC-V and FPGAs: Open Source Hardware Hacking”**
 - https://www.youtube.com/watch?v=vCG5_nxm2G4

Where do FPGAs Come In?

- Field Programmable Gate Array
- Change a chip's HARDWARE in a few minutes
- Make it act like a new chip!



Open Source and FPGAs

- Open Source toolchains for FPGAs!
 - Project IceStorm for Lattice iCE40
 - “A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs”
by [Claire Wolf \(oe1cxw\)](#) at 32c3

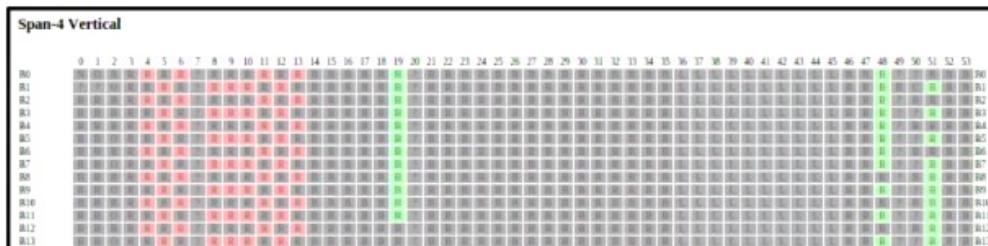


A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs



by [Clifford](#)

Some screenshots from IceStrom Docs:

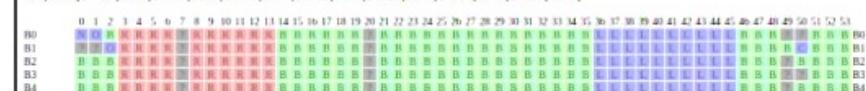


(2 17)	(3 17)	(4 17)	(5 17)	(6 17)
LOGIC Tile (2 16)	RAMT Tile (3 16)	LOGIC Tile (4 16)	LOGIC Tile (5 16)	LOGIC Tile (6 16)
LOGIC Tile (2 15)	RAMB Tile (3 15)	LOGIC Tile (4 15)	LOGIC Tile (5 15)	LOGIC Tile (6 15)
LOGIC Tile (2 14)	RAMT Tile (3 14)	LOGIC Tile (4 14)	LOGIC Tile (5 14)	LOGIC Tile (6 14)

Configuration Bitmap

A LOGIC Tile has 64x config bits in 16 groups of 54 bits each:

B0[53:0], B1[53:0], B2[53:0], B3[53:0], B4[53:0], B5[53:0], B6[53:0], B7[53:0],
B8[53:0], B9[53:0], B10[53:0], B11[53:0], B12[53:0], B13[53:0], B14[53:0], B15[53:0]



Open Source and FPGAs

- Open Source toolchains for FPGAs!
 - Project Trellis for Lattice ECP5
 - “Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5”
 - David Shah (@fpga_dave)
 - youtube.com/watch?v=0se7kNes3EU

Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5

Project Trellis & nextpnr

FOSS Tools for ECP5 FPGAs

David Shah
@fpga_dave

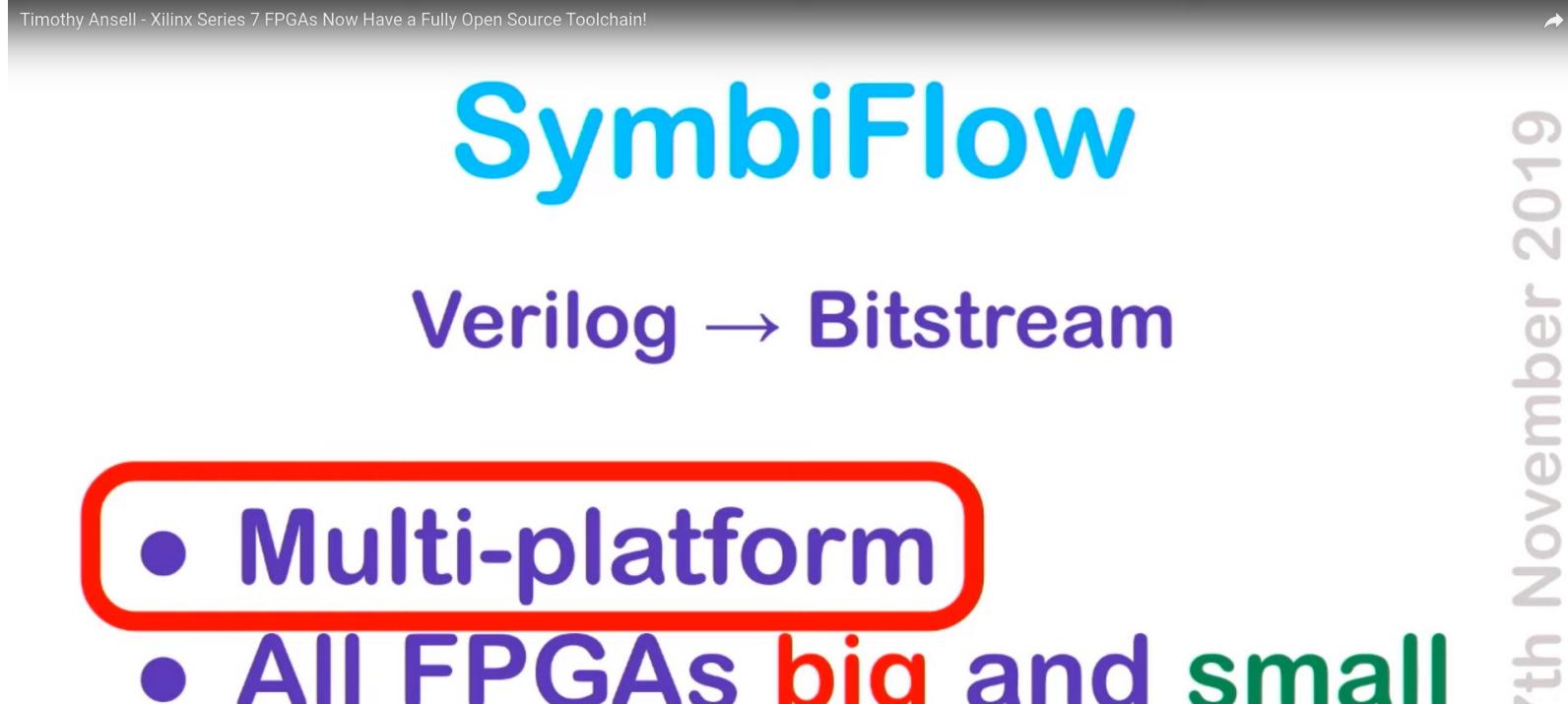
Symbiotic EDA || Imperial College London

FOSDEM 19
org



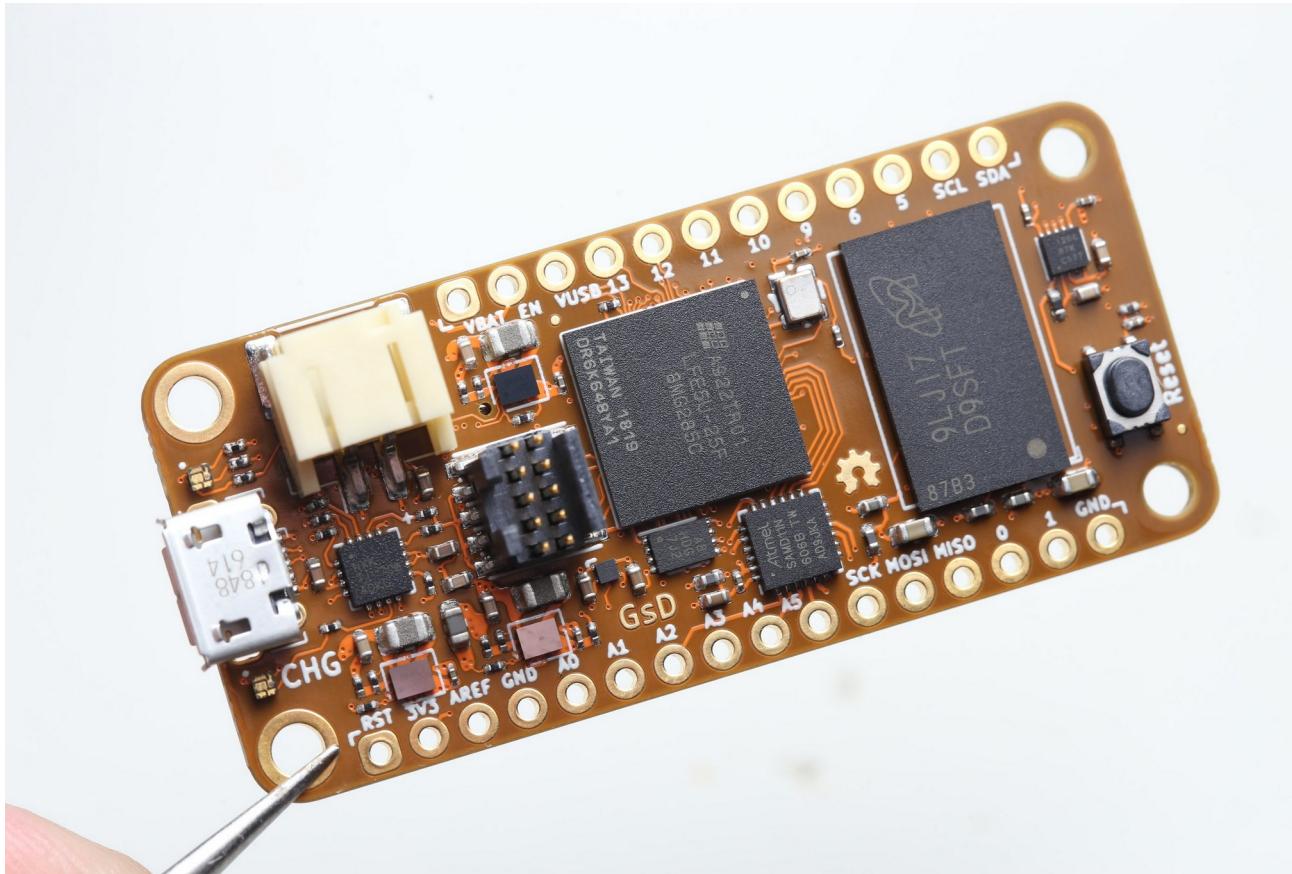
Open Source and FPGAs

- Open Source toolchains for FPGAs!
 - Project X-Ray and SymbiFlow for Xilinx Series 7
 - [Timothy 'mithro' Ansell](#): “Xilinx Series 7 FPGAs Now Have a Fully Open Source Toolchain!” (*almost*)
 - [youtube.com/watch?v=EHePto95qoE](https://www.youtube.com/watch?v=EHePto95qoE)



Open Source and FPGAs

- Open Source Hardware boards with Lattice ECP5 FPGA with open RISC-V “soft” CPU:
 - Orange Crab by Greg Davill
 - <https://github.com/gregdavill/OrangeCrab>





Greg @ #36c3
@GregDavill



Replying to @mithro @pdp7 and 2 others

Done. 😊

```
File Edit View Terminal Tabs Help
SRAM:      4KB
L2:        8KB
MAIN-RAM: 131072KB

----- Initialization -----
Initializing SDRAM...
SDRAM now under software control
Read leveling:
m0, b0: |11100000| delays: 01+-01
best: m0, b0 delays: 01+-01
m1, b0: |11100000| delays: 01+-01
best: m1, b0 delays: 01+-01
SDRAM now under hardware control
Memtest OK

----- Boot -----
Booting from serial...
Press Q or ESC to abort boot completely.
sL5DdSMmkekro
[LXTERM] Received firmware download request from the device.
[LXTERM] Uploading buildroot/Image to 0xc0000000 (4545524 bytes)...
[LXTERM] Upload complete (85.6KB/s).
[LXTERM] Uploading buildroot/rootfs.cpio to 0xc0800000 (8029184 bytes)...
[ 0:43 ] 1.2K views => | 98%
```



Open Source and FPGAs

- Radiona.org ULX3S
 - <https://www.crowdsupply.com/radiona/ulx3s>
-

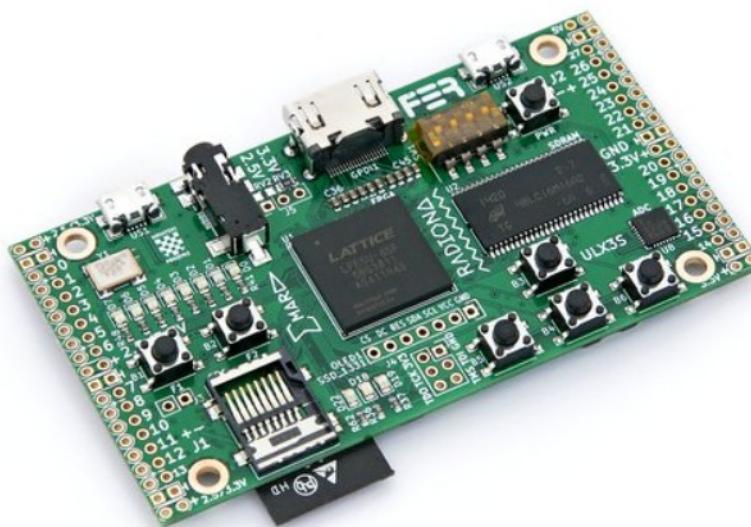
ULX3S

A powerful, open hardware ECP5 FPGA dev board

This project is coming soon. Sign up to receive updates and be notified when this project launches.

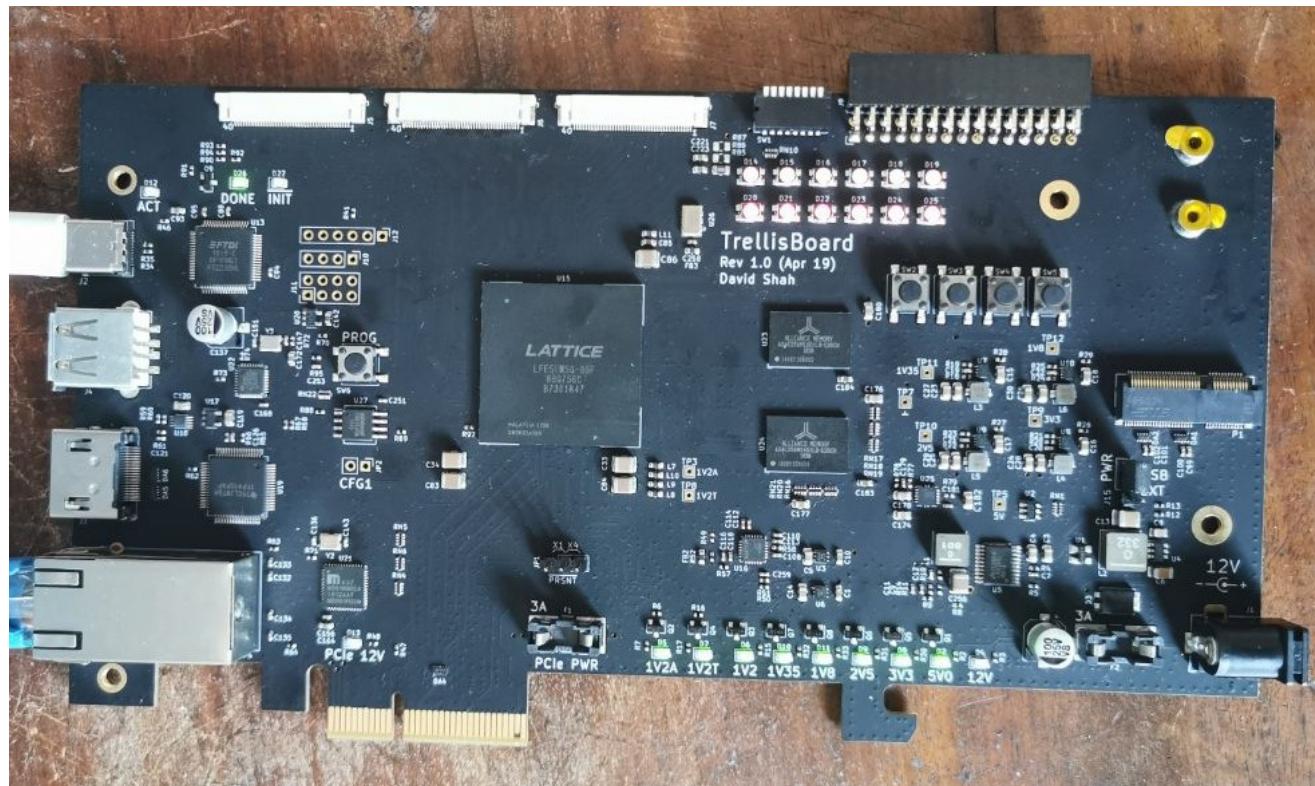
me@example.com

Subscribe



Open Source and FPGAs

- Open Source Hardware boards with Lattice ECP5 FPGA with open RISC-V “soft” CPU:
 - David Shah's Trellis board (Ultimate ECP5 Board)
 - <https://github.com/daveshah1/TrellisBoard>

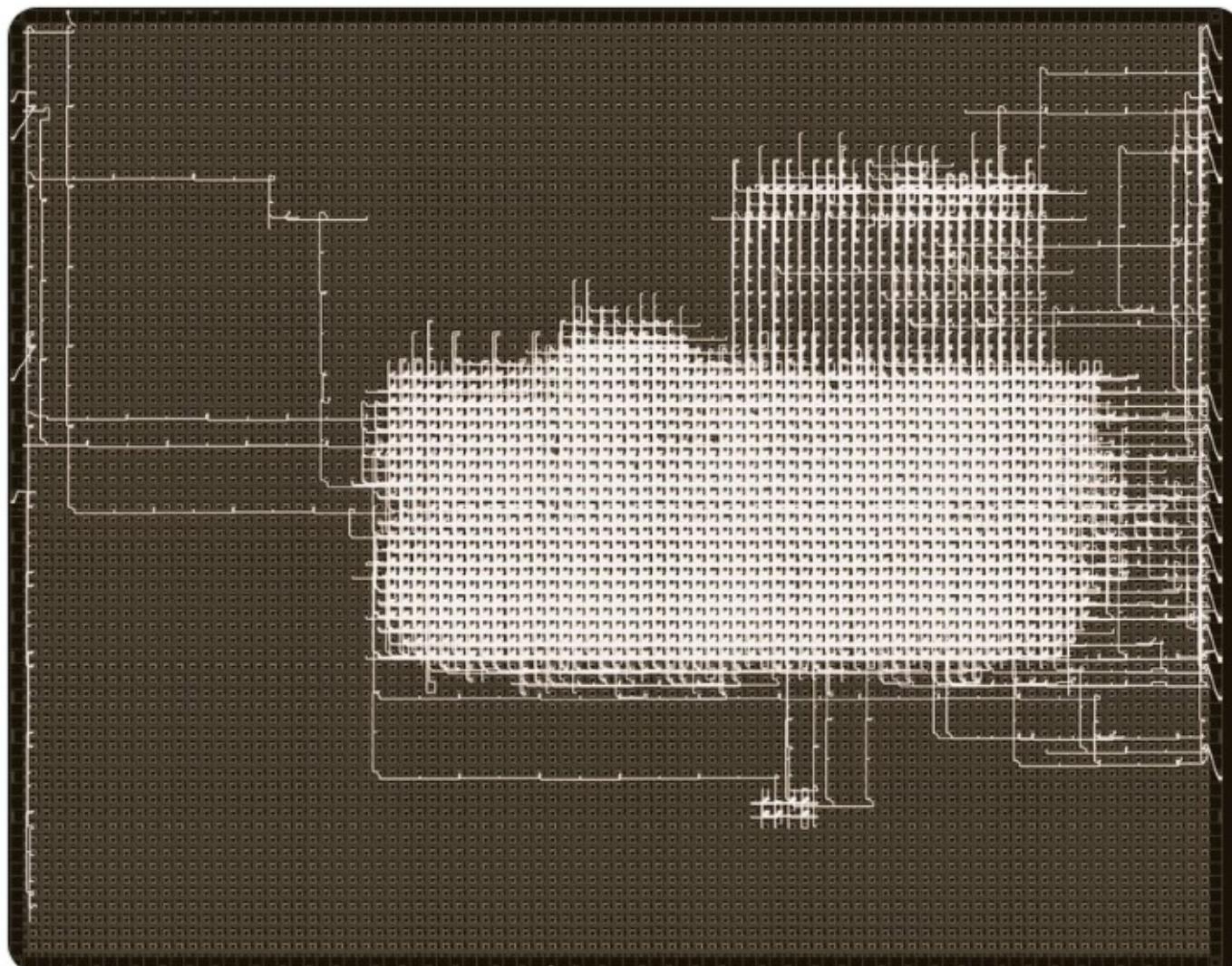




OSS FPGA & EDA tools
@ico_TC



This is how a Linux capable core looks like on an
FPGA. [#nextpnratwork](#)



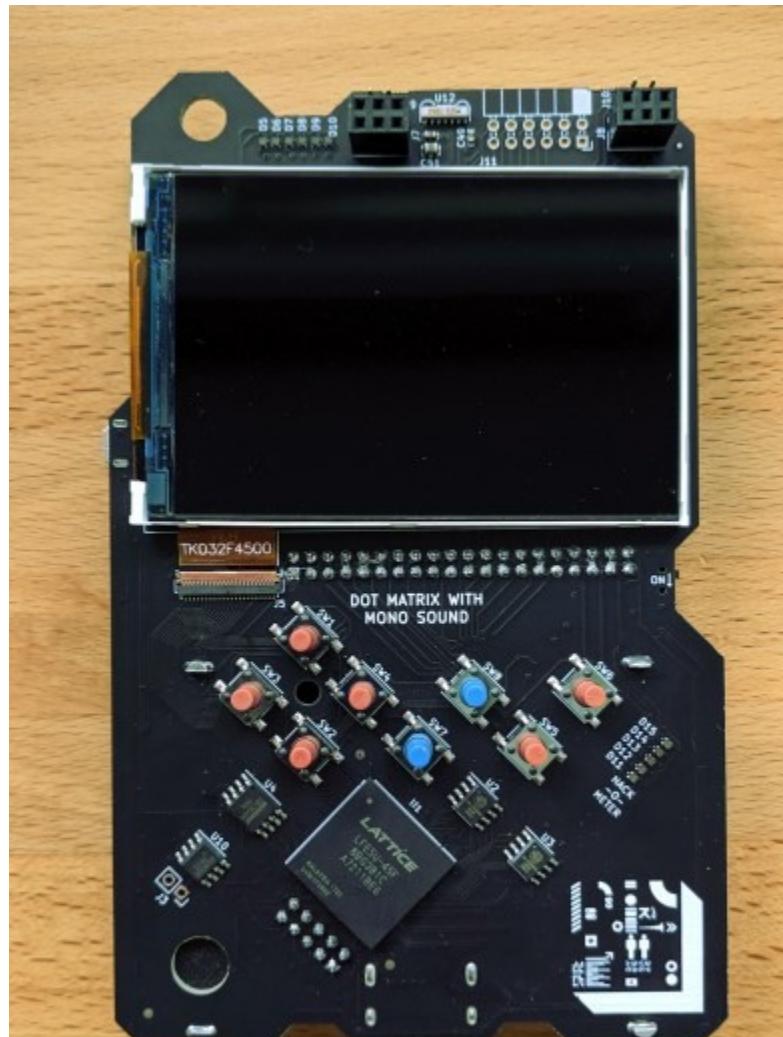
Slides: <https://github.com/pdp7/talks/blob/master/fosdem20.pdf>



Section:
Linux on the Hackaday Badge

Hackaday 2019 Supercon badge

- RISC-V “soft” core on ECP5 FPGA
- Gigantic FPGA In A Game Boy Form Factor



“Team Linux on Badge”



“Team Linux on Badge”

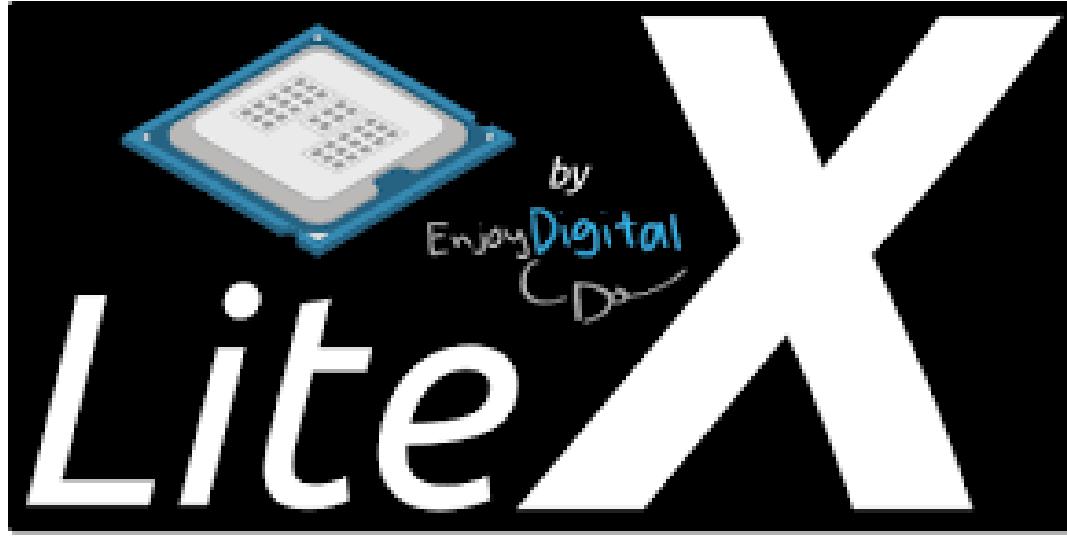
- Blog post: Hackaday Supercon badge boots Linux using SDRAM cartridge
 - <https://blog.oshpark.com/2019/12/20/boot-linux-on-this-hackaday-supercon-badge-with-this-sdram-cartridge/>
- Michael Welling (@QwertyEmdedded), Tim Ansell (@mithro), Sean Cross (@xobs), Jacob Creedon (@jacobcreedon)
- First attempt: use the built-in 16MB SRAM... no luck :(
 - (*though xobs now might have a way to do it*)

“Team Linux on Badge”

- Second attempt:
 - Jacob Creedon designed an a cartridge board that adds 32MB of SDRAM to the Hackaday Supercon badge... before the event!



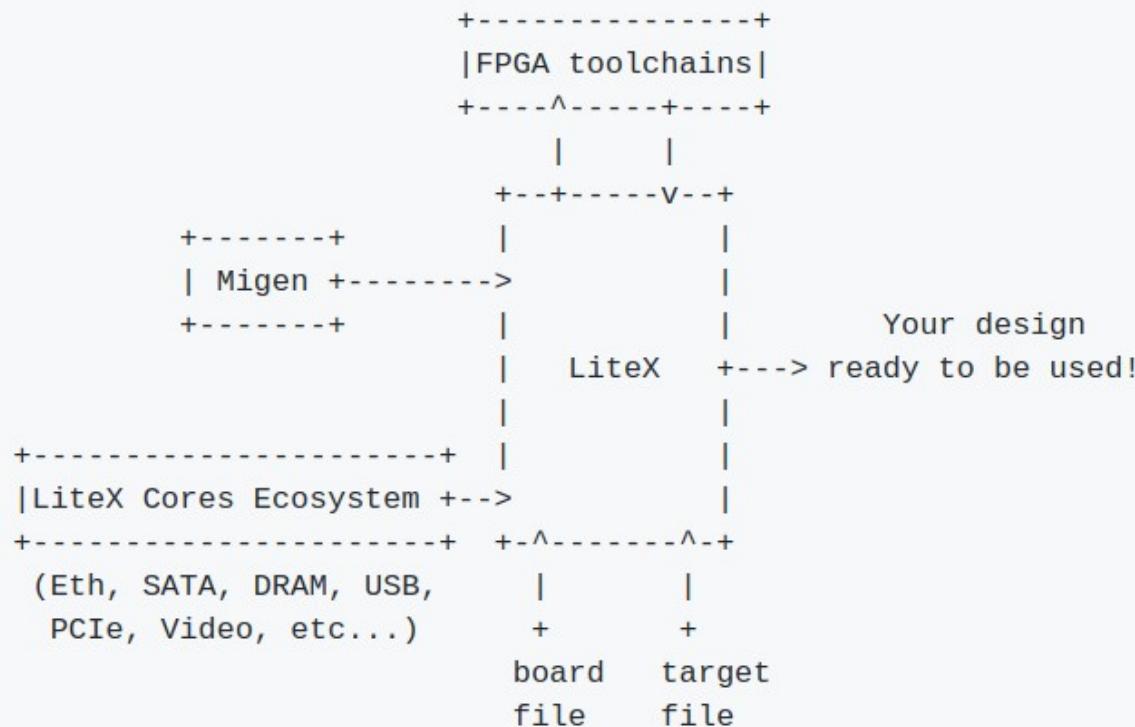




Build your hardware, easily!

- LiteX used to build cores, create SoCs and full FPGA designs.
- LiteX is based on Migen
- Migen lets you do FPGA design in Python!
- <https://github.com/enjoy-digital/litex>

Typical LiteX design flow:



LiteX already supports various softcores CPUs: LM32, Mor1kx, PicoRV32, VexRiscv and is compatible with the LiteX's Cores Ecosystem:

Name	Build Status	Description
LiteDRAM	build passing	DRAM
LiteEth	build passing	Ethernet
LitePCIe	build passing	PCIe
LiteSATA	build passing	SATA

Linux on LiteX-VexRiscv

- VexRiscv: 32-bit Linux Capable RISC-V CPU
 - SoC built using VexRiscv core and LiteX modules like LiteDRAM, LiteEth, LiteSDCard, ...
 - github.com/litex-hub/linux-on-litex-vexriscv



- upstream support for Hackaday Supercon badge:
 - <https://github.com/litex-hub/litex-boards/pull/31>

[litex-hub / litex-boards](#)

Unwatch 7 Unstar 17 Fork 24

Code Issues 2 Pull requests 1 Actions Projects 0 Wiki Security Insights

add the Hackaday Supercon ECP5 badge #31

Merged enjoy-digital merged 1 commit into `litex-hub:master` from `pdp7:master` 21 days ago

Conversation 18 Commits 1 Checks 1 Files changed 2 +461 -0

 pdp7 commented 22 days ago • edited

Contributor + ...

Add the [Hackaday Supercon 2019 badge](#) which has an ECP5 FPGA.

These changes are from a [fork](#) by Michael Welling (@mwelling)

During Supercon, we tried two approaches:

- use the built-in 16MB QSPI SRAM
- use add-on cartridge with 32MB SDRAM by Jacob Creedon

We were not able to get the QSPI SRAM working so I've removed those changes, and I have just added the changes that are needed to boot Linux with the 32MB SDRAM.

In addition to @mwelling, thank you to Jacob Creedon (@jcreedon), @gregdavill, Tim Ansell (@mithro), and Sean Cross (@xobs) who all helped get Linux working on this badge.

Reviewers
No reviews

Assignees
No one assigned

Labels
None yet

Projects
None yet

Milestone

- upstream support for Hackaday Supercon badge:
 - <https://github.com/litex-hub/litex-boards/pull/31>

Merged add the Hackaday Supercon ECP5 badge #31 Changes from all commits ▾ File filter... ▾ Jump to... ▾ ⚙ Review changes ▾

215 litex_boards/partner/platforms/hadbadge.py

```

@@ -0,0 +1,215 @@
+ from litex.build.generic_platform import *
+ from litex.build.lattice import LatticePlatform
+
+ # IOs -----
+
+ _io = [
+     ("clk8", 0, Pins("U18"), IOStandard("LVCMOS33")),
+     ("programn", 0, Pins("R1"), IOStandard("LVCMOS33")),
+     ("serial", 0,
+         Subsignal("rx", Pins("U2"), IOStandard("LVCMOS33"), Misc("PULLMODE=UP")),
+         Subsignal("tx", Pins("U1"), IOStandard("LVCMOS33")),
+     ),
+     ("led", 0, Pins("E3 D3 C3 C4 C2 B1 B20 B19 A18 K20 K19"), IOStandard("LVCMOS33")), # Anodes
+     ("led", 1, Pins("P19 L18 K18"), IOStandard("LVCMOS33")), # Cathodes via FET
+     ("usb", 0,
+         Subsignal("d_p", Pins("F3")),
+         Subsignal("d_n", Pins("G3")),
+         Subsignal("pullup", Pins("E4")),
+         Subsignal("vbusdet", Pins("F4")),
+         IOStandard("LVCMOS33")
+     ),
+     ("keypad", 0,
+         Subsignal("left", Pins("G2"), Misc("PULLMODE=UP"))
+     )
+ ]

```

- upstream support for Hackaday Supercon badge:
 - <https://github.com/litex-hub/litex-boards/pull/31>

Merged add the Hackaday Supercon ECP5 badge #31 Changes from all commits ▾ File filter... ▾ Jump to... ▾ ⚙ ▾ Review changes ▾

246 litex_boards/partner/targets/hadbadge.py

Viewed ...

```
@@ -0,0 +1,246 @@
+#!/usr/bin/env python3
+
+ # This file is Copyright (c) 2018-2019 Florent Kermarrec <florent@enjoy-digital.fr>
+ # This file is Copyright (c) 2018 David Shah <dave@ds0.me>
+ # License: BSD
+
+ import argparse
+ import sys
+
+ from migen import *
+ from migen.genlib.resetsync import AsyncResetSynchronizer
+
+ from litex_boards.platforms import hadbadge
+
+ from litex.soc.cores.clock import *
+ from litex.soc.integration.soc_sdram import *
+ #from litex.soc.integration.soc_core import *
+ from litex.soc.integration.builder import *
+
+ #from .spi_ram_dual import SpiRamDualQuad
+
+ from litedram import modules as litedram_modules
+ from litedram.phy import GENSDRPHY
```

[Code](#)[Issues 17](#)[Pull requests 2](#)[Actions](#)[Security](#)[Insights](#)

add the Hackaday Supercon ECP5 badge #68

Mergedenjoy-digital merged 1 commit into [litex-hub:master](#) from [pdp7:master](#)  21 days ago[Conversation 2](#)[Commits 1](#)[Checks 0](#)[Files changed 1](#)

pdp7 commented 22 days ago

Contributor

+ ...

Add the [Hackaday Supercon 2019 badge](#) which has an ECP5 FPGA.

These changes are from [a fork](#) by Michael Welling (@**mwellings**)

During Supercon, we tried two approaches:

- use the built-in 16MB QSPI SRAM
- use add-on cartridge with 32MB SDRAM by Jacob Creedon

We were not able to get the QSPI SRAM working so I've removed those changes, and I have just added the changes that are needed to boot Linux with the 32MB SDRAM.

In addition to @**mwellings**, thank you to Jacob Creedon (@**jcreedon**), @**gregdavill**, Tim Ansell

Merged

add the Hackaday Supercon ECP5 badge #68

Changes from all commits ▾ File filter... ▾ Jump to... ▾ ⚙

▼ 13 [make.py] ↗

```
@@ -160,6 +160,16 @@ def __init__(self):  
160      160          def load(self):  
161      161              os.system("ujprog build/ulx3s/gateware/top.svf")  
162      162  
163 + # HADBadge support -----  
164 +  
165 + class HADBadge(Board):  
166 +     def __init__(self):  
167 +         from litex_boards.targets import hadbadge  
168 +         Board.__init__(self, hadbadge.BaseSoC, {"serial"})  
169 +  
170 +     def load(self):  
171 +         os.system("dfu-util --alt 2 --download build/hadbadge/gateware/top.bit --reset")  
172 +  
163      173      # OrangeCrab support -----  
164      174  
165      175      class OrangeCrab(Board):  
@@ -209,6 +219,7 @@ def load(self):  
209      219          # Lattice
```

[Code](#)[Issues 21](#)[Pull requests 3](#)[Actions](#)[Projects 0](#)[Wiki](#)[Security](#)[In](#)

add 32MB SDRAM for hadbadge #97

Mergedenjoy-digital merged 1 commit into [enjoy-digital:master](#) from [pdp7:master](#)  21 days ago[Conversation 2](#)[Commits 1](#)[Checks 0](#)[Files changed 1](#)

pdp7 commented 22 days ago

Contributor



...

Add AS4C32M8SA-7TCN 32MB SDRAM used on cartridge PCB by Jacob Creedon (@jcreedon) for the [Hackaday Supercon 2019 badge](#) which has an ECP5 FPGA.

These changes are from [a fork](#) by Michael Welling (@mwelling)

In addition to @mwelling, thank you to Jacob Creedon (@jcreedon), @gregdavill, Tim Ansell (@mithro), and Sean Cross (@xobs) who all helped get Linux working on this badge.

KiCad design files by @jcreedon for the SDRAM cartridge are [available on GitHub](#).

There is also a [shared project](#) to order the SDRAM cartridge PCB.

Refer to [my blog post](#) for more information.

Merged

add 32MB SDRAM for hadbadge #97

Changes from all commits ▾

File filter... ▾

Jump to... ▾



9 litedram/modules.py



```
@@ -190,6 +190,15 @@ class AS4C32M16(SDRAMModule):
190      technology_timings = _TechnologyTimings(tREFI=64e6/8192, tWTR=(2, None), tCCD=(1,
191      speedgrade_timings = {"default": _SpeedgradeTimings(tRP=18, tRCD=18, tWR=12, tRFC=
192
193 +     class AS4C32M8(SDRAMModule):
194 +         memtype = "SDR"
195 +         # geometry
196 +         nbanks = 4
197 +         nrows  = 8192
198 +         ncols   = 1024
199 +         # timings
200 +         technology_timings = _TechnologyTimings(tREFI=64e6/8192, tWTR=(2, None), tCCD=(1,
201 +         speedgrade_timings = {"default": _SpeedgradeTimings(tRP=20, tRCD=20, tWR=15, tRFC=
193
194     # DDR -----
195
```



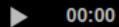
- Opened GitHub issue:
 - optimize performance on Hackaday Badge #35
 - <https://github.com/litex-hub/litex-boards/issues/35>
- Now 10x faster!
 - <https://asciinema.org/a/Pcm3vd1BEdEKY9srYX6MsNfCE>
 - Thanks to [enjoy-digital](#)



Asciicast updated.

```
[ 7.896093] Initramfs unpacking failed: junk in compressed archive
[ 7.953813] workingset: timestamp_bits=30 max_order=13 bucket_order=0
[ 9.236463] Block layer SCSI generic (bsg) driver version 0.4 loaded (major 253)
[ 9.239004] io scheduler mq-deadline registered
[ 9.240102] io scheduler kyber registered
[ 13.977920] f0001000.serial: MMIO 0xf0001000 (irq = 0, base_baud = 0) is a liteuart
[ 13.980290] printk: console [liteuart0] enabled
[ 13.980290] printk: console [liteuart0] enabled
[ 13.982965] printk: bootconsole [sbi0] disabled
[ 13.982965] printk: bootconsole [sbi0] disabled
[ 14.058778] libphy: Fixed MDIO Bus: probed
[ 14.074959] i2c /dev entries driver
[ 14.247461] NET: Registered protocol family 10
[ 14.307974] Segment Routing with IPv6
[ 14.315214] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[ 14.455698] Freeing unused kernel memory: 140K
[ 14.457905] This architecture does not have kernel memory protection.
[ 14.459170] Run /init as init process
mount: mounting tmpfs on /dev/shm failed: Invalid argument
mount: mounting tmpfs on /tmp failed: Invalid argument
mount: mounting tmpfs on /run failed: Invalid argument
Starting syslogd: OK
Starting klogd: OK
Running sysctl: OK
Initializing random number generator... [ 23.063050] random: dd: uninitialized urandom read (512 bytes read)
done.
Starting network: OK
Starting dropbear sshd: [ 27.336210] random: dropbear: uninitialized urandom read (32 bytes read)
OK
```

Welcome to Buildroot



00:00



Linux boots on Hackaday Supercon FPGA badge [10x faster!]

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optimize performance on Hackaday Badge #35

[Edit](#)[New issue](#)[Open](#)

pdp7 opened this issue 17 days ago · 7 comments



pdp7 commented 17 days ago

Contributor



...

Assignees

No one assigned

Labels

None yet

Projects

None yet

Milestone

No milestone

Notifications

Customize

[Unsubscribe](#)

You're receiving notifications because
you're watching this repository.

[Related to comments in PR #31 \(comment\)](#)

The performance of the ECP5 Hackaday Badge with 32MB SDRAM is "painfully" slow.

@mithro suggested there could be some issue with the configuration.

@enjoy-digital has attempted some optimizations:

[#31 \(comment\)](#)

With [enjoy-digital/litedram@ 34e6c24](#) and [enjoy-digital/litex@ fa22d6a](#) we have a ~10% boot time speedup on designs using SDRAM:

- De0Nano: 94.6.s to 84.6s
- ULX3S: 75.9s to 68.2s

On Arty with DDR3 the gain is effect more limited: 8.7s to 8.4s. That would be interesting to test this on the badge.

I will measure if the boot time improve

Open

optimize performance on Hackaday Badge #35

pdp7 opened this issue 17 days ago · 7 comments



pdp7 commented 15 days ago • edited

Contributor

Author

+ 😊 ...

@enjoy-digital WOW! much faster! It gets to login in 28 seconds (previous version was 258 seconds).

Recording:

<https://asciinema.org/a/Pcm3vd1BEdEKY9srYX6MsNfCE>

Text:

```
pdp7@x1:~/dev/enjoy/linux-on-litex-vexriscv$ lxterm --images=images.json /dev  
[LXTERM] Starting....  
lBIOS CRC passed (561ab1e2)
```

```
Migen git sha1: 063188e  
LiteX git sha1: -----
```

```
-===== SoC =====  
CPU: VexRiscv @ 48MHz  
ROM: 32KB  
SRAM: 4KB  
Lo:
```



enjoy-digital committed 15 days ago

1 parent 2317519

commit 39ce39a298f5



Showing **1 changed file** with **5 additions** and **3 deletions**.

8 litex/soc/integration/soc_sdram.py

@@ -26,12 +26,13 @@ class SoCSDRAM(SoCCore):

26 26 }

```
27      27      csr_map.update(SoCCore.csr_map)
```

28

```
-      def __init__(self, platform, clk_freq, l2_size=8192, **kwargs):
```

```
29 +     def __init__(self, platform, clk_freq, l2_size=8192, l2_data_width=128, **kwargs):
```

```
30      30          SoCCore.__init__(self, platform, clk_freq, **kwargs)
```

```
31      31          if not self.integrated_main_ram_size:
```

```
32      32          if self.cpu_type is not None and self.csr_data_width > 32:
```

```
raise NotImplementedException("BIOS supports SDRAM initialization only for c
```

34 - self.l2_size = l2_size

34 + self.l2_size = l2_size

```
35 +         self.l2_data_width = l2_data_width
```

35 36

36 37 self, s dram phy = []

```
37      38          self.wb_sdram_ifs = []
```

Slides:

github.com/pdp7/talks/blob/master/fosdem20.pdf

Drew Fustini
drew@oshpark.com
[@pdp7](https://twitter.com/pdp7)



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