Slides: https://github.com/pdp7/talks/blob/master/rv-pint.pdf

Linux on RISC-V

with open source hardware and open source FPGA tools

Raspberry Pint (May 26th, 2020)

Drew Fustini

drew@beagleboard.org

Twitter: @pdp7

RISC-V AMBASSADOR

Open Source Hardware

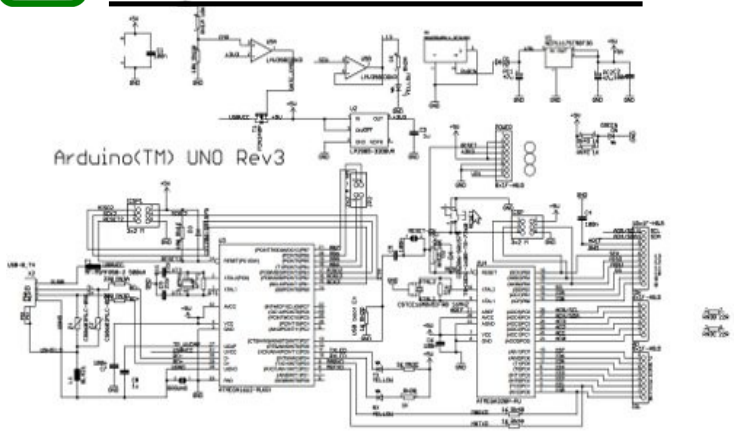
Statement of Principles:

Hardware whose **design** is made **publicly available** so that anyone can **study**, **modify**, **distribute**, **make**, and **sell** the design or hardware based on that design

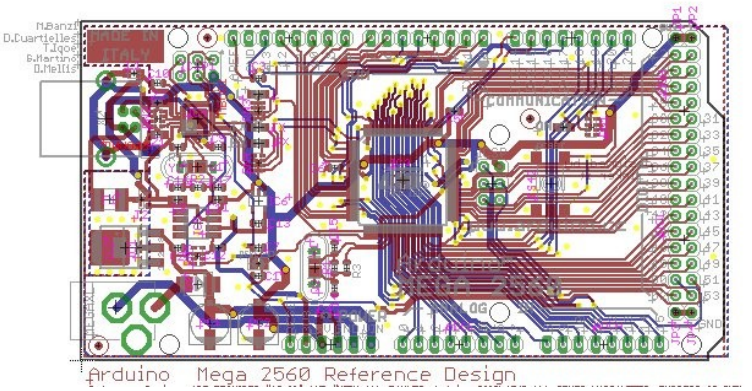
Open Source Hardware

Documentation required for electronics:

☑ Schematics



☑ Board Layout



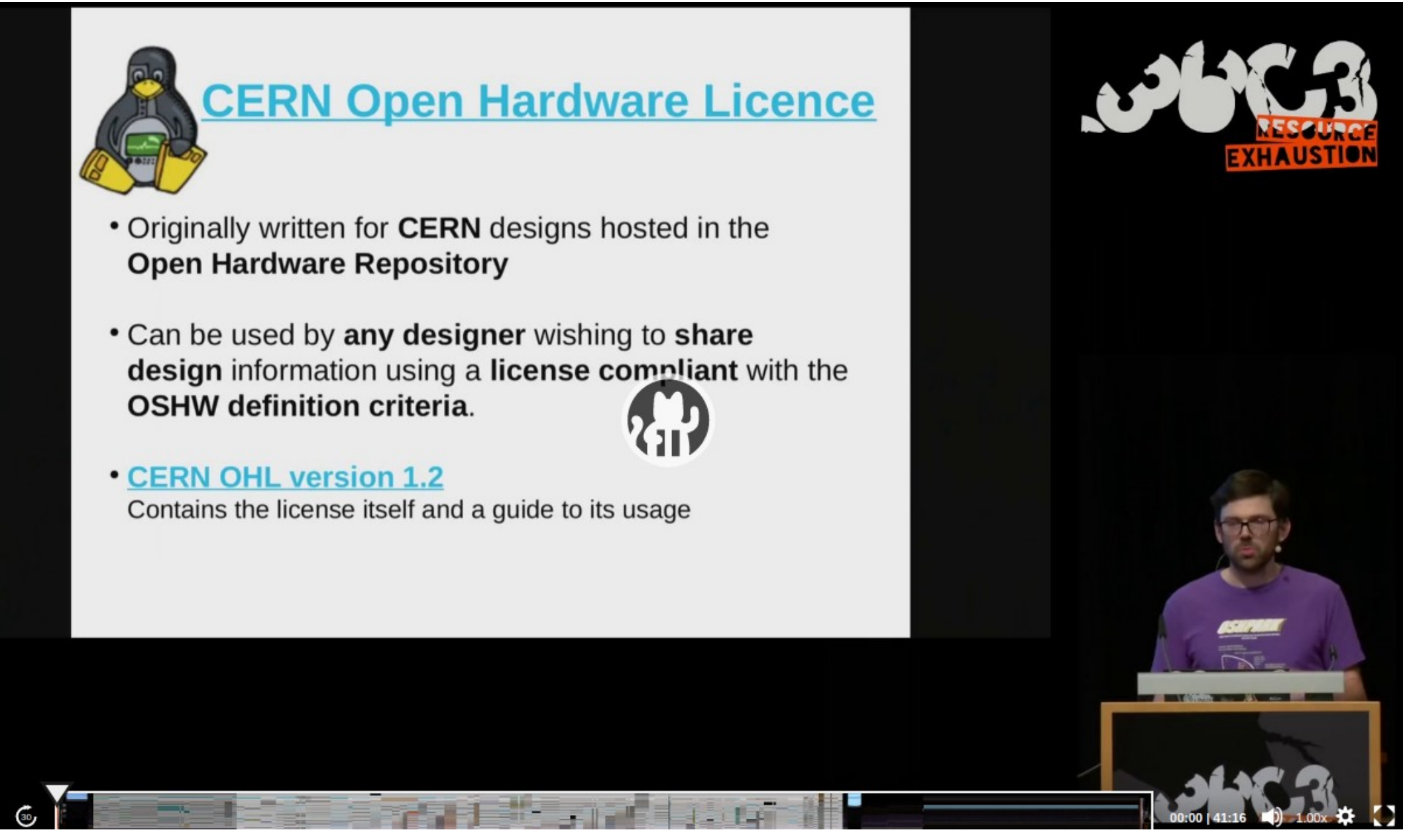
Editable source files for CAD software such as KiCad or EAGLE

☑ Bill of Materials *(BoM)*

Not strict requirement, but best practice is for all components available from distributors in **low quantity**

36c3 talk:

Linux on Open Source Hardware with Open Source chip design



Slides: https://github.com/pdp7/talks/blob/master/fossn20.pdf

Section:
RISC-V
the instruction set for everything?

- When you write a C or C++ program, it is compiled into instructions for the microprocessor (CPU) to execute.

- How does the compiler know what instructions the CPU understands?
  - defined by the **Instruction Set Architecture**
  - The **ISA** is a standard, a set of rules that define the tasks the processor can perform.
  - Examples: x86 (Intel/AMD) and ARM
    - Both are proprietary and need commercial licensing

- **RISC-V: Free and Open RISC Instruction Set Arch**
  - “new instruction set architecture (ISA) that was originally designed to support computer architecture research and education and is now set to become a standard open architecture for industry”

- **RISC-V: Free and Open RISC Instruction Set Arch**
  - Instruction Sets Want To Be Free: A Case for RISC-V
    - David Patterson, UC Berekely – *co-creator of the original RISC!*
    - https://www.youtube.com/watch?v=mD-njD2QKN0
  - RISC-V Summit 2019: State of the Union
    - Krste Asanovic, UC Berkeley
    - https://www.youtube.com/watch?v=jdkFi9_Hw-c

What's Different about RISC-V?

- ***Simple***
  - Far smaller than other commercial ISAs
- ***Clean-slate design***
  - Clear separation between user and privileged ISA
  - Avoids µarchitecture or technology-dependent features
- A ***modular*** ISA designed for ***extensibility/specialization***
  - Small standard base ISA, with multiple standard extensions
  - Sparse and variable-length instruction encoding for vast opcode space
- ***Stable***
  - Base and standard extensions are frozen
  - Additions via optional extensions, not new versions
- ***Community designed***
  - With leading industry/academic experts and software developers

RISC-V Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Commercial software:
Lauterbach, Segger, IAR, Micrium, ExpressLogic, Ashling, AntMicro, Imperas, UltraSoC …

RISC-V Foundation

ISA specification | Golden Model | Compliance

Hardware

Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Shakti, Serv, Swerv, Hummingbird, …

Commercial core providers:
Alibaba, Andes, Bluespec, Cloudbear, Codasip, Cortus, InCore, Nuclei, SiFive, Syntacore, …

Inhouse cores:
Nvidia, WD, +others

RISC-V and Industry

- Designed to be extensible
  - Microcontroller to supercomputer
- RISC-V Foundation now controls standard: riscv.org
  - Over 400 members: companies, universities and more
  - YouTube channel has hundreds of talks!
    - https://www.youtube.com/channel/UC5gLmcFuvdGbajs4VL-WU3g
- Companies like Nvidia and Western Digital will ship millions of devices with RISC-V
- Avoid ARM licensing fees
- Freedom to leverage open source implementations
    - BOOM, Rocket, PULP, SweRV, and many more

- lowRISC is a not-for-profit organisation whose goal is to produce a fully open source System-on-Chip (SoC) in volume
  - “We will produce a SoC design to populate a low-cost community development board and to act as an ideal starting point for derivative open-source and commercial designs”
- OpenTitan project with Google
  - Announcing OpenTitan, the First Transparent Silicon Root of Trust

- My column in the Hackspace Magazine is an introduction to RISC-V and how it is enabling open source chip design:
  - hackspace.raspberrypi.org/issues/27/


Drew Fustini

COLUMN SPARK

Open-source chips

Breaking free of chip design monopolies with RISC-V

Drew Fustini

@pdp7

Drew Fustini is a hardware designer and embedded Linux developer. He is the Vice President of the Open Source Hardware Association, and a board member of the BeagleBoard.org Foundation. Drew designs circuit boards for OSH Park, a PCB manufacturing service, and maintains the Adafruit BeagleBone Python library.

When we think about what open-source hardware means, we usually think about the board design being freely available. But what about the processor? Is there a way to make hardware that is truly open source? This month's column is dedicated to an exciting – and surprisingly political – development in chip design.

When you write a program in the Arduino IDE, it is compiled into instructions for the microcontroller to execute. How does the compiler know what instructions the chip understands? This is defined by the Instruction Set Architecture. The ISA is a standard, a set of rules that define the tasks the processor can perform.

> **The ISA is a standard, a set of rules that define the tasks the processor can perform**

Chances are that both your laptop and the data centre streaming your favourite movie are using an ISA owned by Intel or AMD. The processor in your smartphone is almost certainly using a proprietary ISA licensed from ARM. Proprietary standards can be overpriced, prevent innovation, or even disappear altogether when companies change strategy.

Enter RISC-V, a free and open ISA created by researchers at UC Berkeley, led by Krste Asanović and David Patterson. "We were always jealous that you could get industrial-strength software that was open," Patterson explained to VentureBeat at the RISC-V Summit back in December. "But when it came to hardware, it was proprietary. Now, with RISC-V, we get the same kind of benefit. It helps education, and it helps competition."

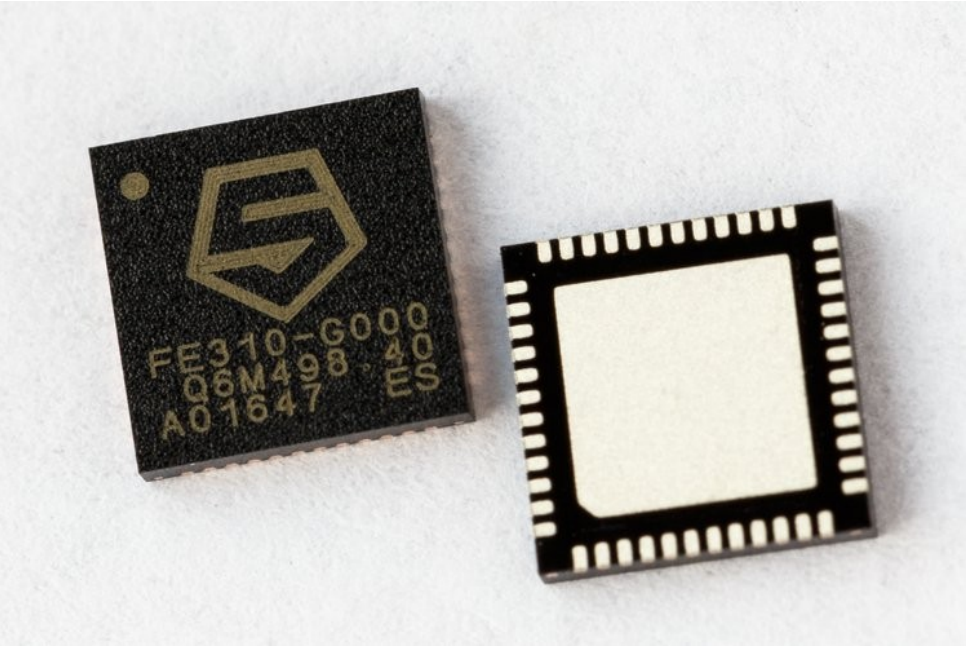
This open standard proved to be useful outside of academia. Nvidia and Western Digital are now shipping millions of devices with RISC-V processors. These companies have the freedom to leverage open-source implementations while avoiding ARM licensing fees – which can really add up when shipping large volumes.

Nations such as India see the importance of being able to create processors that are not under the control of a foreign corporation, who may be forced to build in backdoors for their own government. There is also strong interest from chipmakers in China, especially now that US companies have been banned from doing business with Huawei.

With these financial and political motivations, plus an increasingly mature software ecosystem, including Linux support, it won't be long before you have a device with a RISC-V processor in your home or pocket.

You can learn more about the exciting possibilities that RISC-V unleashes from Dr. Megan Wachs by pointing your web browser to **hsmag.cc/qw4ed1**.

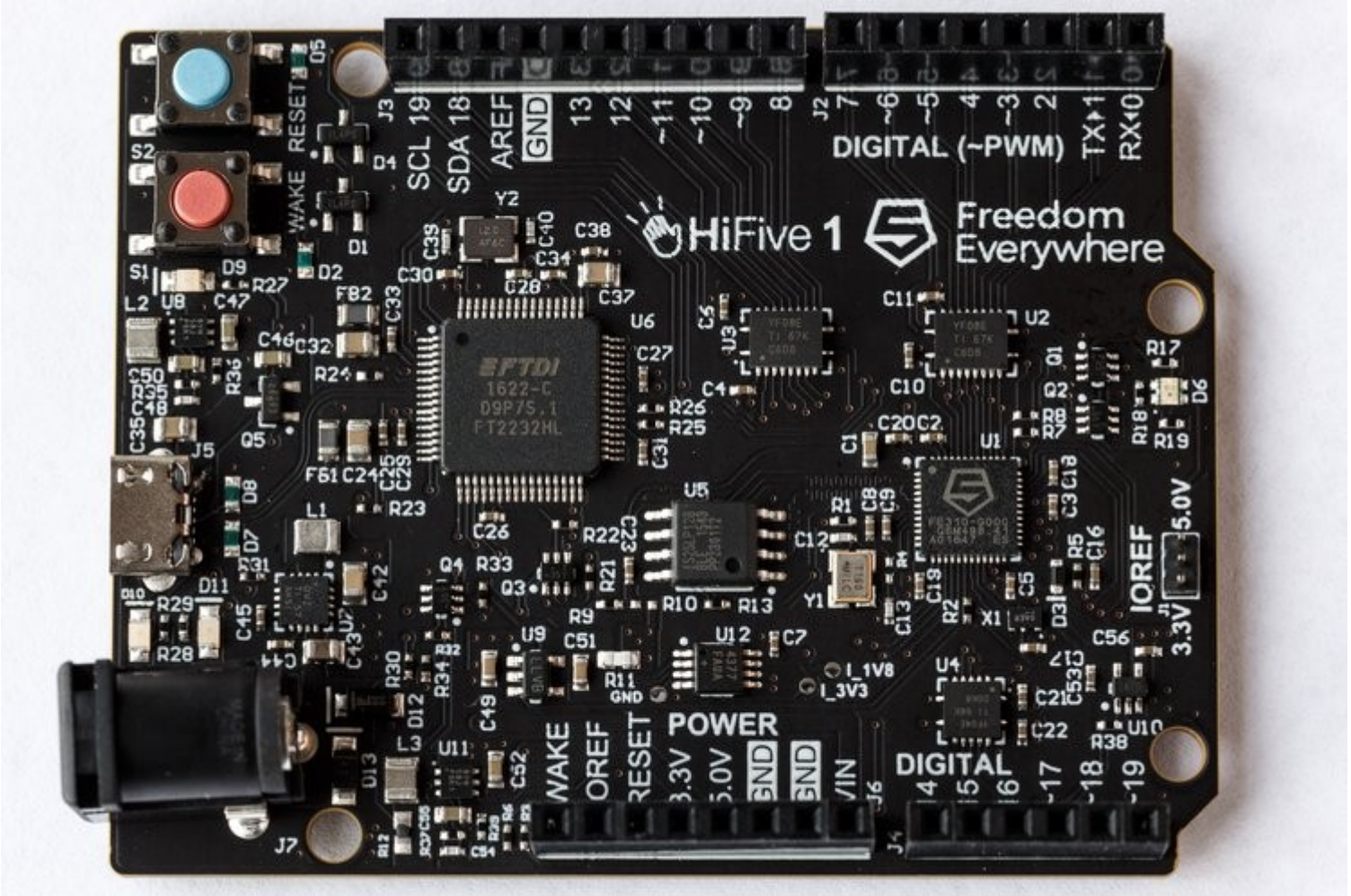
SiFive



- “founded by the creators of the free and open RISC-V architecture as a reaction to the end of conventional transistor scaling and escalating chip design costs”

SiFive FE310 microcontroller

- **HiFive1**: Arduino-Compatible RISC-V Dev Kit

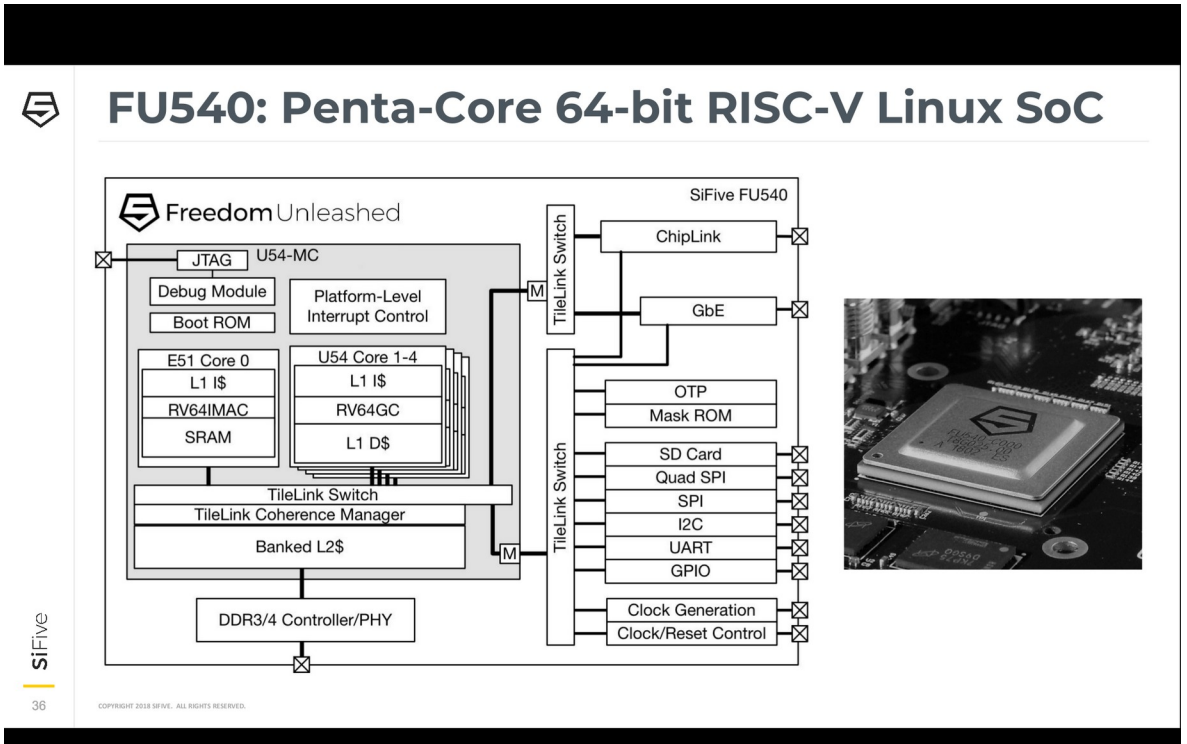


Section:

Linux-capable RISC-V chips

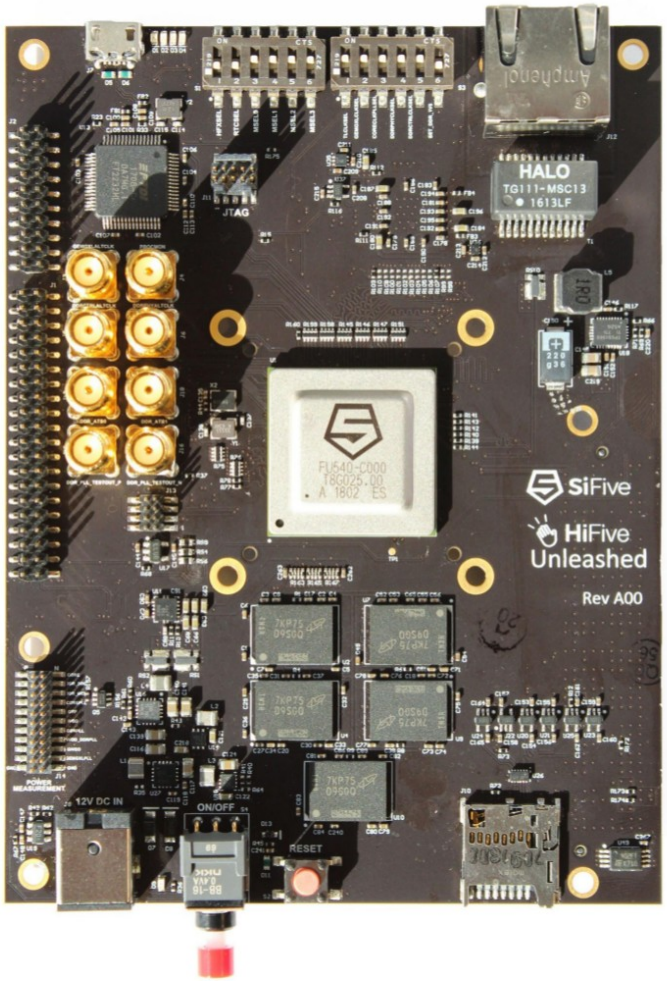
SiFive: Linux on RISC-V

- FOSDEM 2018 talk
  - YouTube: “Igniting the Open Hardware Ecosystem with RISC-V: SiFive's Freedom U500 is the World's First Linux-capable Open Source SoC Platform”
  - Interview with Palmer Dabbelt of SiFive



SiFive: Linux on RISC-V

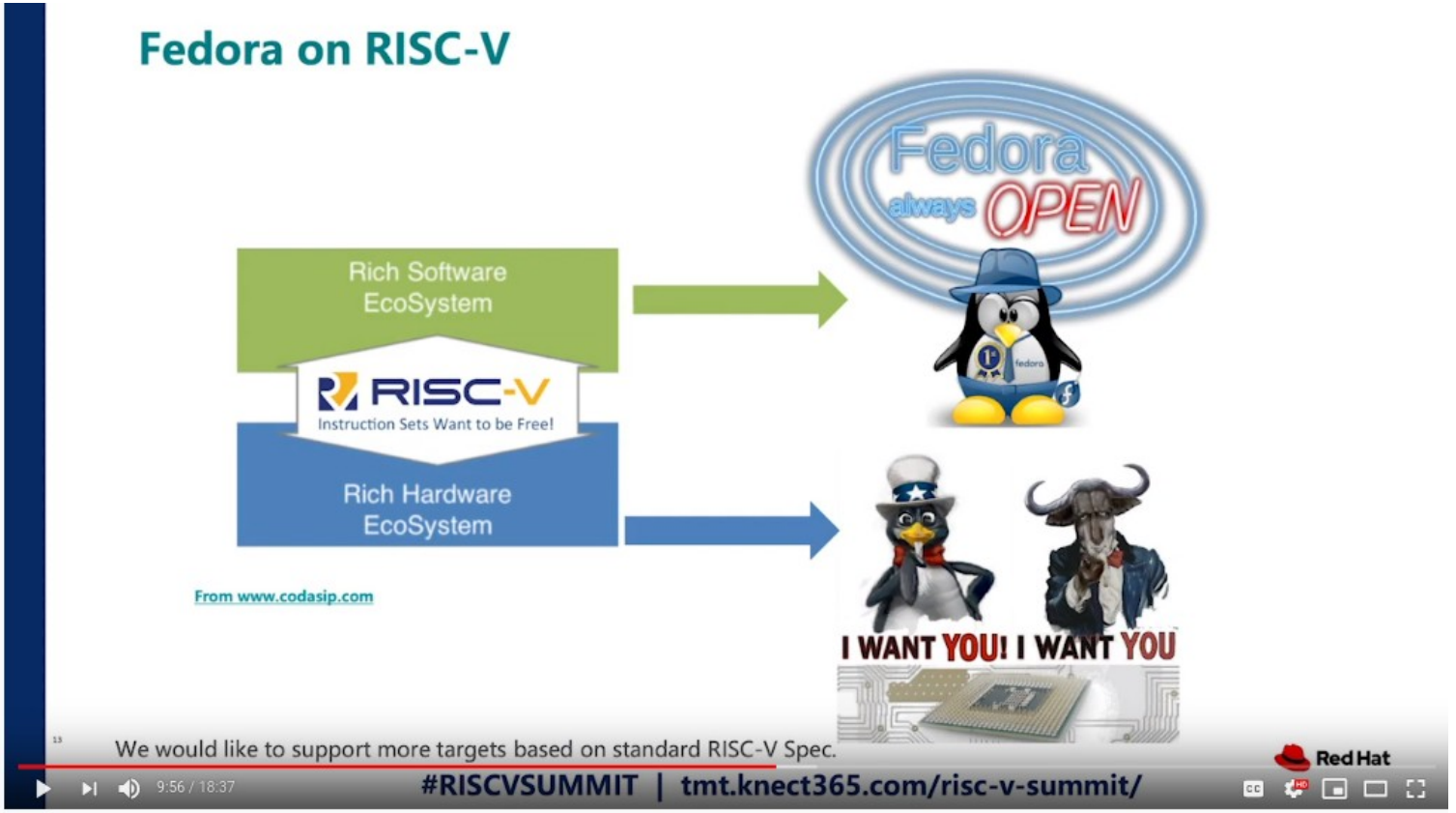
HiFive Unleashed



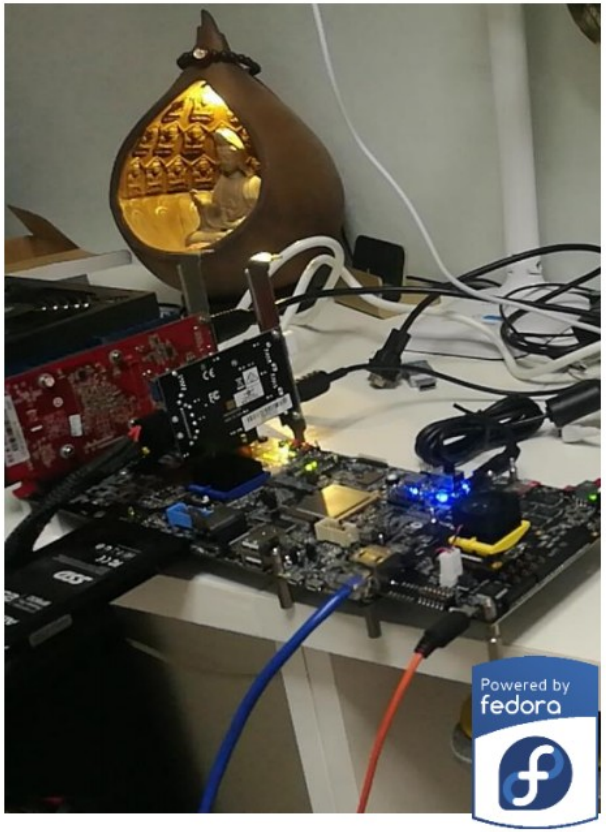
- World's First Multi-Core RISC-V Linux Development Board
  - SiFive FU540-C000 (built in 28nm)
    - 4+1 Multi-Core Coherent Configuration, up to 1.5 GHz
    - 4x U54 RV64GC Application Cores with Sv39 Virtual Memory Support
    - 1x E51 RV64IMAC Management Core
    - Coherent 2MB L2 Cache
    - 64-bit DDR4 with ECC
    - 1x Gigabit Ethernet
  - 8 GB 64-bit DDR4 with ECC
  - Gigabit Ethernet Port
  - 32 MB Quad SPI Flash
  - MicroSD card for removable storage
  - FMC connector for future expansion with add-in cards

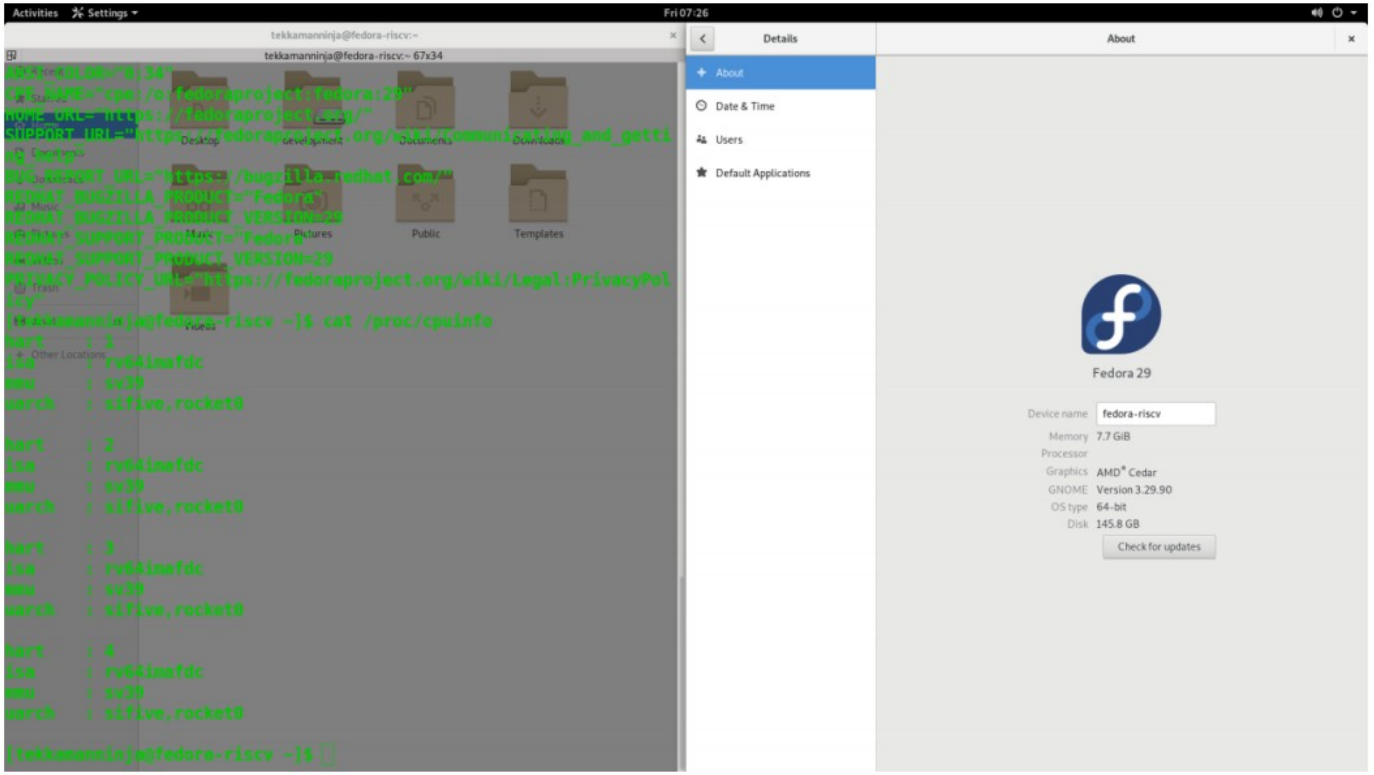
RISC-V Summit 2019: Linux on RISC V Fedora and Firmware Status Update

- https://www.youtube.com/watch?v=WC6e3g8uWdk
- Wei Fu – Software Engineer, Red Hat



Fedora GNOME Image on SiFive Unleashed





Red Hat

Targets

Supported

Virtual: libvirt + QEMU

with graphics parameters (Spice).

Real Hardware: SiFive Unleashed

with Expansion Board, PCI-E graphic Card & SATA SSD

Tested

ANDES TECHNOLOGY

QEMU for AndeStar V5 && ADP-XC7KFF676

Andes QEMU and AndeShape **FPGA** board

ICT

SERVE risc-v

中国科学院计算技术研究所
INSTITUTE OF COMPUTING TECHNOLOGY, CHINESE ACADEMY OF SCIENCES

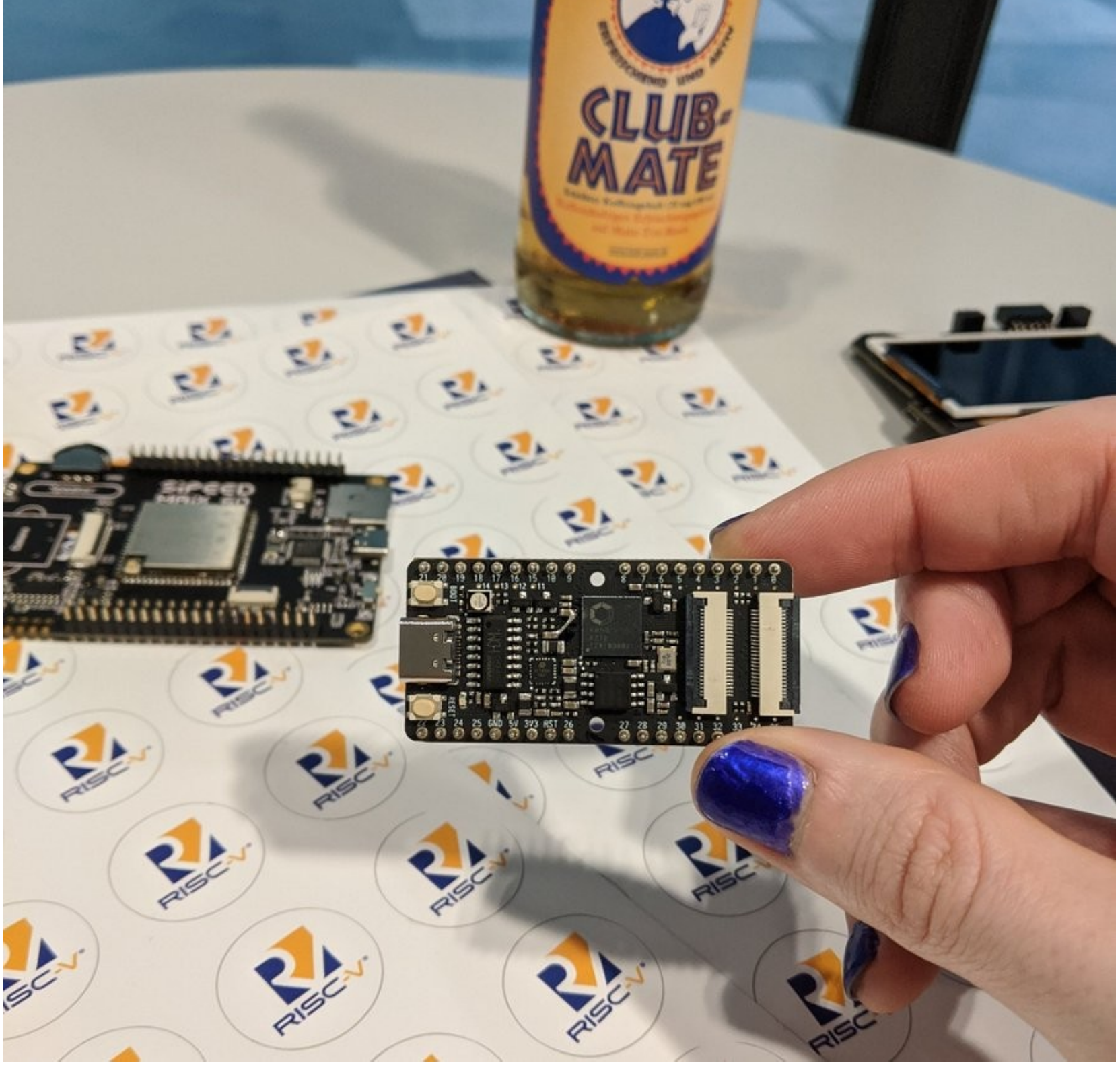
ICT SERVE Platform: FlameCluster

FPGA Cloud development platform (with PCI-E SSD and graphic Card)

RISC-V

This page contains details about a port of Debian for the RISC-V architecture called **riscv64**.

Contents


CLUB-
MATE
SIPEED
RISC-V

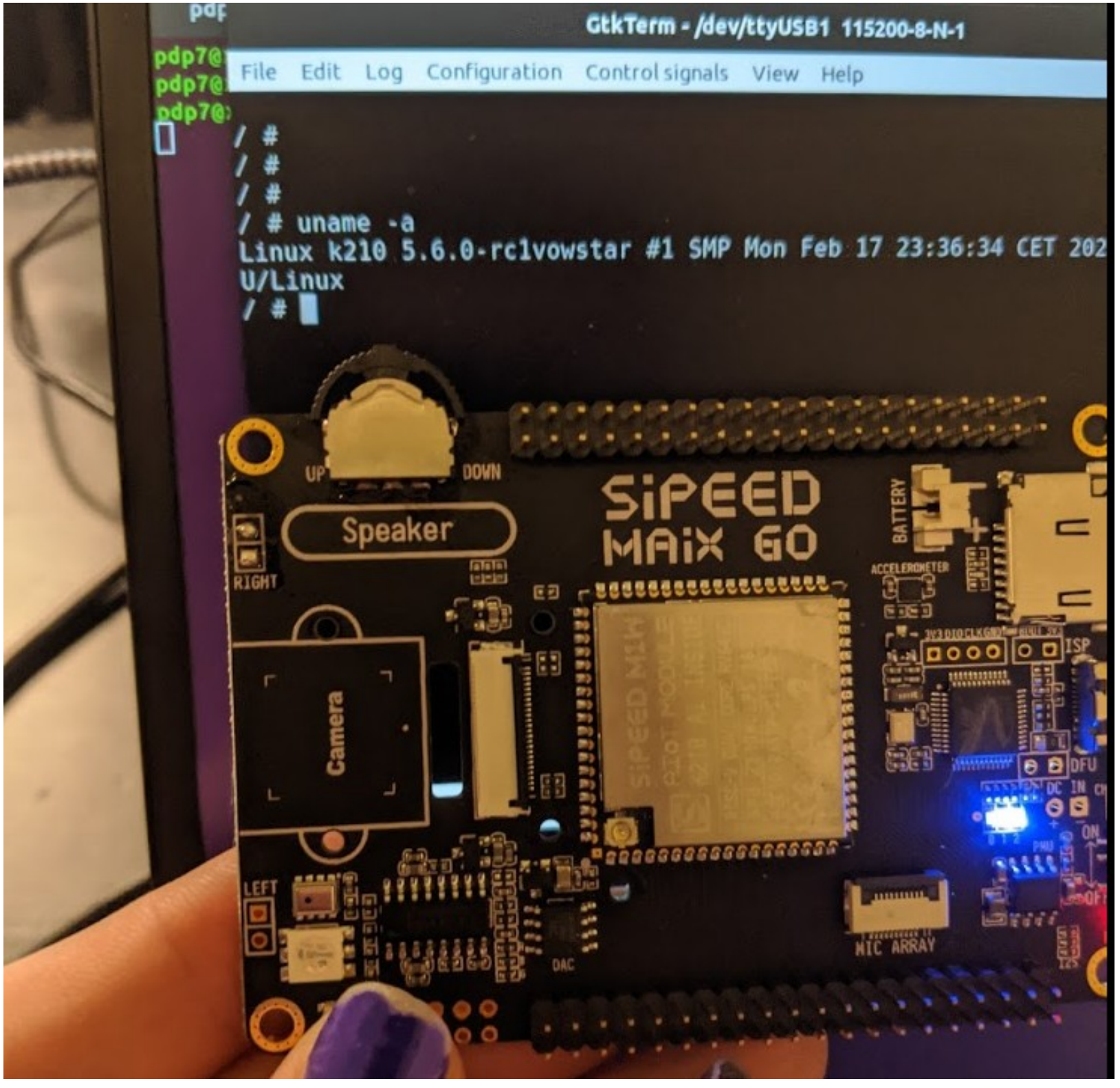
Kendryte K210 SoC + Busybox

Sipeed MAIX Go Board (6+2 MB SRAM)

```
[    0.000000] Linux version 5.1.0-rc5-00314-g375c2321604f (damien@washi) (gcc version 8.2.0 (Buildroot 2018.11-rc2-00003-ga0787e9)) #221 SMP Fri May 10 15:17:17 JST 20
[    0.000000] earlycon: sbi0 at I/O port 0x0 (options '')
[    0.000000] printk: bootconsole [sbi0] enabled
[    0.000000] initrd not found or empty - disabling initrd
[    0.000000] Zone ranges:
[    0.000000]   DMA32    [mem 0x0000000080000000-0x00000000807fffff]
[    0.000000]   Normal   empty
[    0.000000] Movable zone start for each node
[    0.000000] Early memory node ranges
[    0.000000]   node   0: [mem 0x0000000080000000-0x00000000807fffff]
[    0.000000] Initmem setup node 0 [mem 0x0000000080000000-0x00000000807fffff]
[    0.000000] elf_hwcap is 0x112d
[...]
[    0.000000] Built 1 zonelists, mobility grouping off.  Total pages: 2020
[    0.000000] Kernel command line: console=hvc0 earlycon=sbi init=/bin/bash
[    0.000000] Dentry cache hash table entries: 1024 (order: 1, 8192 bytes)
[    0.000000] Inode-cache hash table entries: 512 (order: 0, 4096 bytes)
[    0.000000] Sorting __ex_table...
[    0.000000] Memory: 6284K/8192K available (920K kernel code, 101K rwdata, 158K rodata, 393K init, 95K bss, 1908K reserved, 0K cma-reserved)
[    0.000000] SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=2, Nodes=1
[    0.000000] rcu: Hierarchical RCU implementation.
[    0.000000] rcu: RCU calculated value of scheduler-enlistment delay is 25 jiffies.
[    0.000000] NR_IRQS: 0, nr_irqs: 0, preallocated irqs: 0
[...]
[    0.251433] Freeing unused kernel memory: 392K
[    0.254361] This architecture does not have kernel memory protection.
[    0.259473] Run /bin/bash as init process

BusyBox v1.30.1 (2019-05-10 14:49:46 JST) hush - the humble shell

# mount -t proc none /proc
# cat /proc/cpuinfo
processor : 0
hart : 0
isa : rv64imafdc

processor : 1
hart : 1
isa : rv64imafdc
```

- **Linux now runs the low cost Kendryte K210 RISC-V processor**
  - dual core 64-bit RISC-V at 400MHz with 8MB SRAM
  - Sipeed MAix BiT for RISC-V is only $13!
  - Damien Le Moal at Linux Plumbers Conf: RISC-V NOMMU and M-mode Linux
    - youtube.com/watch?v=ycG592N9EMA&t=10394
    - jump to 2h 53m
  - Many RISC-V Improvements Ready For Linux 5.5: M-Mode, SECCOMP, Other Features
  - How to Build & Run Linux on Kendryte K210 RISC-V NOMMU Processor


File Edit Log Configuration Control signals View Help
/ # uname -a
Linux k210 5.6.0-rc1vowstar #1 SMP Mon Feb 17 23:
/ # cat /proc/meminfo |head
MemTotal: 6656 kB
MemFree: 2496 kB
MemAvailable: 2080 kB
Buffers: 0 kB
Cached: 1916 kB
SwapCached: 0 kB
Active: 0 kB
Inactive: 0 kB
Active(anon): 0 kB
Inactive(anon): 0 kB
/ # cat /proc/cpuinfo
processor : 0
hart : 0
isa : rv64imafdc
processor : 1
hart : 1
isa : rv64imafdc
/ # tcc -run -nostdlib hello.c
hello.c:2: warning: implicit declaration of functi
hello show 'n tell
/ #
TYPE-C
/dev/ttyUSB0 115200-8-N-1

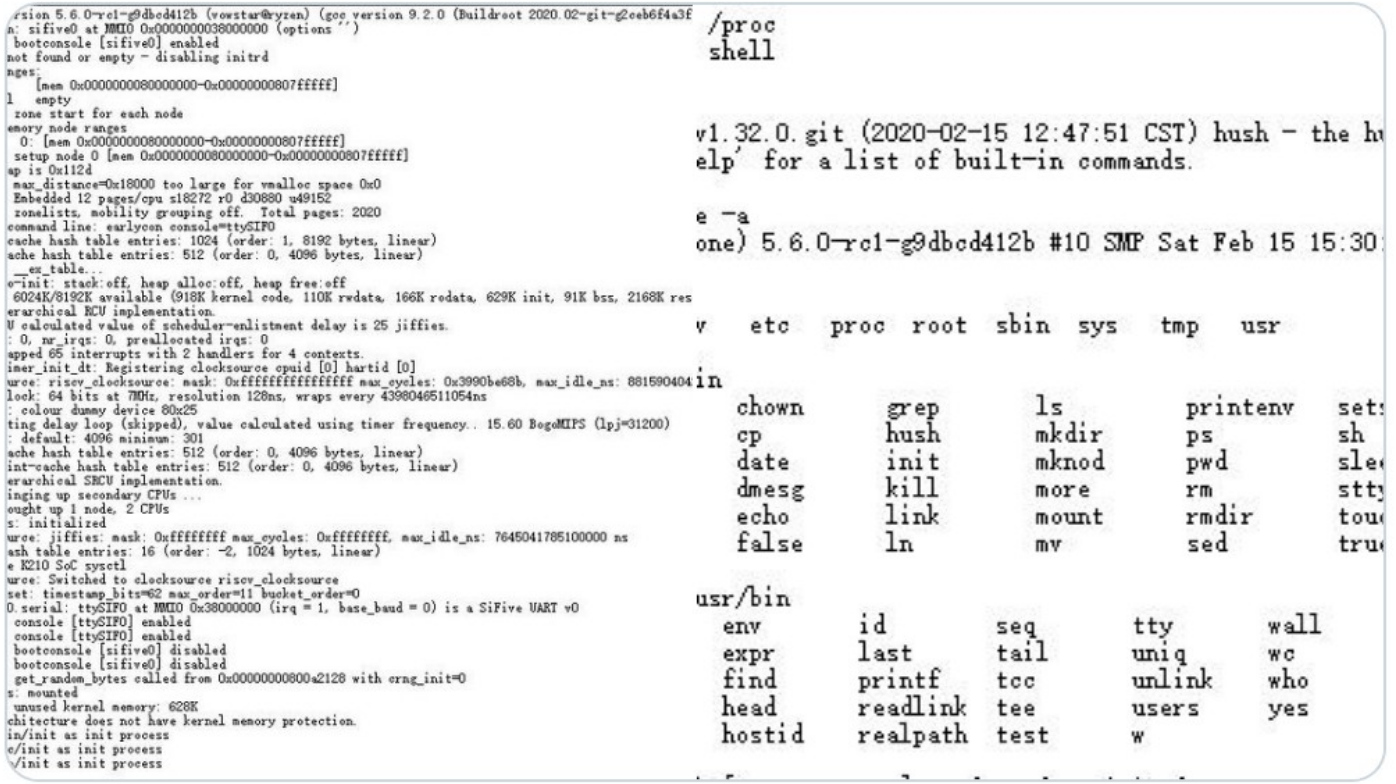

GtkTerm - /dev/ttyUSB1 115200-8-N-1
File Edit Log Configuration Control signals View Help
/ #
/ #
/ #
/ # uname -a
Linux k210 5.6.0-rc1vowstar #1 SMP Mon Feb 17 23:36:34 CET 202
U/Linux
/ #
UP
DOWN
Speaker
RIGHT
SiPEED
MAiX GO
BATTERY
ACCELEROMETER
ISP
DFU
Camera
LEFT
DAC
MIC ARRAY
DC IN
ON

- Sipeed now has prebuilt Linux 5.6
  - https://twitter.com/SipeedIO/status/1228594799675990016/

← **Tweet**

Sipeed
@SipeedIO

The prebuild linux-5.6.0-rc1 image for Maix Boards, Just burn and try it~
dl.sipeed.com/MAIX/MaixLinux…



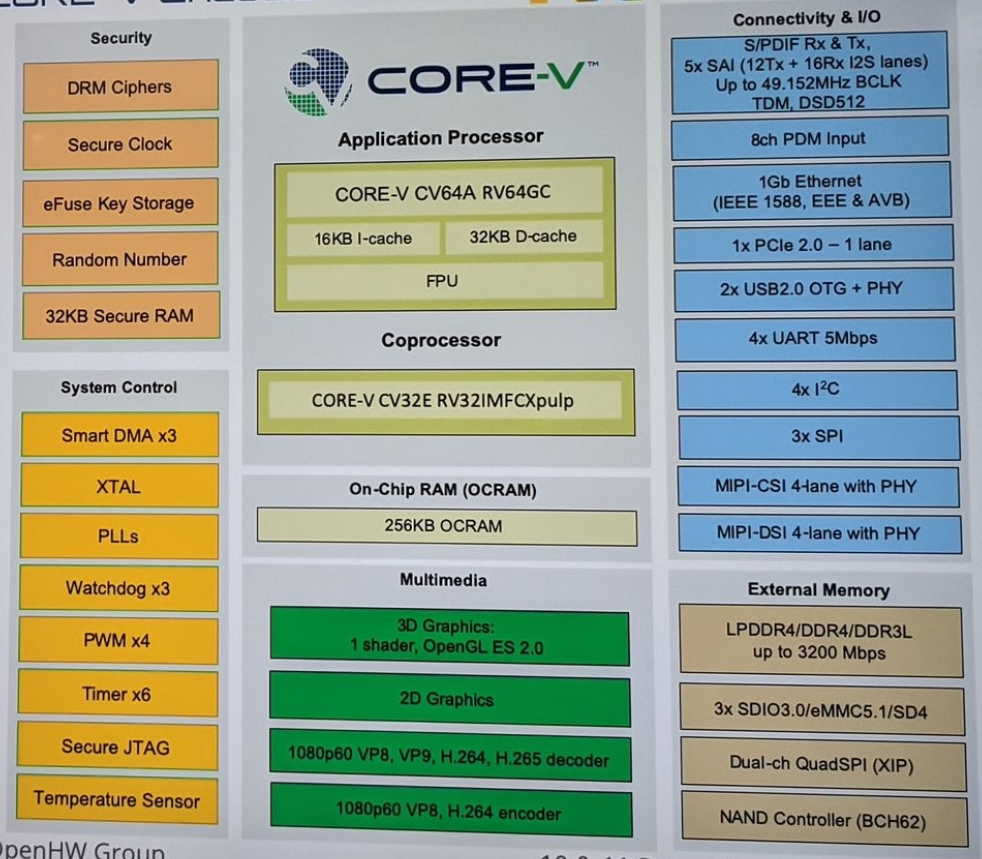
Coming in 2020

- Microchip PolarFire SoC FPGA
  - Hard RISC-V with FPGA fabric… like the Xilinx Zync for ARM
- OpenHW Core-V SoC which is similar to NXP iMX with RISC-V instead of ARM!
  - "OpenHW Group Unveils CORE-V Chassis SoC Project, Building on PULP Project IP"

CORE-V™ Chassis – tapeout 2H 2020

CORE-V Chassis based on NXP iMX Platform CORE-V™

- Linux capable 1.5GHz CV64A host CPU and CV32E coprocessor
- X32/x16 (LP)DDR4, DDR3L memory
- 3D / 2D GPUs with OpenGL support
- MIPI-DSI / CSI display / camera controllers
- Security: DRM Ciphers, key storage, random number generator, etc.
- GigE MAC
- PCIe 2.0 x1 port
- 2 USB 2.0 interfaces
- 3 SDIO interfaces for boot source, storage, etc



OPENHW GROUP™ PROVEN PROCESSOR IP

Slides: https://github.com/pdp7/talks/blob/master/rv-munich.pdf

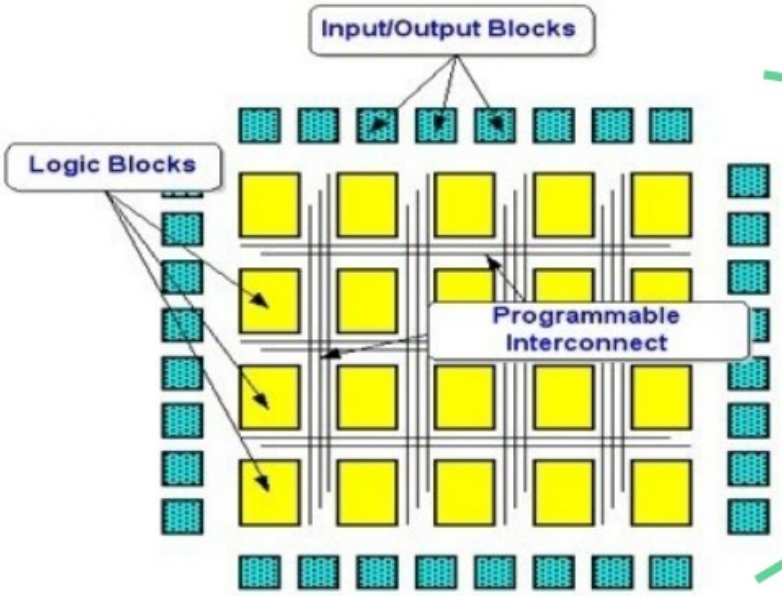
Section:

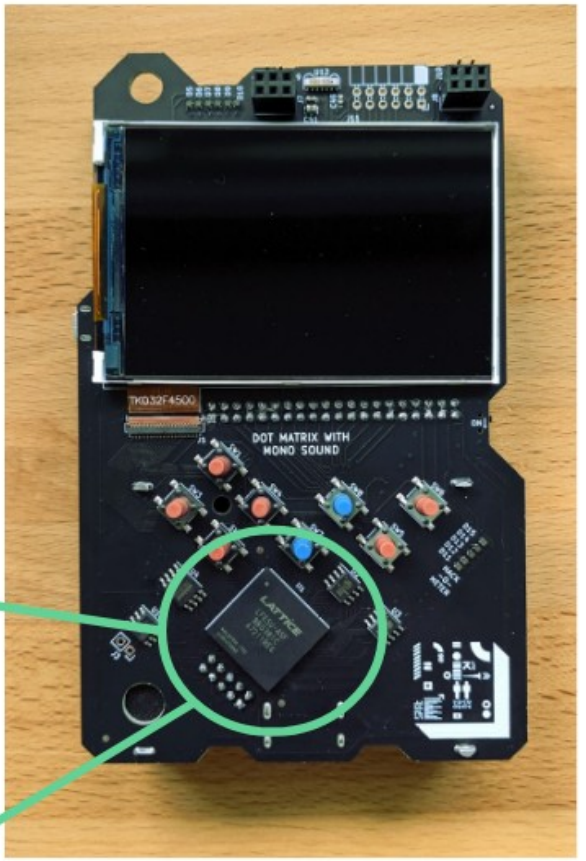
Open Source FPGA tools

- Keynote at Hackday Supercon 2019 by Dr. Megan Wachs of SiFive
- **“RISC-V and FPGAs: Open Source Hardware Hacking”**
  - https://www.youtube.com/watch?v=vCG5_nxm2G4

Where do FPGAs Come In?

- Field Programmable Gate Array
- Change a chip's HARDWARE in a few minutes
- Make it act like a new chip!





Open Source toolchains for FPGAs

- Project IceStorm for Lattice iCE40
  - “A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs”
    by Claire Wolf (oe1cxw) at 32c3

media.ccc.de

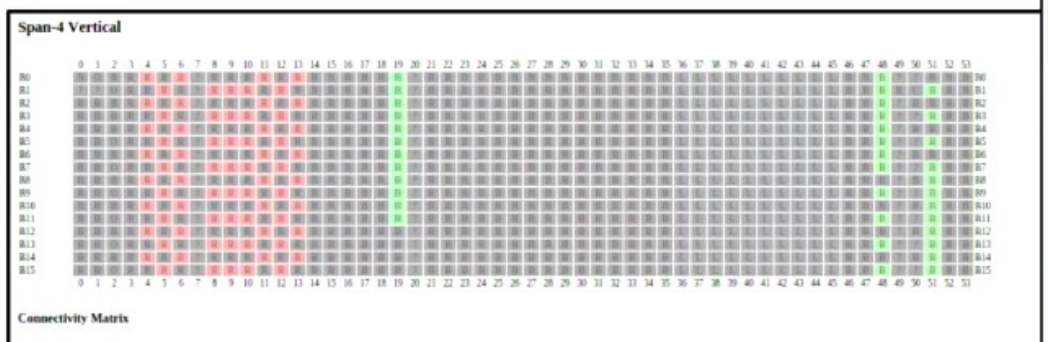
Search...

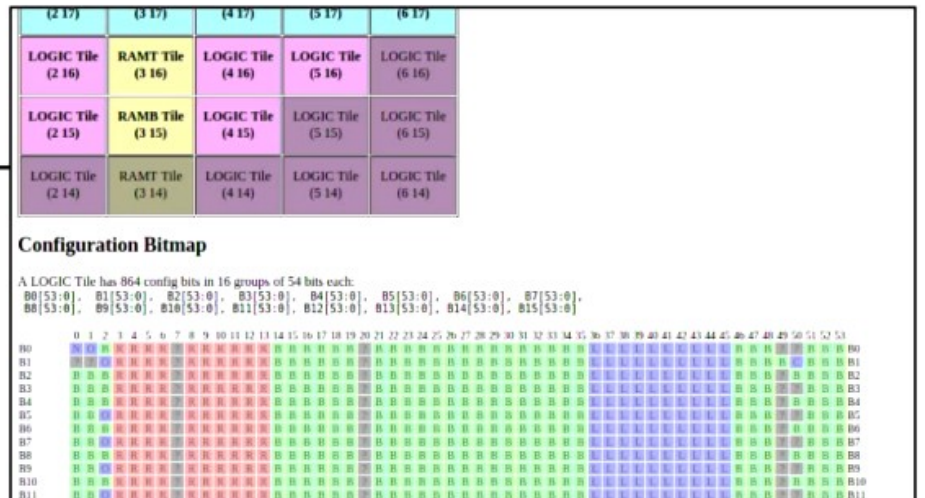
browse › congress › 2015 › event

A Free and Open Source Verilog-to-Bitstream Flow for iCE40 FPGAs

Clifford

Some screenshots from IceStrom Docs:



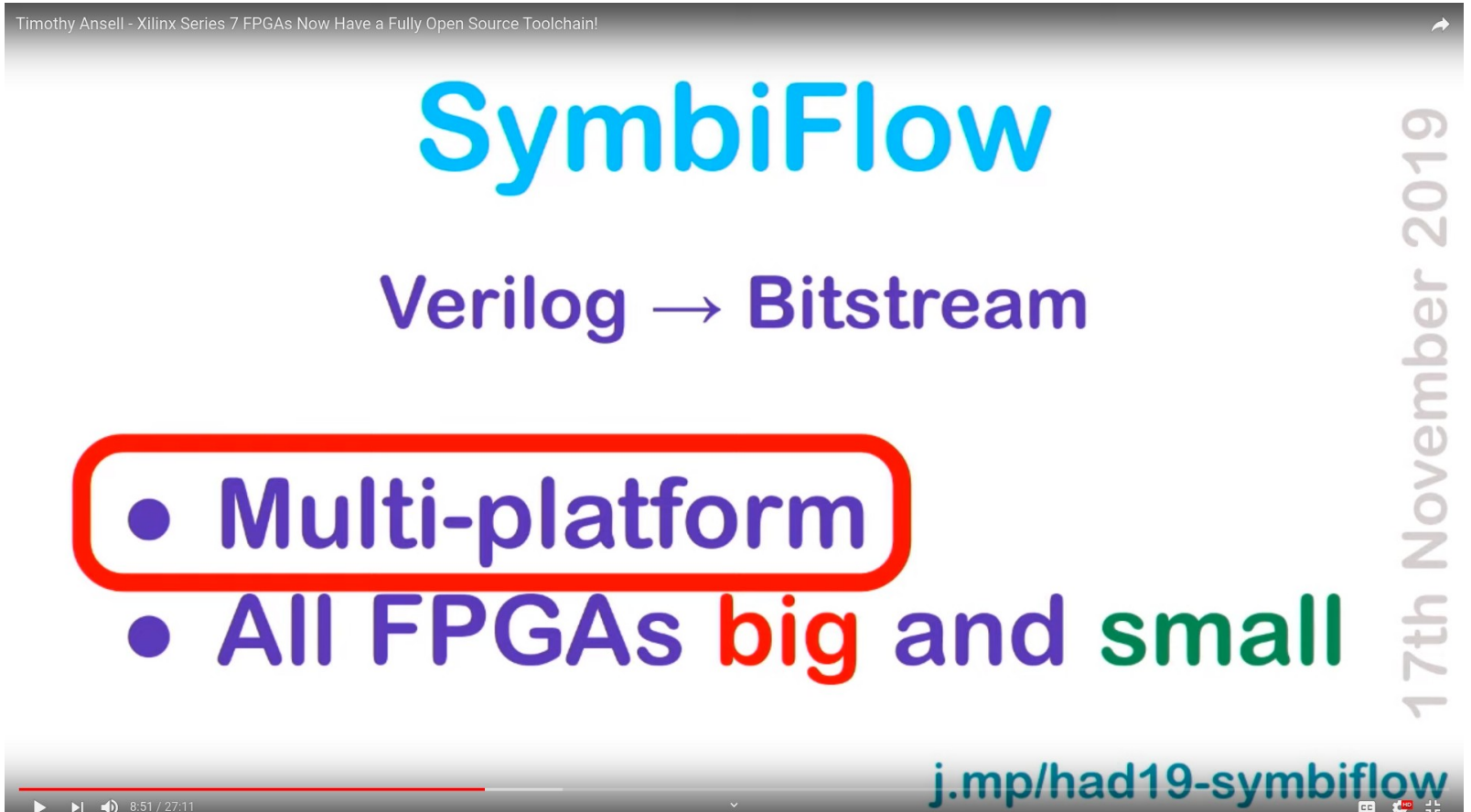


Open Source toolchains for FPGAs

- Project Trellis for Lattice ECP5
  - “Project Trellis and nextpnr FOSS FPGA flow for the Lattice ECP5”
    - David Shah (@fpga_dave)
      - youtube.com/watch?v=0se7kNes3EU

Open Source toolchains for FPGAs

- Project X-Ray & SymbiFlow for Xilinix Series 7
  - Timothy ‘mithro’ Ansell: “Xilinx Series 7 FPGAs Now Have a Fully Open Source Toolchain!” *(almost)*
    - youtube.com/watch?v=EHePto95qoE



Open Source and FPGAs

- Hackspace Magazine column about how about open source FPGA tools developed by Claire Wolf (oe1cxw), David Shah and others have made FPGAs more accessible than ever before to makers and hackers:
  - hackspace.raspberrypi.org/issues/26/

The rise of the FPGA

Reconfigure your chips to suit your project

Drew Fustini

@pdp7

Drew Fustini is a hardware designer and embedded Linux developer. He is the Vice President of the Open Source Hardware Association, and a board member of the BeagleBoard.org Foundation. Drew designs circuit boards for OSH Park, a PCB manufacturing service, and maintains the Adafruit BeagleBone Python library.

FPGAs have been the talk of the town at many of this year's hacker conferences. But what exactly is an FPGA, and why are they so hot right now?

FPGA stands for Field Programmable Gate Array, a digital logic chip that can be programmed to reconfigure the internal hardware. An FPGA does not run software – it physically changes the configuration of its gate arrays to adapt to the task at hand, making an FPGA an incredibly versatile tool. Need 25 PWM pins for a project? No problem. Want to replicate the functionality of a vintage CPU? Your FPGA has you covered. Not only is an FPGA versatile, but it is also better at handling timing-critical tasks than a microcontroller. You can filter high-speed sensor data before it's read by your processor, or offload repetitive tasks like debouncing buttons, reducing the burden on your microcontroller.

FPGAs are hot right now, but they're not a new technology – they've been used in industry for decades. However, pricey FPGA development boards, and the massive proprietary software suites needed to develop FPGA designs, means that there has historically been limited adoption in the maker community.

When you write an Arduino program, you're using a language called Wiring, a variation of C++. When you press compile, this high-level code is used to generate a binary file that the processor on the Arduino board executes to achieve the purpose of your program. Similarly, we describe the circuits we want in an FPGA using a high-level, text-based format known as a hardware description language (HDL), such as Verilog. The HDL design is then transformed by a synthesis tool into the basic building blocks that exist in the FPGA.

This process is normally done with proprietary software from the FPGA vendor, but these tools can take ages to download and devour disk space. That is, until Project IceStorm, led by Clifford Wolf, enabled a complete open-source workflow for the Lattice iCE40 FPGA.

FPGAs are hot right now but they're not a new technology – they've been used in industry for decades

This opened the door for low-cost, open hardware boards such as myStorm Blackice, TinyFPGA, iCEBreaker, and Fomu, which are great tools for teaching workshops and building projects.

The Lattice ECP5 FPGA is capable of more advanced features than the iCE40, and it now has an open-source workflow too, thanks to Project Trellis led by David Shah. This enabled the ECP5-powered Supercon badge to have cool features like HDMI video, while still being open for anyone to hack on without requiring proprietary tools.

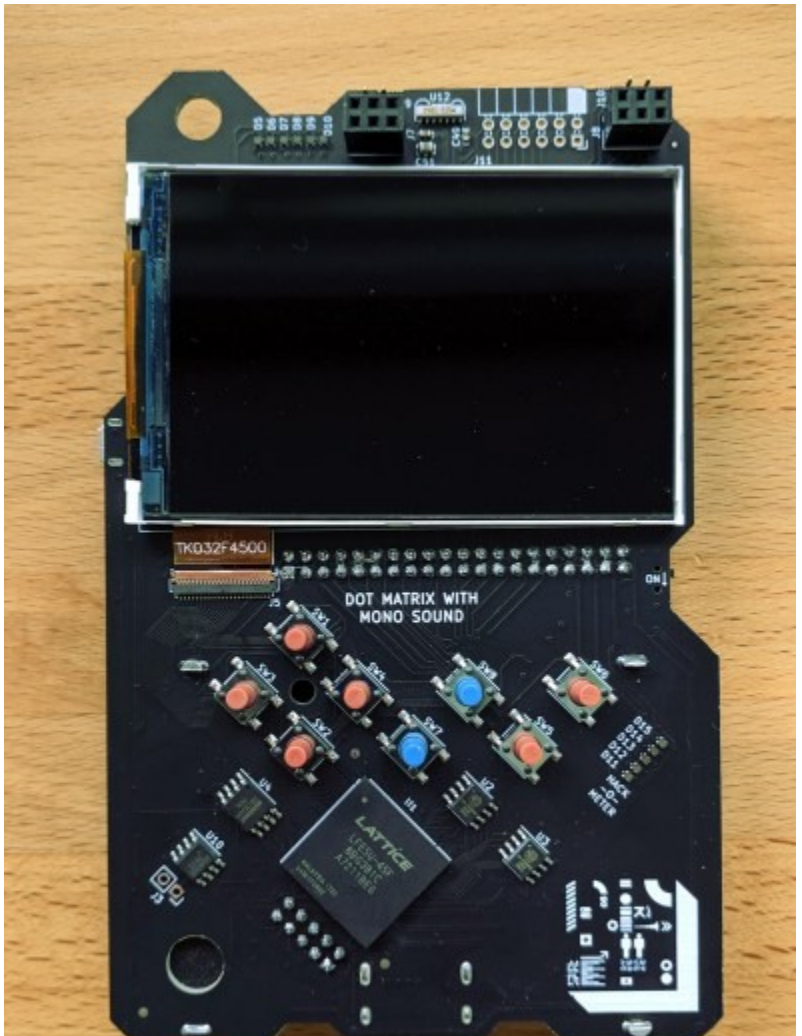
FPGAs are a fascinating technology with lots of awesome applications. If you want to find out more, start off by reading Luke Valenty's *The Hobbyists Guide to FPGAs* on **Hackaday.io** (**hsmag.ce/G0AQwR**), and watch Tim Ansell's Supercon talk to learn about the exciting future of open-source FPGA tools (**hsmag.cc/kyStPD**).

Slides: https://github.com/pdp7/talks/blob/master/rv-munich.pdf

Section:
Linux on the Hackaday Badge

Hackaday 2019 Supercon badge

- RISC-V “soft” core on ECP5 FPGA
- Gigantic FPGA In A Game Boy Form Factor



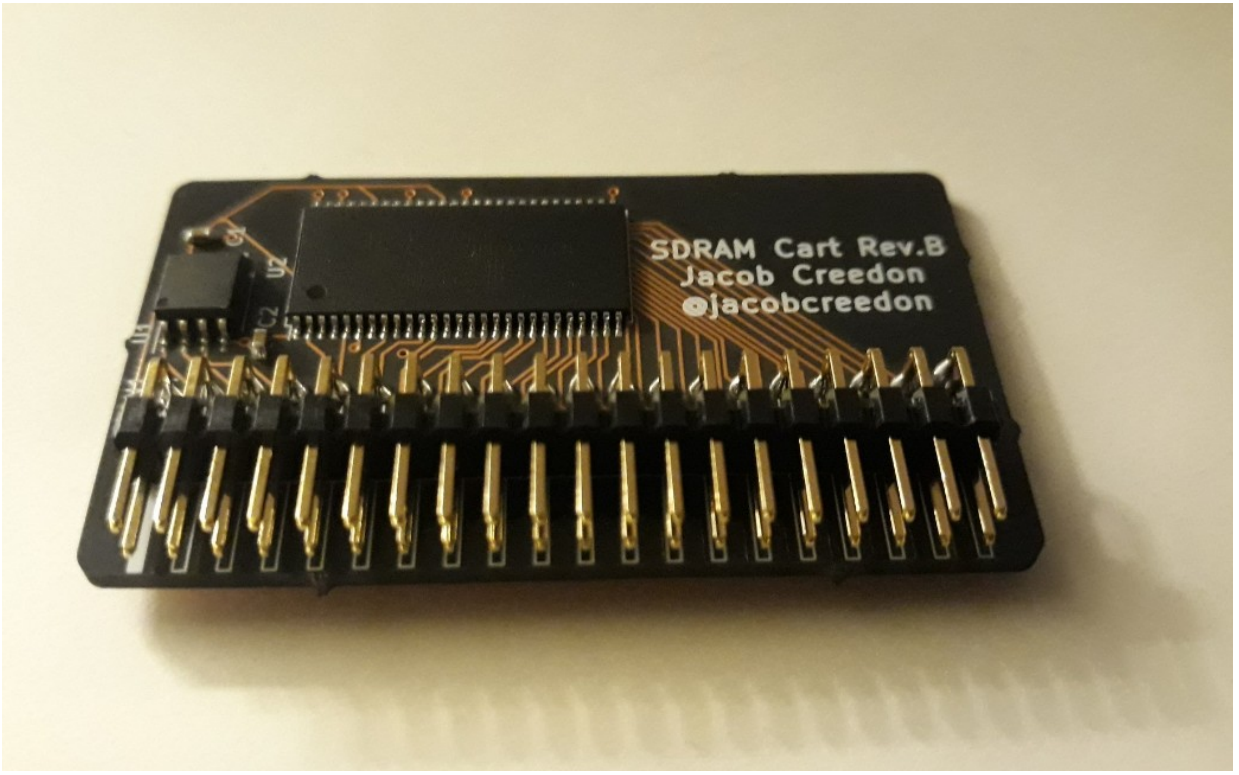
“Team Linux on Badge”

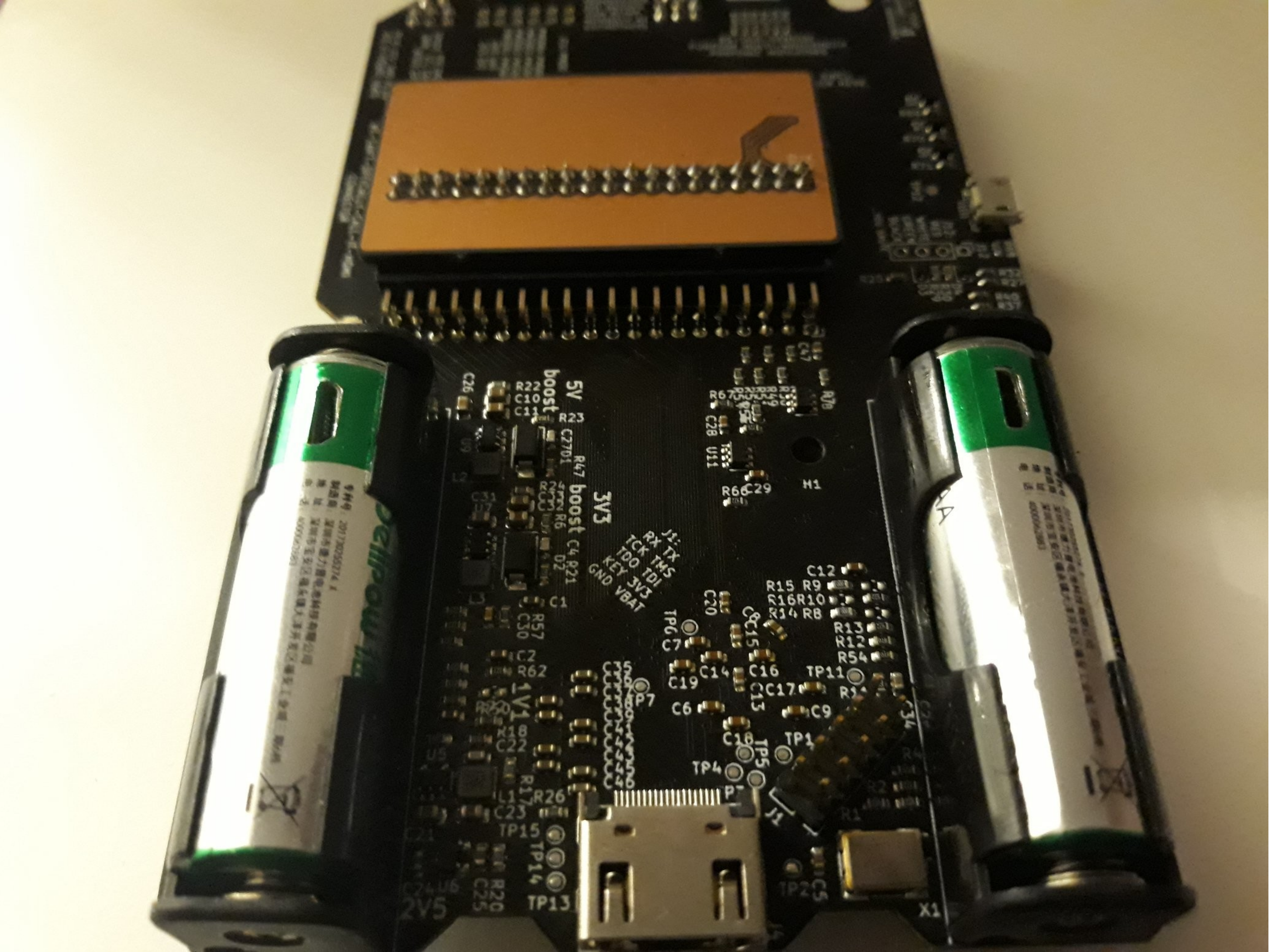
“Team Linux on Badge”

- Blog post: Hackaday Supercon badge boots Linux using SDRAM cartridge
  - https://blog.oshpark.com/2019/12/20/boot-linux-on-this-hackaday-supercon-badge-with-this-sdram-cartridge/
- Michael Welling (@QwertyEmedded), Tim Ansell (@mithro), Sean Cross (@xobs), Jacob Creedon (@jacobcreedon)
- First attempt: use the built-in 16MB SRAM… no luck :(
  - *(though xobs now might have a way to do it)*

“Team Linux on Badge”

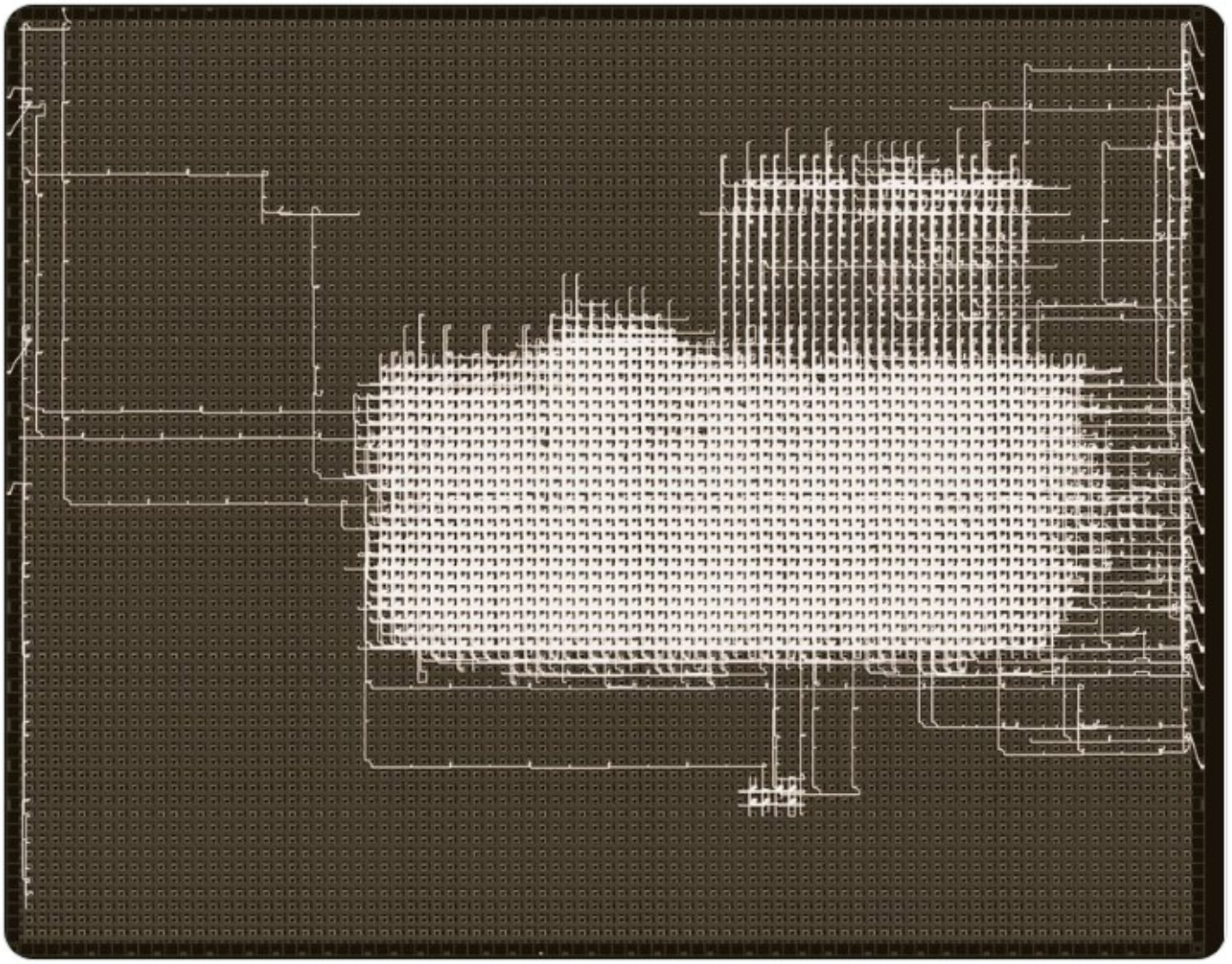
- Second attempt:
  - Jacob Creedon designed an a cartridge board that adds 32MB of SDRAM to the Hackaday Supercon badge… before the event!




5V
boost
3V3
boost
J1:
RX TX
TCK TMS
TDO TDI
KEY 3V3
GND VBAT
1V1
2V5
H1
X1
TP1
TP2
TP4
TP5
TP6
TP7
TP11
TP13
TP14
TP15
R22
C10
C11
R23
C26
R47
R24
R6
C4
R21
D2
C1
C30
R57
C2
R62
R18
C22
R17
R26
L1
C23
C24
U6
C25
R20
U5
R67
C28
U11
R66
C29
C12
R15 R9
R16 R10
R14 R8
R13
R12
R54
C20
C7
C8
C15
C14
C16
C19
C13
C17
C6
C9
C18
C35
C5
R1
R2
J1

OSS FPGA & EDA tools
@ico_TC

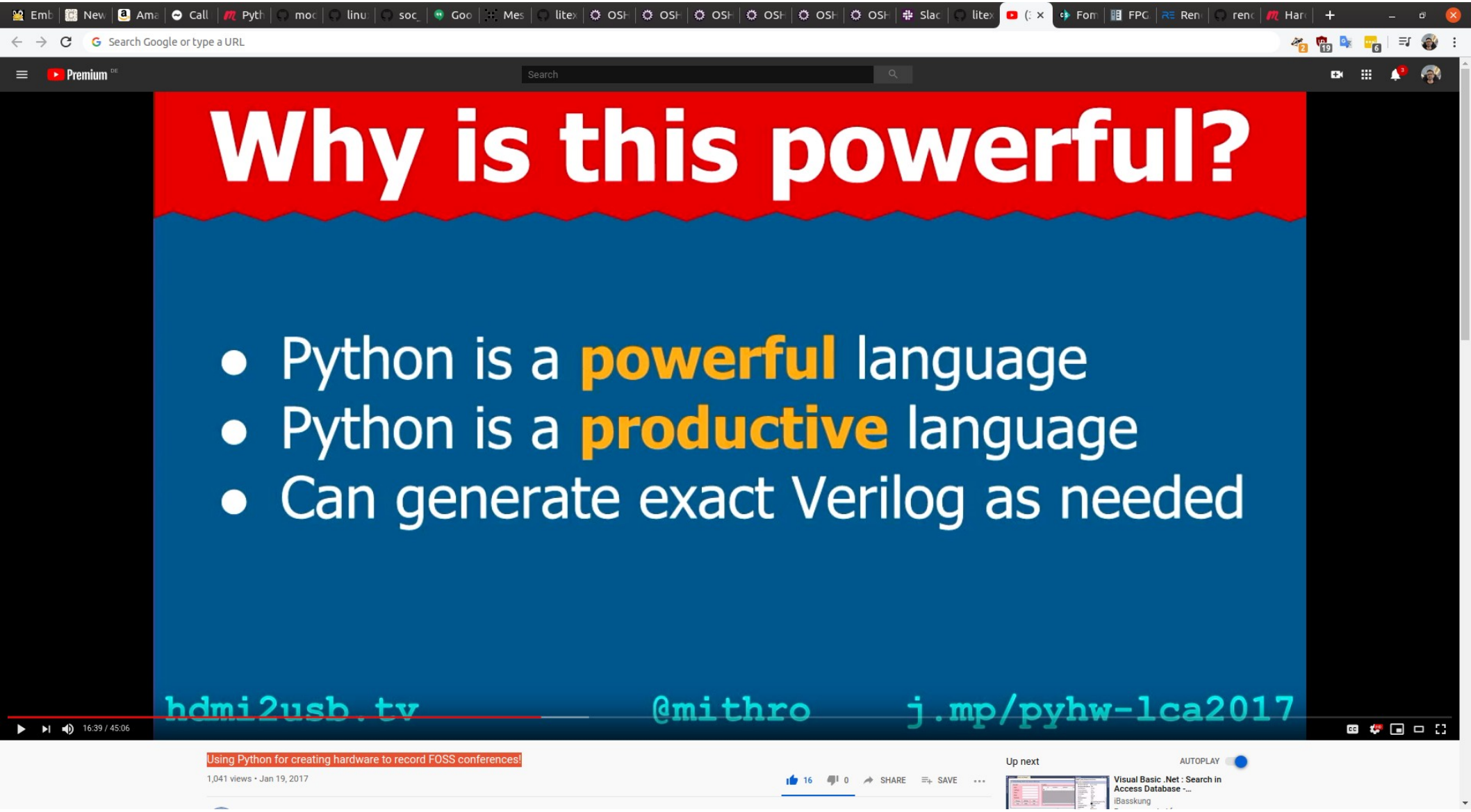
This is how a Linux capable core looks like on an FPGA.#nextpnratwork



12:42 AM · Dec 15, 2019 · Twitter for Android

Designing Hardware in Python?

- Yes!
- “Using Python for creating hardware to record FOSS conferences!”
- Tim “mithro” Ansell
- youtube.com/watch?v=MkVX_mh5dOU



Using Python for creating hardware to record FOSS conferences!

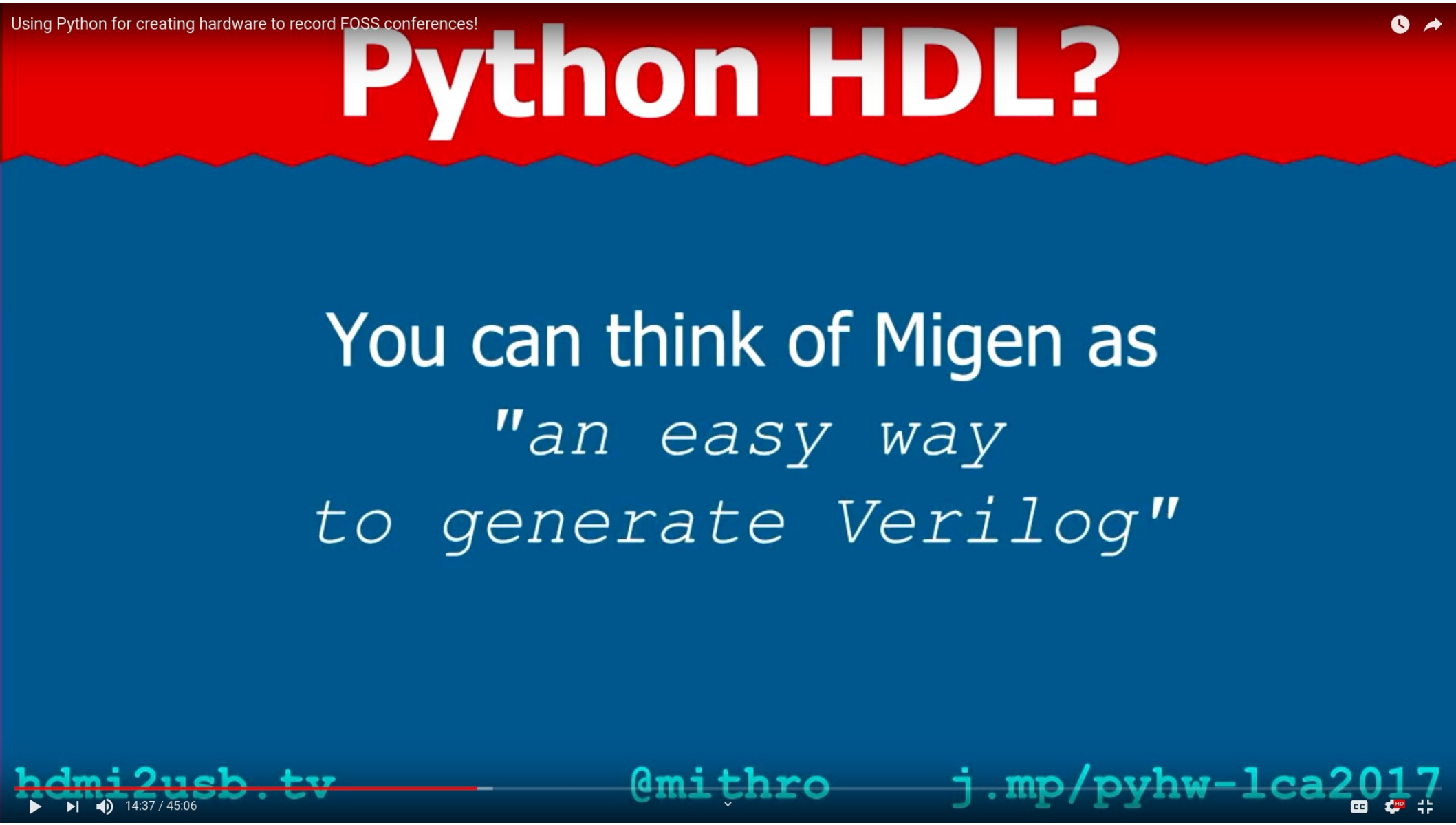
1,041 views • Jan 19, 2017

16 0 SHARE SAVE

Up next AUTOPLAY

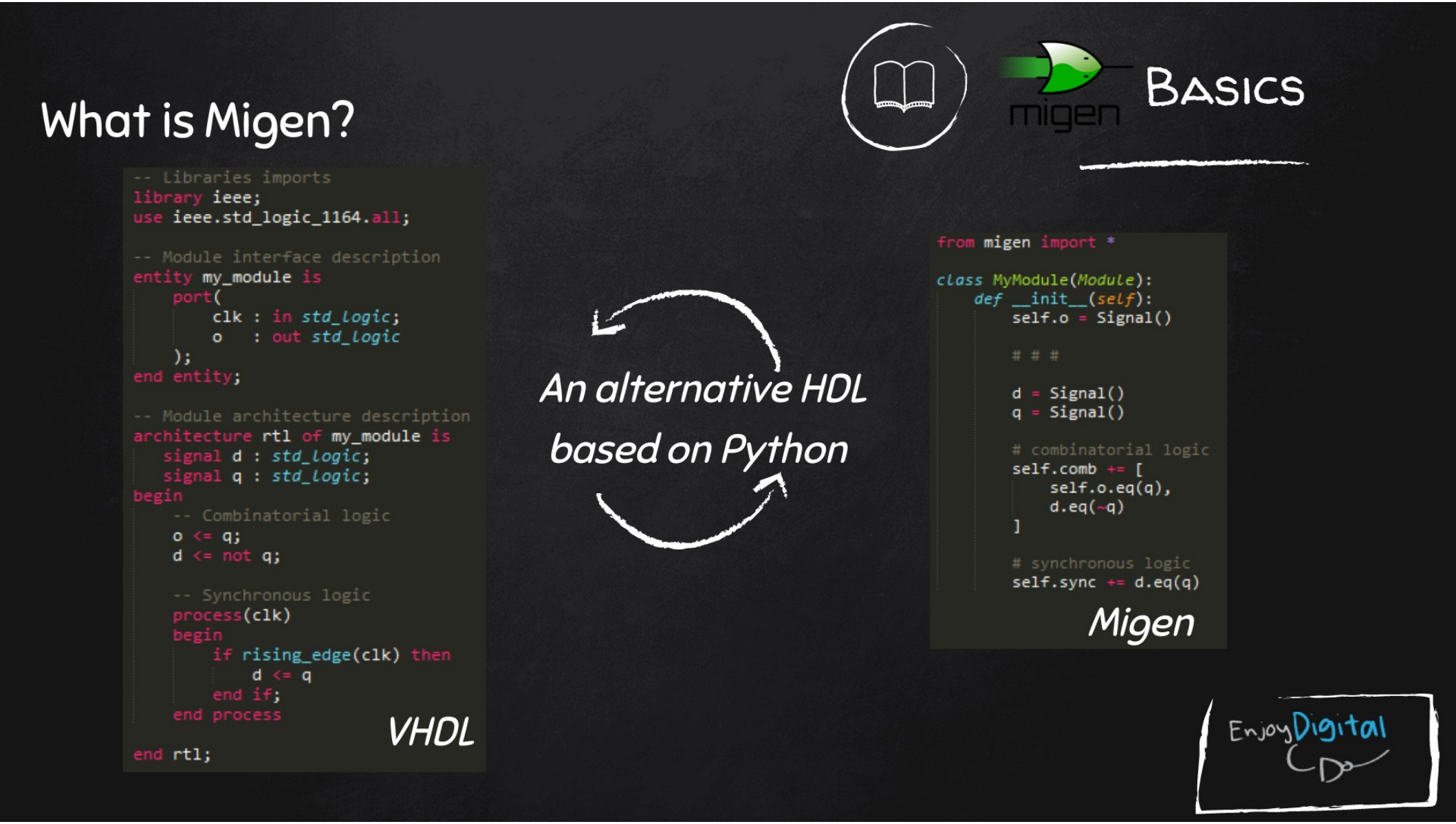
Visual Basic .Net : Search in Access Database -...

iBasskung


Using Python for creating hardware to record FOSS conferences!
Python HDL?
You can think of Migen as
"an easy way
to generate Verilog"
hdmi2usb.tv
@mithro
j.mp/pyhw-lca2017
14:37 / 45:06


Using Python for creating hardware to record FOSS conferences!
Blink Led - Migen
class Blinker(Module):
def __init__(self, led, cycles=15000000):
counter = Signal(max=cycles)
self.sync += counter.eq(counter - 1)
self.comb += led.eq(counter[-1])
Most significant bit
connected to LED signals
hdmi2usb.tv
@mithro
j.mp/pyhw-lca2017
15:52 / 45:06

Slides: https://github.com/litex-hub/fpga_101



Slides: https://github.com/litex-hub/fpga_101

FPGAs for custom System on Chip

- *SoC can be create with VHDL or Verilog or System Verilog. That's what is generally used in the industry but very verbose and error prone. (Not a problem if you have the money and the number of developers...).*
- *We already that Migen can be use to create digital designs. LiteX provides a higher level of abstraction.*

migen

+

LITEX

migen INSIDE

=

Build your hardware easily!

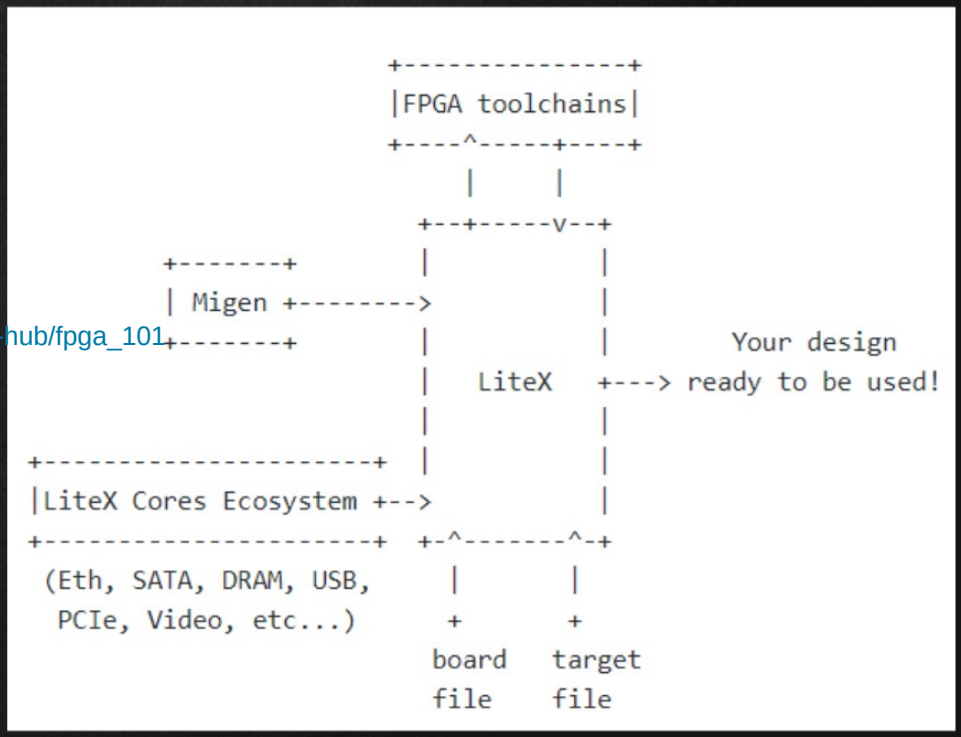
EnjoyDigital

- LiteX used to build cores, create SoCs and full FPGA designs.
- LiteX is based on Migen
- Migen lets you do FPGA design in Python!
- https://github.com/enjoy-digital/litex

Slides: https://github.com/litex-hub/fpga_101

FPGAs for custom System on Chip

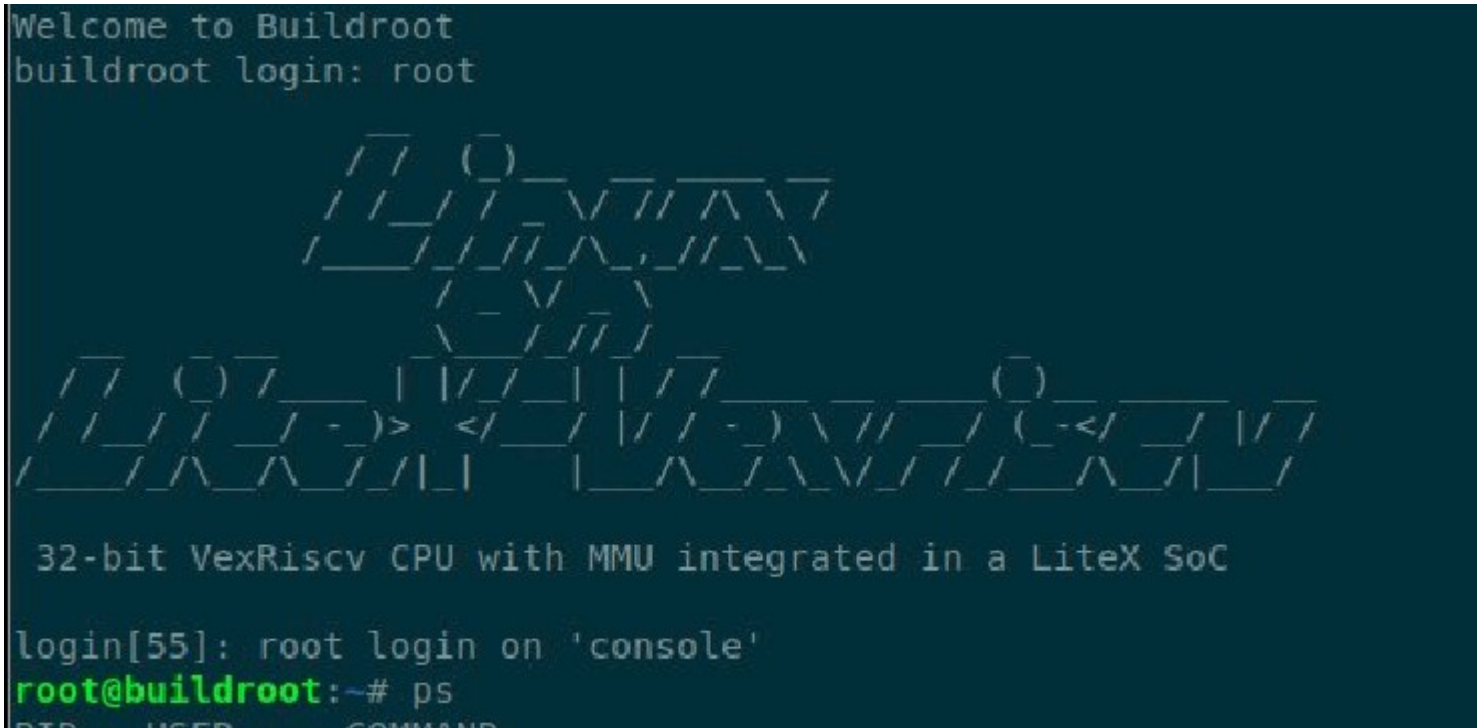
- *LiteX automates parts of the SoC design (buses, registers, software) and allow being more efficient.*
- *It provides most of the base elements required in a modern SoC (buses, streams, fifos, arbiters, muxes, etc...)*
- *It is compatible with all the LiteX core ecosystem (DRAM, Ethernet, PCIe, SATA, USB controllers...)*
- *Can be found at: github.com/enjoy-digital/litex*

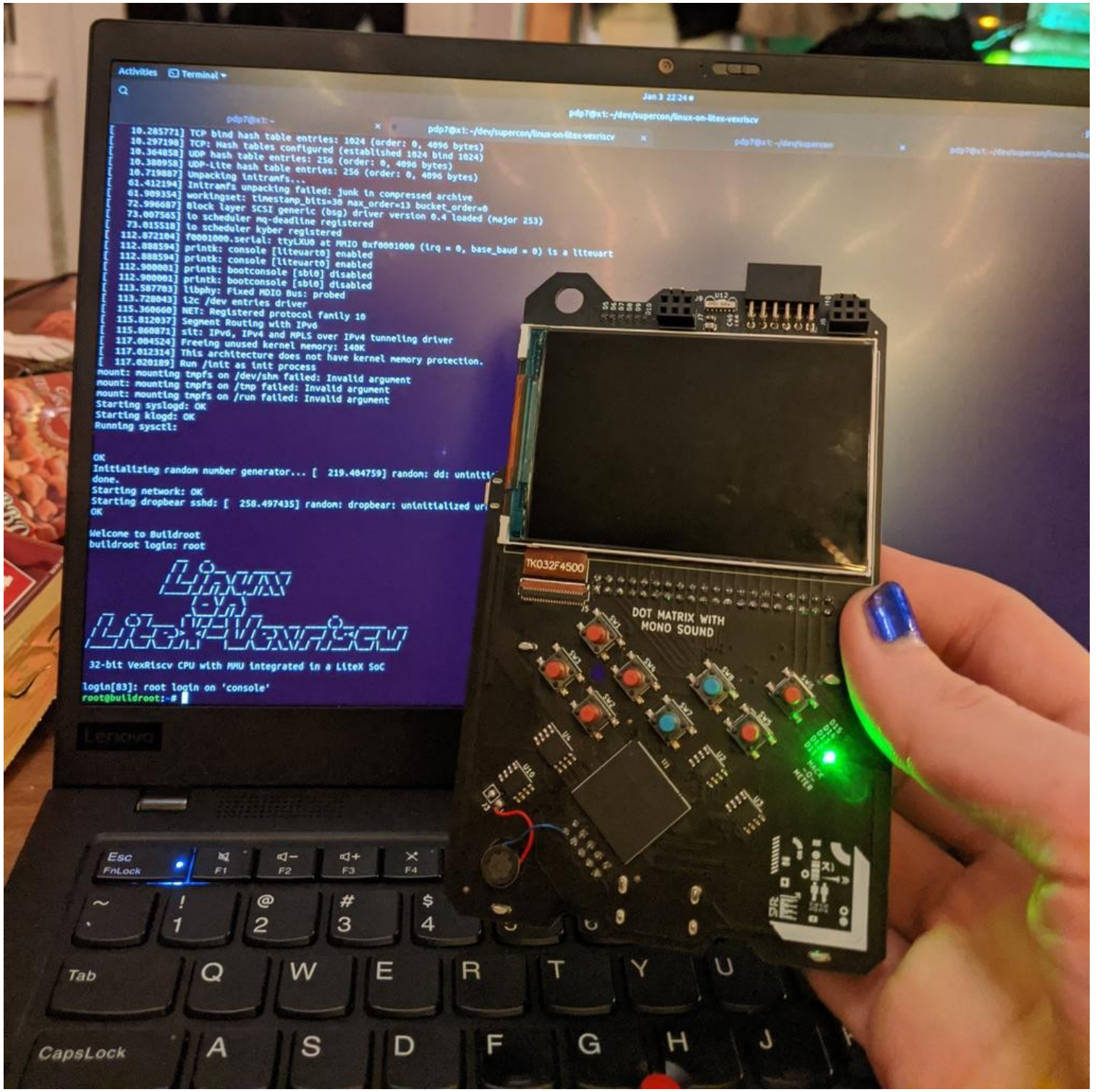


EnjoyDigital

Linux on LiteX-VexRiscv

- VexRiscv: 32-bit Linux Capable RISC-V CPU
- SoC built using VexRiscv core and LiteX moduels like LiteDRAM, LiteEth, LiteSDCard, ...
  - github.com/litex-hub/linux-on-litex-vexriscv




Activities
Terminal
Jan 3 22:24
pdp7@x1: ~/dev/supercon/linux-on-litex-vexriscv
[10.285771] TCP bind hash table entries: 1024 (order: 0, 4096 bytes)
[10.297198] TCP: Hash tables configured (established 1024 bind 1024)
[10.364858] UDP hash table entries: 256 (order: 0, 4096 bytes)
[10.380958] UDP-Lite hash table entries: 256 (order: 0, 4096 bytes)
[10.719887] Unpacking initramfs...
[61.412194] Initramfs unpacking failed: junk in compressed archive
[61.909354] workingset: timestamp_bits=30 max_order=13 bucket_order=0
[72.996687] Block layer SCSI generic (bsg) driver version 0.4 loaded (major 253)
[73.007565] io scheduler mq-deadline registered
[73.015518] io scheduler kyber registered
[112.872104] f0001000.serial: ttyLXU0 at MMIO 0xf0001000 (irq = 0, base_baud = 0) is a liteuart
[112.888594] printk: console [liteuart0] enabled
[112.888594] printk: console [liteuart0] enabled
[112.900001] printk: bootconsole [sbi0] disabled
[112.900001] printk: bootconsole [sbi0] disabled
[113.587703] libphy: Fixed MDIO Bus: probed
[113.728043] i2c /dev entries driver
[115.360660] NET: Registered protocol family 10
[115.812037] Segment Routing with IPv6
[115.860871] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[117.004524] Freeing unused kernel memory: 140K
[117.012314] This architecture does not have kernel memory protection.
[117.020189] Run /init as init process
mount: mounting tmpfs on /dev/shm failed: Invalid argument
mount: mounting tmpfs on /tmp failed: Invalid argument
mount: mounting tmpfs on /run failed: Invalid argument
Starting syslogd: OK
Starting klogd: OK
Running sysctl:
OK
Initializing random number generator... [219.404759] random: dd: uninitialized
done.
Starting network: OK
Starting dropbear sshd: [258.497435] random: dropbear: uninitialized
OK
Welcome to Buildroot
buildroot login: root
Linux on LiteX-VexRiscv
32-bit VexRiscv CPU with MMU integrated in a LiteX SoC
login[83]: root login on 'console'
root@buildroot:~#
TK032F4500
DOT MATRIX WITH
MONO SOUND
Lenovo
Esc
FnLock
F1
F2
F3
F4
Tab
CapsLock

- upstream support for Hackaday Supercon badge:
  - https://github.com/litex-hub/litex-boards/pull/31

litex-hub / **litex-boards**

Unwatch 7 | Unstar 17 | Fork 24

Code | Issues 2 | Pull requests 1 | Actions | Projects 0 | Wiki | Security | Insights

add the Hackaday Supercon ECP5 badge #31

Edit

Merged **enjoy-digital** merged 1 commit into `litex-hub:master` from `pdp7:master` 21 days ago

Conversation 18 | Commits 1 | Checks 1 | Files changed 2 | +461 −0

pdp7 commented 22 days ago • edited — Contributor

Add the Hackaday Supercon 2019 badge which has an ECP5 FPGA.

These changes are from a fork by Michael Welling (**@mwelling**)

During Supercon, we tried two approaches:

- use the built-in 16MB QSPI SRAM
- use add-on cartiridge with 32MB SDRAM by Jacob Creedon

We were not able to get the QSPI SRAM working so I've removed those changes, and I have just added the changes that are needed to boot Linux with the 32MB SDRAM.

In addition to **@mwelling**, thank you to Jacob Creedon (**@jcreedon**), **@gregdavill**, Tim Ansell (**@mithro**), and Sean Cross (**@xobs**) who all helped get Linux working on this badge.

Reviewers

No reviews

Assignees

No one assigned

Labels

None yet

Projects

None yet

Milestone

- upstream support for Hackaday Supercon badge:
  - https://github.com/litex-hub/litex-boards/pull/31

Merged **add the Hackaday Supercon ECP5 badge** #31

Changes from **all commits** ▾ **File filter...** ▾ **Jump to...** ▾ ⚙ ▾ Review changes ▾

215 litex_boards/partner/platforms/hadbadge.py

```
@@ -0,0 +1,215 @@
+ from litex.build.generic_platform import *
+ from litex.build.lattice import LatticePlatform
+
+ # IOs ----------------------------------------------------------------------------------------------
+
+ _io = [
+     ("clk8", 0, Pins("U18"), IOStandard("LVCMOS33")),
+     ("programn", 0, Pins("R1"), IOStandard("LVCMOS33")),
+     ("serial", 0,
+         Subsignal("rx", Pins("U2"), IOStandard("LVCMOS33"), Misc("PULLMODE=UP")),
+         Subsignal("tx", Pins("U1"), IOStandard("LVCMOS33")),
+     ),
+     ("led", 0, Pins("E3 D3 C3 C4 C2 B1 B20 B19 A18 K20 K19"), IOStandard("LVCMOS33")),  # Anodes
+     ("led", 1, Pins("P19 L18 K18"), IOStandard("LVCMOS33")), # Cathodes via FET
+     ("usb", 0,
+         Subsignal("d_p", Pins("F3")),
+         Subsignal("d_n", Pins("G3")),
+         Subsignal("pullup", Pins("E4")),
+         Subsignal("vbusdet", Pins("F4")),
+         IOStandard("LVCMOS33")
+     ),
+     ("keypad", 0,
+         Subsignal("left", Pins("G2"), Misc("PULLMODE=UP")),
```

- upstream support for Hackaday Supercon badge:
  - https://github.com/litex-hub/litex-boards/pull/31

Merged **add the Hackaday Supercon ECP5 badge** #31
Changes from **all commits** ▾ **File filter...** ▾ **Jump to...** ▾ ⚙ ▾ **Review changes** ▾

246 litex_boards/partner/targets/hadbadge.py Viewed

```
@@ -0,0 +1,246 @@
+ #!/usr/bin/env python3
+
+ # This file is Copyright (c) 2018-2019 Florent Kermarrec <florent@enjoy-digital.fr>
+ # This file is Copyright (c) 2018 David Shah <dave@ds0.me>
+ # License: BSD
+
+ import argparse
+ import sys
+
+ from migen import *
+ from migen.genlib.resetsync import AsyncResetSynchronizer
+
+ from litex_boards.platforms import hadbadge
+
+ from litex.soc.cores.clock import *
+ from litex.soc.integration.soc_sdram import *
+ #from litex.soc.integration.soc_core import *
+ from litex.soc.integration.builder import *
+
+ #from .spi_ram_dual import SpiRamDualQuad
+
+ from litedram import modules as litedram_modules
+ from litedram.phy import GENSDRPHY
```

Merged **add the Hackaday Supercon ECP5 badge** #68

Changes from **all commits** ▾ **File filter...** ▾ **Jump to...** ▾ ⚙ ▾

▾ 13 make.py

```
@@ -160,6 +160,16 @@ def __init__(self):
160 160         def load(self):
161 161             os.system("ujprog build/ulx3s/gateware/top.svf")
162 162
163     ++ # HADBadge support ---------------------------------------------------------------------
164     + 
165     + class HADBadge(Board):
166     +     def __init__(self):
167     +         from litex_boards.targets import hadbadge
168     +         Board.__init__(self, hadbadge.BaseSoC, {"serial"})
169     + 
170     +     def load(self):
171     +         os.system("dfu-util --alt 2 --download build/hadbadge/gateware/top.bit --reset")
172     + 
163 173   # OrangeCrab support --------------------------------------------------------------------
164 174
165 175   class OrangeCrab(Board):
@@ -209,6 +219,7 @@ def load(self):
209 219         # Lattice
```

add 32MB SDRAM for hadbadge #97

Merged **enjoy-digital** merged 1 commit into `enjoy-digital:master` from `pdp7:master` 21 days ago

Conversation 2 | Commits 1 | Checks 0 | Files changed 1

pdp7 commented 22 days ago — Contributor

Add AS4C32M8SA-7TCN 32MB SDRAM used on cartridge PCB by Jacob Creedon (**@jcreedon**) for the Hackaday Supercon 2019 badge which has an ECP5 FPGA.

These changes are from a fork by Michael Welling (**@mwelling**)

In addition to **@mwelling**, thank you to Jacob Creedon (**@jcreedon**), **@gregdavill**, Tim Ansell (**@mithro**), and Sean Cross (**@xobs**) who all helped get Linux working on this badge.

KiCad design files by **@jcreedon** for the SDRAM cartridge are available on GitHub.

There is also a shared project to order the SDRAM cartridge PCB.

Refer to my blog post for more information

Merged

add 32MB SDRAM for hadbadge #97

Changes from **all commits** ▾ **File filter...** ▾ **Jump to...** ▾ ⚙ ▾

9 litedram/modules.py

```
@@ -190,6 +190,15 @@ class AS4C32M16(SDRAMModule):
190 190         technology_timings = _TechnologyTimings(tREFI=64e6/8192, tWTR=(2, None), tCCD=(1,
191 191         speedgrade_timings = {"default": _SpeedgradeTimings(tRP=18, tRCD=18, tWR=12, tRFC=
192 192
    193 + class AS4C32M8(SDRAMModule):
    194 +     memtype = "SDR"
    195 +     # geometry
    196 +     nbanks = 4
    197 +     nrows  = 8192
    198 +     ncols  = 1024
    199 +     # timings
    200 +     technology_timings = _TechnologyTimings(tREFI=64e6/8192, tWTR=(2, None), tCCD=(1,
    201 +     speedgrade_timings = {"default": _SpeedgradeTimings(tRP=20, tRCD=20, tWR=15, tRFC=
193 202
194 203   # DDR ----------------------------------------------------------------------------
195 204
```

ProTip! Use [n] and [p] to navigate between commits in a pull request.

optimize performance on Hackaday Badge #35

Edit | New issue

Open **pdp7** opened this issue 17 days ago · 7 comments

pdp7 commented 17 days ago — Contributor

Related to comments in PR #31 (comment)

The performance of the ECP5 Hackaday Badge with 32MB SDRAM is "painfully" slow.

@mithro suggested there could be some issue with the configuration.

@enjoy-digital has attempted some optimizations:
#31 (comment)

> With enjoy-digital/litedram@ `34e6c24` and enjoy-digital/litex@ `fa22d6a` we have a ~10% boot time speedup on designs using SDRAM:
>
> - De0Nano: 94.6.s to 84.6s
> - ULX3S: 75.9s to 68.2s
>
> On Arty with DDR3 the gain is effect more limited: 8.7s to 8.4s. That would be interesting to test this on the badge.

I will measure if the boot time improve

Assignees

No one assigned

Labels

None yet

Projects

None yet

Milestone

No milestone

Notifications Customize

Unsubscribe

You're receiving notifications because you're watching this repository.

Open

optimize performance on Hackaday Badge #35

pdp7 opened this issue 17 days ago · 7 comments

pdp7 commented 15 days ago • edited

Contributor Author

@enjoy-digital WOW! much faster! It gets to login in 28 seconds (previous version was 258 seconds).

Recording:
https://asciinema.org/a/Pcm3vd1BEdEKY9srYX6MsNfCE

Text:

```
pdp7@x1:~/dev/enjoy/linux-on-litex-vexriscv$ lxterm --images=images.json /dev
[LXTERM] Starting....
lBIOS CRC passed (561ab1e2)

 Migen git sha1: 063188e
 LiteX git sha1: --------

--========== SoC ==========--
CPU:       VexRiscv @ 48MHz
ROM:       32KB
SRAM:      4KB
```

enjoy-digital committed 15 days ago 1 parent 2317519 commit 39ce39a298f5

Showing **1 changed file** with **5 additions** and **3 deletions**.

8 litex/soc/integration/soc_sdram.py

```
@@ -26,12 +26,13 @@ class SoCSDRAM(SoCCore):
        }
        csr_map.update(SoCCore.csr_map)

-       def __init__(self, platform, clk_freq, l2_size=8192, **kwargs):
+       def __init__(self, platform, clk_freq, l2_size=8192, l2_data_width=128, **kwargs):
            SoCCore.__init__(self, platform, clk_freq, **kwargs)
            if not self.integrated_main_ram_size:
                if self.cpu_type is not None and self.csr_data_width > 32:
                    raise NotImplementedError("BIOS supports SDRAM initialization only for c
-           self.l2_size = l2_size
+           self.l2_size       = l2_size
+           self.l2_data_width = l2_data_width

            self._sdram_phy    = []
            self._wb_sdram_ifs = []
```

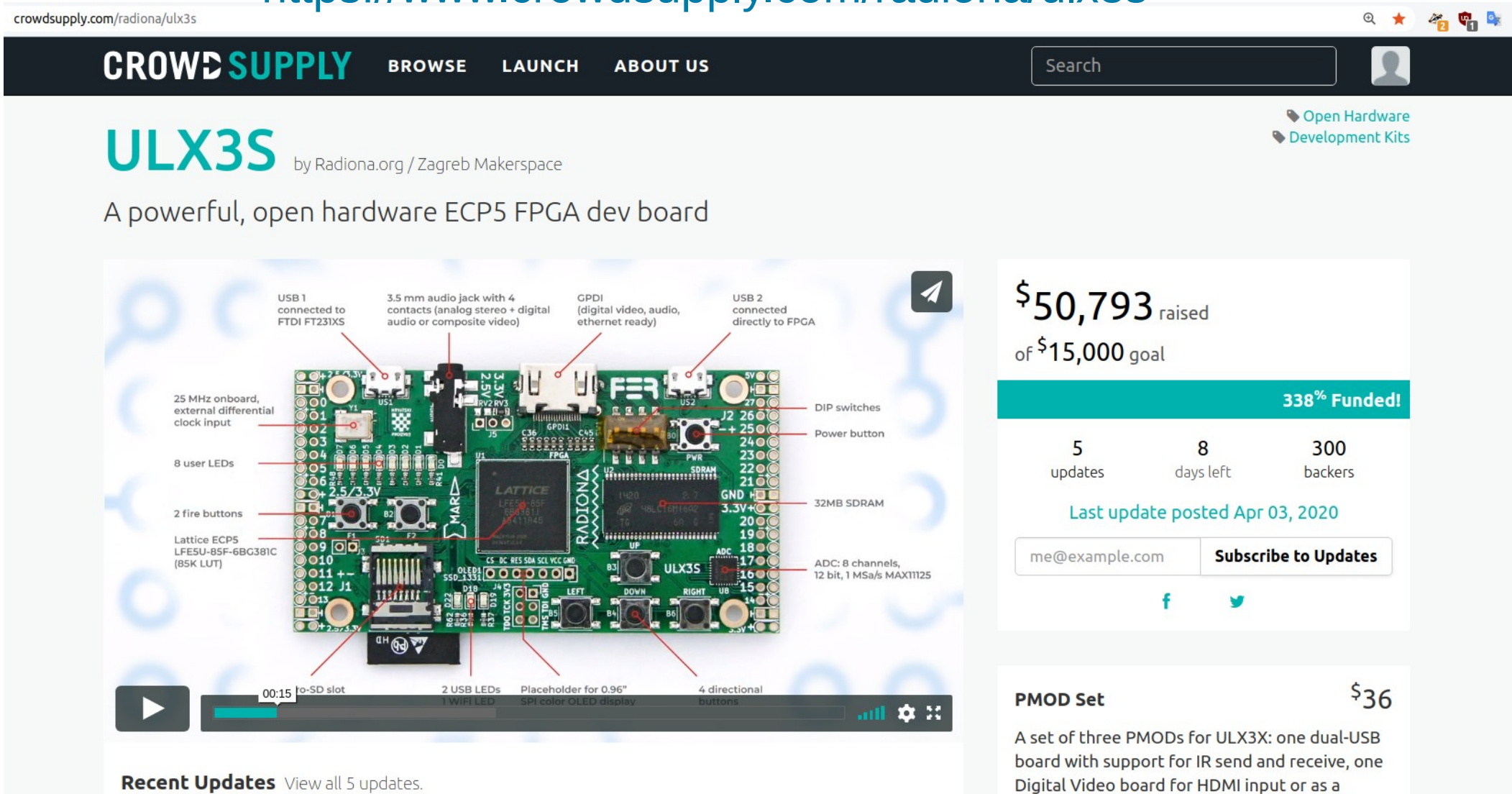
- Greg Davill got the screen working with LiteVideo!
  - twitter.com/GregDavill/status/1231082623633543168

Slides: https://github.com/pdp7/talks/blob/master/rv-munich.pdf

Open Source boards with ECP5 FPGA *(can run Linux)*

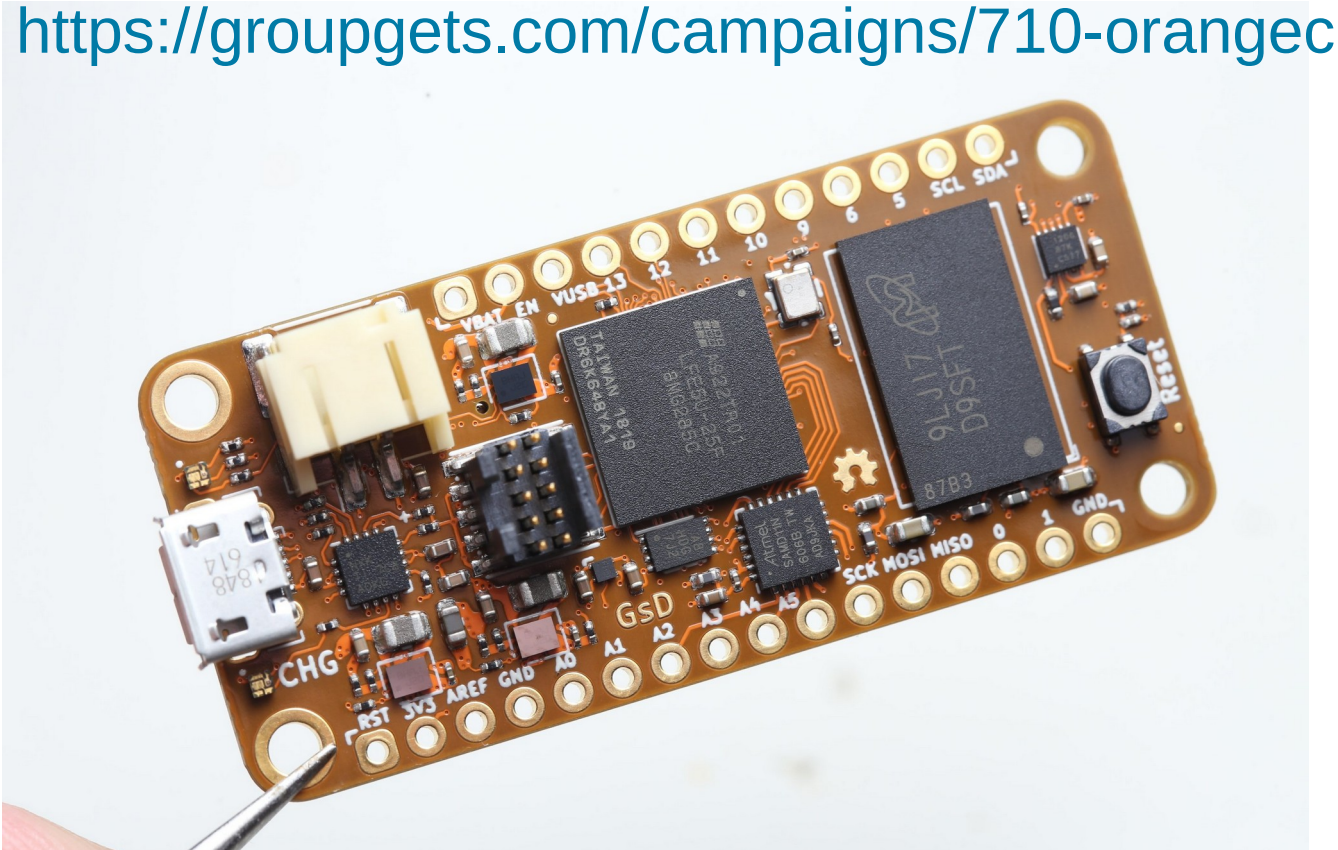
Open Source ECP5 boards

- Radiona.org ULX3S
  - https://www.crowdsupply.com/radiona/ulx3s



Open Source ECP5 boards

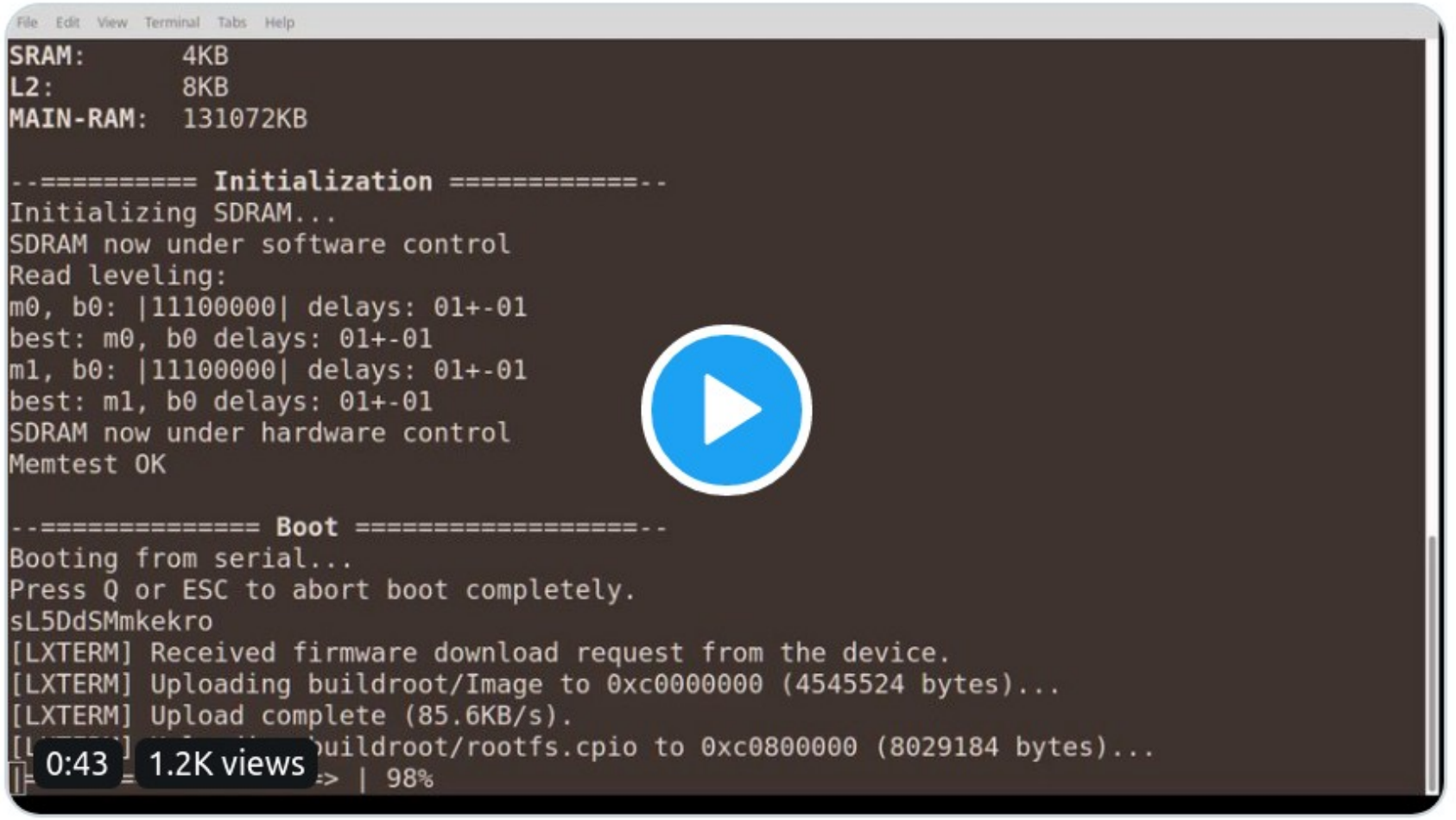
- Lattice ECP5 FPGA in Adafruit Feather form factor and 128MB DDR RAM:
  - Orange Crab by Greg Davill
    - https://github.com/gregdavill/OrangeCrab
    - https://groupgets.com/campaigns/710-orangecrab



Greg @ #36c3
@GregDavill

Replying to @mithro @pdp7 and 2 others

Done. 😃



4:55 PM · Dec 28, 2019 · Twitter Web App

Open Source ECP5 boards

- Orange Crab by Greg Davill
  - https://groupgets.com/campaigns/710-orangecrab

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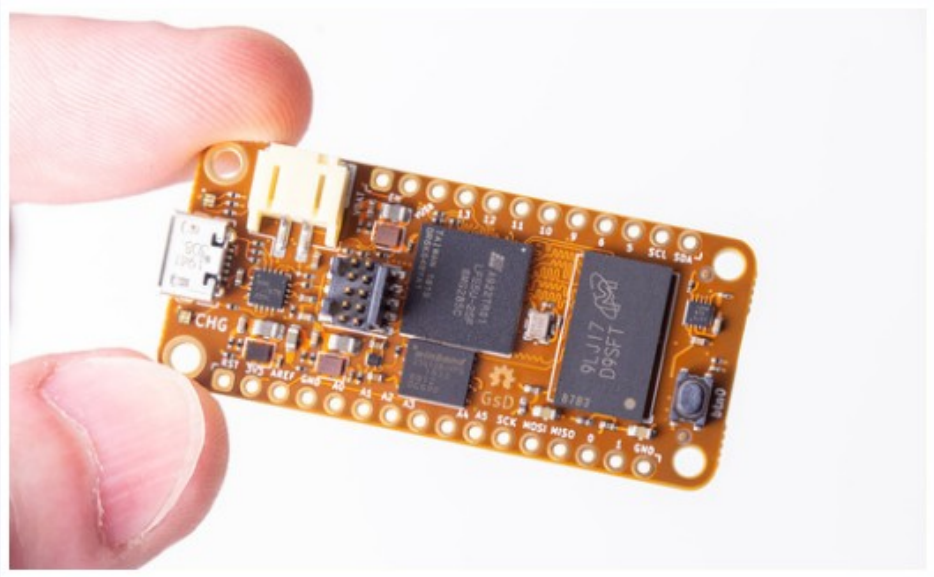

OrangeCrab

Single-unit price: **$99.00** + shipping

Campaign scheduled end date: Mon, 13 Apr 2020 16:19:00 PDT

Backers: 174

Target: 200

Funded: 286

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Want to learn FPGAs? Try Fomu!

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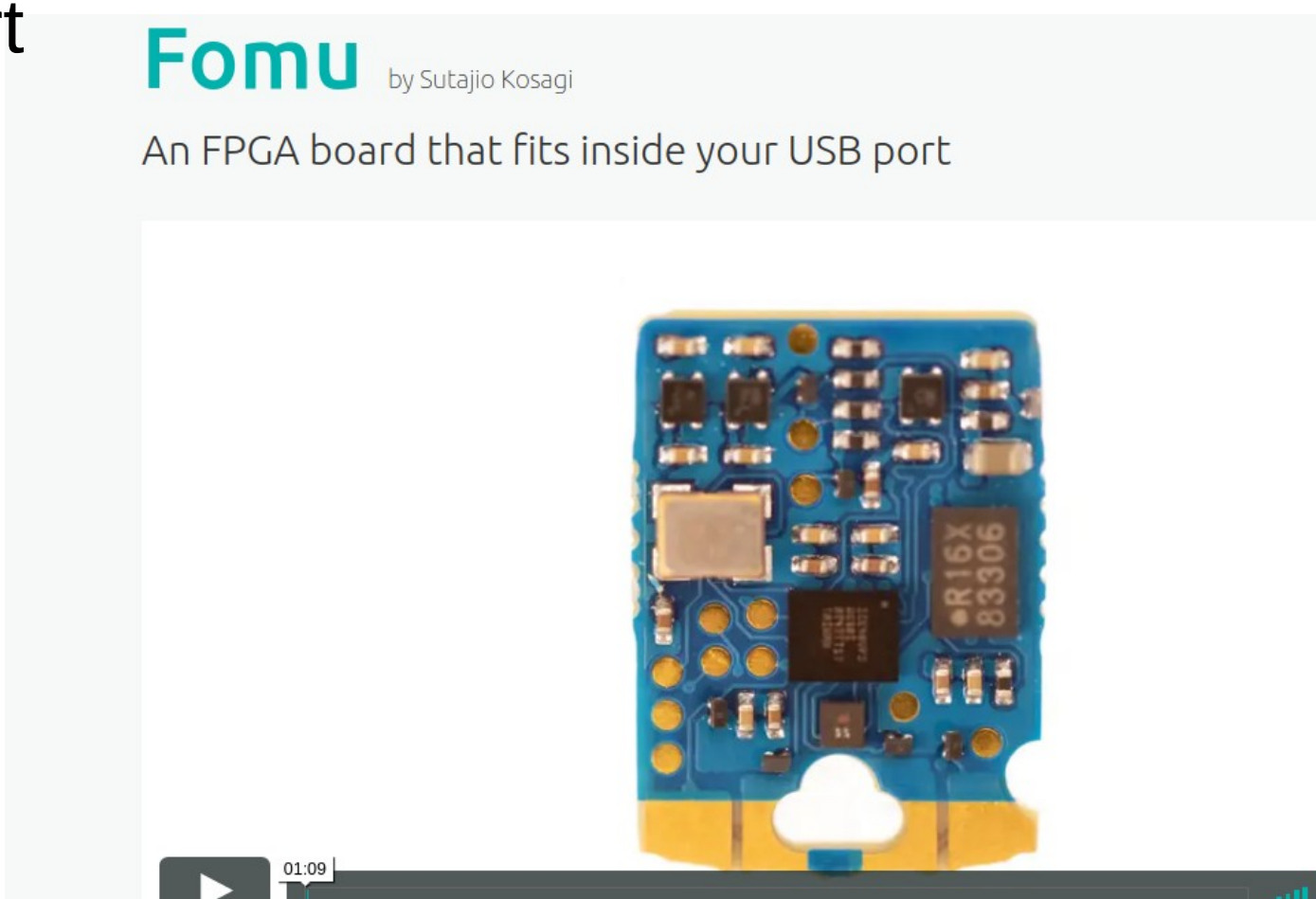
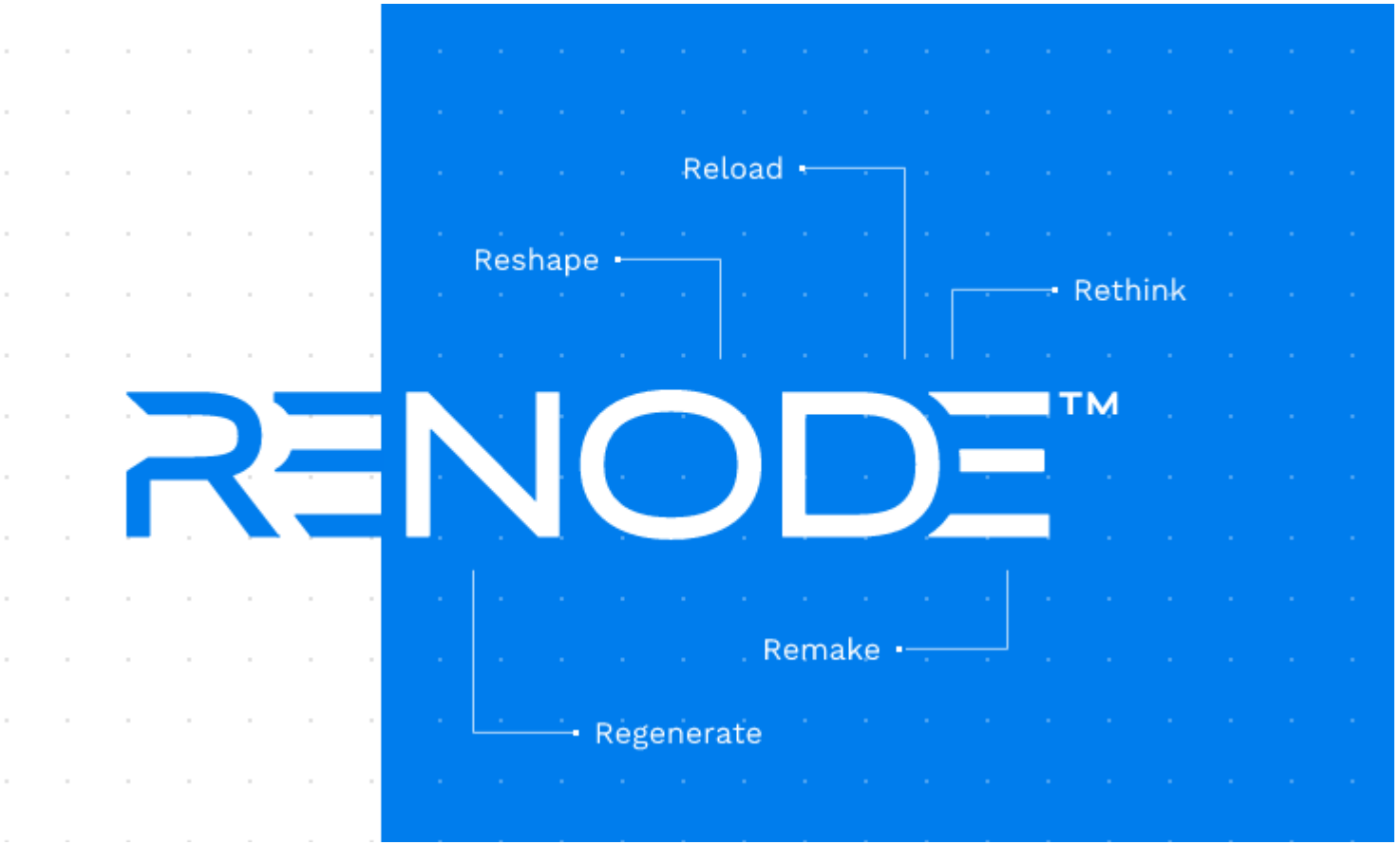
- Fits in USB port
- RGB LED
- Learn:
  - MicroPython
  - Verilog
  - LiteX



No hardware? Try Renode!

- https://renode.io/



No hardware? Try Renode!

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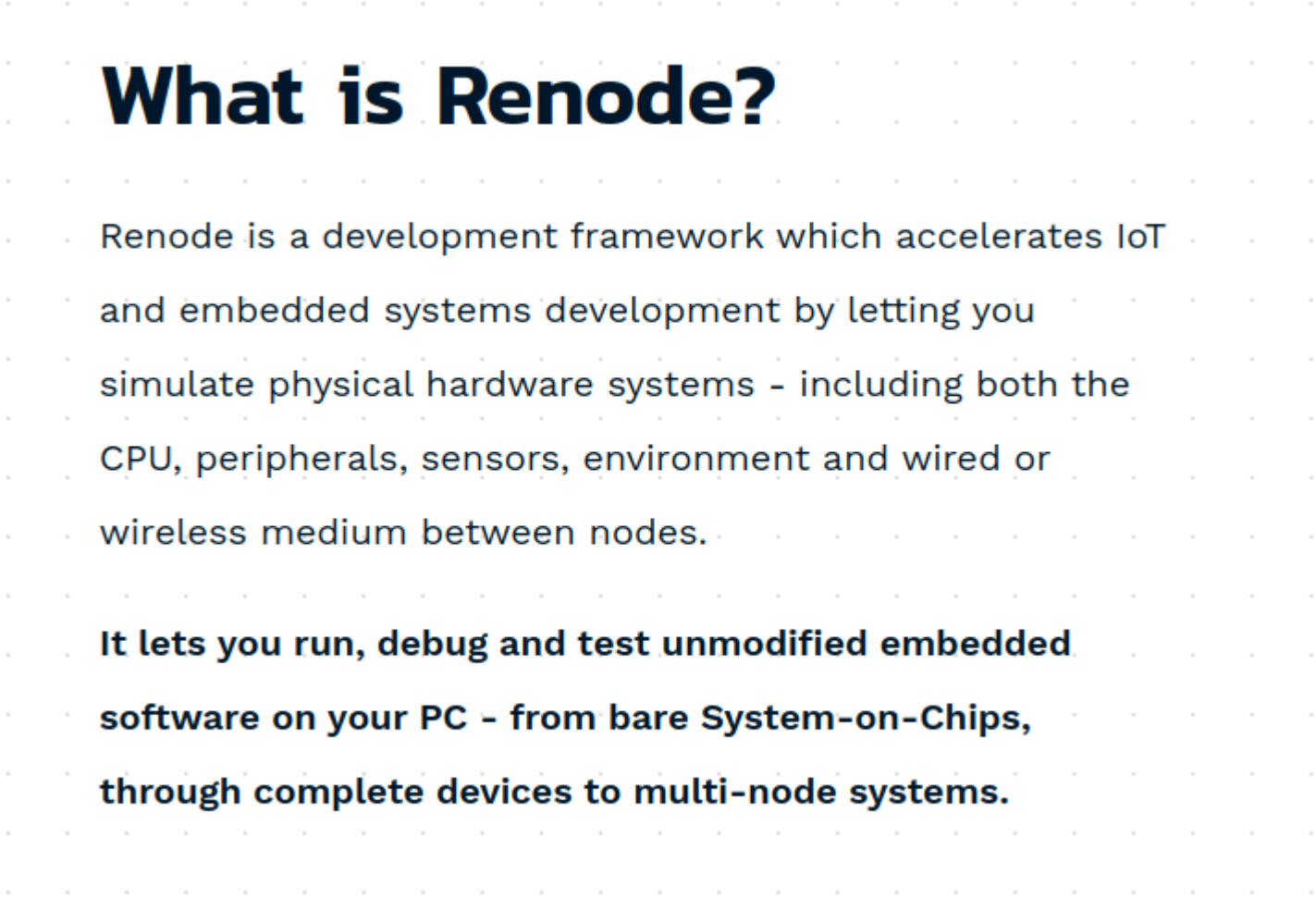


SiFive HiFive1

single-node/sifive_fe310.resc

SiFive HiFive Unleashed

single-node/hifive_unleashed.resc

Microchip PolarFire SoC Hardware Development Platform

single-node/polarfire-soc.resc

Toradex Colibri T30

single-node/tegra3.resc

OpenISA VEGAboard

single-node/vegaboard_ri5cy.resc

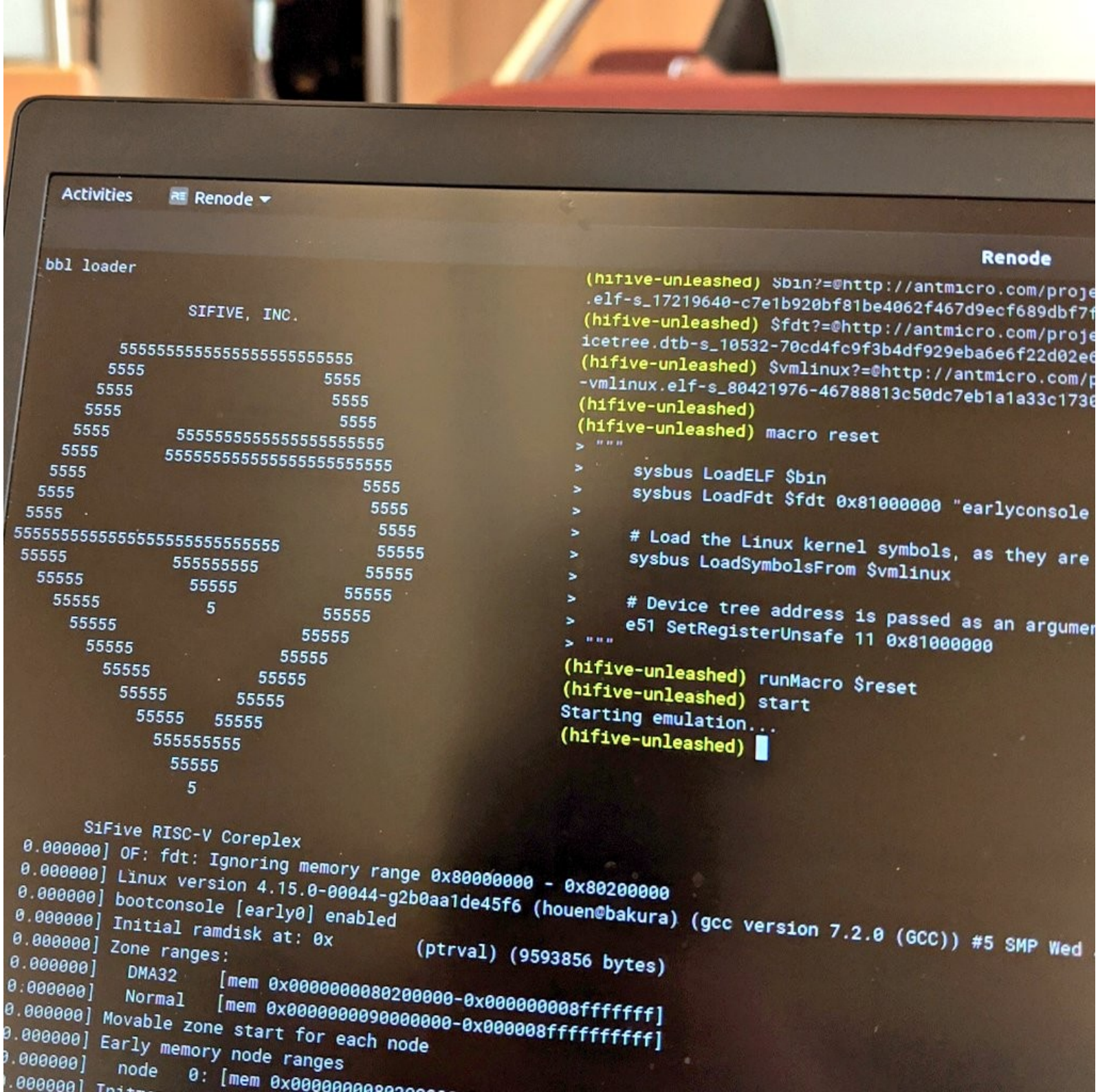
Intel Quark SE Microcontroller Evaluation Kit C1000

single-node/quark_c1000.resc

Fomu

LiteX/VexRiscv on Digilent Arty

Xilinx ZedBoard


Activities
Renode
Renode
bbl loader
SIFIVE, INC.
(hifive-unleashed) $bin?=@http://antmicro.com/proje
.elf-s_17219640-c7e1b920bf81be4062f467d9ecf689dbf7f
(hifive-unleashed) $fdt?=@http://antmicro.com/proje
icetree.dtb-s_10532-70cd4fc9f3b4df929eba6e6f22d02e6
(hifive-unleashed) $vmlinux?=@http://antmicro.com/p
-vmlinux.elf-s_80421976-46788813c50dc7eb1a1a33c173
(hifive-unleashed)
(hifive-unleashed) macro reset
> """
> sysbus LoadELF $bin
> sysbus LoadFdt $fdt 0x81000000 "earlyconsole
>
> # Load the Linux kernel symbols, as they are
> sysbus LoadSymbolsFrom $vmlinux
>
> # Device tree address is passed as an argumen
> e51 SetRegisterUnsafe 11 0x81000000
> """
(hifive-unleashed) runMacro $reset
(hifive-unleashed) start
Starting emulation...
(hifive-unleashed)
SiFive RISC-V Coreplex
0.000000] OF: fdt: Ignoring memory range 0x80000000 - 0x80200000
0.000000] Linux version 4.15.0-00044-g2b0aa1de45f6 (houen@bakura) (gcc version 7.2.0 (GCC)) #5 SMP Wed
0.000000] bootconsole [early0] enabled
0.000000] Initial ramdisk at: 0x (ptrval) (9593856 bytes)
0.000000] Zone ranges:
0.000000] DMA32 [mem 0x0000000080200000-0x00000000ffffffff]
0.000000] Normal [mem 0x0000000090000000-0x000008ffffffffff]
0.000000] Movable zone start for each node
0.000000] Early memory node ranges
0.000000] node 0: [mem 0x

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- Slides:

  github.com/pdp7/talks/blob/master/rv-pint.pdf
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