




File: tranZPUter-SW\_z80-700\_v1\_3.sch



File: tranZPUter-SW\_k64fx512-700\_v1\_3.sch

File: tranZPUter-SW\_VideoInterface-700\_v1\_3.sch



File: tranZPUter-SW\_CPLDFPGA\_Programming-700\_v1\_3.sch

File: tranZPUter-SW\_FPGA2-700\_v1\_3.sch

[illegible]

File: tranZPUter-SW\_PowerSupply-700\_v1\_3.sch



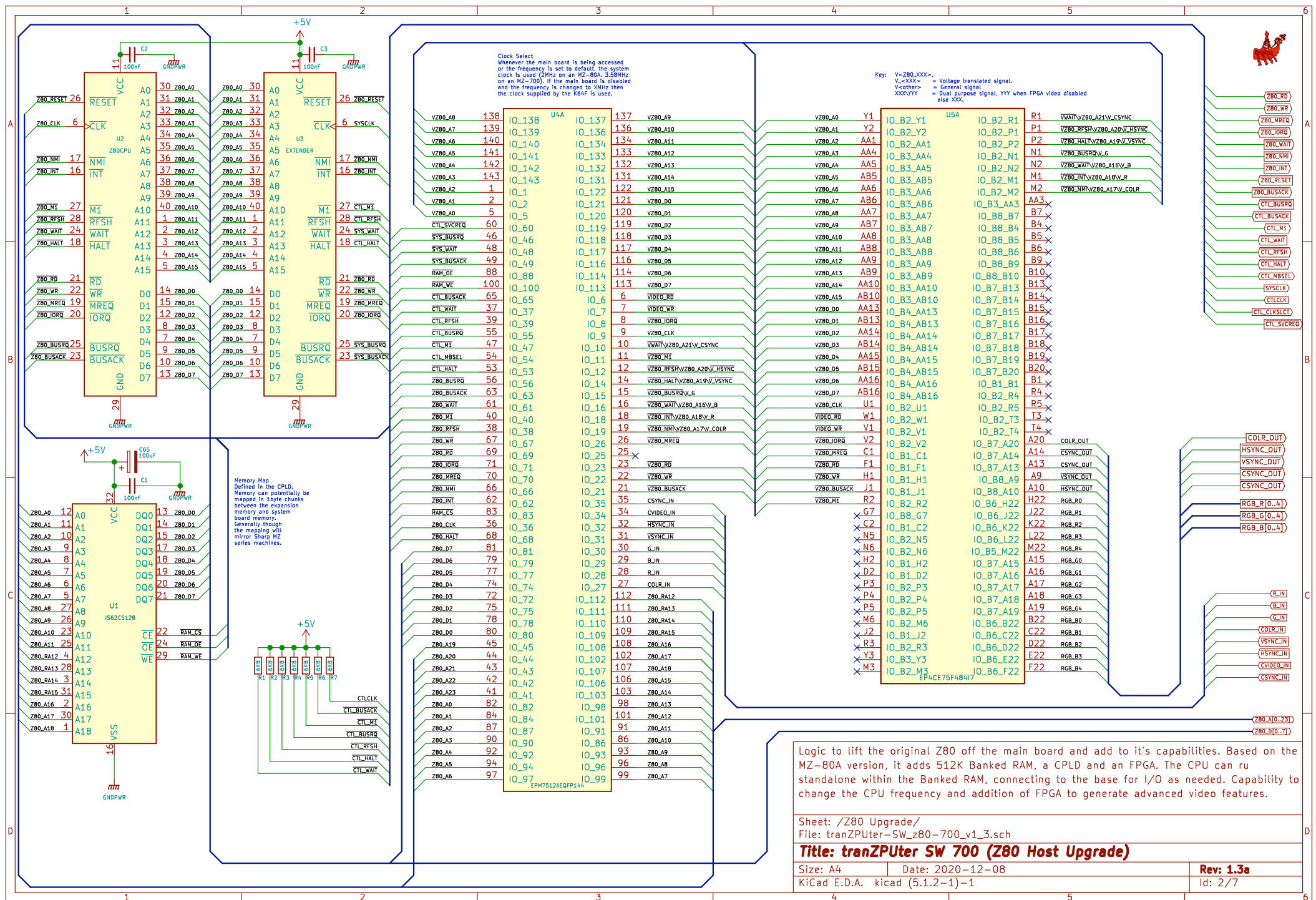
Capabilities upgrade for the Sharp MZ80A.  
Providing upgraded hardware and an optional MPU for provision of SD services to host,  
alternative soft processors, ZPUTA Menu System and additional resources to enhance  
the Sharp MZ80A.

Sheet: /  
File: tranZPUter-SW-700\_v1\_3.sch

**Title: tranZPUter SW 700**

Size: A4	Date: 2020-06-19	Rev: <b>1.3</b>
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 1/7

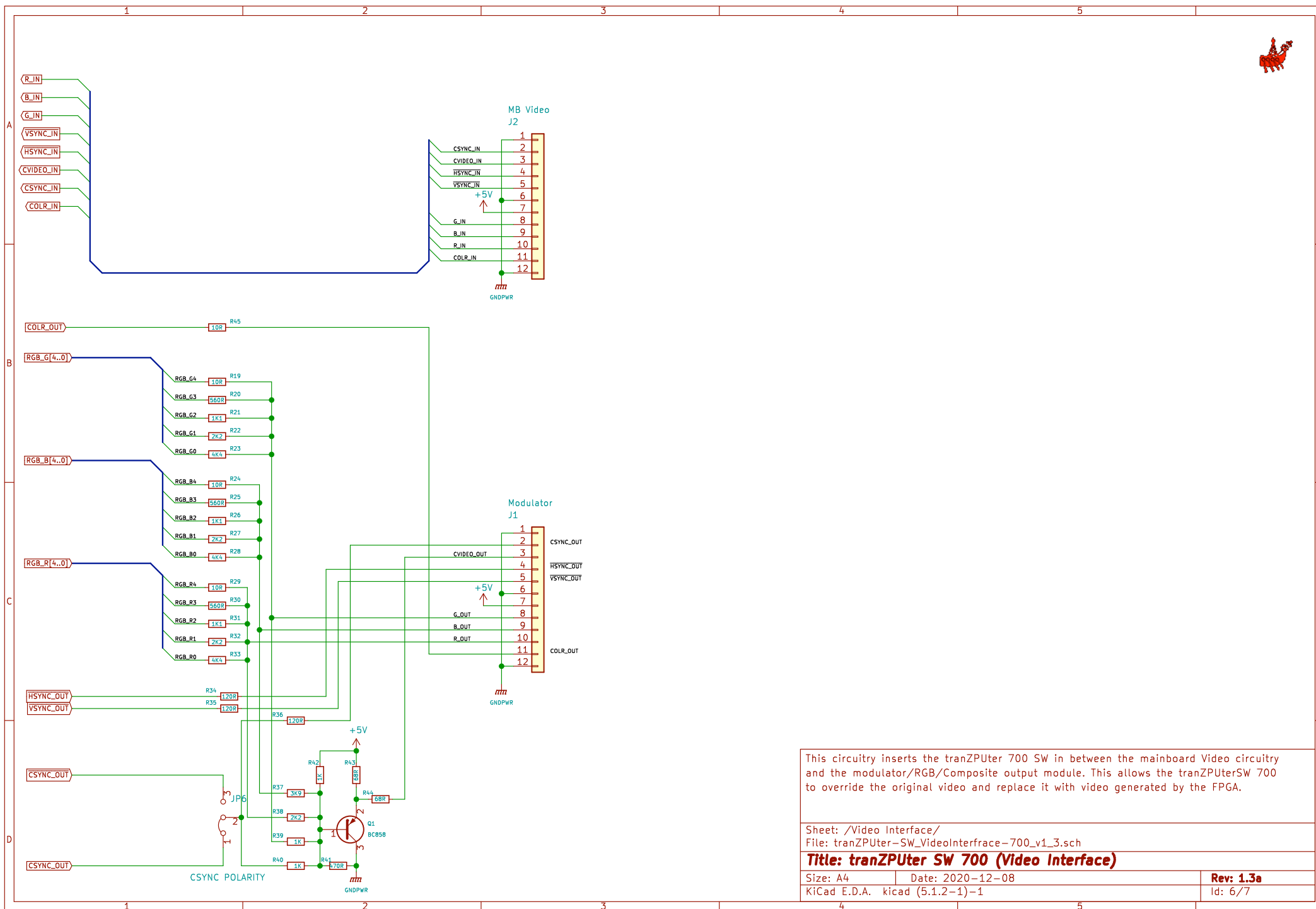
Rev: 1.3  
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This circuitry inserts the tranZPUter 700 SW in between the mainboard Video circuitry and the modulator/RGB/Composite output module. This allows the tranZPUterSW 700 to override the original video and replace it with video generated by the FPGA.		
Sheet: /Video Interface/ File: tranZPUter-SW_VideoInterface-700_v1_3.sch		
<b>Title: tranZPUter SW 700 (Video Interface)</b>		
Size: A4	Date: 2020-12-08	Rev: 1.3a
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 6/7



<del>X</del> Y7	IO_B3_Y7	U58	IO_B5_N21	<del>N21</del>
<del>X</del> Y8	IO_B3_Y8		IO_B8_A4	<del>A4</del>
<del>X</del> B2	IO_B1_B2		IO_B5_P20	<del>P20</del>
<del>X</del> L6	IO_B2_L6		IO_B5_P21	<del>P21</del>
<del>X</del> E3	IO_B1_E3		IO_B8_A5	<del>A5</del>
<del>X</del> AB4	IO_B3_AB4		IO_B5_R17	<del>R17</del>
<del>X</del> F2	IO_B1_F2		IO_B5_R18	<del>R18</del>
<del>X</del> G3	IO_B1_G3		IO_B5_R19	<del>R19</del>
<del>X</del> G4	IO_B1_G4		IO_B5_R20	<del>R20</del>
<del>X</del> G5	IO_B1_G5		IO_B5_R21	<del>R21</del>
<del>X</del> H3	IO_B1_H3		IO_B8_A6	<del>A6</del>
<del>X</del> H4	IO_B1_H4		IO_B5_T17	<del>T17</del>
<del>X</del> H5	IO_B1_H5		IO_B5_T18	<del>T18</del>
<del>X</del> H6	IO_B1_H6		IO_B5_T19	<del>T19</del>
<del>X</del> H7	IO_B1_H7		IO_B5_T20	<del>T20</del>
<del>X</del> AB3	IO_B3_AB3		IO_B5_U19	<del>U19</del>
<del>X</del> E1	IO_B1_E1		IO_B5_U20	<del>U20</del>
<del>X</del> W2	IO_B2_W2		IO_B5_U21	<del>U21</del>
<del>X</del> R14	IO_B4_R14		IO_B5_U22	<del>U22</del>
<del>X</del> R16	IO_B4_R16		IO_B5_V21	<del>V21</del>
<del>X</del> T15	IO_B4_T15		IO_B5_V22	<del>V22</del>
<del>X</del> T16	IO_B4_T16		IO_B5_W19	<del>W19</del>
<del>X</del> U12	IO_B4_U12		IO_B5_W20	<del>W20</del>
<del>X</del> U14	IO_B4_U14		IO_B5_W21	<del>W21</del>
<del>X</del> U15	IO_B4_U15		IO_B5_W22	<del>W22</del>
<del>X</del> U16	IO_B4_U16		IO_B5_Y21	<del>Y21</del>
<del>X</del> U17	IO_B4_U17		IO_B5_Y22	<del>Y22</del>
<del>X</del> V12	IO_B4_V12		IO_B6_B21	<del>B21</del>
<del>X</del> V13	IO_B4_V13		IO_B6_C20	<del>C20</del>
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<del>X</del> W13	IO_B4_W13		IO_B6_E21	<del>E21</del>
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<del>X</del> Y17	IO_B4_Y17		IO_B6_F20	<del>F20</del>
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<del>X</del> M16	IO_B5_M16		IO_B8_A8	<del>A8</del>
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<del>X</del> M20	IO_B5_M20		IO_B6_H17	<del>H17</del>
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<del>X</del> P22	IO_B5_P22		IO_B6_H19	<del>H19</del>
<del>X</del> N18	IO_B5_N18		IO_B6_H20	<del>H20</del>
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<del>X</del> J18	IO_B6_J18	U5C	IO_B7_E15	<del>E15</del>
<del>X</del> J19	IO_B6_J19		IO_B7_E16	<del>E16</del>
<del>X</del> J20	IO_B6_J20		IO_B7_F11	<del>F11</del>
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<del>X</del> R22	IO_B5_R22		IO_B7_F14	<del>F14</del>
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<del>X</del> A3	IO_B8_A3		IO_B3_U11	<del>U11</del>
<del>X</del> L21	IO_B6_L21		IO_B3_U9	<del>U9</del>
<del>X</del> B3	IO_B8_B3		IO_B3_V10	<del>V10</del>
<del>X</del> U2	IO_B2_U2		IO_B3_V11	<del>V11</del>
<del>X</del> AB17	IO_B4_AB17		IO_B3_V5	<del>V5</del>
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<del>X</del> AB19	IO_B4_AB19		IO_B3_V9	<del>V9</del>
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<del>X</del> J3	IO_B1_J3		IO_B8_C10	<del>C10</del>
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<del>X</del> C13	IO_B7_C13		IO_B8_C7	<del>C7</del>
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<del>X</del> C17	IO_B7_C17		IO_B8_D10	<del>D10</del>
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Unused components of the Cyclone IV FPGA.

Sheet: /Unused FPGA Blocks/  
File: tranZPUter-SW\_FPGA2-700\_v1\_3.sch

**Title: tranZPUter SW 700 (FPGA 2)**

Size: A4

Date: 2020-12-08

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Id: 7/7