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H1   H2
M2.5 M2.5

GNDPWR

Capabilities upgrade for the Sharp MZ80A.
Providing upgraded hardware and an optional MPU for provision of SD services to host,
alternative soft processors, ZPUTA Menu System and additional resources to enhance
the Sharp MZ80A.

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Clock Select
Whenever the main board is being accessed or the frequency is set to default, the system clock is used (2MHz on an MZ-80A, 3.58MHz on an MZ-700). If the main board is disabled and the frequency is changed to XMHz then the clock supplied by the K64F is used.

Secondary Clock frequency generated by the Control MPU

BUSACK Info
Low = mainboard circuits disabled except NMI,INT, WAIT, RESET and CLK.
BUSACK is set low if expansion memory has priority as defined by latch 273 and Flash RAM decoding, or set low if the Z80 is in tri-state mode and the MPU is requesting the mainboard circuits to be disabled.

I/O & Memory Map
Defined in the Flash RAM. Memory can potentially be mapped in 64byte chunks between the expansion memory and system board memory. Generally though the mapping will mirror Sharp MZ series machines.

A glitch on the 39SF040 causes the A16:18 lines to pulse high for 10ns on activation of WE and as U2 has a 0ns delay on address lines to data latch it required the addition of U13A to shape and delay WE. It occurs on RD but is not critical.

IO Range Configurations
Base set in the the Flash RAM decoder.
0x20-0x2F
0x60-0x6F (default)
0xA0-0xAF
0xF0-0xFF

The K64F hasnt got the performance to reliably intercept an IORQ in the region 0xE0-0xFF and remap the request so this circuit inserts a WAIT until the K64F sets the CTL_BUSRQ low.

Logic to lift the original Z80 off the main board and add to it's capabilities by adding 512K Banked RAM which can be mapped into any location in the original machine. The CPU can also run standalone within the Banked RAM, connecting to the base for I/O as needed. Capability to change the CPU frequency to match the MZ700/MZ80B spec's.

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Title: tranZPUter SW (Z80 Host Upgrade)

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+5V +3.3V

C12 100nF C13 100uF 16V C14 100nF C15 100uF 16V

GNDPWR BT1 M5621F GNDPWR

GNDPWR

U12
Teensy3.5

3.3V VBAT VUSB Vin 3.3V 3.3V 3.3V_(250mA)
85 86 81 48 66 15 46

Pin	Signal	Net
2	I/O_0_(B16)	Z80_D0
3	I/O_1_(B17)	Z80_D1
21	I/O_29_(B18)	Z80_D2
22	I/O_30_(B19)	Z80_D3
61	I/O_43_(B20)	Z80_D4
64	I/O_46_(B21)	Z80_D5
62	I/O_44_(B22)	Z80_D6
63	I/O_45_(B23)	Z80_D7

37	I/O_15_(C0)	Z80_A0
44	I/O_22_(C1)	Z80_A1
45	I/O_23_(C2)	Z80_A2
11	I/O_9_(C3)	Z80_A3
12	I/O_10_(C4)	Z80_A4
35	I/O_13_(C5)	Z80_A5
13	I/O_11_(C6)	Z80_A6
14	I/O_12_(C7)	Z80_A7

In order to aid software speed and simplicity
the signals have been ordered according
to ARM GPIO Port and Bit rather than the
Teensy pin number. This will aid in reducing
time taken for an interrupt to process as it
performs less instructions to piece
together an address or data signal.

Z80_IORQ 10 I/O_8_(D3) I/O_35_(C8) 27 Z80_A8
Z80_MREQ 9 I/O_7_(D2) I/O_36_(C9) 28 Z80_A9
Z80_WR 68 I/O_48_(D9) I/O_37_(C10) 29 Z80_A10
SYSCLK 17 I/O_25_(A5) I/O_38_(C11) 30 Z80_A11
Z80_RD 75 I/O_55_(D11) I/O_3_(A12) 5 Z80_A12
Z80_WAIT 74 I/O_54_(D15) I/O_4_(A13) 6 Z80_A13
CTL_CLK 36 I/O_14_(D1) I/O_26_(A14) 18 Z80_A14
CTL_BUSRQ 4 I/O_2_(D0) I/O_27_(A15) 19 Z80_A15
CTL_BUSACK 43 I/O_21_(D6) I/O_33_(E24) 25 Z80_A16
Z80_BUSACK 7 I/O_5_(D7) I/O_34_(E25) 26 Z80_A17
CTL_HALT 71 I/O_51_(D14) I/O_24_(E26) 16 Z80_A18
CTL_CLKSLCT 67 I/O_47_(D8) I/O_20_(D5) 42 CTL_M1

78 ADC1_(ADC_DM0) DAC1_(A1_SE23) 33
79 ADC0_(ADC_DP0) DAC0_(A0_SE23) 32
80 AREF_(VREFH)

58 I/O_40_(A28) I/O_57_(E11) 77 SYSREQ
59 I/O_41_(A29) I/O_56_(E10) 76 SVCREQ
60 I/O_42_(A26) I/O_52_(D13) 72 TZ_BUSACK
Z80_NMI 31 I/O_39_(A17) I/O_6_(D4) 8 Z80_RESET
Z80_INT 20 I/O_28_(A16) I/O_32_(B11) 24
CTL_RFSH 73 I/O_53_(D12) I/O_31_(B10) 23
Z80_MEMO 38 I/O_16_(B0) I/O_50_(B5) 70 ENIOWAIT
  I/O_49_(B4) 69 Z80_MEM4
82 RESET I/O_18_(B3) 40 Z80_MEM3
83 PROGRAM I/O_19_(B2) 41 Z80_MEM2
  I/O_17_(B1) 39 Z80_MEM1
51 D+_(USB1_DP)
50 D-_(USB1_DM) DC 56
49 USB5V DD 57
  DE 55

GND GND GND GND GND GND GND Analog_GND
54 53 52 84 65 1 34 47

GNDPWR

Z80_D[0..7] Z80_A[0..18]

Z80_RD
Z80_WR
Z80_MREQ
Z80_IORQ
Z80_WAIT
Z80_NMI
Z80_INT
Z80_RESET
Z80_BUSACK
CTL_BUSRQ
CTL_BUSACK
CTL_M1
CTL_RFSH
CTL_HALT
CTL_CLK
SYSCLK
CTL_CLKSLCT
Z80_MEM[0..4]
ENIOWAIT
SVCREQ
SYSREQ
TZ_BUSACK

The Teensy 3.5 MPU from PJRC.COM.
A fully self-contained MPU using the Freescale K64F series MPU based on the
Cortex-M4 ARM processor. This device is 5V tolerant so no specific voltage conversion
is required.

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