Sheet: Z80 Upgrade

File: tranZPUter-SW_z80-700_v1_3.sch

Sheet: NXP K64FX512

File: tranZPUter-SW_k64fx512-700_v1_3.sch

Sheet: Video Interface

File: tranZPUter-SW_VideoInterface-700_v1_3.sch

Sheet: CPLD and FPGA Programming

File: tranZPUter-SW_CPLDFPGA_Programming-700_v1_3.sch

Sheet: Unsed FPGA Blocks

File: tranZPUter-SW_FPGA2-700_v1_3.sch

Sheet: Power Supply

File: tranZPUter-SW_PowerSupply-700_v1_3.sch

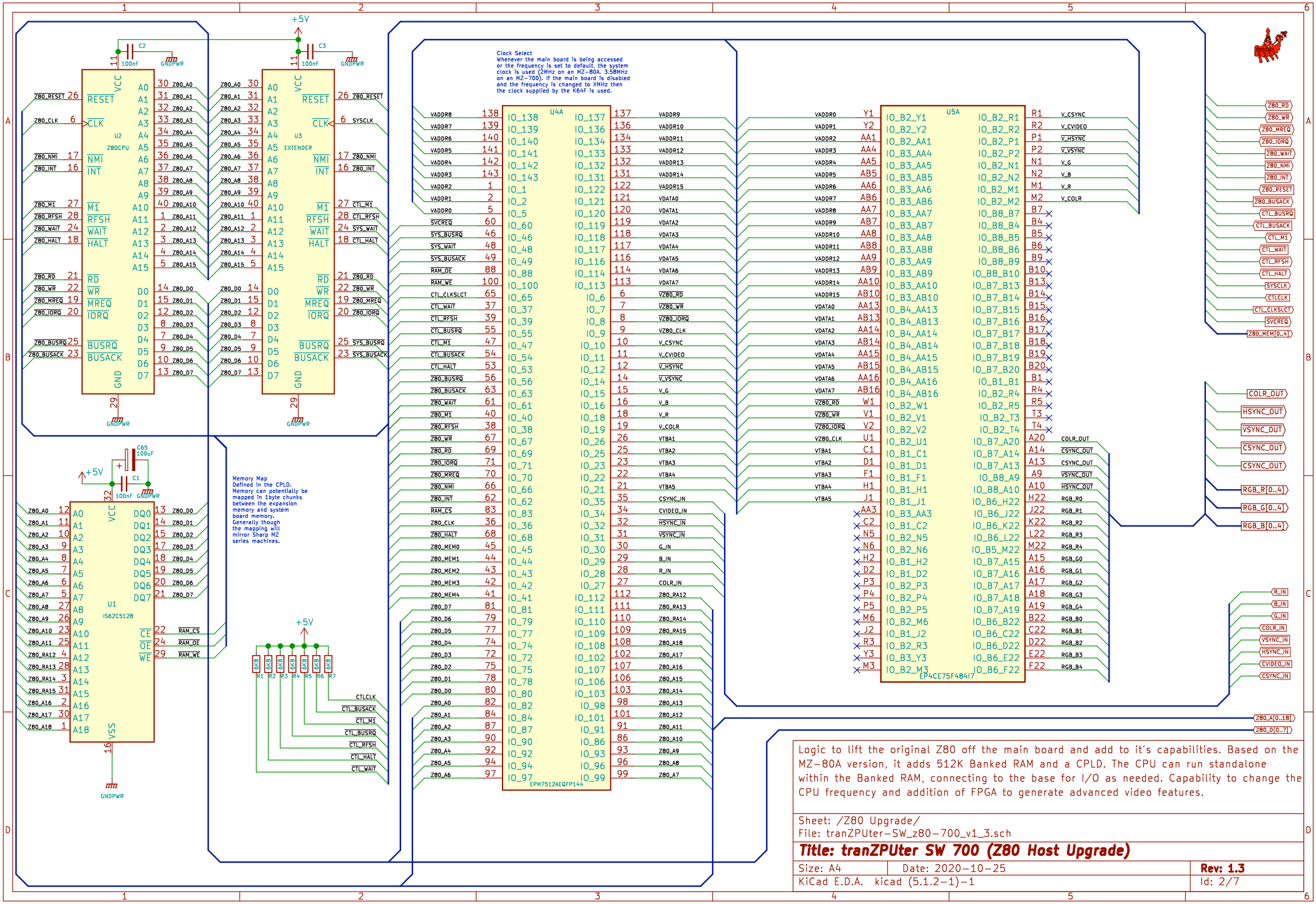
LG1
Argo Logo

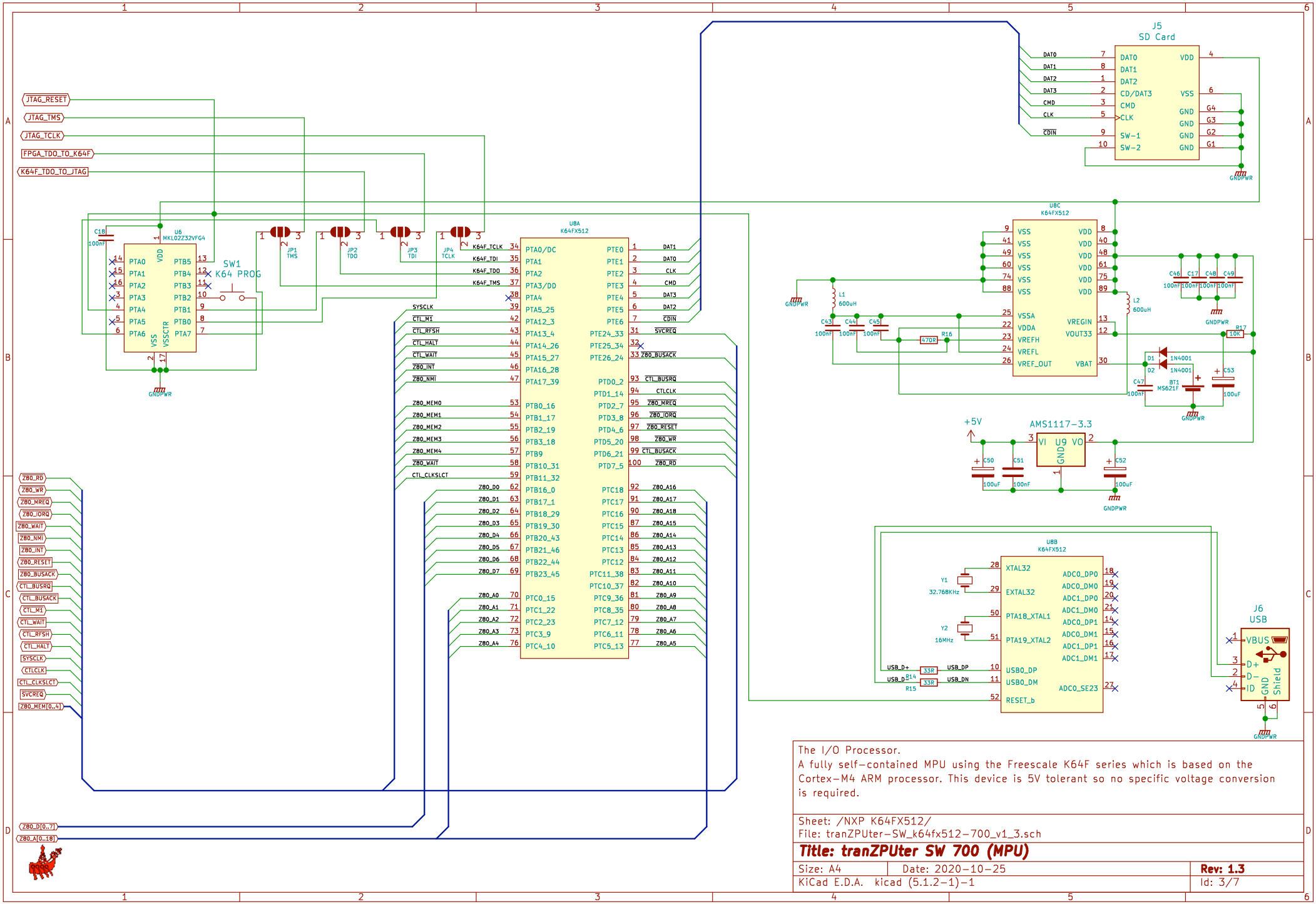
Capabilities upgrade for the Sharp MZ80A.
Providing upgraded hardware and an optional MPU for provision of SD services to host, alternative soft processors, ZPUTA Menu System and additional resources to enhance the Sharp MZ80A.

Sheet: /
File: tranZPUter-SW-700_v1_3.sch

Title: tranZPUter SW 700

Size: A4	Date: 2020-06-19	**Rev: 1.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 1/7


Clock Select
Whenever the main board is being accessed or the frequency is set to default, the system clock is used (2MHz on an MZ-80A, 3.58MHz on an MZ-700). If the main board is disabled and the frequency is changed to XMHz then the clock supplied by the K64F is used.
Memory Map
Defined in the CPLD.
Memory can potentially be mapped in 1byte chunks between the expansion memory and system board memory.
Generally though the mapping will mirror Sharp MZ series machines.
U2
Z80CPU
U3
EXTENDER
U4A
EPM7512AEQFP144
U5A
EP4CE75F48417
U1
IS62C5128
+5V
GNDPWR
C2
C3
C65
C1
100nF
100uF
Logic to lift the original Z80 off the main board and add to it's capabilities. Based on the MZ-80A version, it adds 512K Banked RAM and a CPLD. The CPU can run standalone within the Banked RAM, connecting to the base for I/O as needed. Capability to change the CPU frequency and addition of FPGA to generate advanced video features.
Sheet: /Z80 Upgrade/
File: tranZPUter-SW_z80-700_v1_3.sch
Title: tranZPUter SW 700 (Z80 Host Upgrade)
Size: A4
Date: 2020-10-25
Rev: 1.3
KiCad E.D.A. kicad (5.1.2-1)-1
Id: 2/7

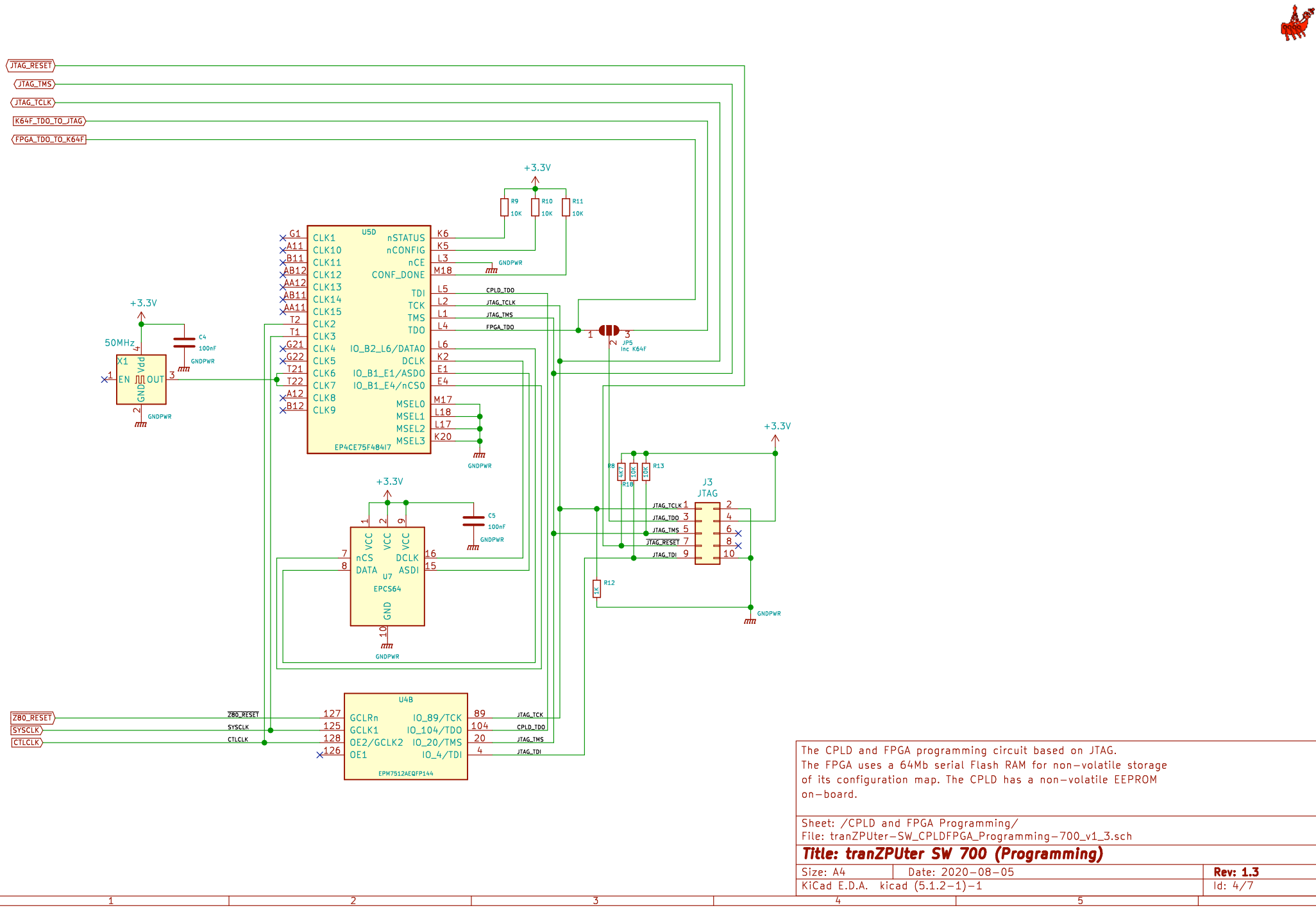


The I/O Processor.
A fully self-contained MPU using the Freescale K64F series which is based on the Cortex-M4 ARM processor. This device is 5V tolerant so no specific voltage conversion is required.

Sheet: /NXP K64FX512/
File: tranZPUter-SW_k64fx512-700_v1_3.sch

Title: tranZPUter SW 700 (MPU)

Size: A4	Date: 2020-10-25	**Rev: 1.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 3/7

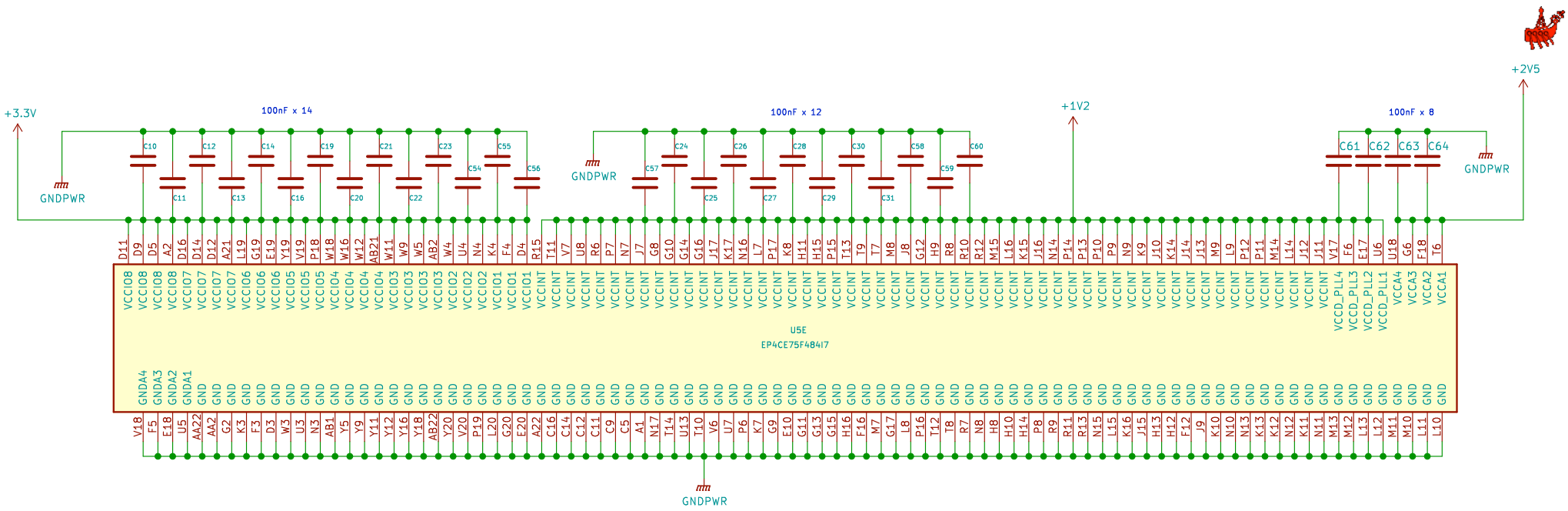


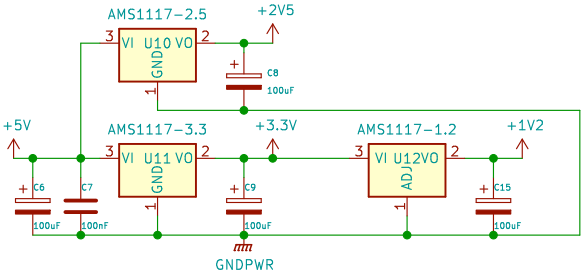
The CPLD and FPGA programming circuit based on JTAG.
The FPGA uses a 64Mb serial Flash RAM for non-volatile storage of its configuration map. The CPLD has a non-volatile EEPROM on-board.

Sheet: /CPLD and FPGA Programming/
File: tranZPUter-SW_CPLDFPGA_Programming-700_v1_3.sch

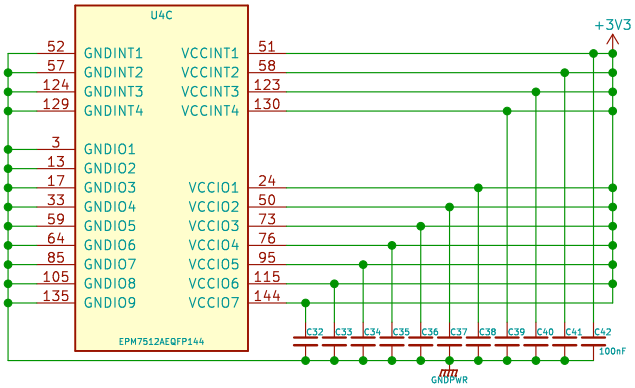
Title: tranZPUter SW 700 (Programming)

Size: A4	Date: 2020-08-05	**Rev: 1.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 4/7





Seperate 3.3V for the CPLF/FPGA , the K64F has it's own regulator.
This is intentional for board routing and power demands of the 3.3V rail.

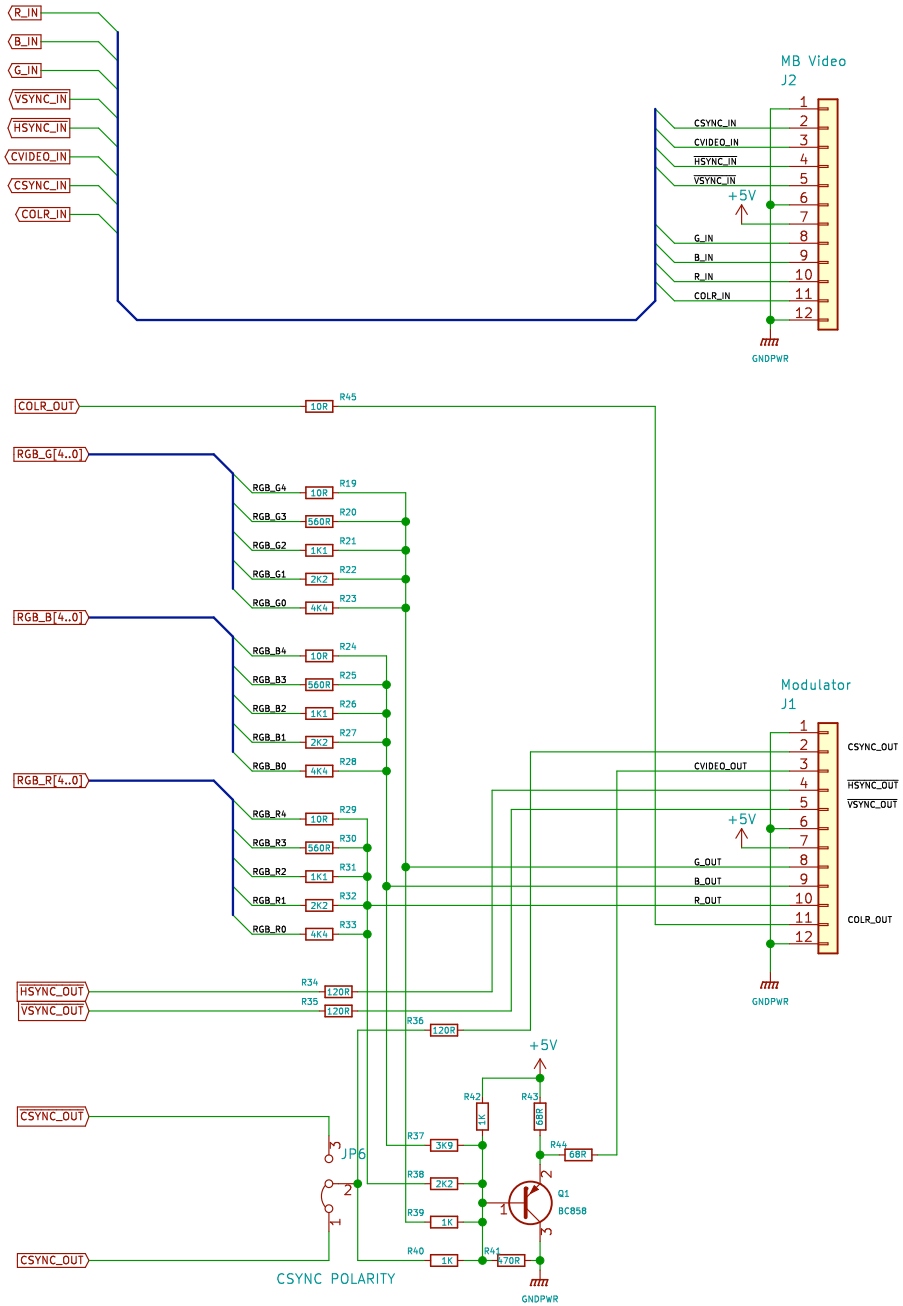


Decoupling and voltage regulators to provide CPLD and FPGA with 1.2V (core FPGA), 2.5V (analogue FPGA, PLL) and 3.3V (FPGA I/O and CPLD) voltages.

Sheet: /Power Supply/
File: tranZPUter-SW_PowerSupply-700_v1_3.sch

Title: tranZPUter SW 700 (Power Supply)

Size: A4	Date: 2020-10-25	**Rev: 1.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 5/7

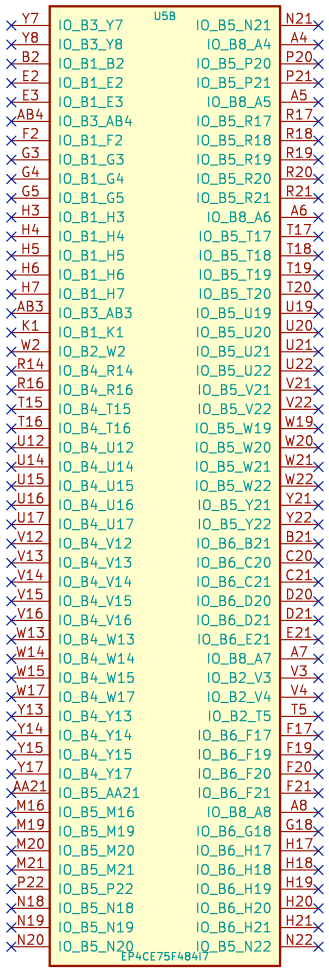


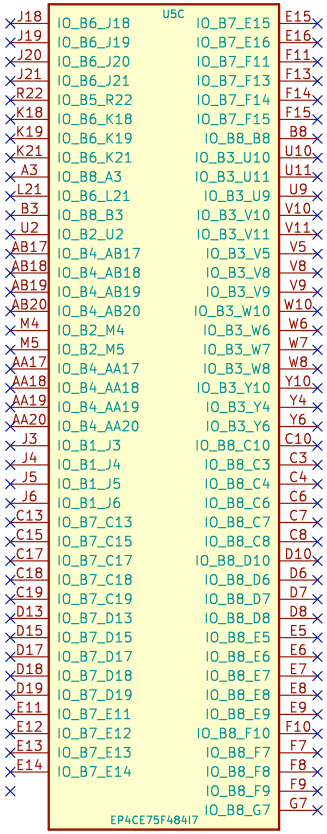
This circuitry inserts the tranZPUter 700 SW in between the mainboard Video circuitry and the modulator/RGB/Composite output module. This allows the tranZPUterSW 700 to override the original video and replace it with video generated by the FPGA.

Sheet: /Video Interface/
File: tranZPUter-SW_VideoInterface-700_v1_3.sch

Title: tranZPUter SW 700 (Video Interface)

Size: A4	Date: 2020-10-25	**Rev: 1.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 6/7





Unused components of the Cyclone IV FPGA.

Sheet: /Unsed FPGA Blocks/
File: tranZPUter-SW_FPGA2-700_v1_3.sch

Title: tranZPUter SW 700 (FPGA 2)

Size: A4	Date: 2020-10-25	**Rev: 1.3**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 7/7