Sheet: Z80 Upgrade

File: tranZPUter_z80_v2_0.sch

Sheet: FPGA_1

File: tranZPUter_fpga_v2_0.sch

Sheet: FPGA_RAM

File: tranZPUter_fpga2_v2_0.sch

Sheet: FPGA_2

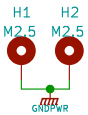
File: tranZPUter_fpga3_v2_0.sch

Sheet: PSU

File: tranZPUter_power_v2_0.sch

Sheet: FPGA_DECOUPLING

File: tranZPUter_power_fpga_v2_0.sch



Capabilities upgrade for the Sharp MZ80A.
Providing upgraded hardware and an optional MPU for provision of SD services to host, alternative soft processors, ZPUTA Menu System and additional resources to enhance the Sharp MZ80A.

Sheet: /
File: tranZPUter_v2_0.sch

Title: tranZPUter SW

Size: A4	Date: 2020-07-04	**Rev: 2.1**
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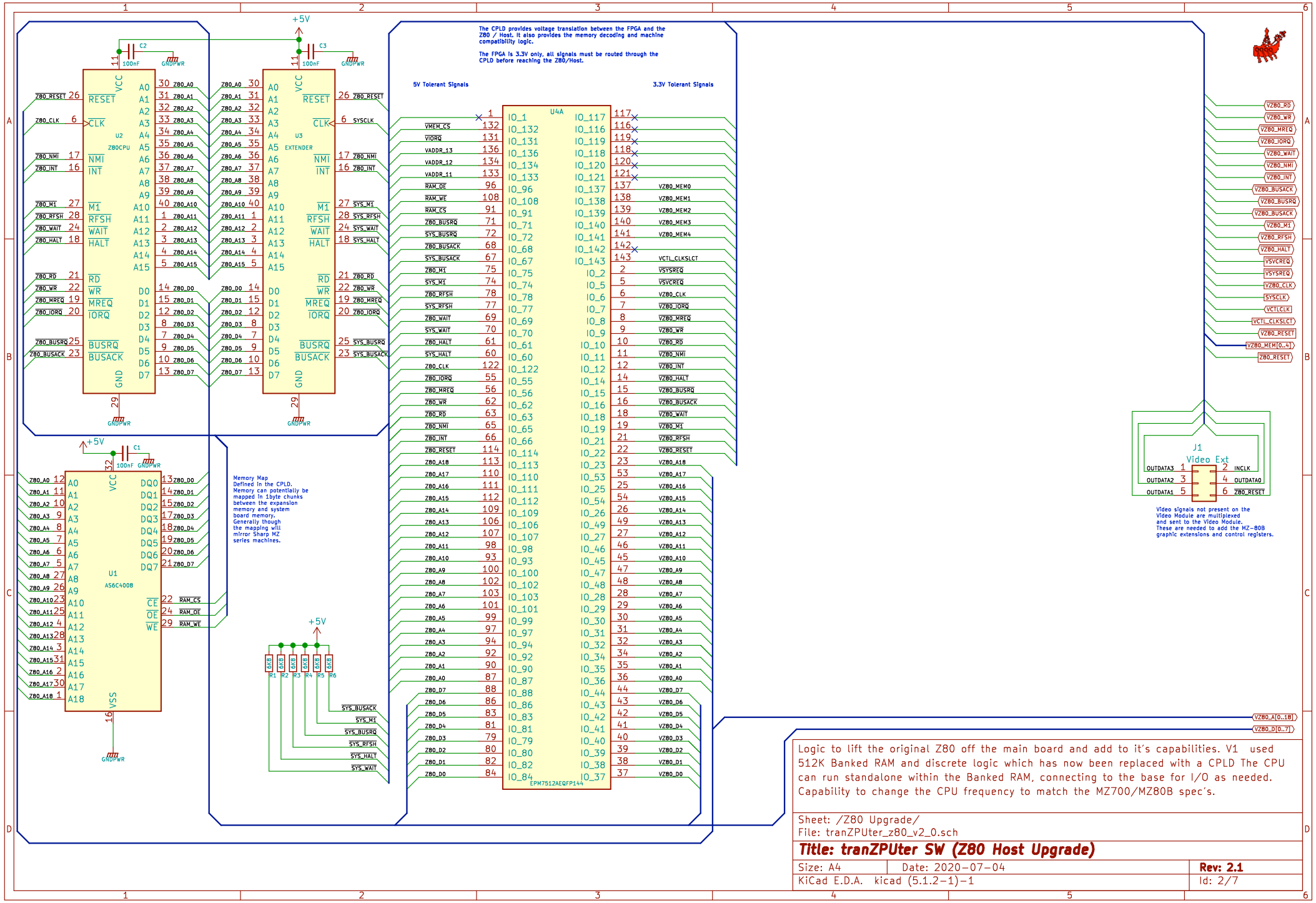
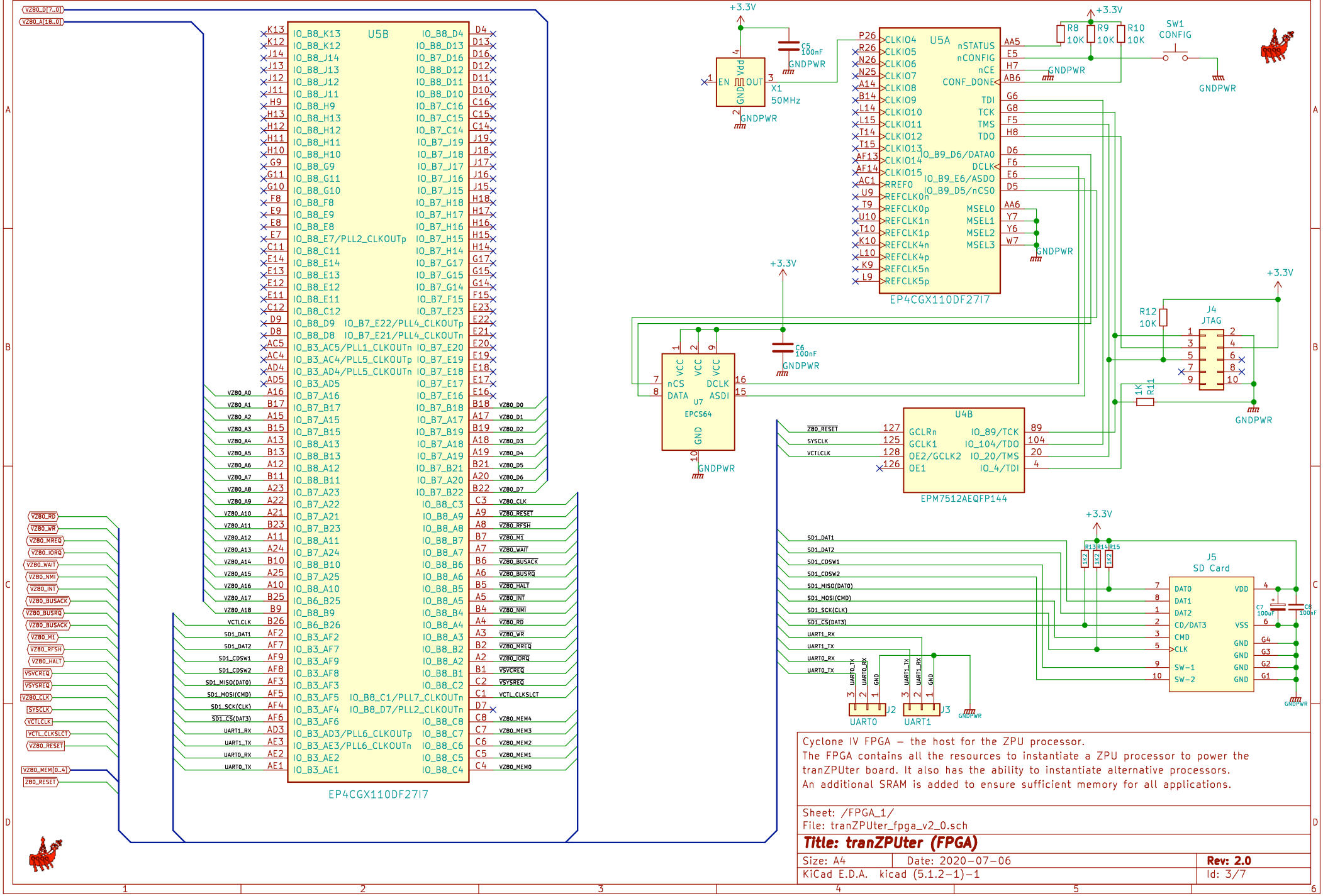
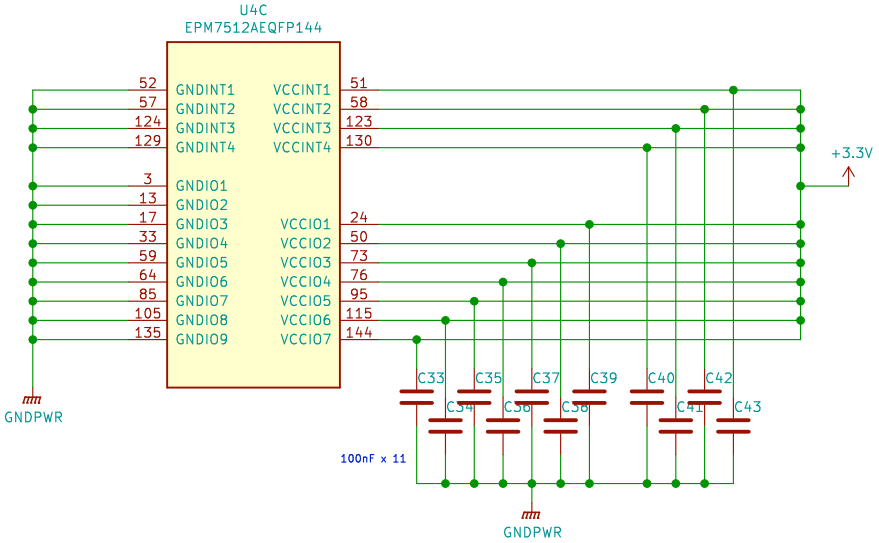
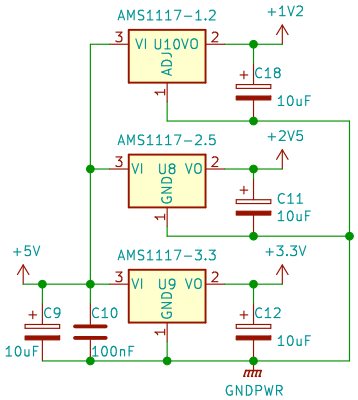

The CPLD provides voltage translation between the FPGA and the Z80 / Host. It also provides the memory decoding and machine compatibility logic.
The FPGA is 3.3V only, all signals must be routed through the CPLD before reaching the Z80/Host.
5V Tolerant Signals
3.3V Tolerant Signals
U2 Z80CPU
U3 EXTENDER
U4A
EPM7512AEQFP144
U1 AS6C4008
Memory Map Defined in the CPLD. Memory can potentially be mapped in 1byte chunks between the expansion memory and system board memory. Generally though the mapping will mirror Sharp MZ series machines.
J1 Video Ext
Video signals not present on the Video Module are multiplexed and sent to the Video Module. These are needed to add the MZ-80B graphic extensions and control registers.
Logic to lift the original Z80 off the main board and add to it's capabilities. V1 used 512K Banked RAM and discrete logic which has now been replaced with a CPLD The CPU can run standalone within the Banked RAM, connecting to the base for I/O as needed. Capability to change the CPU frequency to match the MZ700/MZ80B spec's.
Sheet: /Z80 Upgrade/
File: tranZPUter_z80_v2_0.sch
Title: tranZPUter SW (Z80 Host Upgrade)
Size: A4
Date: 2020-07-04
Rev: 2.1
KiCad E.D.A. kicad (5.1.2-1)-1
Id: 2/7


U5B
EP4CGX110DF27I7
U5A
EP4CGX110DF27I7
U4B
EPM7512AEQFP144
U7
EPCS64
X1
50MHz
J4
JTAG
J5
SD Card
J2
UART0
J3
UART1
SW1
CONFIG
+3.3V
GNDPWR
Cyclone IV FPGA – the host for the ZPU processor.
The FPGA contains all the resources to instantiate a ZPU processor to power the tranZPUter board. It also has the ability to instantiate alternative processors.
An additional SRAM is added to ensure sufficient memory for all applications.
Sheet: /FPGA_1/
File: tranZPUter_fpga_v2_0.sch
Title: tranZPUter (FPGA)
Size: A4
Date: 2020-07-06
Rev: 2.0
KiCad E.D.A. kicad (5.1.2-1)-1
Id: 3/7



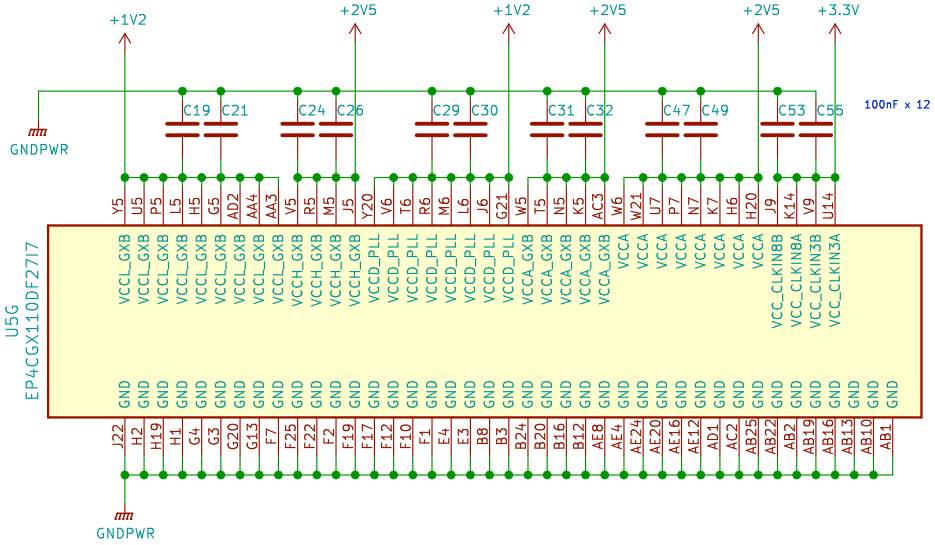


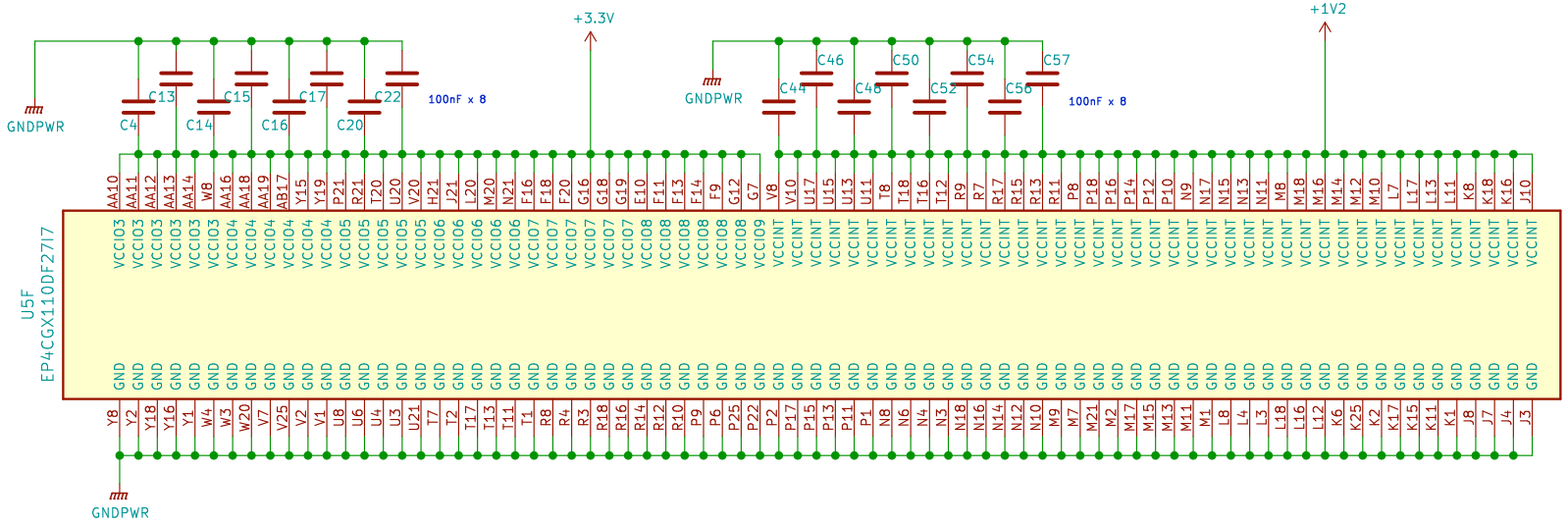
The FPGA has requirement for 3 seperate voltages, 3.3V, 2.5V and 1.2V. The CPLD only requires 3.3V but plenty of decoupling.

Sheet: /PSU/
File: tranZPUter_power_v2_0.sch

Title: Power Supply and CPLD Decoupling

Size: A4	Date: 2020-08-10	**Rev: v2.0**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 4/7



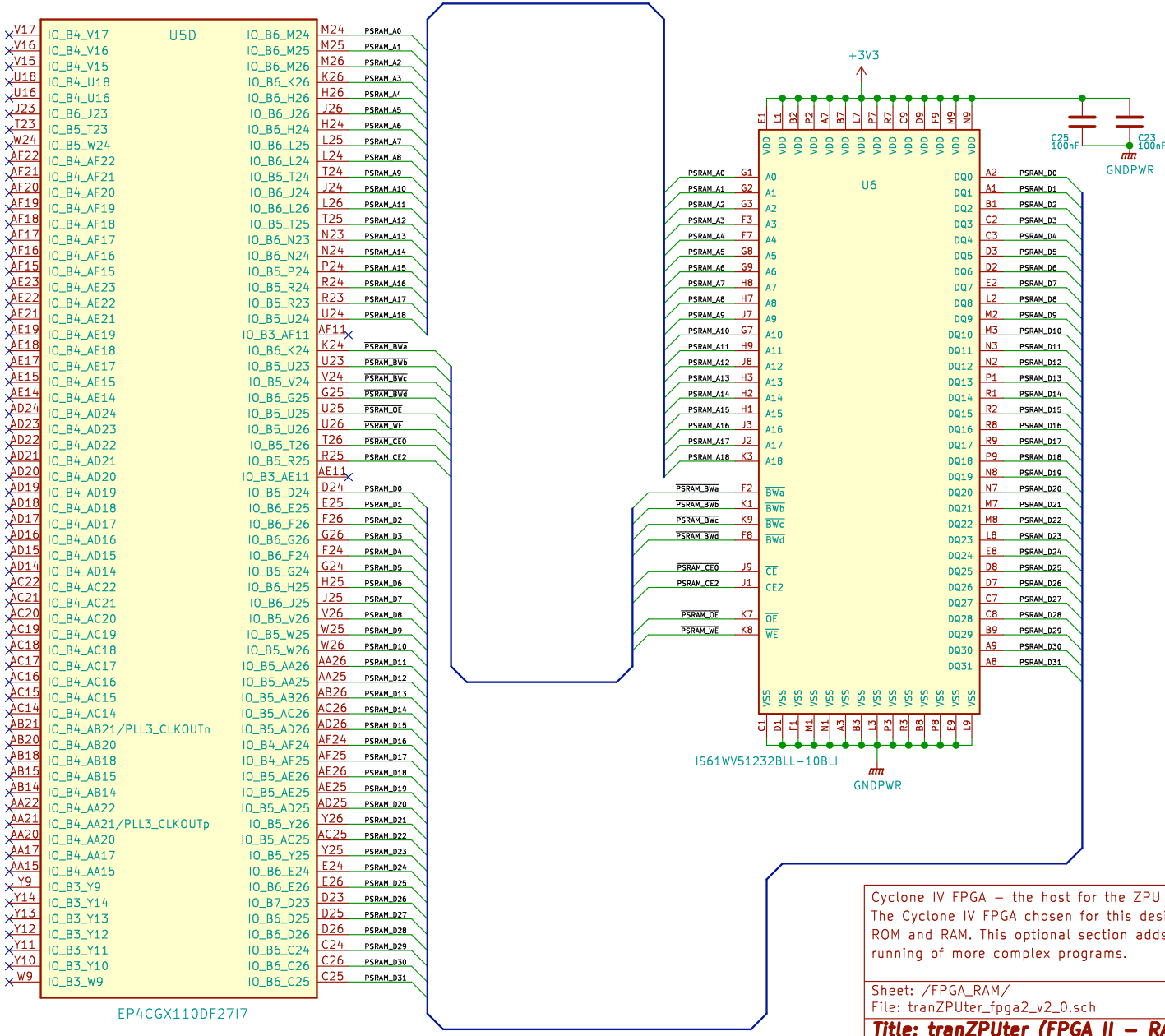


The FPGA has requirement for 3 seperate voltages, 3.3V, 2.5V and 1.2V.

Sheet: /FPGA_DECOUPLING/
File: tranZPUter_power_fpga_v2_0.sch

Title: FPGA Power Supply and Decoupling

Size: A4	Date: 2020-08-10	**Rev: v2.0**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 5/7

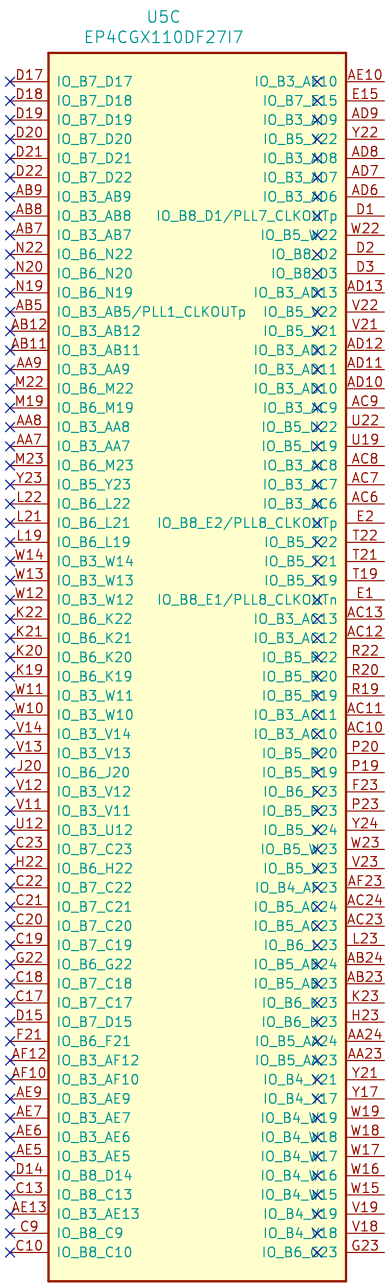


Cyclone IV FPGA – the host for the ZPU processor.
The Cyclone IV FPGA chosen for this design has approx 600KB of free BRAM for cache, ROM and RAM. This optional section adds further memory for the ZPU processor to enable running of more complex programs.

Sheet: /FPGA_RAM/
File: tranZPUter_fpga2_v2_0.sch

Title: tranZPUter (FPGA II – RAM)

Size: A4	Date: 2020-07-06	**Rev: 2.0**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 6/7



Cyclone IV FPGA – the host for the ZPU processor.
The Cyclone IV FPGA chosen for this design has a lot more I/O ports than are needed.
This sheet just assigns them to no connect.

Sheet: /FPGA_2/
File: tranZPUter_fpga3_v2_0.sch

Title: tranZPUter (FPGA III – Unassigned)

Size: A4	Date: 2020-07-06	**Rev: 2.0**
KiCad E.D.A. kicad (5.1.2-1)-1		Id: 7/7