Z80 (CPU Interface)

File: tzpuFusionX_CPU_Interface_v1_0.kicad_sch

SOM2D02 (CPU Interface)

File: tzpuFusionX_FPGA_CPU_v1_0.kicad_sch

SOM2D02 (IO)

File: tzpuFusionX_FPGA_CPU_Memory_v1_0.kicad_sch

SOM2D02 (Video)

File: tzpuFusionX_FPGA_Video_v1_0.kicad_sch

Power Supply

File: tzpuFusionX_PowerSupply_v1_0.kicad_sch

LG1
Argo Logo

FID1

FID2

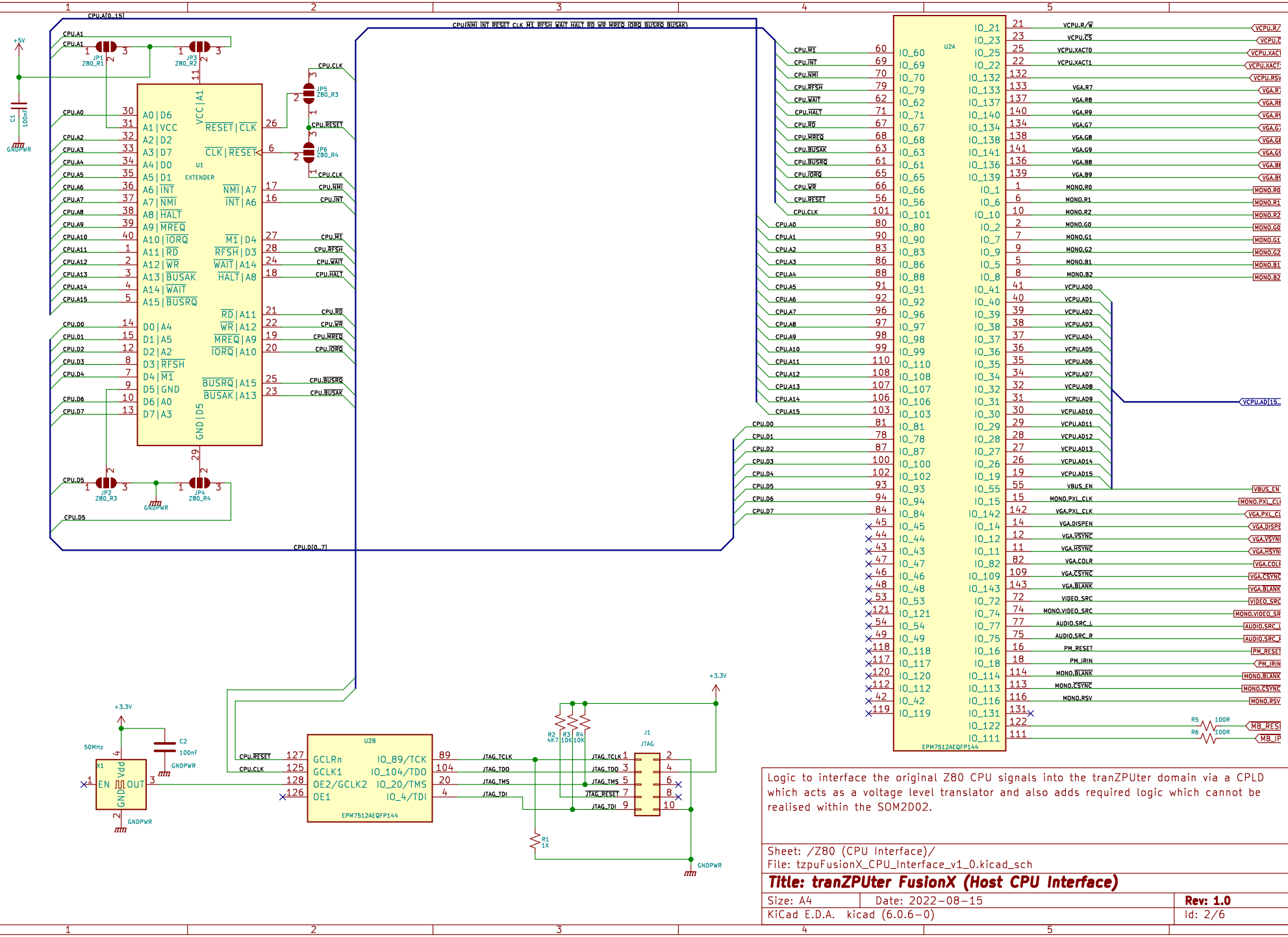
FID3

Capabilities upgrade for the Sharp MZ Series Computers.
Z80 CPU is replaced by a Linux based System On a Module offering dual-core ARM Cortex A7 CPU's, 256MB RAM and 2G NAND. The upgraded host acts as a Linux host or using a soft Z80 CPU, an upgraded Z80 system.

Sheet: /
File: tzpuFusionX_v1_0.kicad_sch

Title: tranZPUterX Fusion

Size: A4	Date: 2022-08-15	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.6-0)		Id: 1/6

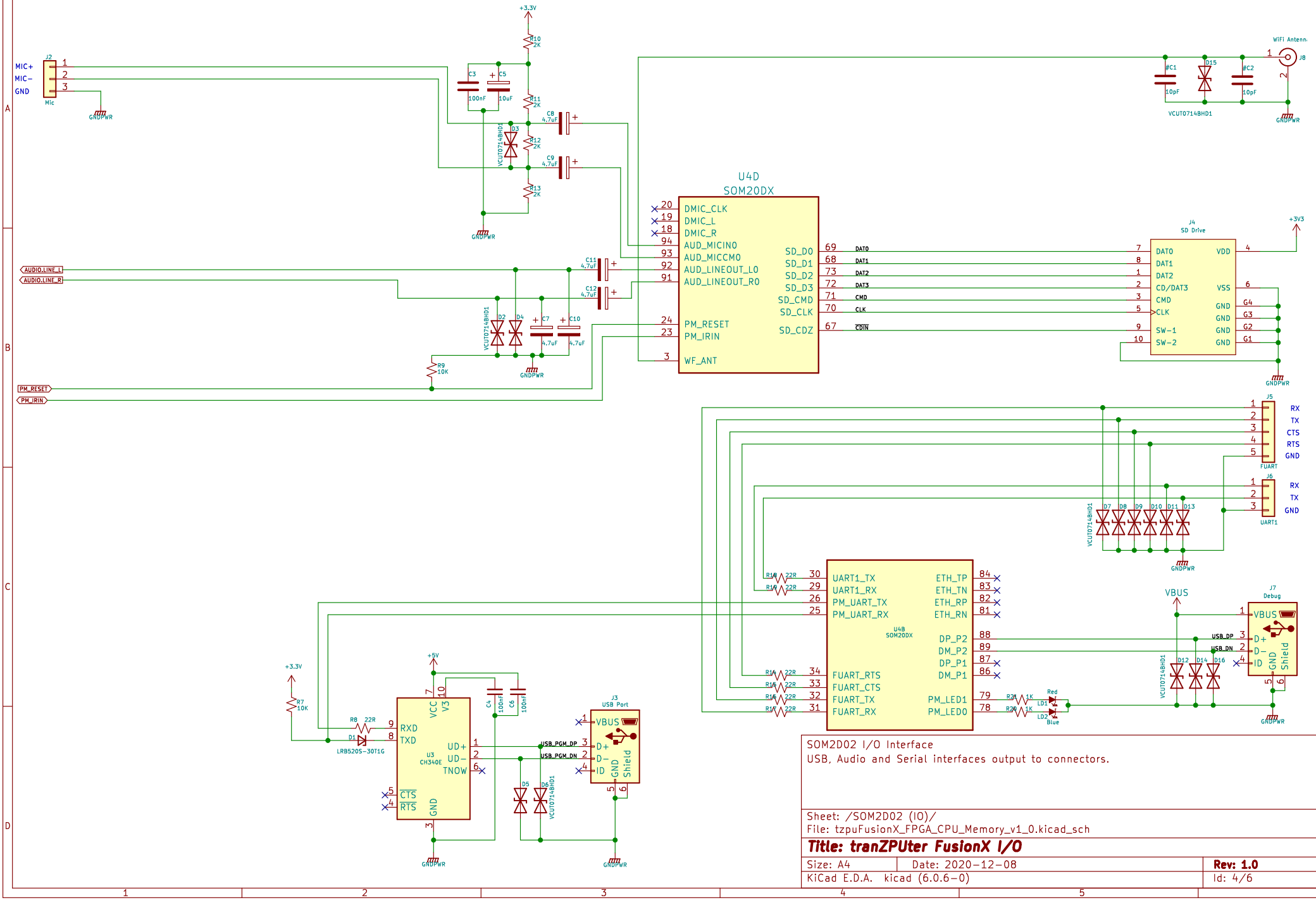


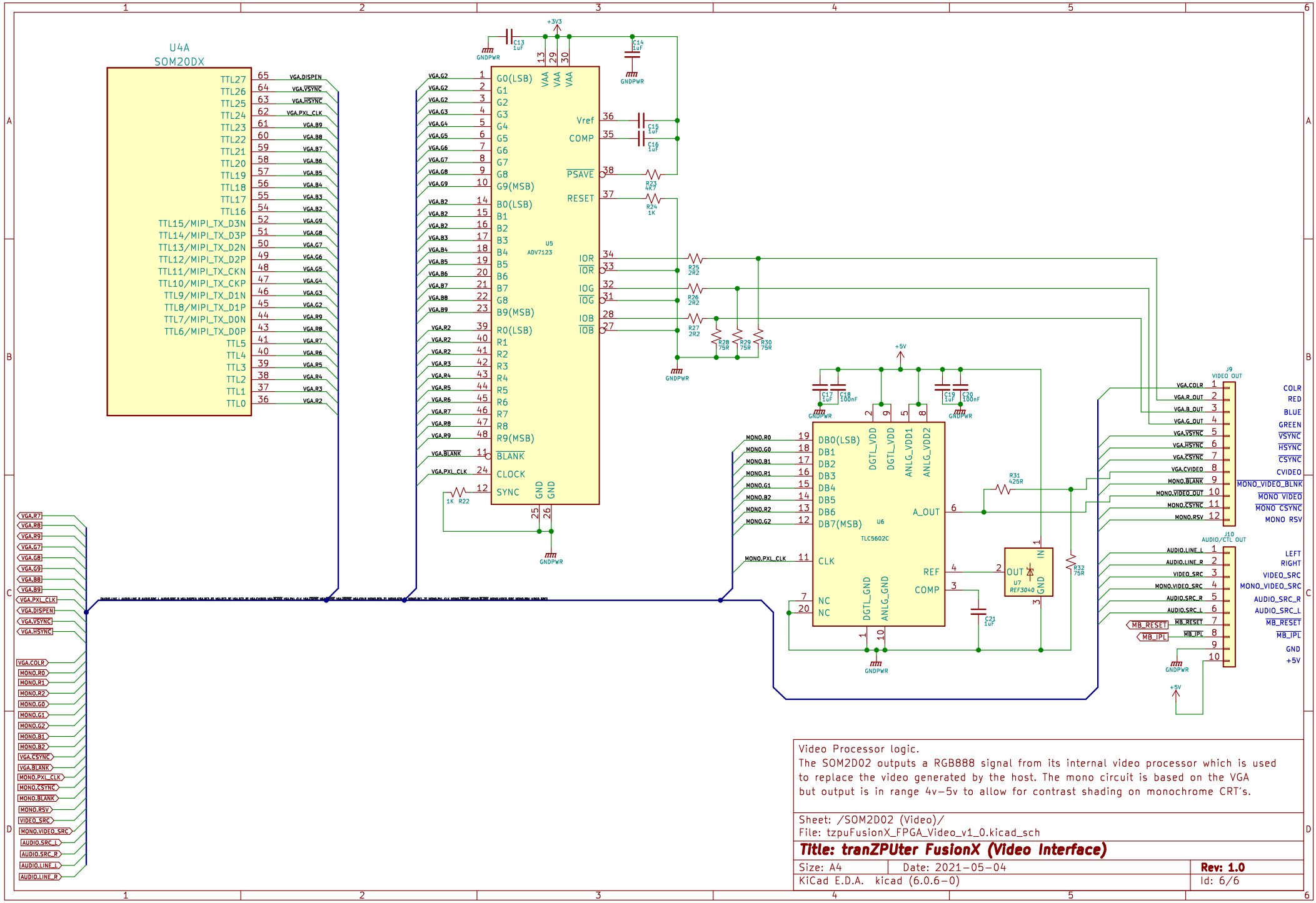
Logic to interface the original Z80 CPU signals into the tranZPUter domain via a CPLD which acts as a voltage level translator and also adds required logic which cannot be realised within the SOM2D02.

Sheet: /Z80 (CPU Interface)/
File: tzpuFusionX_CPU_Interface_v1_0.kicad_sch

Title: tranZPUter FusionX (Host CPU Interface)

Size: A4	Date: 2022-08-15	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.6-0)		Id: 2/6


MIC+
MIC-
GND
Mic
GNDPWR
+3.3V
AUDIO_LINE_L
AUDIO_LINE_R
PM_RESET
PM_IRIN
U4D
SOM20DX
DMIC_CLK
DMIC_L
DMIC_R
AUD_MICIN0
AUD_MICCM0
AUD_LINEOUT_L0
AUD_LINEOUT_R0
PM_RESET
PM_IRIN
WF_ANT
SD_D0
SD_D1
SD_D2
SD_D3
SD_CMD
SD_CLK
SD_CDZ
DAT0
DAT1
DAT2
DAT3
CMD
CLK
CDIN
J4
SD Drive
DAT0
DAT1
DAT2
CD/DAT3
CMD
CLK
SW-1
SW-2
VDD
VSS
GND
WiFi Antenn.
J8
VCUT0714BHD1
U4B
SOM20DX
UART1_TX
UART1_RX
PM_UART_TX
PM_UART_RX
FUART_RTS
FUART_CTS
FUART_TX
FUART_RX
ETH_TP
ETH_TN
ETH_RP
ETH_RN
DP_P2
DM_P2
DP_P1
DM_P1
PM_LED1
PM_LED0
J5
FUART
RX
TX
CTS
RTS
GND
J6
UART1
J7
Debug
VBUS
USB_DP
USB_DN
Shield
U3
CH340E
LRB520S-30T1G
J3
USB Port
USB_PGM_DP
USB_PGM_DN
Red
Blue
SOM2D02 I/O Interface
USB, Audio and Serial interfaces output to connectors.
Sheet: /SOM2D02 (IO)/
File: tzpuFusionX_FPGA_CPU_Memory_v1_0.kicad_sch
Title: tranZPUter FusionX I/O
Size: A4
Date: 2020-12-08
Rev: 1.0
KiCad E.D.A. kicad (6.0.6-0)
Id: 4/6

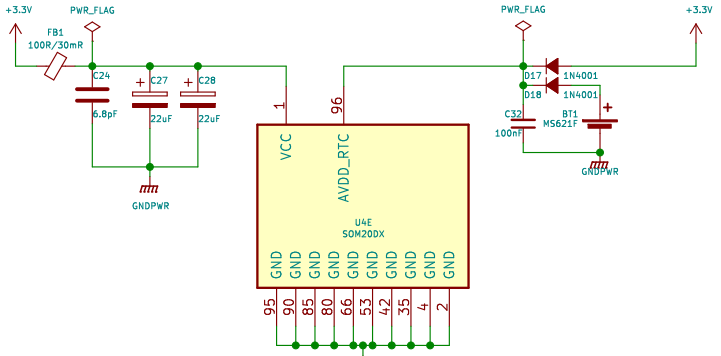


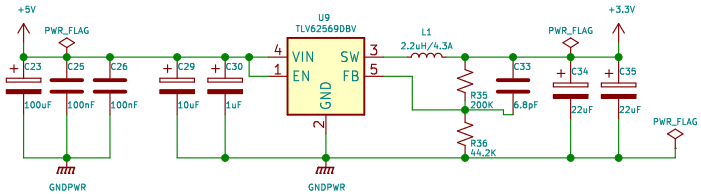
Video Processor logic.
The SOM2D02 outputs a RGB888 signal from its internal video processor which is used to replace the video generated by the host. The mono circuit is based on the VGA but output is in range 4v–5v to allow for contrast shading on monochrome CRT's.

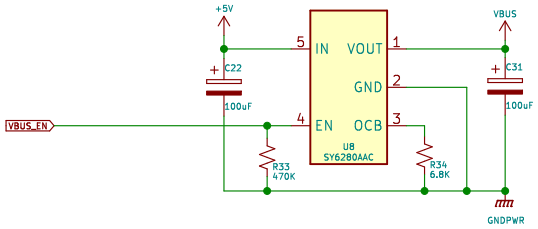
Sheet: /SOM2D02 (Video)/
File: tzpuFusionX_FPGA_Video_v1_0.kicad_sch

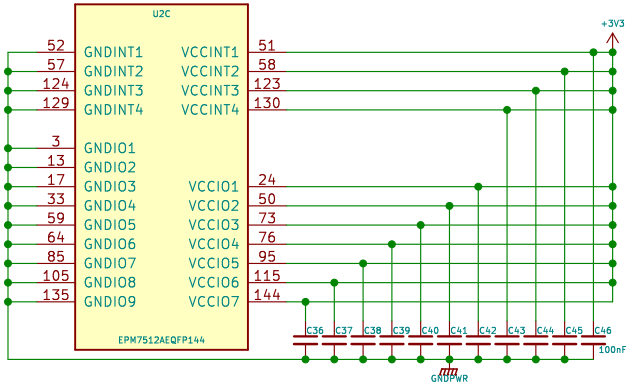
Title: tranZPUter FusionX (Video Interface)

Size: A4	Date: 2021-05-04	Rev: 1.0
KiCad E.D.A. kicad (6.0.6-0)		Id: 6/6







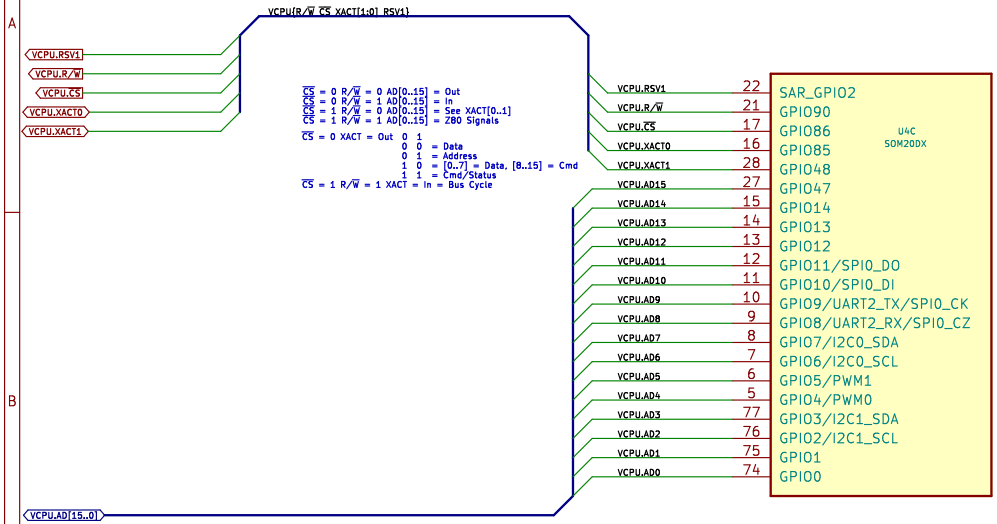


Decoupling and voltage regulators to provide CPLD and SOM with 3.3V, RTC backup and USB bus with 5V/1A.

Sheet: /Power Supply/
File: tzpuFusionX_PowerSupply_v1_0.kicad_sch

Title: tranZPUter FusionX (Power Supply)

Size: A4	Date: 2021-05-04	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.6-0)		Id: 7/6



The host CPU is replaced with a Dual-Core System On a Module running Linux. This module instantiates a software Z80 CPU to drive the underlying host and utilise its resources.

Sheet: /SOM2D02 (CPU Interface)/
File: tzpuFusionX_FPGA_CPU_v1_0.kicad_sch

Title: tranZPUter FusionX (SOM2D02 CPU Interface)

Size: A4	Date: 2022-08-15	**Rev: 1.0**
KiCad E.D.A. kicad (6.0.6-0)		Id: 8/6