Rev 0.5:
- Connect PLD pin 18 to CS
- Set MEML to ground
- Reserve 1 temporary
- Add missing bypass caps

Rev 0.6:
- Split off second PLD for addressing
- Add two delay gates
- Add 2 jumpers to 1st pld
- Add 1 jumper to 2nd pld
- Add input latch option
- Add spare footprint

Rev 0.10
- Add 74HCT14 for hysteresis
- Invert BMEMW and BMEMR
- Wire in the flipflop
- wire addr sel to CSIN on PLD
- replace second PLD w/ GAL22V10D
- add trigger flipflop
- eliminate data in buffer
- latches on address bus

Rev 0.15
- Option for compupro-like ws generator

Rev 0.18
- Added option WE-delay circuit
- Flipped polarity of CSIN

Rev 0.20
- Fix the jumpers on the 533!!!
- CAS, RAS not hooked up
- ORG0 output port needs noninverted data
- add 74S03 option

Rev 0.23
- hardwire WE to pld-I11
- hardwire CASD to OP2
- add M/BMEM jumpers

SJ5/SJ6 - do not bridge (i.e. leave unsoldered)
SJ7/SJ8 - bridge pads 1 and 2 on each of these
SJ9/SJ10 - bridge these two solder joins

Memory Bank Selection, in 8K increments

Address Latches

Data Write (Input) Latch

Data Read (output) Latch

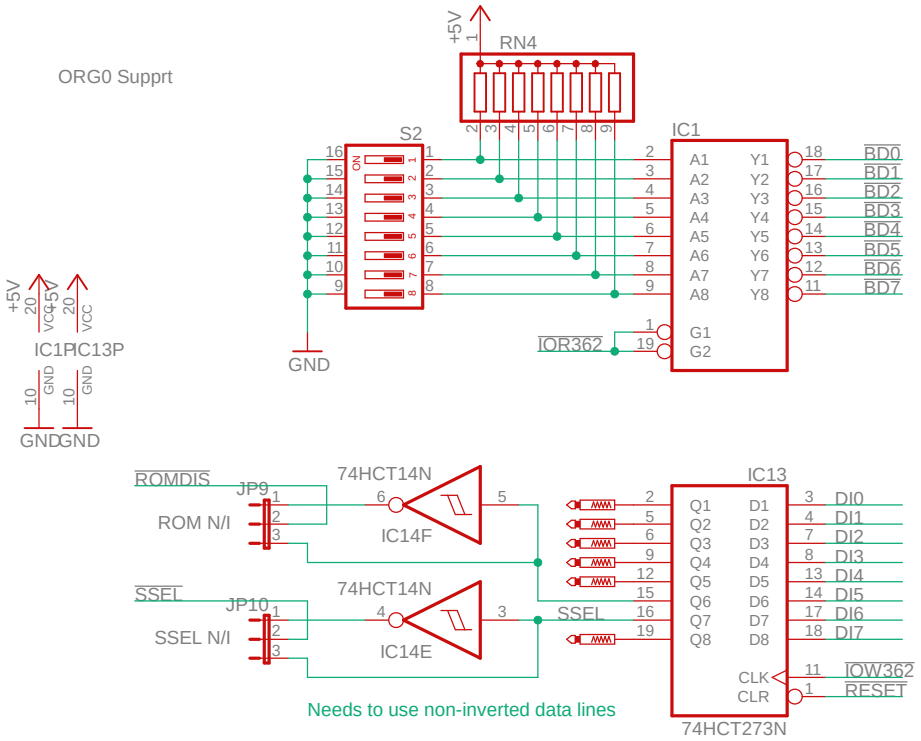
Primary Timing Control PLD

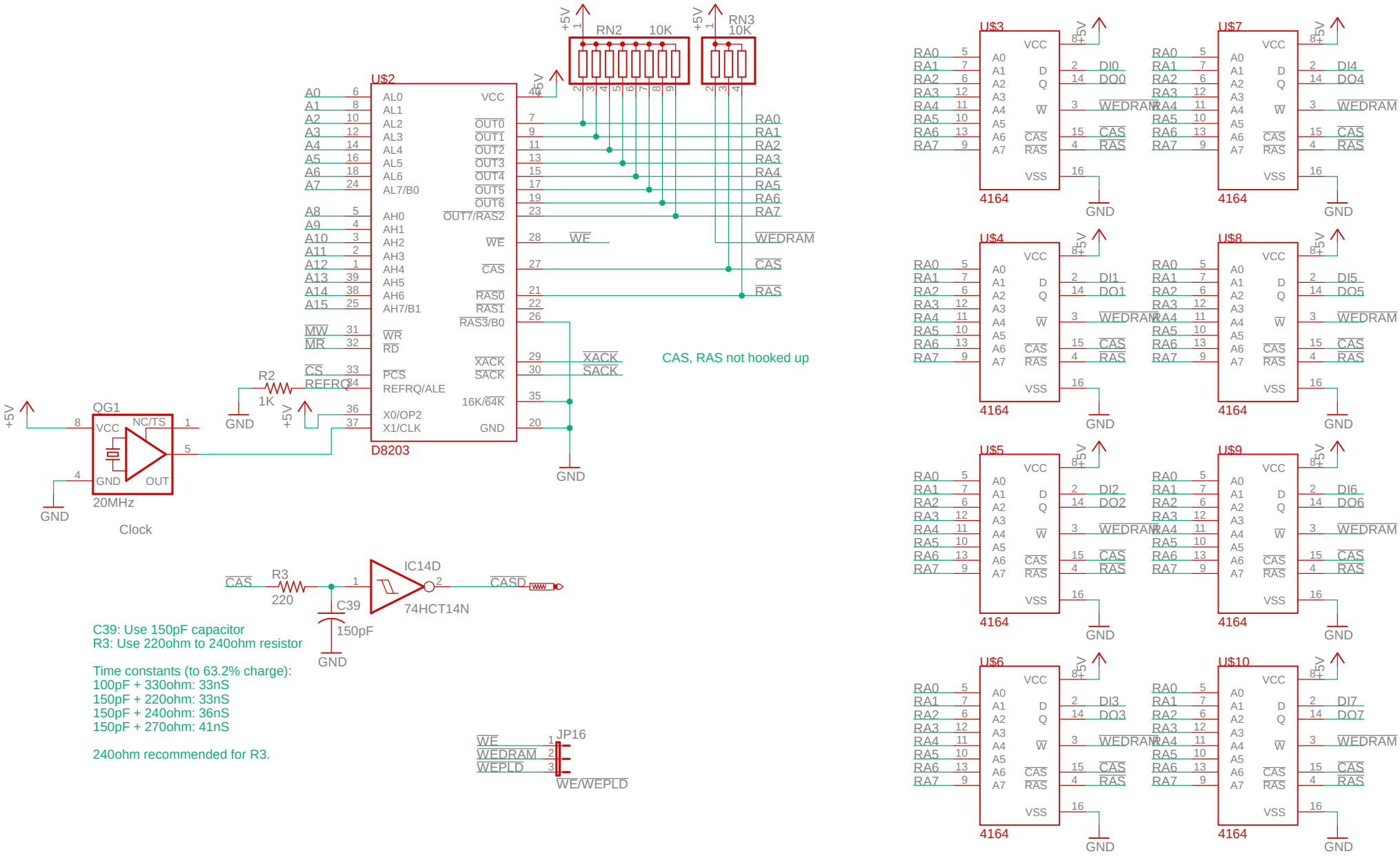
Two spare 74LS123 to use for delays as necessary

Addressing and RW trigger PLD

Eliminate false triggers on MEMR/MEMW from noise on the bus.

Spare FlipFlop


ORG0 Supprt
+5V
RN4
S2
IC1
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
IOR362
GND
IC1P
IC13P
GND
ROMDIS
JP9
ROM N/I
74HCT14N
IC14F
SSEL
JP10
SSEL N/I
IC14E
IC13
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
IOW362
RESET
74HCT273N
Needs to use non-inverted data lines


U$2
D8203
RN2 10K
RN3 10K
+5V
GND
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
AL0 AL1 AL2 AL3 AL4 AL5 AL6 AL7/B0 AH0 AH1 AH2 AH3 AH4 AH5 AH6 AH7/B1
VCC
OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7/RAS2
WE
CAS
RAS0 RAS1 RAS3/B0
WR RD
XACK SACK
PCS REFRQ/ALE
16K/64K
X0/OP2 X1/CLK
RA0 RA1 RA2 RA3 RA4 RA5 RA6 RA7
WEDRAM
CAS
RAS
XACK
SACK
MW MR CS
R2 1K REFRQ
QG1
VCC NC/TS GND OUT
20MHz
Clock
CAS R3 220 C39 150pF
IC14D
74HCT14N
CASD
C39: Use 150pF capacitor
R3: Use 220ohm to 240ohm resistor
Time constants (to 63.2% charge):
100pF + 330ohm: 33nS
150pF + 220ohm: 33nS
150pF + 240ohm: 36nS
150pF + 270ohm: 41nS
240ohm recommended for R3.
CAS, RAS not hooked up
WE
WEDRAM
WEPLD
JP16
WE/WEPLD
U$3
U$4
U$5
U$6
U$7
U$8
U$9
U$10
4164
VCC VSS
A0 A1 A2 A3 A4 A5 A6 A7
D Q W CAS RAS
DI0 DO0
DI1 DO1
DI2 DO2
DI3 DO3
DI4 DO4
DI5 DO5
DI6 DO6
DI7 DO7