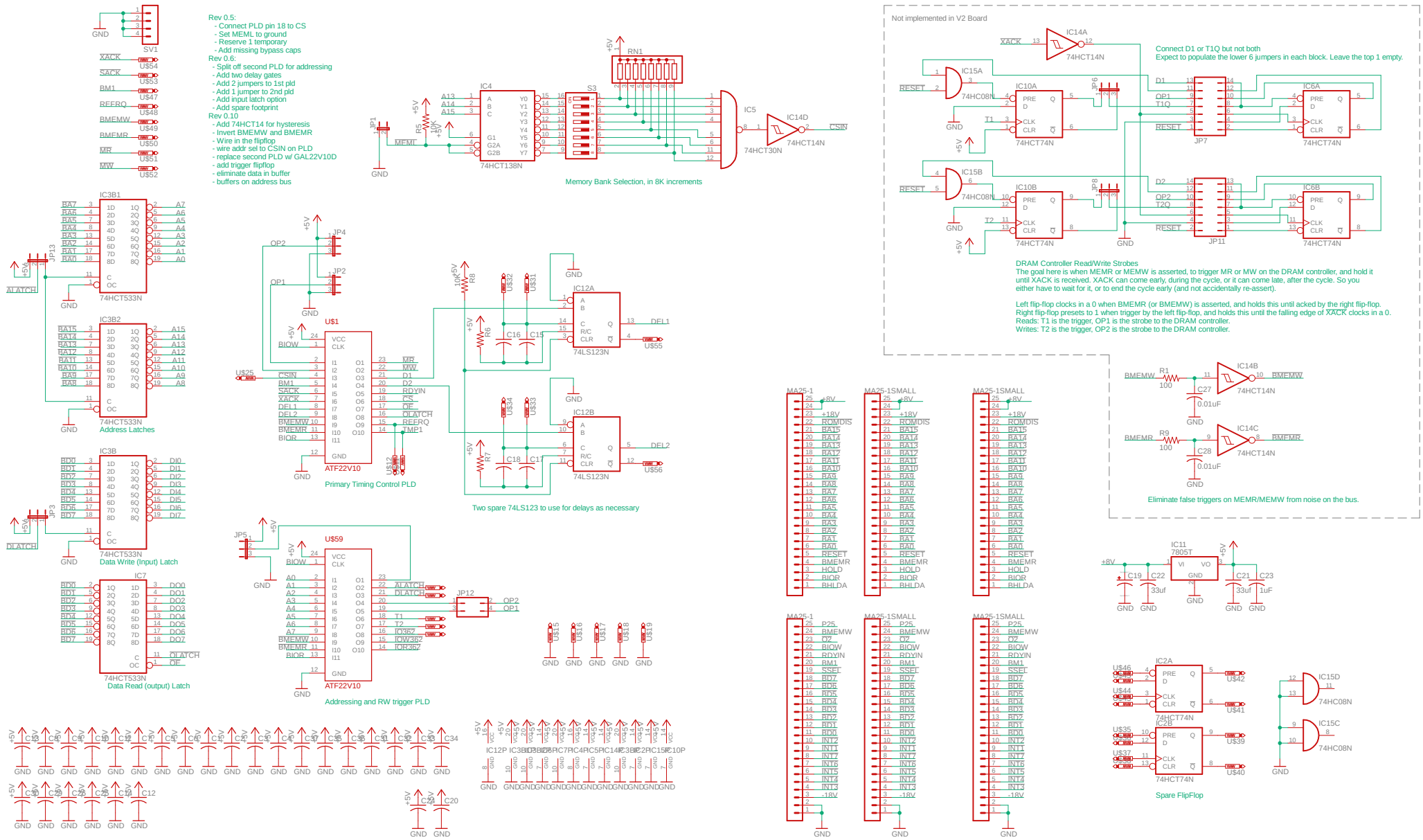
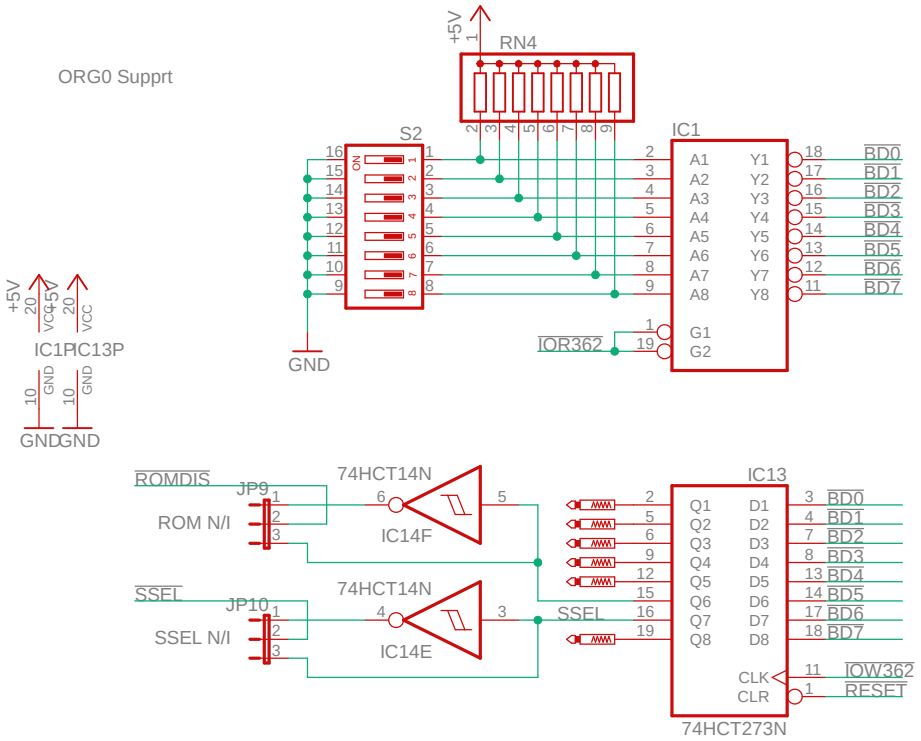
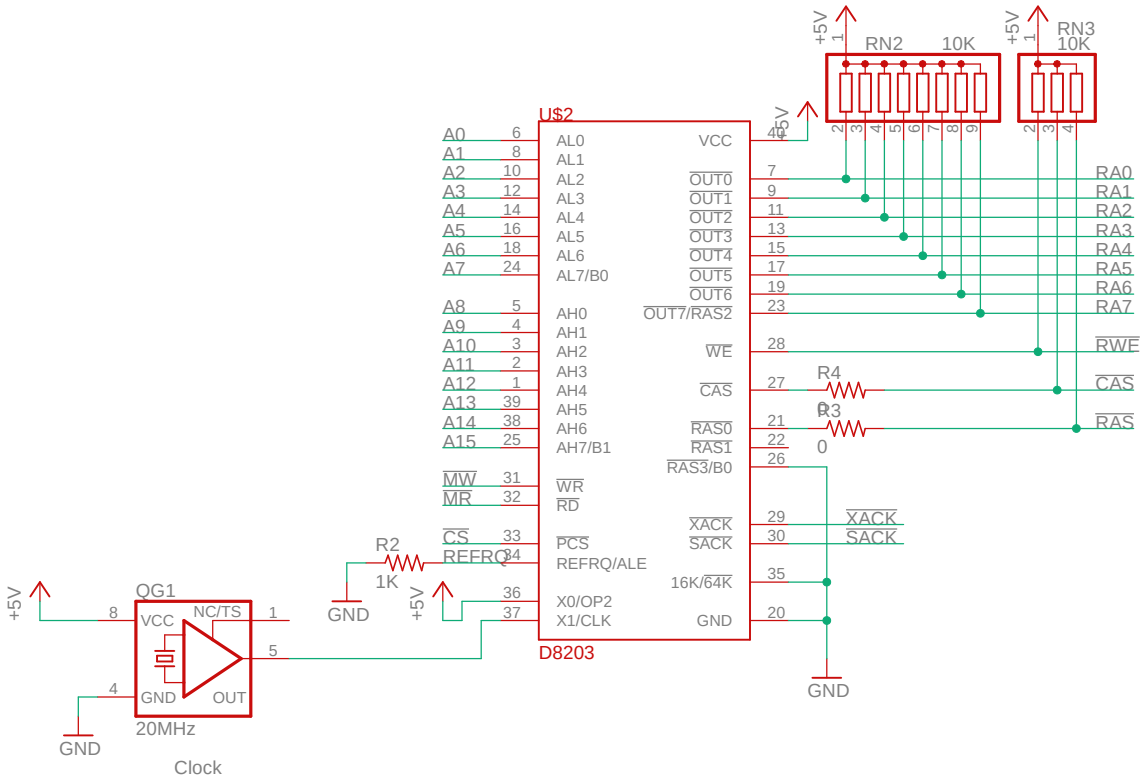
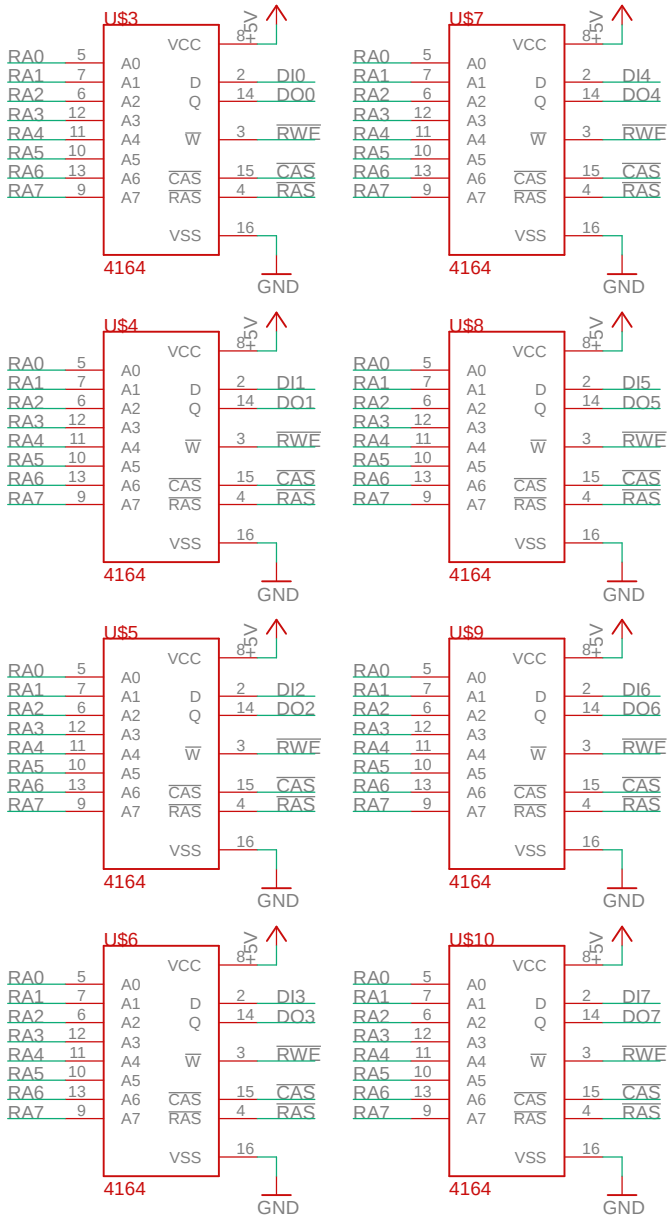

Rev 0.5:
- Connect PLD pin 18 to CS
- Set MEML to ground
- Reserve 1 temporary
- Add missing bypass caps
Rev 0.6:
- Split off second PLD for addressing
- Add two delay gates
- Add 2 jumpers to 1st pld
- Add 1 jumper to 2nd pld
- Add input latch option
- Add spare footprint
Rev 0.10
- Add 74HCT14 for hysteresis
- Invert BMEMW and BMEMR
- Wire in the flipflop
- wire addr sel to CSIN on PLD
- replace second PLD w/ GAL22V10D
- add trigger flipflop
- eliminate data in buffer
- buffers on address bus
Memory Bank Selection, in 8K increments
Not implemented in V2 Board
Connect D1 or T1Q but not both
Expect to populate the lower 6 jumpers in each block. Leave the top 1 empty.
DRAM Controller Read/Write Strobes
The goal here is when MEMR or MEMW is asserted, to trigger MR or MW on the DRAM controller, and hold it until XACK is received. XACK can come early, during the cycle, or it can come late, after the cycle. So you either have to wait for it, or to end the cycle early (and not accidentally re-assert).
Left flip-flop clocks in a 0 when BMEMR (or BMEMW) is asserted, and holds this until acked by the right flip-flop.
Right flip-flop presets to 1 when trigger by the left flip-flop, and holds this until the falling edge of XACK clocks in a 0.
Reads: T1 is the trigger, OP1 is the strobe to the DRAM controller.
Writes: T2 is the trigger, OP2 is the strobe to the DRAM controller.
Address Latches
Primary Timing Control PLD
Two spare 74LS123 to use for delays as necessary
Data Write (Input) Latch
Data Read (output) Latch
Addressing and RW trigger PLD
Eliminate false triggers on MEMR/MEMW from noise on the bus.
Spare FlipFlop


ORG0 Supprt
+5V
RN4
S2
IC1
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
IOR362
GND
IC1P
IC13P
GND
ROMDIS
JP9
ROM N/I
74HCT14N
IC14F
SSEL
JP10
SSEL N/I
IC14E
IC13
IOW362
RESET
74HCT273N


RN2
10K
RN3
10K
U$2
D8203
R4
0
R3
0
R2
1K
OG1
20MHz
Clock
GND
+5V
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RWE
CAS
RAS
XACK
SACK


U$3
U$4
U$5
U$6
U$7
U$8
U$9
U$10
4164
GND
+5V
DI0
DO0
DI1
DO1
DI2
DO2
DI3
DO3
DI4
DO4
DI5
DO5
DI6
DO6
DI7
DO7