EE663: Frequency Synthesizers,Clock and Data recovery

Project Report

Name: Peace Panmei
Entry No: 2023EEM1020

April 5, 2024

Project Name: Design and Implementation of Phase-Locked Loop in Cadence Design Suit.

A phase-locked loop (PLL) is a circuit designed to align the output signal of an oscillator with a reference or input signal, ensuring synchronization in both frequency and phase within a given system. In the synchronized or locked state, the phase error between the output signal of the oscillator and the reference signal is either zero or remains constant. If a phase error accumulates, a control mechanism intervenes to minimize the phase error by acting on the oscillator. In this control system, the phase of the output signal becomes locked to the phase of the reference signal, hence the term "phase-locked loop." The project aims to develop a square-wave output frequency generator, primarily utilizing the PLL as a frequency multiplier, achieved by multiplying the frequency of the reference oscillator

1 Phase Frequency Detector

First, we design the PFD using a masters slave D flip flop implementing it with the help of 3 input and 2 input NAND gates.

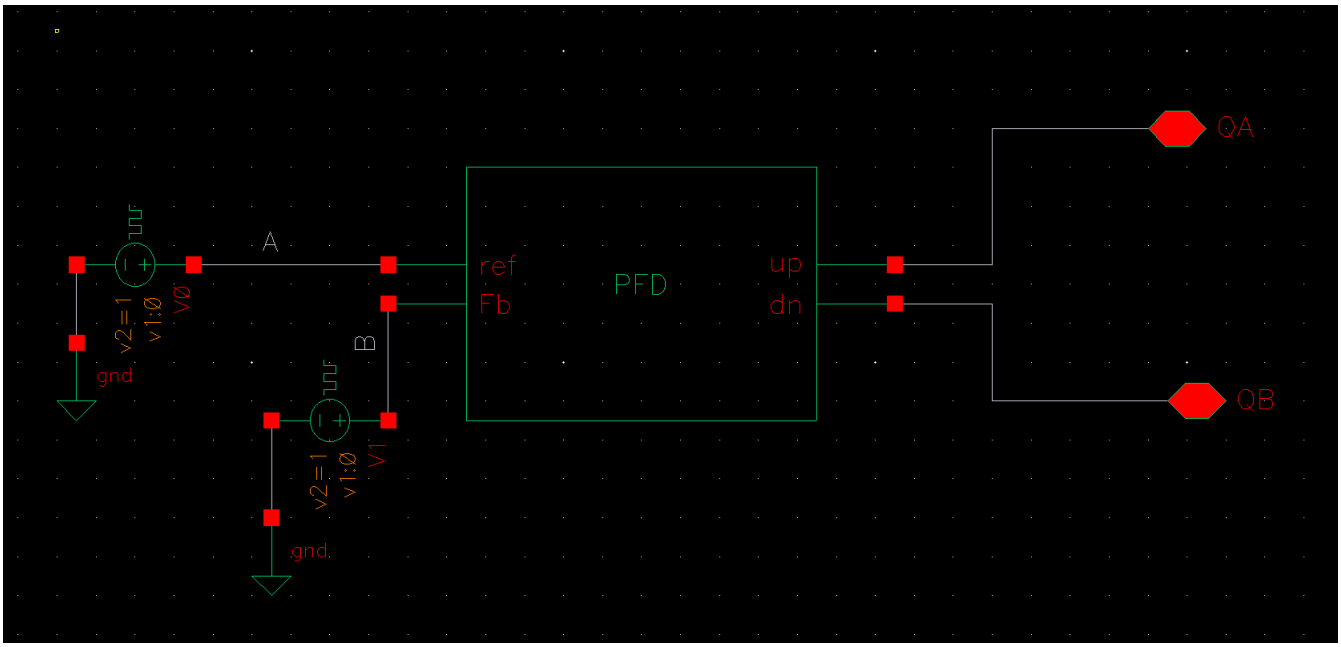

Figure 1: Test Bench for PFD

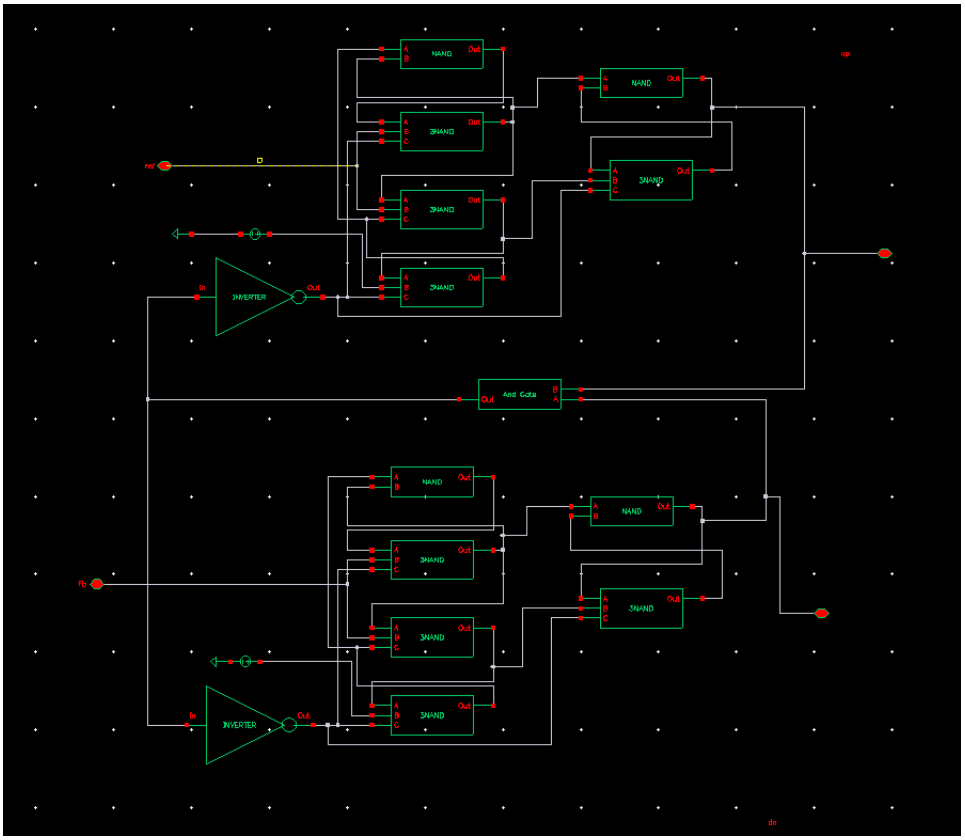

Figure 2: Internal circuitry

The CMOS implementation of the logic gates are shown below

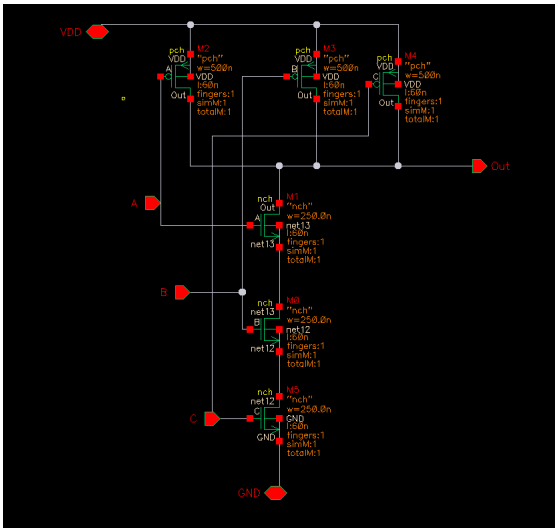

Figure 3: CMOS implementation of 3 input NAND gate

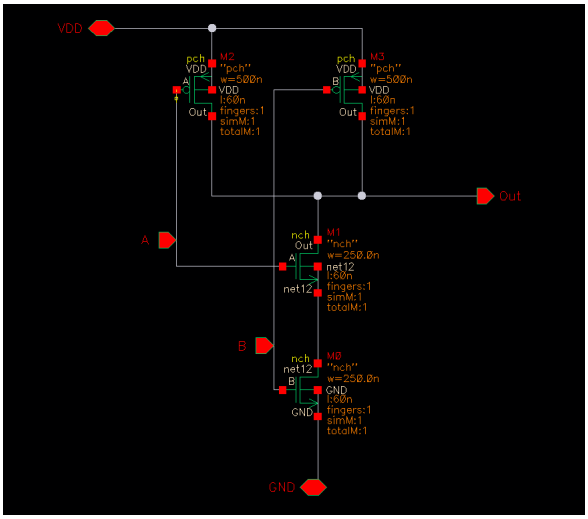

Figure 4: CMOS implementation of 2 input NAND gate

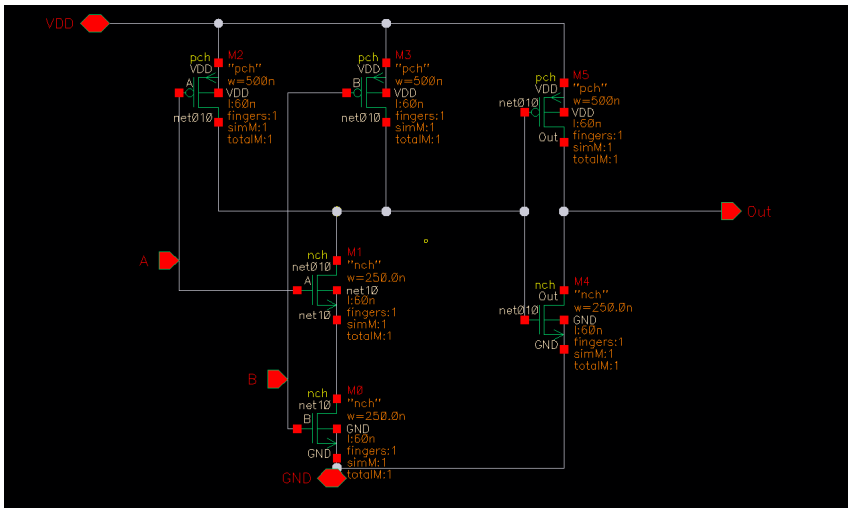

Figure 5: CMOS implementation of AND gate

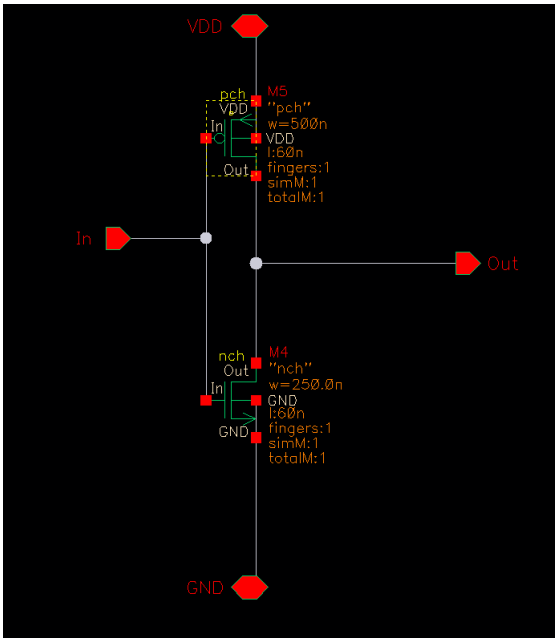

Figure 6: CMOS implementation of Inverter

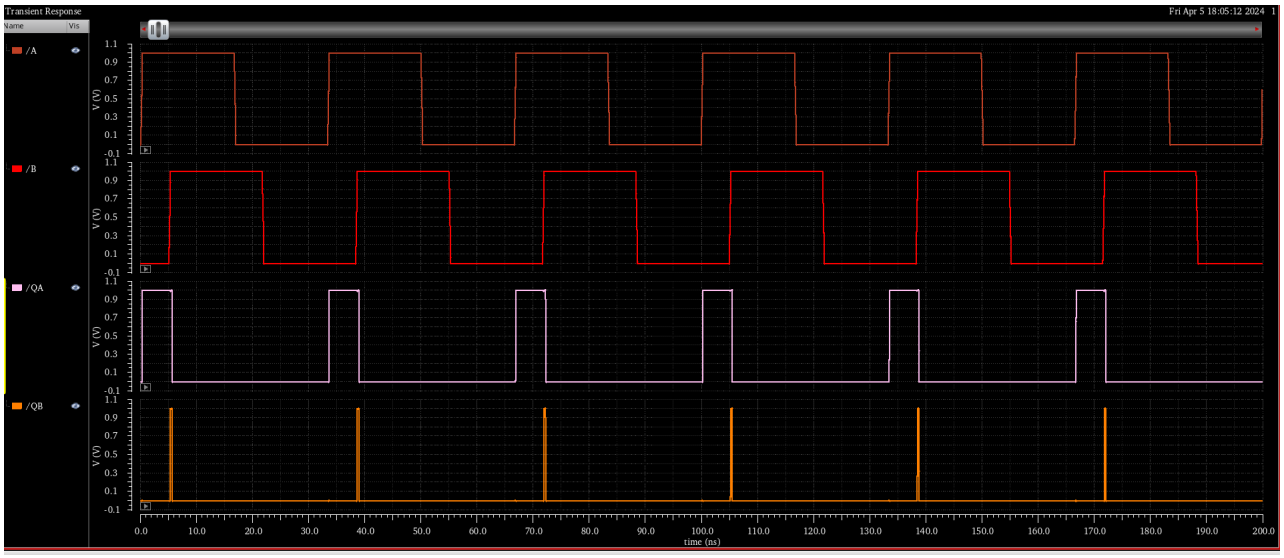

Figure 7: Output of PFD

2 Charge Pump

Charge Pump consist of switches which turns on and off as per the incoming signal of the PFD and the current charges a capacitor to a certain voltage and is sent to the VCO as the Control Voltage

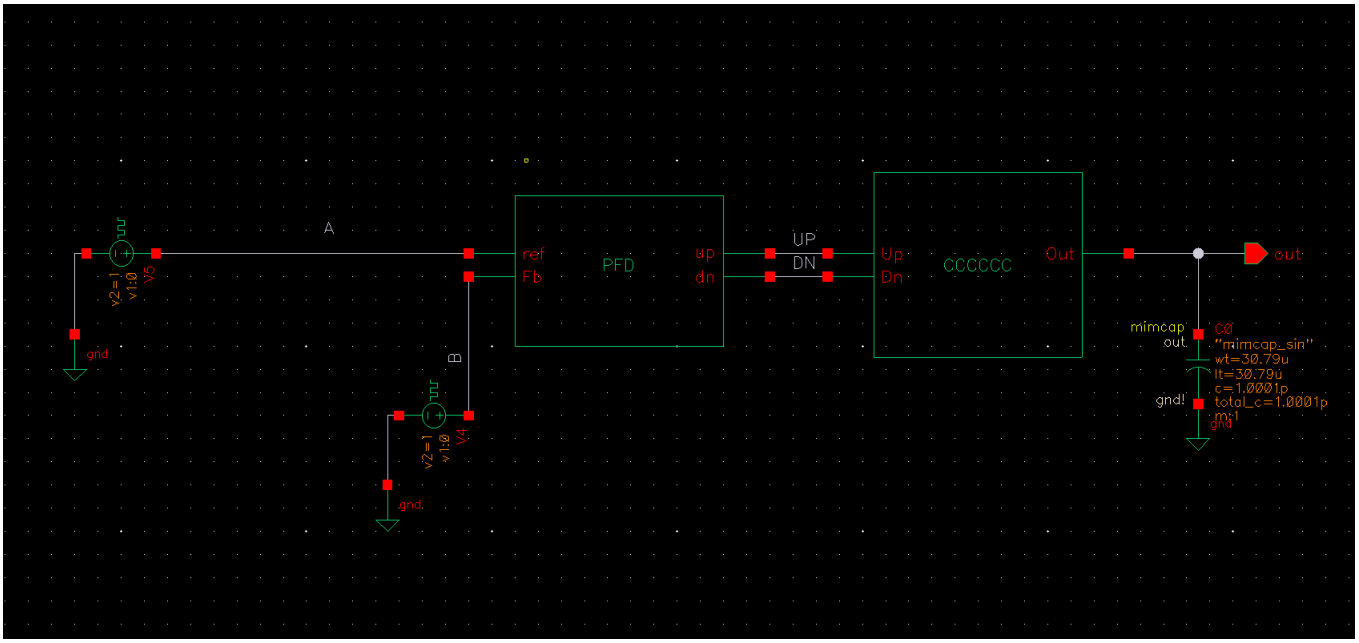

Figure 8: Test Bench for Charge Pump

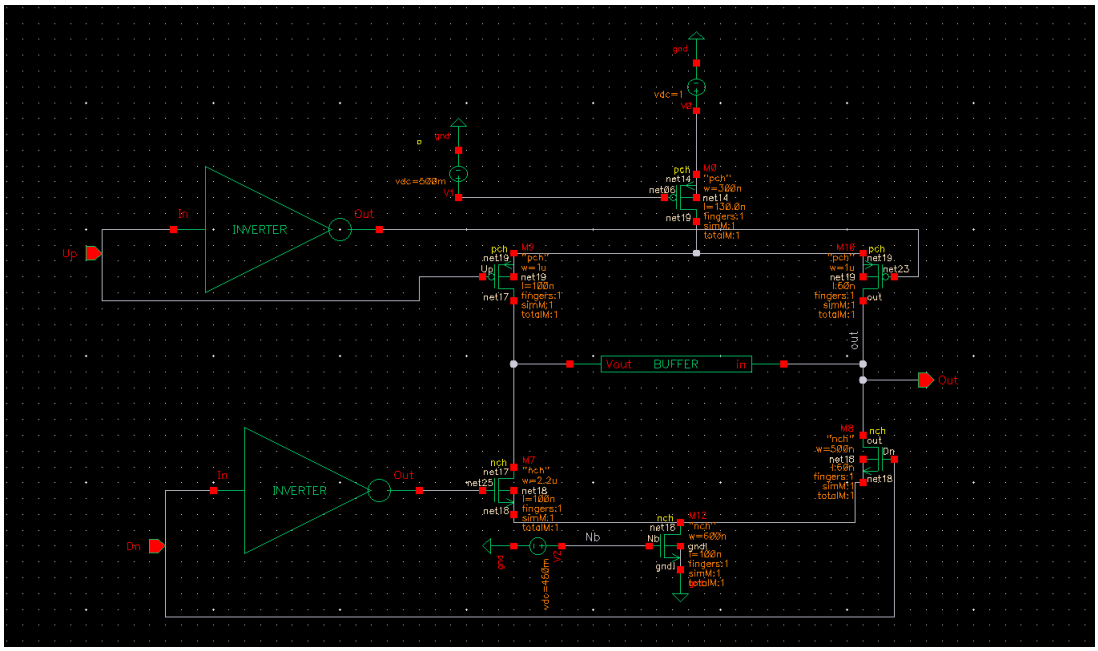

Figure 9: Internal circuitry

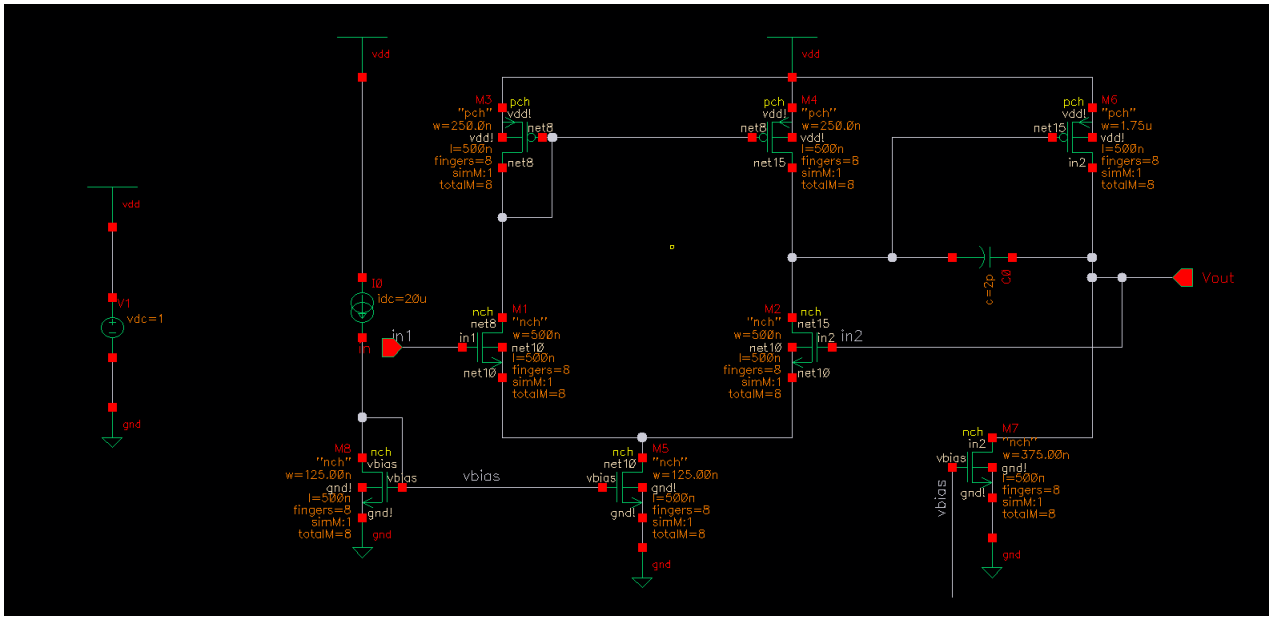

Figure 10: Circuitry of Buffer stage

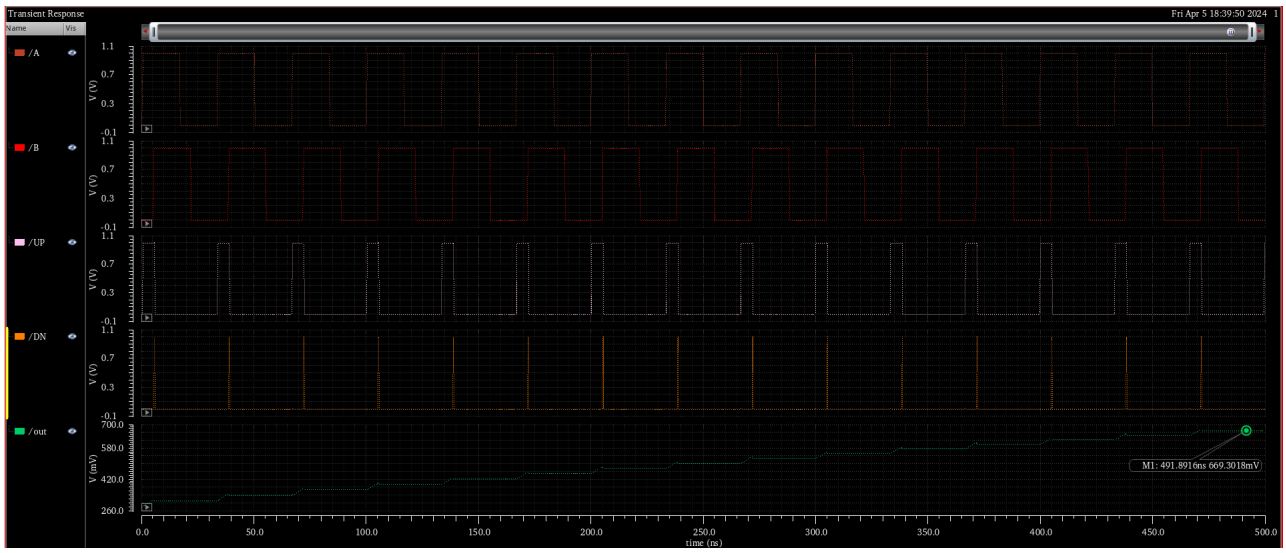

Figure 11: Output of Charge Pump

The charge pump was tested along with the PFD and it can be can see that the charge pump charges the capacitor till 669mv for a transient run duration of 500ns

3 VCO

The VCO acts as the main frequency generator for the PLL. It takes in a voltage and the output frequency changes as per the input voltage. The architecture used here is a current starved VCO which changes the frequency of oscillation by controlling the current.

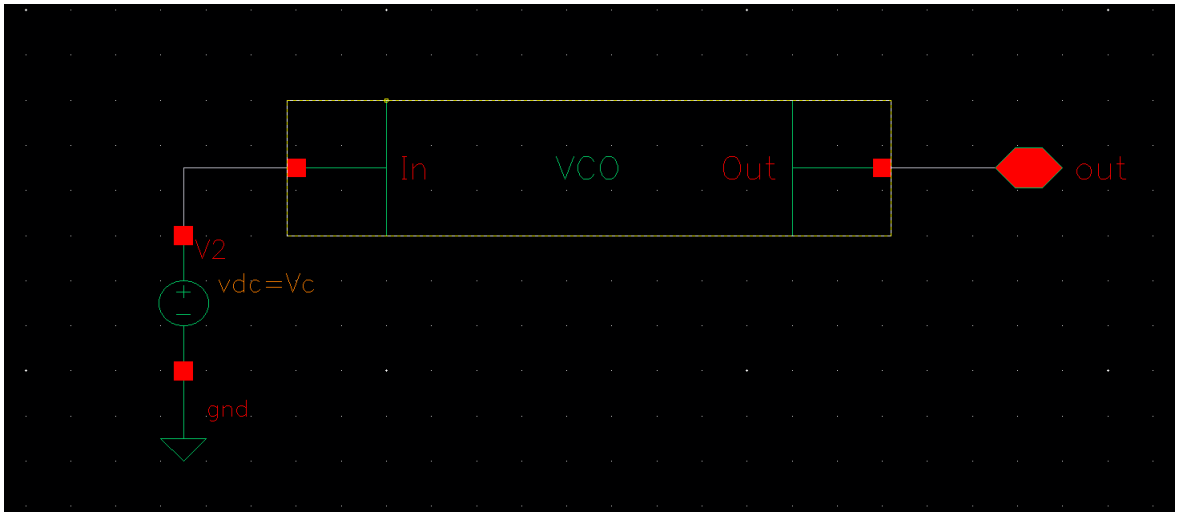

Figure 12: Test Bench for VCO

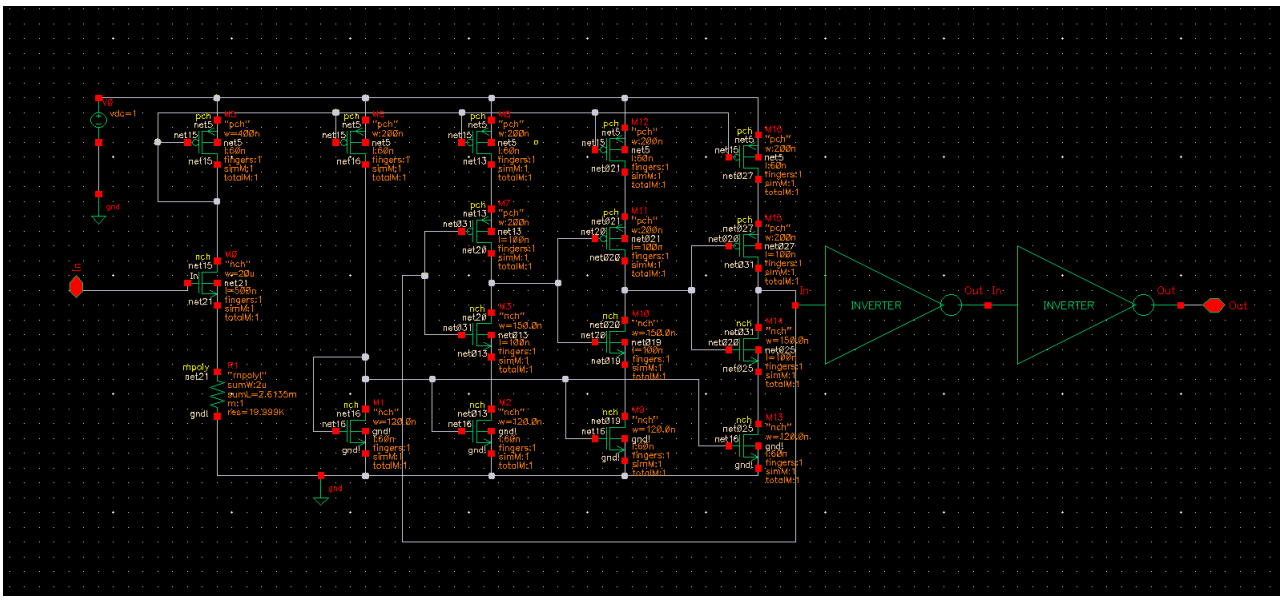

Figure 13: Internal circuitry of VCO

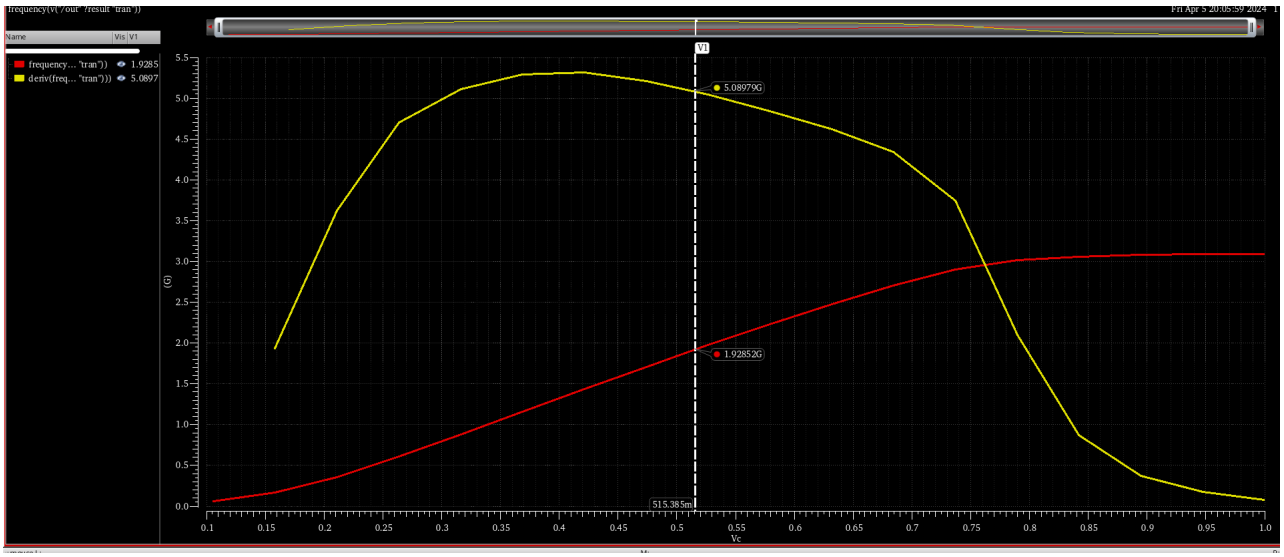

Figure 14: Output of VCO

The output shown in figure 14 is the plot for Vcontrol vs frequency. At around Vc=515mV we get the required oscillation of 1.92GHz and the corresponding Kvco which is the slope of the Vc vs Freqeuncy curve . Here,

$$K_{vco} \approx 5GHz$$

4 Low Pass Filter

Theoretical Calculations:
Given,

$$Frequency_{ref} = 30MHz$$

$$Frequency_{out} = 1.92GHz$$

Assuming a value of phase margin as,$(\phi_m = 60)$

$$b = \frac{C_1}{C_2}$$

$$\omega_z = \frac{1}{R_1 C_1}$$

$$b = 2((\tan\phi_m)^2 + \tan\phi_m\sqrt{1+\tan\phi_m^2})$$

$$b = 12.92$$

Also,

$$w_{uloop} = \sqrt{(b+1)}\omega_z$$

$$w_{uloop} = \frac{\omega_{ref}}{20}$$

$$w_{uloop} = \frac{2\pi \times 3 \times 10^7}{20}$$

$$w_{uloop} = 9.42 \times 10^6 rad/sec$$

$$\omega_z = \frac{w_{uloop}}{\sqrt{b+1}}$$

$$\omega_z = \frac{9.42 \times 10^6}{\sqrt{13.92}}$$

$$\omega_z = 2.52 \times 10^6 rad/sec$$

From Simulation, we find the value of KVCO
$K_{VCO} \approx 5GHz$
Also, the value of the current is found to be around, $I_{cp} \approx 7\mu$A.

$$\frac{K_{VCO}}{N} I_O = \frac{(b+1)^{\frac{3}{2}}}{b} C_1 \omega_z^2$$

$$C_1 = 21.4pF$$

$$\omega_z = \frac{1}{RC_1}$$

Also, b is given by

$$b = \frac{C_1}{C_2}$$

Therefore,

$$C_2 = 1.65pF$$

Now,

$$R = \frac{1}{\omega_z \times C_1}$$

Therefore,

$$R = 18.5kOhms$$

The total capacitance is approximately 23pF

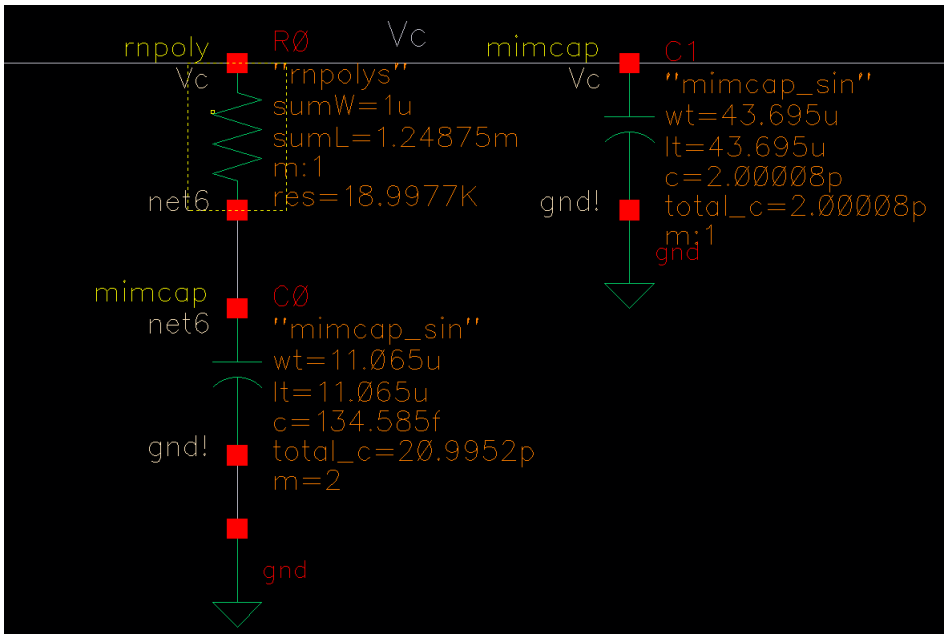

Figure 15: The low pass filter

5 Frequency Divider

The frequency Divider circuit takes an input frequency and gives an output frequency which divides the input frequency into the number of required divisions. Here we employ six stages of $f/2$ divider circuits.

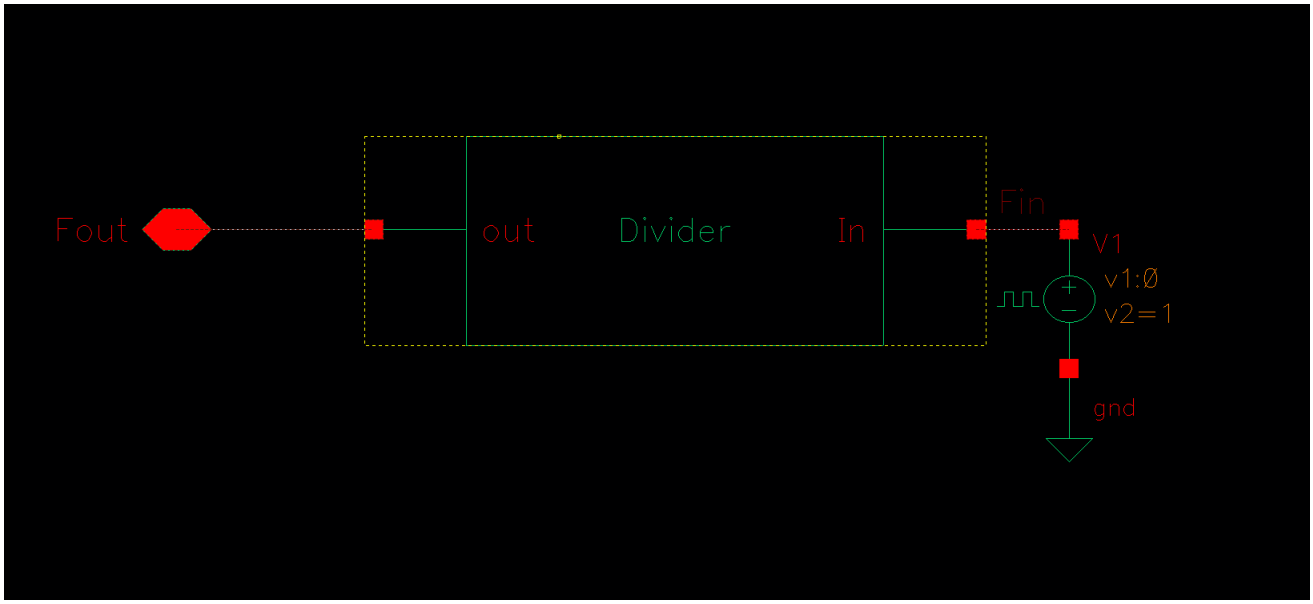

Figure 16: Test Bench for Frequency Divider

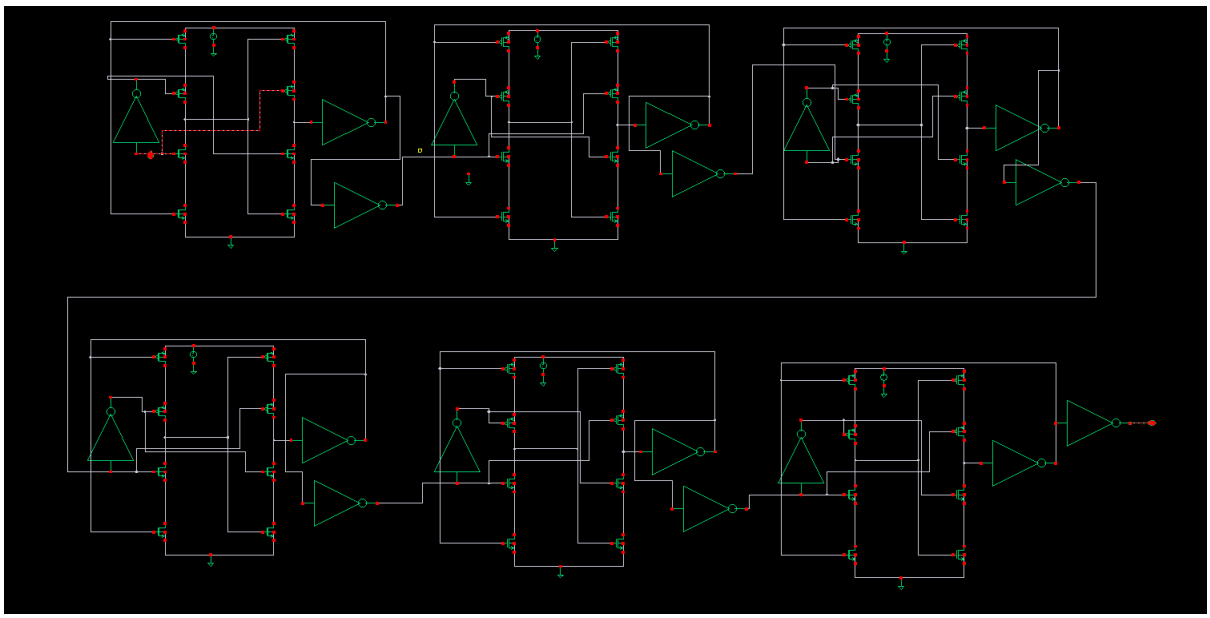

Figure 17: Internal circuitry of Divider

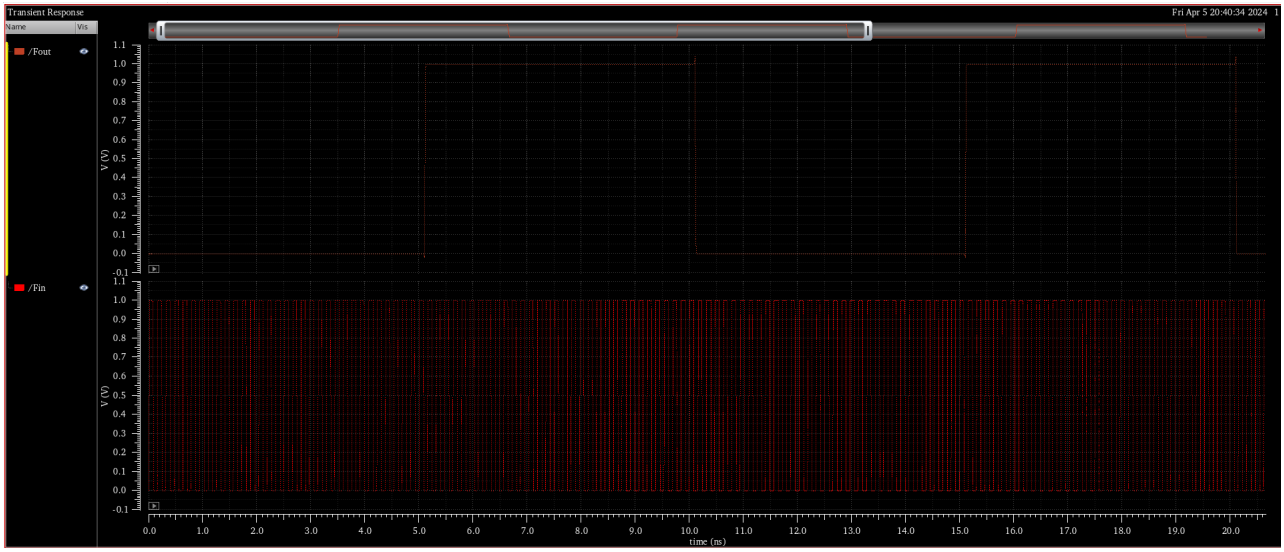

Figure 18: Output of Divider

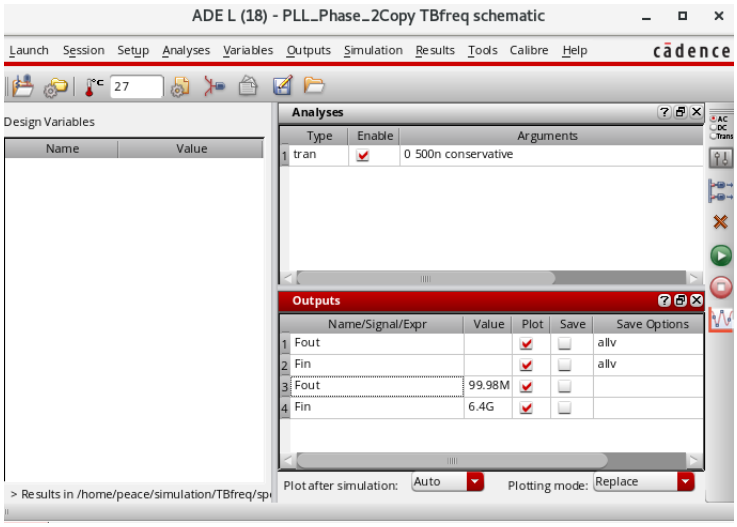

Figure 19: ADEL showing the output and the input frequency of the Divider

We can see from the ADEL window and the output transient silumation that the input frequency of 6.4GHz is divided into 100MHZ which shows the correct division of the input frequency.(i.e 64 divisions)

6 Full Phase Locked Loop

This section contains the block diagram level of the complete Phase Locked Loop. And also the final locked state of the PLL is also shown

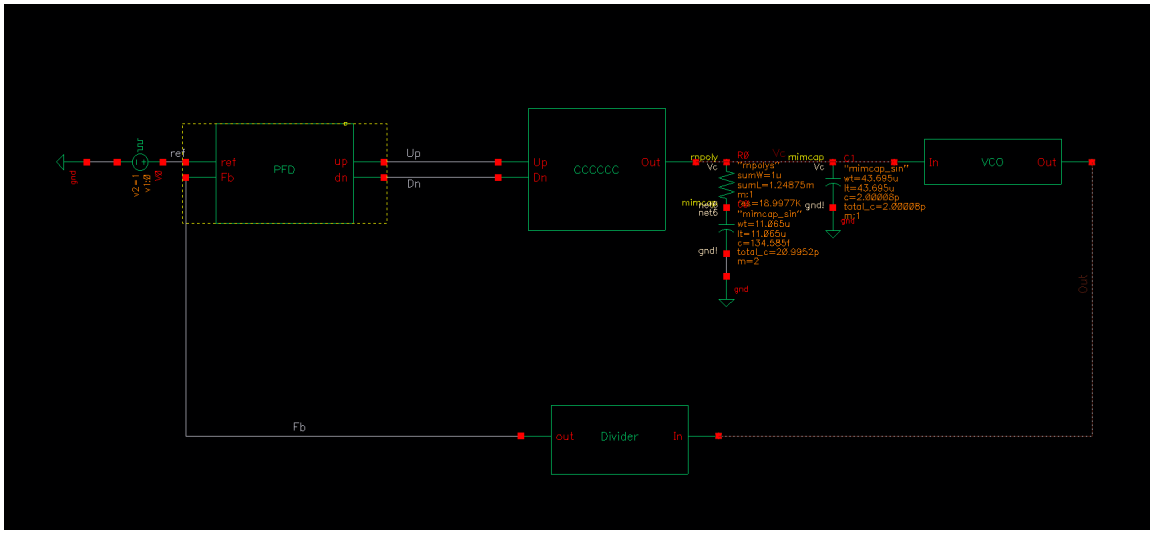

Figure 20: The complete block diagram of the Phase Locked Loop

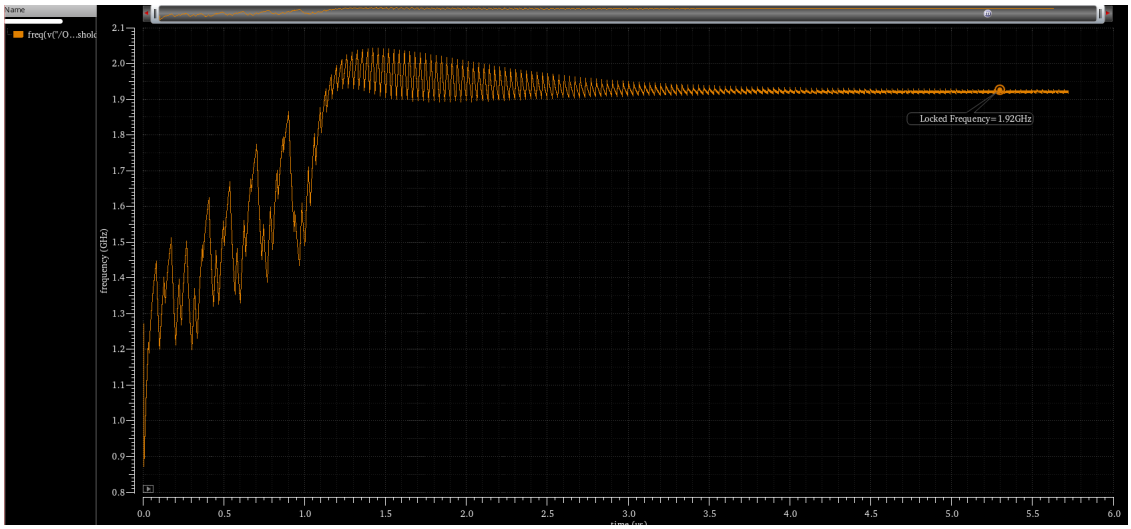

Figure 21: Final Locked state of the Phase Locked Loop

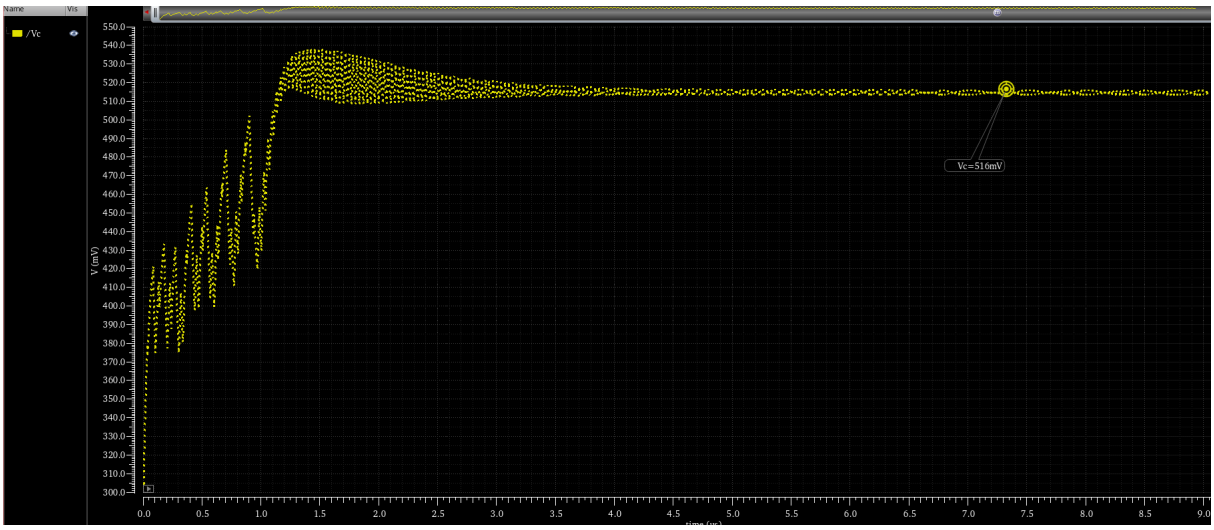

Figure 22: Output of Charge pump(also known as Vcontrol)

It can be observed from figure-21 and figure-22 that the oscillation frequency of the VCO changes as per the V control and the final state of the PLL is locked at 1.92GHz and at Vc=514mV.

7 Conclusion

For the given specification of $Frequency_{ref} = 30MHz$ and $Frequency_{out} = 1.92GHz$, the PLL was designed and implemented at the full transistor level. Also, output of each block was checked and we found that the final locked state is at the required frequency of 1.92GHz.