A Comparator Designed in 65-nm CMOS with Improved Delay Time and Low Supply Voltages down to 0.65V

Peace Panmei
Deoartment of Electrical Engineering
Indian Institute of Technology Ropar

2023eem1020@iitrpr.ac.in

***Abstract*—This document contains two types of Comparator designed in the 65-nm complementary metal-oxide-semiconductor process. First, the conventional latch type with cross coupled inverters and an a single tail is presented, followed by an improved version with modified latch. The improved version presented here provides a faster operation with delay greatly reduced and having an optimal performance down to low supply voltages till 0.65V.**

***Index Terms*—Comparator, complementary metal-oxide-semiconductor process, low supply voltage**

I. Introduction

Newest technologies in the semiconductor industry requires higher packing density of chips, thus, requiring lower gate length technologies. This leads to CMOS technologies suffering from low supply voltage. It leads to headroom issues affecting dc performance negatively. However, shorter gate length decreases the parasitics involved and thus ac performance gets better. Gate leakage due to tunneling is also problem for short channel transistors limiting the ability to minimize offsets, thus proving, a challenging task for developing robust circuits with stacking a large number of transistors.

The comparator is a circuit which plays a very important role in the conversion of signals from analog domain to digital domain. The basic operation of a comparator is that the circuit compares two analog signals and gives an output which can be treated as logic high and low. The logic levels determine the polarity of the difference of the input applied. The basic comparator uses a cross-coupled inverters employing the concept of latch and positive feedback for speedy decision making. Application of such architecture is found in fash ADC due to their fast decision making capability. Also, there are certain memory application such as SRAM and they act as the sense amplifier for the logic levels of the memory cells.

II. The conventional Comparator

A conventional comparator is shown in figure:1. The circuit works on the principle of set and reset. Initially, the clock is set to GND and the output is set to VDD. In this phase, N6 remains off and P2 and P3 are turned on(PMOS turns on at logic zero clock) thus pulling both OUT and OUTBAR to VDD. This defines the initial condition requirement for the circuit to have a logic high and reset the comparator.

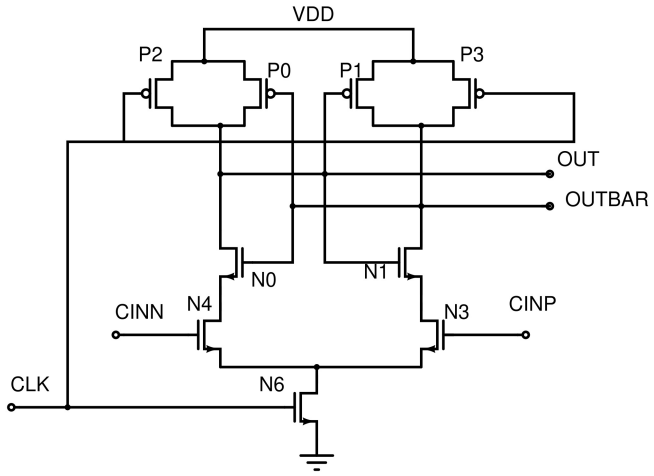

Fig. 1. A conventional Comparator

A. Operation

The operation of the comparator, i.e. , the comparison phase is done by supplying inputs at both CINN and CINP. Now, the clock goes to logic high(CLK=VDD) and assuming a condition, $CINP > CINN$, the circuit operation proceed as follows. Since $CINP > CINN$, N3 will pull down OUTBAR to $VDD - Vt_p$ at a faster rate than N4 will pull down OUT to the same voltage level. This initiate regerenation and P0 will turn on before P1 and OUT-OUTBAR is the amplified signal of CINP-CINN. Thus, OUT is pulled to VDD and OUTBAR will be pulled down to GND. When the condition of input is CINN¿CINP, the circuit will work vice versa. P1 turns on before P0 and the regenerative latch pull OUTBAR to VDD and OUT to GND. Such circuit often have an advantage in robustness and against noise and mismatch due to the room for using large input transistors, N2 and N3.

The switching is not affected by the capacitances of the input transistors because the output is not directly connected to the input transitors. Taking a case where, OUT goes to VDD, N0 is turned off and thus OUT is being isolated from the N4, allowing large size transistors for input signals. But the disadvantages of this architecture is that the circuit has a high delay due to the transistors stack on top of the other. Thus, a need for lowering delay arises and the following section contains a similar type of comparator with modified latch to tackle the delay of the circuit.

B. Simulation Result

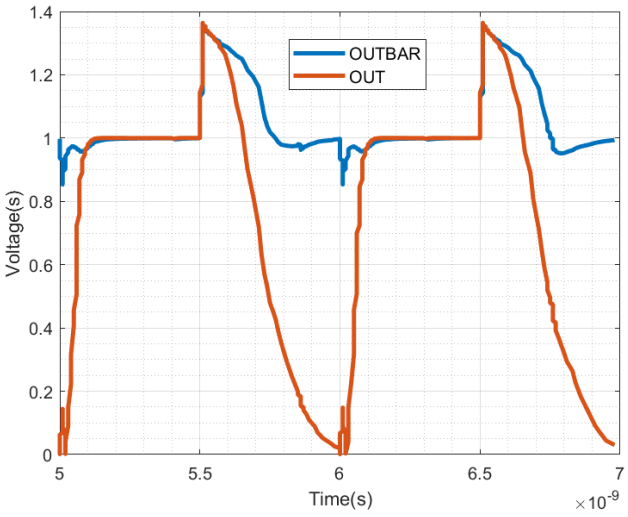

Fig. 2. Transient Simulation result of conventional comparator

III. Comparator with Modified Latch

This section presents the modified latch of the circuit in figure:3. Here, the latch is expanded into multiple paths between the supply rails, namely around N0, N1, P0, P1, and P5 and consequently, transistors N0 and N1 are turned on. In the comparison phase, similar to the prior architecture, the initial condition is set by keeping both OUT=VDD,OUTBAR=VDD and FB=GND,FBBAR=GND. Also, with N2 and N3, the input transistors, P0 and P1 are turned on, sets up a load for the the transistors to certain working points thus, privading a sufficient gate-source voltage in contradition to the conventional comparator. Regeneration is done with N0, N1, P0 and P1. Here also, there is no effect of the parasitic capacitances from input transistors and also provides a high input impedance.

A. Operation

First, the reset phase is initiated by giving CLK=GND. Now, N6 turns off and P2 and P3 turns on pulling both OUT and OUTBAR to VDD by P2 and P3 respectively and consequently, both P4 and P5 remains off. Also N4 and N5 are on and pulls FB and FBBAR to GND. This causes P1 and P0 to turns on and contribute to pulling OUT and OUTBAR to VDD. The comparison phase starts when CLK

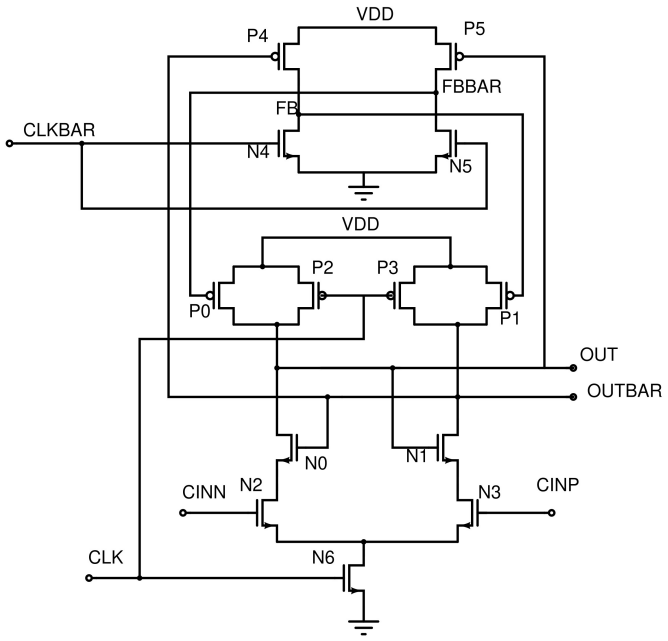

Fig. 3. A Comparator with modified latch

goes high, i.e., CLK=VDD. N6 will turn on and P2, P3 ,N4 and N5 will also goes off. Initially OUT=OUTBAR=VDD and FB=FBBAR=VSS and assuming a condition for startup as $CINP > CINN$ the analysis is done subsequently. Here, N1 and N2 are initially on and with the assumed condition that $CINP > CINN$, N3 pulls down OUTBAR at a faster rate than N2 will pull down OUT. N0 and N1 also contribute to a small amount of positive feedback. Complete feedback starts when p4 starts conducting and charges FB towards VDD but N4 and N5 remains off. Since FB is charged to VDD, P1 turns off but P0 keeps conducting because OUT is being pulled to VDD. P5 remains off (since OUT=VDD) and FBBAR is still near GND. Now, N1 is on(OUT=VDD),P4 is on(since OUTBAR=GND) and P5 is also on(since FBBAR=VDD) and N0 is off(since OUTBAR=GND), P1 is off(since FB=VDD) and P5 is off(since OUT=VDD). Thus, OUT remains at VDD and OUTBAR goes to GND and the output determines when $CINP > CINN$ and give a logic level high.The decision time starts when the voltage level of CLK has reaches 50 percent of VDD. The vice versa happens when $CINP < CINN$ and OUT will be pulled to VSS and OUTBAR TO VDD.

B. Simulation Result

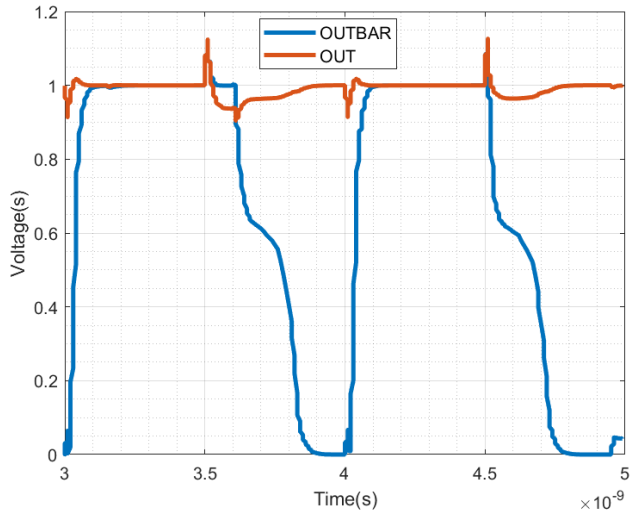

Fig. 4. Transient simulation results of Comparator with modified latch

IV. Delay Analysis

Simulation has been done for finding the decision making speed of the comparator. At higher supply voltages, both the comparator perform equally well with supply with lower delay due to the similarities in the design. But when the supply goes down to around 0.65V the modified latch comparator shows much better results.

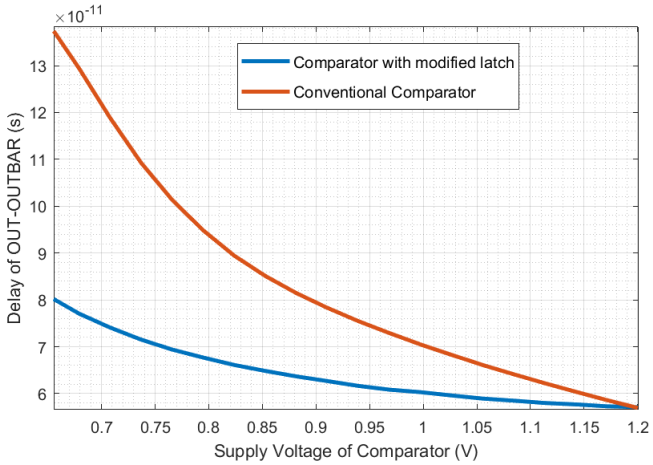

Fig. 5. Comparison of Delay for conventional comparator and the comparator with improved delay

Acknowledgment

I would like to express my utmost gratitude and thanks towards my supervisor Prof. Devarshi Das for giving me an opportunity to study and work in this term project. I would like to extend my heart-felt appreciation for the determination and help in this term project. I would also like to acknowledge and extend my heartfelt gratitude to my senior research members and peers for their unending support and valuable suggestions in the ongoing term project.

References

[1] B. Goll and H. Zimmermann, "A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V," in *IEEE Transactions on Circuits and Systems II*: Express Briefs, vol. 56, no. 11, pp. 810-814, Nov. 2009, doi: 10.1109/TCSII.2009.2030357.

[2] S. Srivastava and N. Gupta, "Analysis and Design of Low Voltage Low Power Inverter Based Double Tail Comparator," *2017 International Conference on Innovations in Control, Communication and Information Systems* (ICICCI), Greater Noida, India, 2017, pp. 1-4, doi: 10.1109/ICICCIS.2017.8660927.

[3] X. Yu, "Investigation on novel comparator design," *2022 IEEE 2nd International Conference on Data Science and Computer Application* (ICDSCA), Dalian, China, 2022, pp. 638-645, doi: 10.1109/ICDSCA56264.2022.9988168.

[4] Carusone TC Johns D Martin KW. Analog Integrated Circuit Design. 2nd ed. John Wiley & Sons; 2012.