

A comparative study on different OP-AMP compensation techniques

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by

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Declaration

I declare that this written submission represents the analysis of Op-Amp compensation techniques. I have adequately cited and referenced the original sources. I also declare that no falsified interpretation has been done and I have adhered to all the ethics and principles of academic integrity. Further, if any violation of the aforementioned statement is found I will be held responsible and I fully understand the consequences.

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Abstract

An Op-amp with different compensation technique are presented herein. Compensation techniques are methods that are added in the Op-amp circuitry to improve the frequency response. By adopting different methods of compensations, requirements for various application are made possible. First, the technique of the conventional miller compensation using a single miller capacitor is presented. This technique creates an instability in the system, for which another method of compensation, in addition to the miller capacitor is added. This added circuit is also known as the voltage buffer circuit. Both these methods has been implemented and simulated in 65nm tecnology.

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Chapter 1

Introduction

An Operational Amplifier is an analog CMOS circuit which finds many application in the field of microelectronics. One such application is the the use of Op-Amp as a feedback system. Such usage in a feedback system requires for the Op-amp to have high stability without affecting the gain offered by the circuit. This report contains the analysis of a compensated Op-amp using a single Miller Capacitor. The Op-amp under study is a two stage Op-amp which consist of a differential stage and a common source stage. This cascading of two stages is to increase the overall gain of the Op-amp. But, such cascading of multiple stages results in the increase of the number of Poles and new Zeroes being introduced in the system. For this we use a compensation technique,namely the Miller Compensation. Even with introducing a compensation such as a miller capacitor, we encounter another problem of a zero arising due to the added capacitor which in turn affects the stability. One solution to overcome this is the introduction of a buffer stage. Detailed analysis and comparisons are shown in later stages in chapter 2 and 3 .

Chapter 2

An Uncompensated Op-Amp

An uncompensated Op-Amp [1], as shown in figure 2.1, consist of a differential stage and an output Common stage. M1, M2, M3 and M4 made up the first stage, where M1 and M2 are the differential pair and M3 and M4 are the respective loads. The second stage consists of M6 and M7 in a Common source topology with M5 as the load.

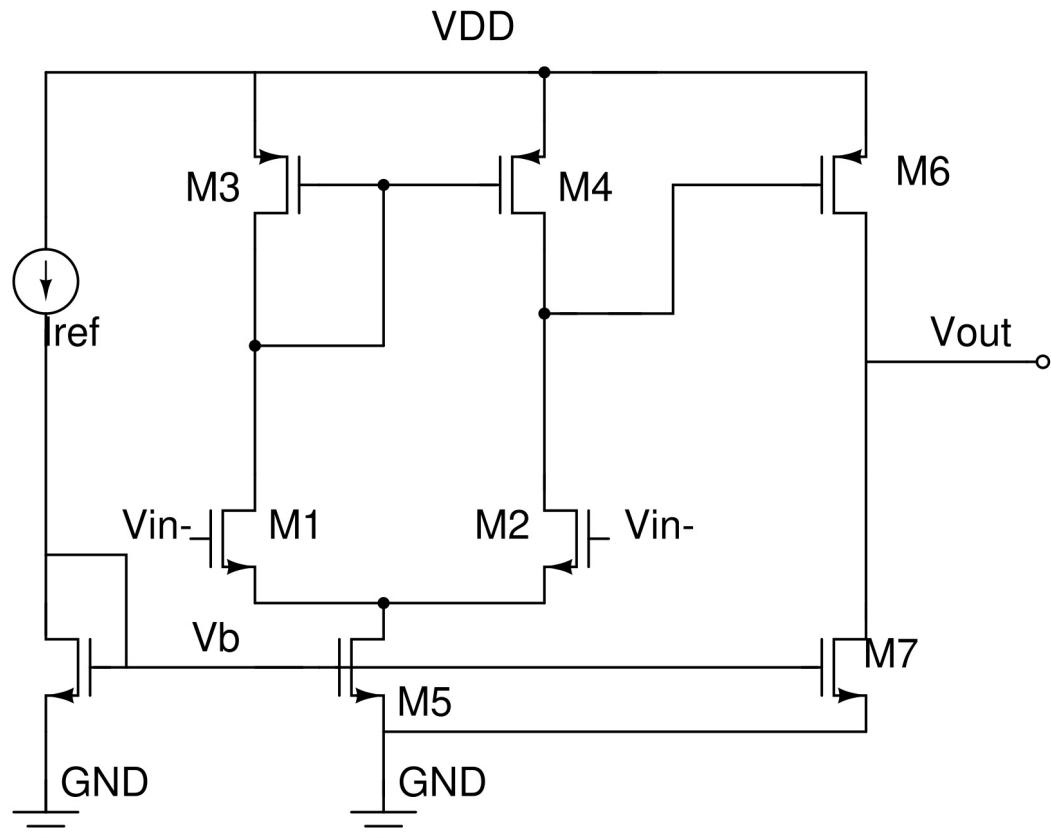


Figure 2.1: Uncompensated Opamp

2.1 Small signal analysis

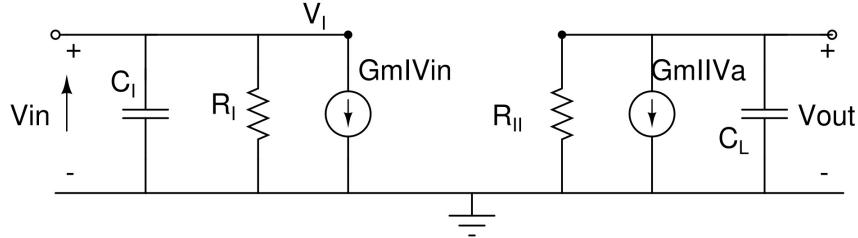


Figure 2.2: Small signal model of non compensated Opamp

At V_I,

$$\frac{V_I}{R_I} + \frac{V_I}{\frac{1}{sC_I}} = -gm_I Vin \quad (2.1)$$

Here,

$$R_I = r_{o2} || r_{o4}$$

And C_I is the parasitic capacitances involved with the first stage. Similarly at V_{out},

$$V_I = \frac{-gm_I Vin}{\frac{1}{R_I} + sC_I} \quad (2.2)$$

$$\frac{V_{out}}{R_{II}} + \frac{V_{out}}{\frac{1}{sC_{II}}} = -gm_{II} V_I \quad (2.3)$$

Here,

$$R_{II} = r_{o6} || r_{o7}$$

And C_{II} is the parasitic capacitances involved with the second stage. from 2.1 and 2.2 we have

$$V_{out} = \frac{gm_I gm_{II}}{\left(\frac{1}{R_I} + sC_I\right)\left(\frac{1}{R_{II}} + sC_{II}\right)} \quad (2.4)$$

Therefore,

$$P1 = \frac{-1}{R_I C_I} \quad (2.5)$$

$$P2 = \frac{-1}{R_{II} C_{II}} \quad (2.6)$$

The figure below 2.3 shows the frequency response of the uncompensated system.

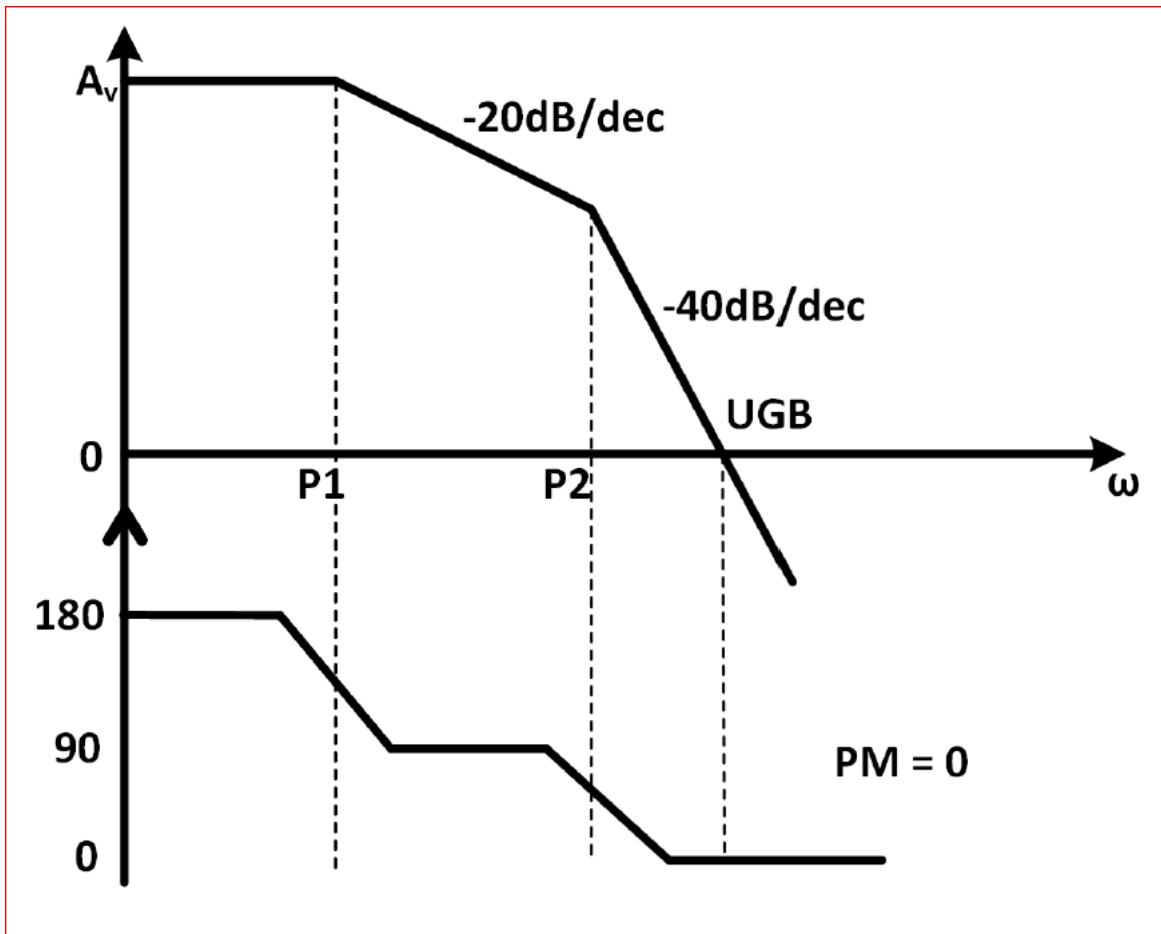


Figure 2.3: Frequency response of Opamp without compensation [2]

As seen in figure 2.3 the phase plot suffer a drop of a total 180° due to the two poles P1 and P2. This is because the Phase crossover frequency comes before reaching Gain crossover frequency. This affects the stability of the feedback system because the Phase margin available for the feedback system goes to zero degree.

In order to minimize the effect of the the double poles affecting the phase margin, the poles can be moved in such a way that P1 moves towards origin and P2 move away from the origin. This can be achieved by increasing the capacitance C_I of first stage and also decreasing the value of C_{II} and R_{II} . For achieving the required changes in the system, we introduced the method of pole splitting using a Miller Capacitor[shown in figure3.1].

Chapter 3

Compensation of Op-Amp

3.1 The Miller Compensation

For splitting the poles of the Op-amp, an additional capacitor C_c is added between the first and the second stage of the Op-amp. It can be observed in figure3.1 that the miller capacitor is added between the drain of M3,M4 and the drain of M6,M7. Figure 3.1 shows the compensated Op-amp.

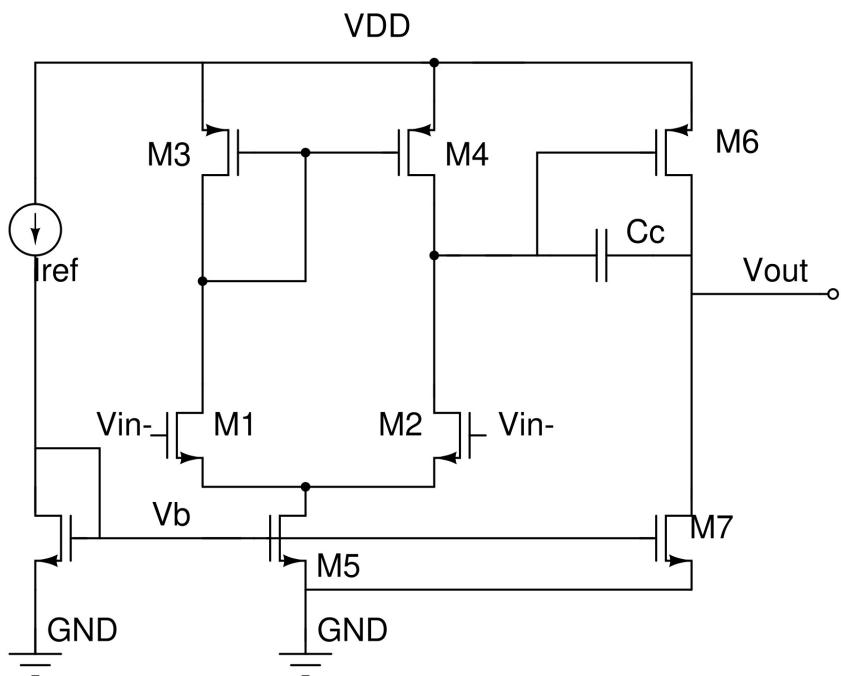


Figure 3.1: Miller Compensated Op-Amp

The small signal model for the compensated op-amp is shown in figure3.2.

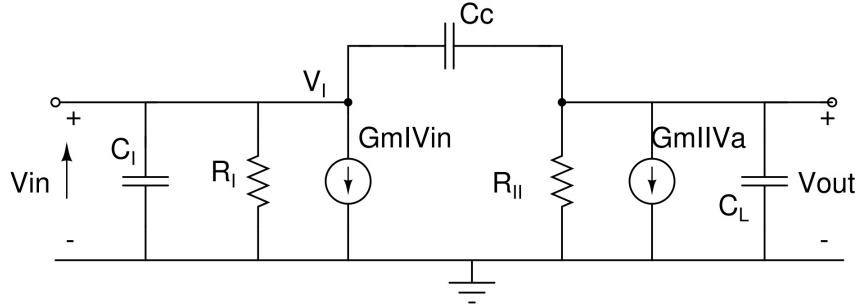


Figure 3.2: Small signal model of miller compensated Op-amp

The resulting transfer function as derived in [2] for the small signal model is,

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}g_{mII}R_I R_{II}(1 - sC_c g_{mII})}{1 + s[R_I(C_I + C_c) + R_{II}(C_{II} + C_c) + g_{mII}R_I R_{II}C_c] + s^2 R_I R_{II}[C_I C_{II} + C_c C_I + C_c C_{II}]}$$

Assuming poles to be far apart from each other, the poles can be written as

$$P1* \sim \frac{-1}{g_{mI}R_I R_{II}C_c} \quad (3.1)$$

And,

$$\begin{aligned} P2* &\sim \frac{-g_{mII}C_c}{C_I C_{II} + C_{II} C_c + C_I C_c} \\ &\sim \frac{-g_{mII}}{C_c} \end{aligned} \quad (3.2)$$

] if

$$C_{II} \gg C_I$$

and,

$$C_c \gg C_I$$

Also,

$$Z1 = \frac{-g_{mII}}{C_c}$$

Here, C_I is the input capacitance, C_{II} is the output capacitance, $Z1$ is the zero introduced by the miller capacitance and C_c is the Miller capacitance.

Also, the DC gain is given by

$$Ao = g_{mI}g_{mII}R_I R_{II}$$

where,

$$g_{mI} = g_{m1} \quad \& \quad g_{mII} = g_{m6} \quad \& \quad R_I = r_{o2}||r_{o4} \quad \& \quad R_{II} = r_{o6}r_{o7}$$

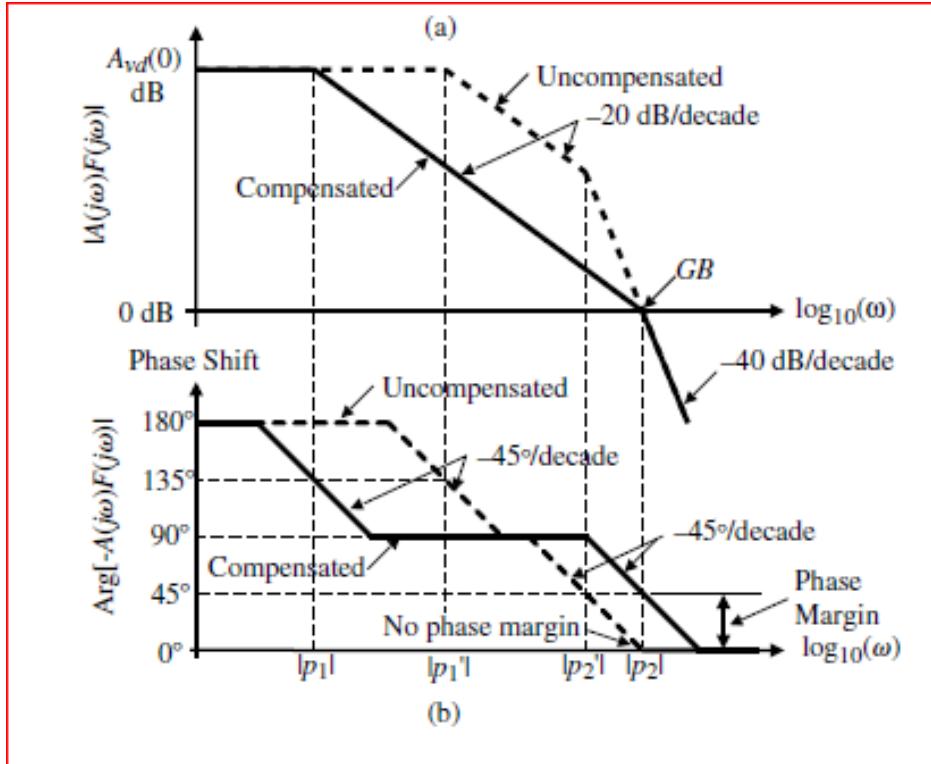


Figure 3.3: Frequency response and Phase plot of a compensated [2]

The phase margin is given by,

$$\text{Phase Margin} = \phi = -180^\circ - \arctan\left(\frac{\omega_u}{P_1}\right) - \arctan\left(\frac{\omega_u}{P_2}\right) - \arctan\left(\frac{\omega_u}{Z_1}\right) \quad (3.3)$$

where,

$$\omega_u = \text{Unity Gain Bandwidth}$$

Comparing equation (2.5,2.6) and equation (3.1,3.2), we see that the pole P_1^* value is shifted towards the origin while the second pole P_2^* moved away from the origin. The same can be seen from figure 3.3. Because of this phenomena, the bode plot drop by -20dB slope and reaches UGB without suffering a second drop in the slope. Therefore, Gain crossover frequency come before the phase cross-over frequency. And thus,a certain phase margin is available and this enhances the stability of the Op-Amp.

3.2 Compensation using Voltage Buffer stage

Although a miller compensated Op-amp created some certain margin, it was observed that the additional capacitor that was being added created a right hand plane zero that restricts certain useful parameters. The current path created by the compensation capacitor created the zero and it leads to some reduction of the phase margin as governed by the phase margin equation in equation 3.3. Also, the zero limits the maximum Gain Bandwidth Product that the Op-Amp can attain. In order to compensate the effect of the zero, different techniques can be employed. One such technique is the use of a voltage buffer stage as done in [3]. This method of compensating the right hand plane zero is called Voltage Buffer Compensation [3].

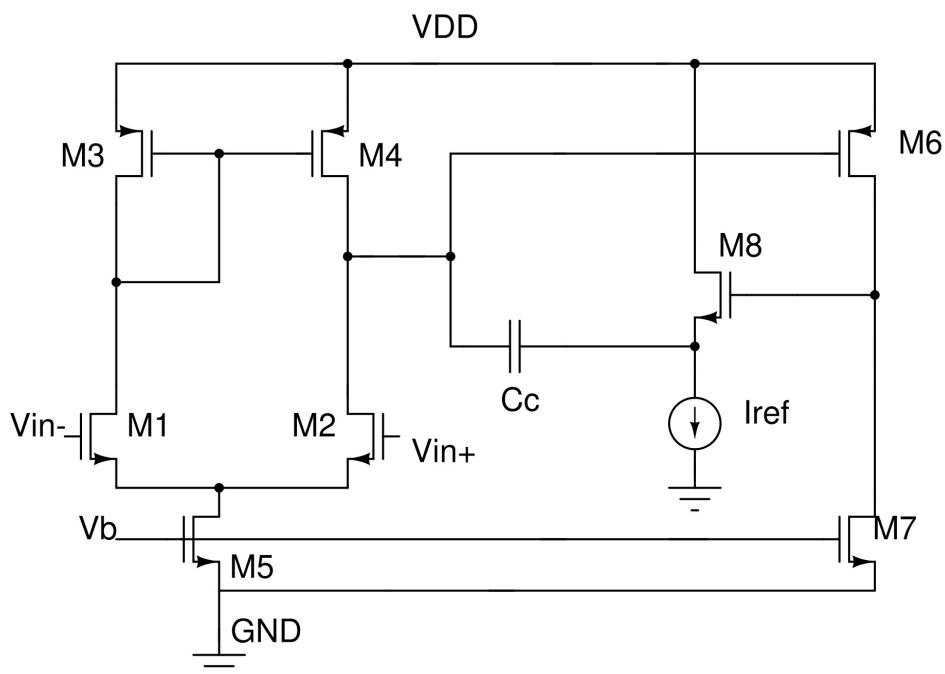


Figure 3.4: A Miller Op-amp with a Voltage Buffer stage

The use of a voltage buffer breaks the forward path previously introduced by the miller capacitor C_c . Then Capacitor C_c and M8 form the buffer stage as shown in figure 3.4.

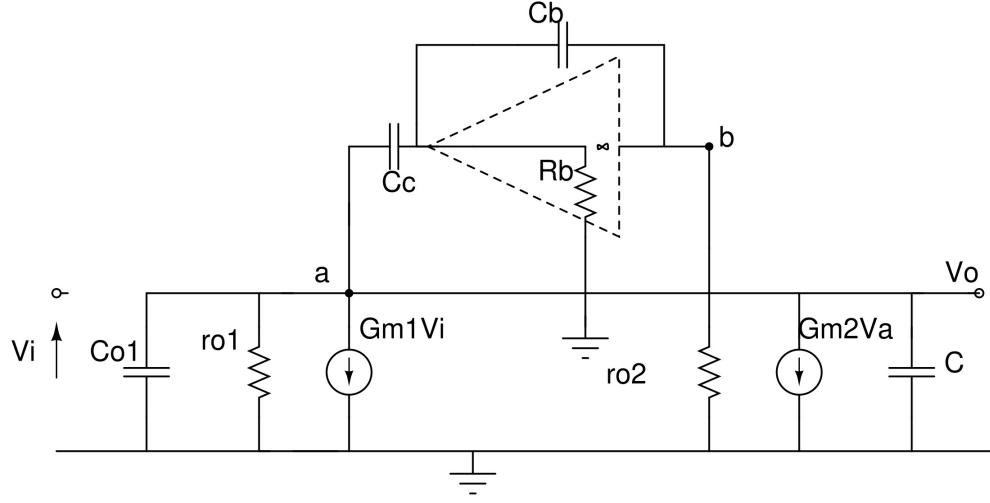


Figure 3.5: Small signal model of Op-amp with voltage buffer

From the small signal model, the calculated Transfer function as calculated in [3] is given by,

$$TF = A_o \frac{a_2 s^2 + a_1 s + 1}{b_3 s^3 + b_2 s^2 + b_1 s + 1}$$

here, $A_o = Gm_1 r_{o1} Gm_2 r_{o2}$ and $Gm_1 = g_{m1,2}$ and $Gm_2 = g_{m6}$ are the transconductance of stage 1 and 2 respectively

$$a1 = (C_c + C_b)r_b$$

$$a2 = -C_c C_b \frac{r_b}{Gm2}$$

$$b1 = aC_c(r_{o1}Gm2r_{o2} + r_{o1} + r_b) + C_Lr_{o2} + C_{o1}r_{o1} + Cb[r_b + r_{o2}(1 - a)] \sim aC_c r_{o1} Gm2r_{o2}$$

$$b2 = C_c C_b r_{o1} Gm_2 r_{o2} r_b + (C_c C_L + C_c C_b + C_L) C_b r_{o1} r_b + (C_c C_{o1} + C_c C_b + C_{o1} C_b)$$

$$+ (C_c C_L + C_L C_{o1}) r_{o1} r_{o2} + (C_c C_b + C_{o1} C_b) r_{o1} r_{o2}$$

$$\sim (C_c C_L + C_L C_{o1}) r_{o1} r_{o2} + C_c C_b r_{o1} Gm_2 r_{o2} r_b$$

$$b3 = \{C_c[C_L(C_{o1} + C_b) + C_{o1}C_b] + C_L C_{o1} C_b\} r_{o1} r_{o2} r_b$$

$$\sim C_c(C_{o1} + C_b) r_{o1} r_{o2} r_b$$

If the poles and zeroes are spaced equally, they can be written as

$$P1 \sim \frac{-1}{b1} \sim \frac{-1}{\alpha r_{o1} Gm2 r_{o2} C_c}$$

$$P2 \sim \frac{-b1}{b2} \sim \frac{-\alpha Gm2}{C_L + C_b Gm2 r_b}$$

$$P3 \sim \frac{-b2}{3} \sim \frac{-1}{(C_{o1} + C_b) r_b}$$

$$Z1\sim \frac{-1}{a1}\sim \frac{-1}{C_cr_b}$$

$$Z2\sim \frac{-a1}{a2}\sim \frac{-Gm2}{C_b}$$

Chapter 4

Simulation Results

4.1 Miller Compensation Method

The schematic for Miller Compensated Circuit is setup as shown in the figure below.

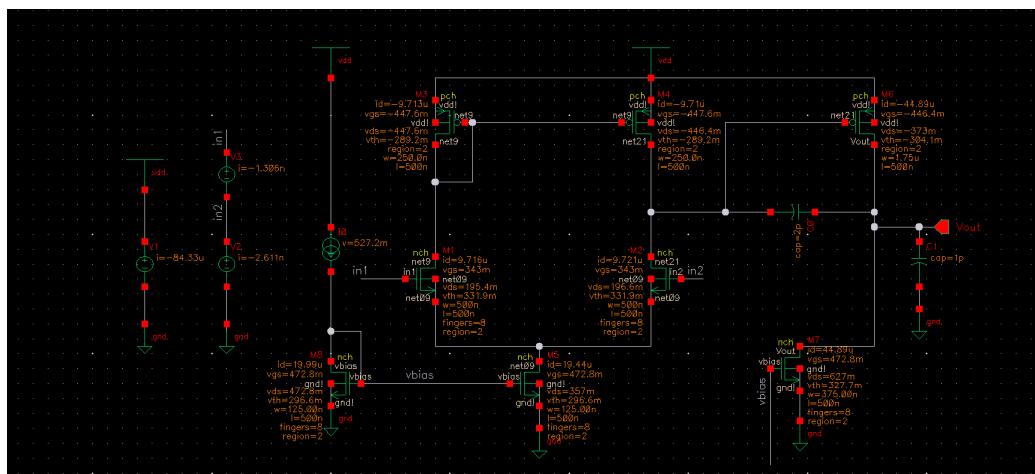


Figure 4.1: Schematic for Miller Compensated Opamp

4.1.1 Gain and Phase

For measuring the Gain and Phase, a test bench setup shown in figure 4.2

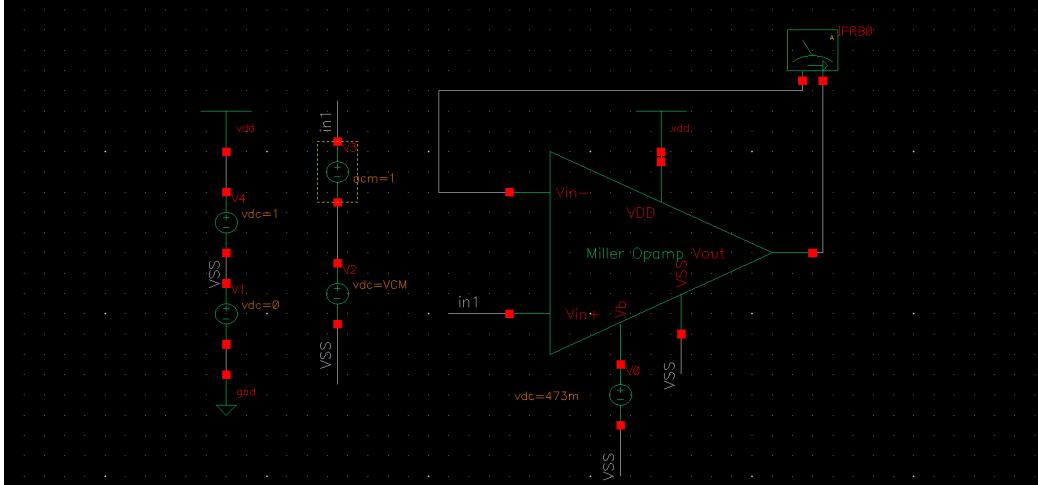


Figure 4.2: Test Bench for Gain and Phase

Figure 4.3 shows the Gain and the Phase plot from the resulting simulation. The results are $Gain = 55.38dB$ shown by the yellow marker and the Phase Margin is $\phi \sim 61.76deg$ show by the vertical line at approximately 0dB gain

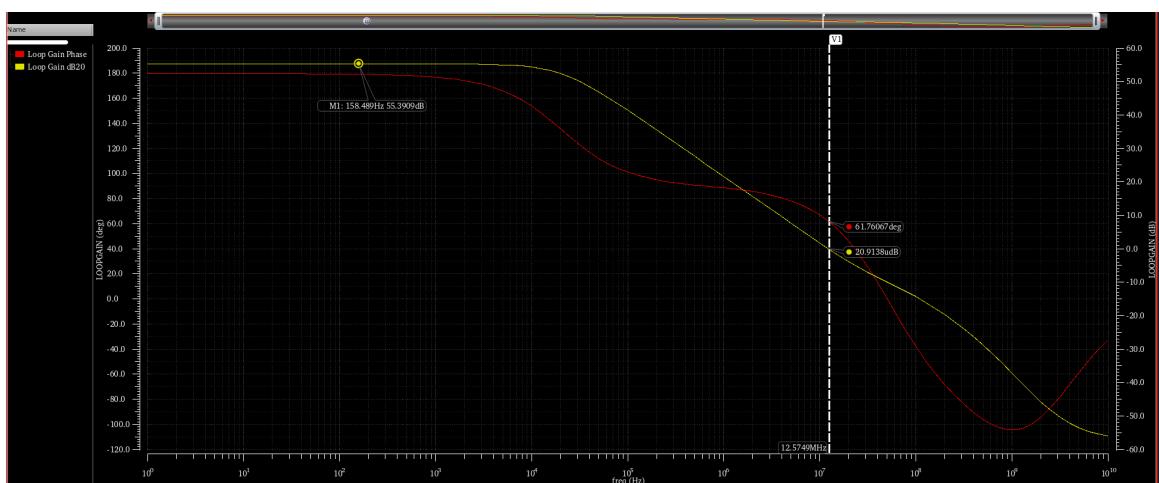


Figure 4.3: Gain and Phase results of Miller Compensated Op-Amp

4.1.2 Slew Rate

For the test bench of Slew Rate, the input and the output is shorted and figure 4.4 shows the same.

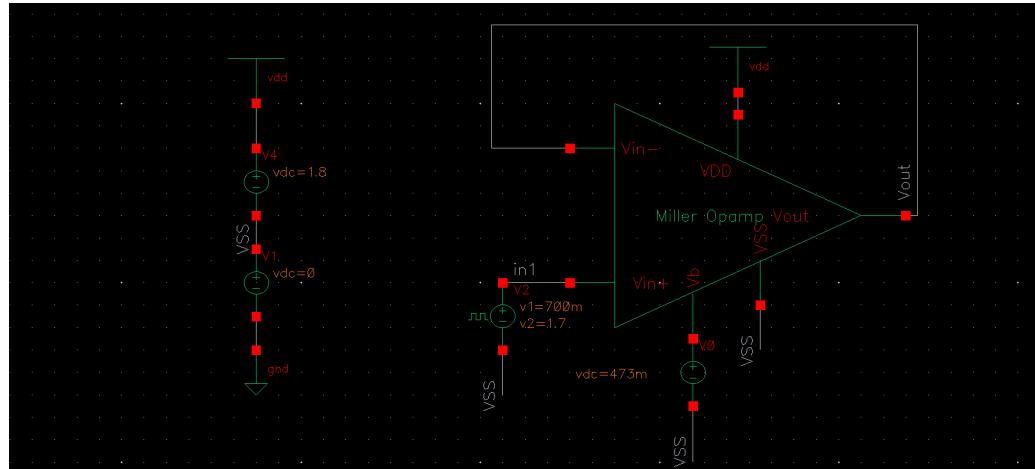


Figure 4.4: Test Bench for slewrate measurement

Here the slew is approximately at 10.484M shown by the yellow cross marker in figure4.5

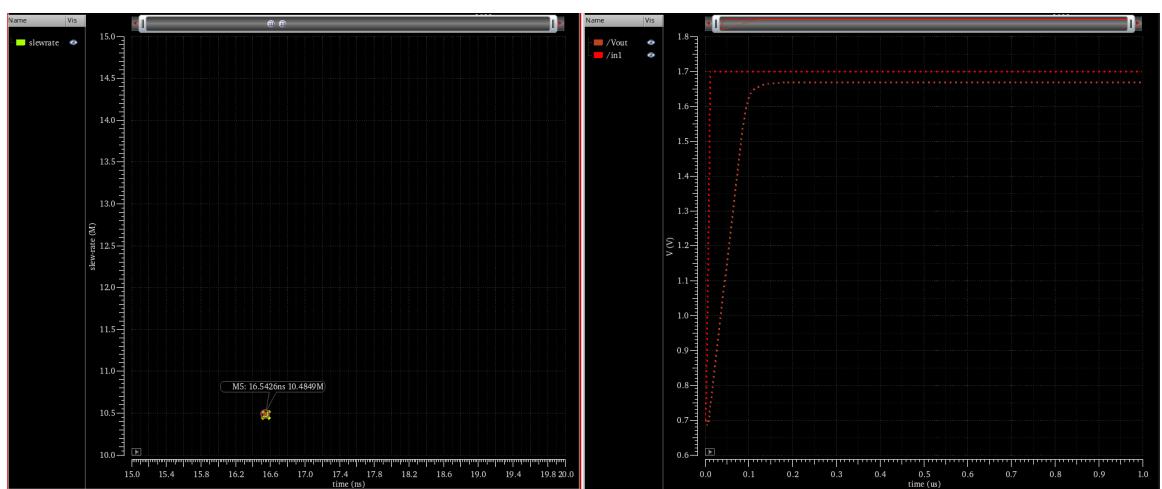


Figure 4.5: Slew rate results of Miller Compensated Opamp

4.2 Voltage Buffer Compensation

Similar to the previous schematic, the schematic for Voltage buffer compensation technique Circuit is setup as shown in the figure below.

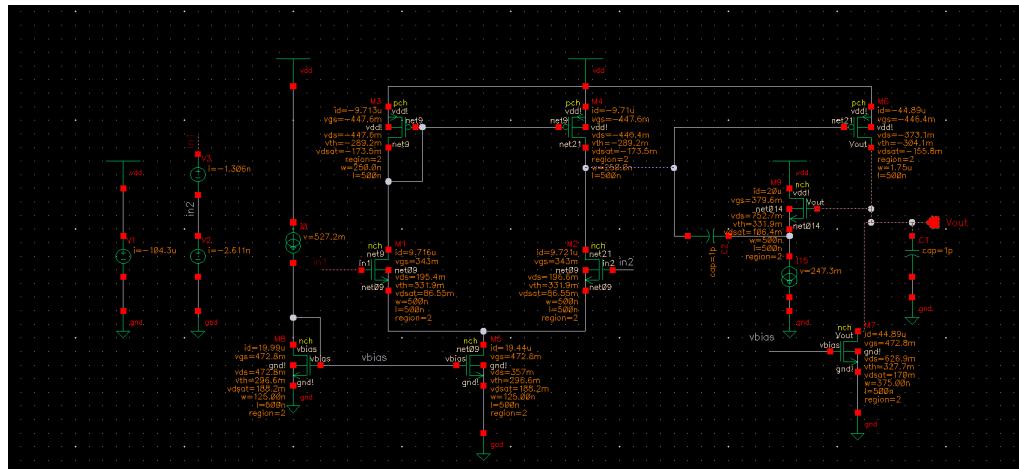


Figure 4.6: Schematic for Voltage buffer Compensated Opamp

Here, the voltage buffer stage is added between the output of the first stage and the second stage and the path offered by the nullifying capacitor is blocked nullifying the zero.

4.2.1 Gain and Phase

For measuring the Gain and Phase, a test bench setup shown in figure 4.7

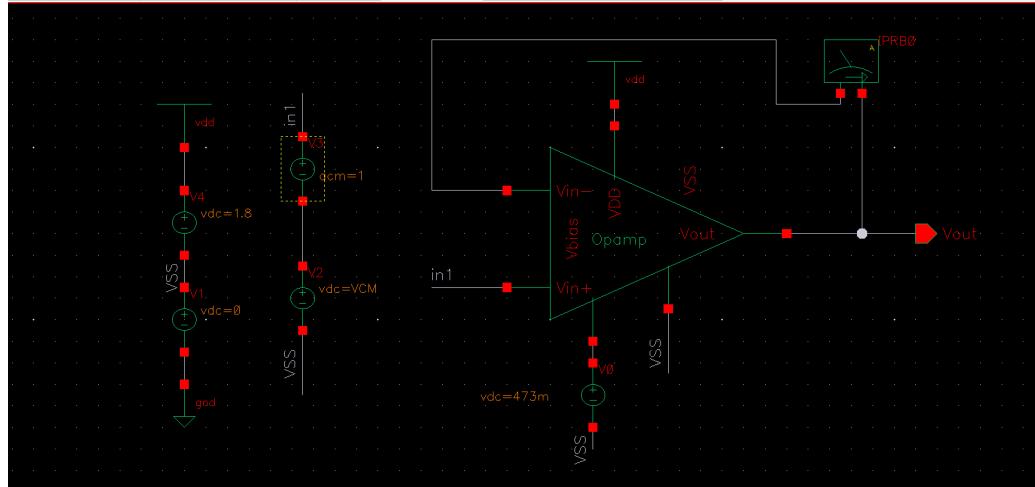


Figure 4.7: Test Bench for Gain and Phase

Figure 4.8 shows the Gain and the Phase plot from the resulting simulation. The results are $Gain = 63.1957dB$ shown by the yellow marker and the Phase Margin is $\phi \sim 99.03deg$ show by the vertical line at approximately 0dB gain

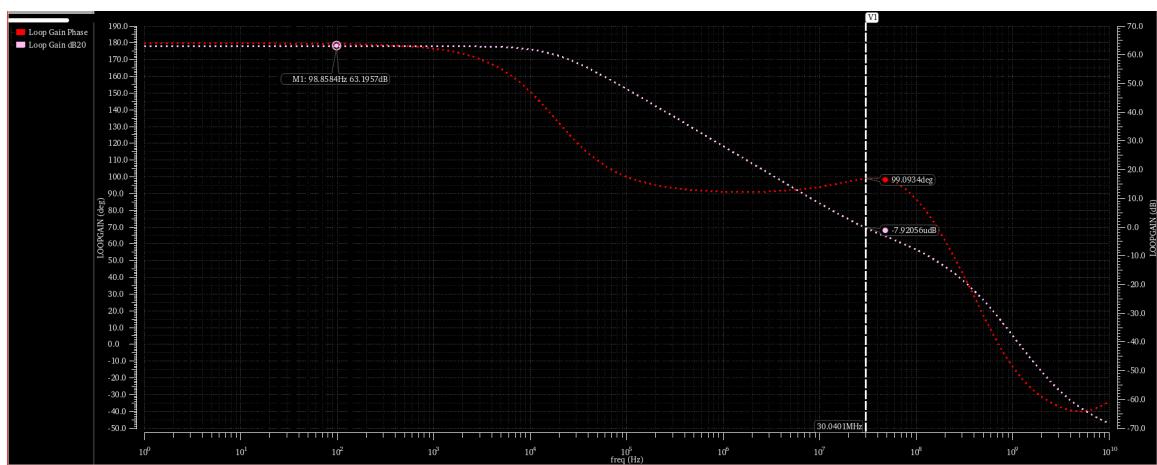


Figure 4.8: Gain and Phase results of Miller Compensated Op-Amp

4.2.2 Slew Rate

For the test bench of Slew Rate, the input and the output is shorted and figure 4.9 shows the same.

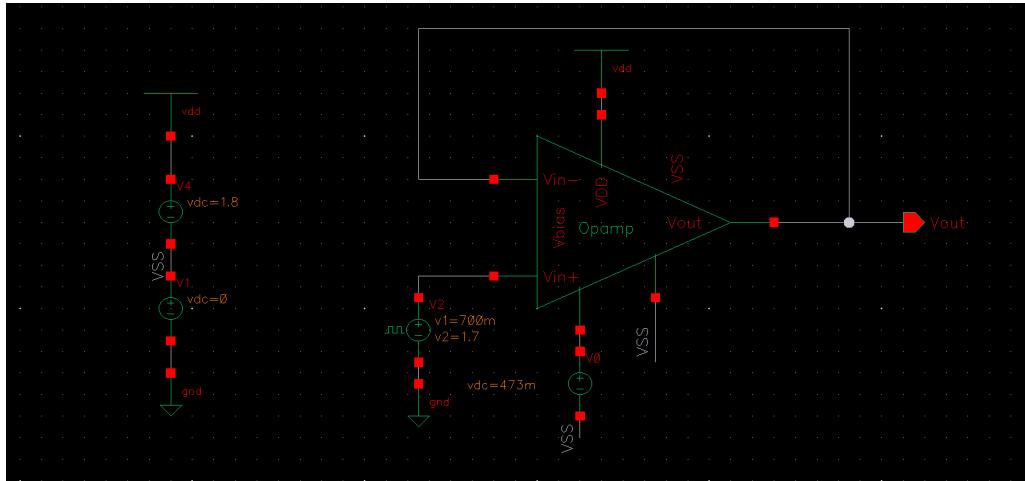


Figure 4.9: Test Bench for slewrate measurement

Here the slew is approximately at 20.25M shown by the yellow yellow marker in figure 4.10

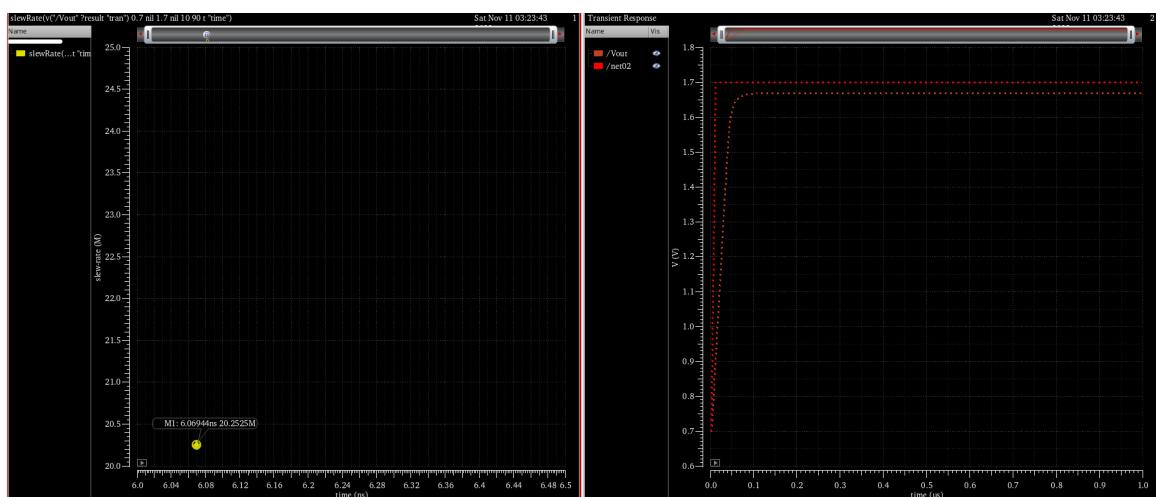


Figure 4.10: Slew rate results of Voltage Buffer Compensated Opamp

Chapter 5

Comparison and Conclusion

5.1 Comparison

This section shows the comparison between Miller Compensation technique [1] , [2] and Voltage Buffer Compensation technique [3].

Parameters	Miller Compensation	Voltage Buffer Compensation
Gain	55.39dB	63.197dB
Phase Margin	61.76deg	99.03deg
Slewrate	10.4849M	20.25M

Table 5.1: A comparison table for the two compensation technique

5.2 Conclusion

This seminar report presented the analysis of different types of compensation technique for an Op-amp. Two types of technique were studied namely the conventional miller compensation and the suggested improved technique as in [3]. From the simulation results, we observed that with the introduction of a buffer stage in addition to the miller capacitor, the phase margin increases from 61.76deg to 99.10deg. The increase in phase margin increases the stability of the Op-amp. Also, we can see the increase the gain from 55.39dB to 63.19dB implying that the Gain Band-width Product is also being improved. Thus, we can see that the Voltage Buffer Compensation Technique is a technique superior to the prior Miller Compensation technique.

References

- [1] R. Kammar, “Design and characteristics measurement of miller compensated two-stage operational amplifier in 1.8v, 180nm cmos,” University of Hyderabad, Tech. Rep., 2019.
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