

A study on different design approaches of low voltage bulk driven OTA

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by

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Declaration

I declare that this written submission represents the comparative analysis of various journals which I have adequately cited and referenced the original sources. I also declare that no falsified interpretation has been done and I have adhered to all the ethics and principles of academic integrity. Further, if any violation of the aforementioned statement is found I will be held responsible and I fully understand the consequences.

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Abstract

A bulk driven Operational Transconductance Amplifier is studied. Three types of OTA designed for body driving is presented. All the design under study are multi-stage. The first one uses a feedback to improve the transconductance and also uses a single miller compensation to optimize area. It can drive a load capacitance of 5uF. The second design uses a differential pair introduced into a conventional design to improve its transconductance. A cascode model is used to enhance input stage operations. The third design[only results are taken] allows a higher gain due to the double body transconductance employed at the first and the third stage.

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Chapter 1

Introduction

With the advancement of electronics and scaling of devices for various applications, the need for ultra low power design techniques has become a necessity. This lead to many recent technological developments of low power design approaches. Keeping the power consumption at minimum. Thus, reducing the size of the battery and the overall volume of the device. This small volume allows its application in the field of biomedical sciences.

In CMOS technology, for a very low power application, the most feasible technique is to bias the MOS in subthreshold region. Thus, for the operation of Mosfet in weak inversion, body biasing is proven to be the most effective solution [1]. Body effect is usually considered as an unwanted effect of the MOS transistor but studies have been made in order to utilize this effect for smaller signals. This effect refers to the transconductance provided by the body of the MOS. In order to operate the transistor as a body driven device, a conduction channel inversion layer formed after proper gate biasing and input is applied to the body of MOS. However the transconductance provided by the bulk of the MOS is lower as compared to the conventional gate driven counterparts. This in turn limits the DC voltage gain and also affects the gain bandwidth product. In this bulk driving methodology, it increases the operable range of the MOS because the minimum threshold required to maintain the biasing is no longer in play.

In this report, three designs of bulk driven OTA have been studied and their architecture are described in the following chapters. The first design [1] is implemented in a 65nm technology with a voltage of 0.3V followed by the second design [2].

Chapter 2

Design Approach 1

In this architecture [1], shown in Figure 2.1, we employ a differential pair M1-M2 without the use of a tail current source. Current mirror M13 and the current source I_B provides the biasing for the differential pair M1-M2. M3 and M4 along with the corresponding resistors R_A and R_B , act as the load of the differential pair. The body of M4 and the drain of M3 is connected and the body of M3 and the drain of M4 is also connected. Therefore, M3 and M4 will act like a diode connected load because of the equal potential of gate and drain. This is because, at dc, there will be no current flowing in the resistor R_A and R_B . And eventually, $V_{SG6}=V_{SG3}$ and $V_{SG4}=V_{SG8}$.

We know, for a pmos threshold voltage is given by,

$$V_T = V_{TO} - \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

Also neglecting channel length modulation and saturation condition,

$$\frac{I_{D6,8}}{I_{D3,4}} = \frac{W/L_{6,8}}{W/L_{3,4}} \left[\frac{1 - \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})}{V_{SG} + V_{TO}} \right]^2$$

As for the second stage, I_{D11} is set by the mirror current I_{D8} and also the mirror M_9 and M_{10} set the current for the output stage. To ensure the class A-B operation, M_{11} and M_{12} performs the sinking and sourcing of the output stage current. Even though we apply the input signal to the body of the MOS, M_1 and M_2 produces similar results of a differential pair. This produces a transconductance which can be enhanced by the cross connection of bulk and drain of M_3 and M_4 .

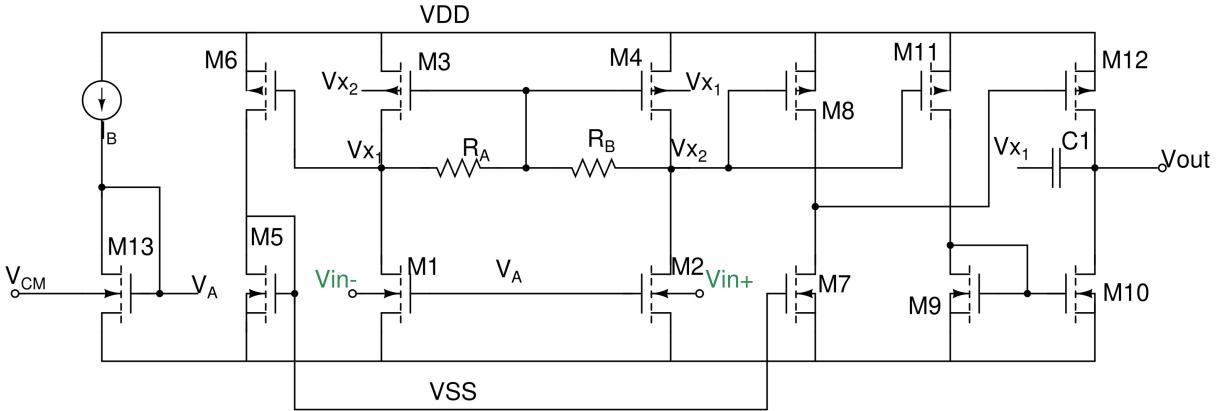


Figure 2.1: Schematic of the first architecture OTA

The differential gain of the first stage is given by,

$$A_{01} = -\frac{1}{2} G_{mb} R_{A,B} || r_{o1} = -\frac{1}{2} \frac{g_{mb1,2}}{(1 - g_{mb3,4} R_{A,B} || r_{o1})} R_{AB} || r_{o1}$$

where $g_{mb1,2}$ and $g_{mb3,4}$ are the transconductances produced by the body effect of M_{1-2} and M_{3-4} respectively. To increase the gain we keep the denominator less than 1 but very close to 1.

Now, the overall gain of the OTA is given by,

$$A_{01} = G_{mb} g_{m6,8} g_{m12} (R_{A,B} || r_{o1}) r_{o2} r_{o3}$$

where $r_{o2} = r_{d7} || r_{d8}$ and $r_{o3} = r_{d10} || r_{d12}$ are the output impedances of the second and third stage respectively.

In this design [1], a single miller capacitor is used to compensate for the frequency response. Considering the adequate parasitic capacitance and load capacitance at the output of the second stage, the open loop transfer function can be approximated as

$$A(s) = A_0 \frac{(1 + s/p1)}{(1 + s/p2)(1 + a1 + a2 + a2s^2)}$$

where A_0 is the dc overall gain,

$$p1 = \frac{1}{g_{m6,8} g_{m12} (R || r_{o1}) r_{o2} r_{o3} C_c + r_{o3} C_L}$$

$$a1 = \frac{C_L(C_c R_{A,B} + 2C_{o2} r_{o2})}{2}$$

$$a2 = \frac{C_L C_c R_{A,B} C_{o2} r_{o2}}{2}$$

$$\begin{aligned}
z1 &= \frac{g_{m3,4}}{2C_c} \\
z2 &= \frac{g_{m8}g_{m12}}{C_{o2}(g_{m10} - g_{m3,4})} \\
z3 &= \frac{g_{m10} - g_{m3,4}}{2C_{X2}} \\
p4 &= \frac{g_{m3,4}}{2C_{X2}}
\end{aligned}$$

For Gain Bandwidth , z2,z3,p4 is neglected considering the parasitics which is very small as compared to C_L and C_c .

$$GBW = A_0 p1 = \frac{G_{mb}}{C_c + \frac{C_L}{g_{m6,8}g_{12}(R||r_{o1})r_{o2}}}$$

For Phase Margin, we have the expression as

$$PM = \tan^{-1} \left(\frac{1 - a_2(\omega_{GBW})^2}{a_1\omega_{GBW}} \right) + \tan^{-1} \left(\frac{\omega_{GBW}}{z1} \right)$$

Chapter 3

Design approach 2

In the second approach design [2], as shown in Figure 3.1 an ultra low voltage OTA is studied. The design consists of two fully differential stages followed by a single ended output stage. This is to increase robustness to PVT variation. The architecture is designed in a 130nm CMOS technology with an input voltage of 0.3V. The first stage is bulk driven in order to meet rail to rail capability. Whereas, in the second stage the gate is driven to increase the overall DC gain. And in the next stage, body driving at input is carried out in order to allow mirror gate driving at the output. The frequency compensation is carried out by a Reverse Nested Miller circuit [] .

3.1 First Stage

Here $M_{p1,2}$ and $M_{n1,2}$ make up the first stage. The biasing is done by V_{bg} , generated from the reference circuit and the input driving is given to the body of $M_{p1,2}$. The common mode feedback controls the gate of $M_{n1,2}$. The differential gain can be expressed as

$$A_{d1} = \frac{g_{mbn1,2} + g_{mbp1,2}}{g_{dsn1,2} + g_{dsp1,2}} \frac{1}{1 + s \frac{C_{o1}}{g_{dsn1,2} + g_{dsp1,2}}}$$

C_{o1} is the capacitance at the output node of the first stage and can be expressed by

$$C_{o1} = C_{gdn1,2} + C_{gd1,2} + C_{in2} + C_{bdn1,2} + C_{bdp1,2}$$

Neglecting the effect of the common mode feedback loop, the gain can be expressed as

$$A_{vc1} = \frac{G_{b1}}{G_{o1}}$$

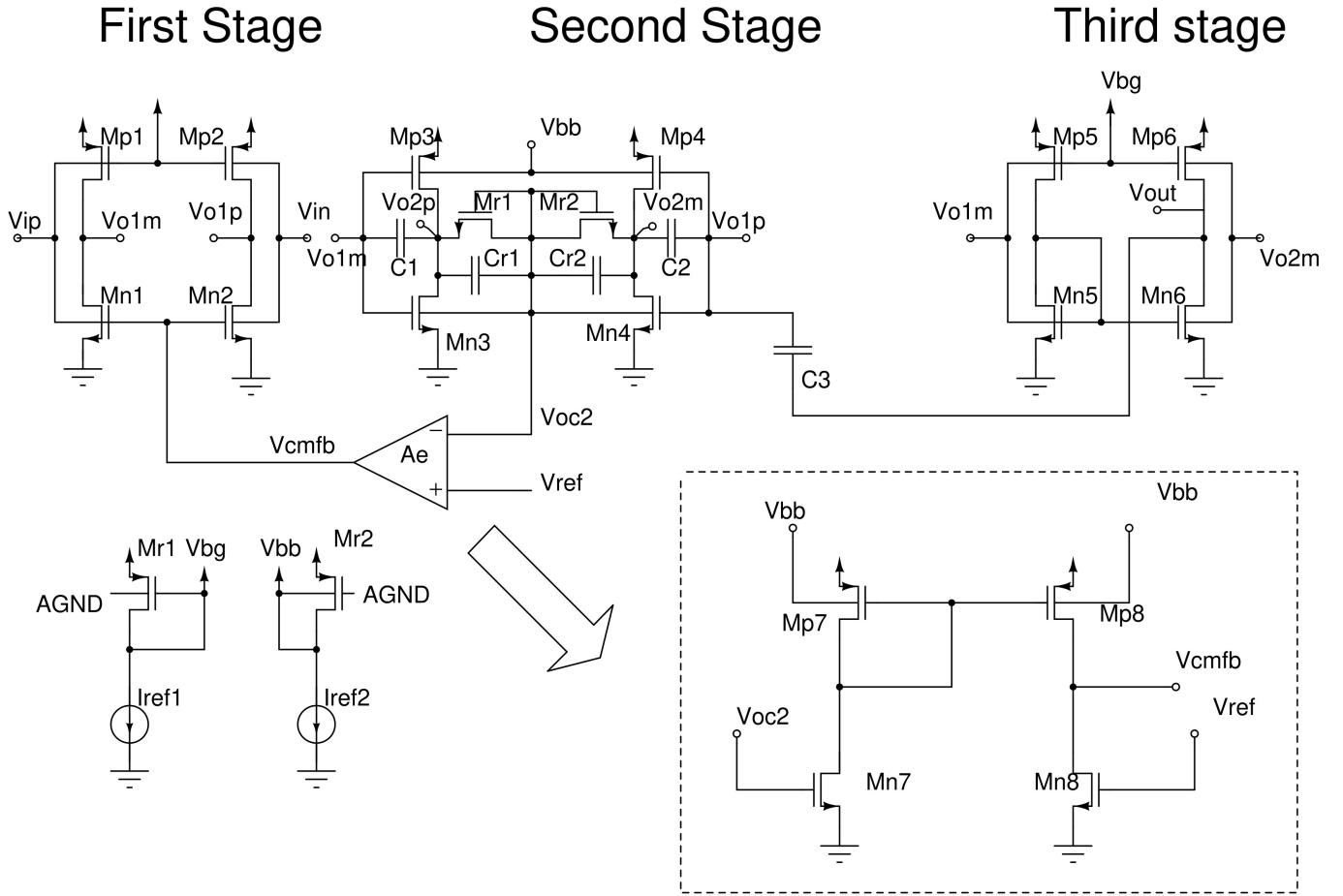


Figure 3.1: Schematic of the second architecture OTA

3.2 Second Stage

The second stage consist of transistor $M_{p3,4}$ and $M_{n3,4}$. Here the transistors are gate driven and body biased. As body biasing increases the sensitivity to PVT variations, the technique of local CFMB [2] is implemented with the help of Pseudo resistors $M_{R1,2}$ to increase immunity to PVT variation of second stage. The differential gain of this stage is given by

$$A_{vd2} = \frac{g_{mn3,4} + g_{mp3,4}}{g_{dsn3,4} + g_{dsn3,4} + g_{R1,2}} \frac{1}{1 + s \frac{C_{o2}}{g_{dsn3,4} + g_{dsn3,4} + g_{R1,2}}}$$

here, the conductance of $M_{NR1,2}$ is represented by $g_{R1,2}$ also,

$$C_{o2} = C_{gdN3,4} + C_{gdP3,4} + C_{in3} + C_{bdN34} + C_{bdP3,4} + C_{R1,2}$$

The common mode gain is given by,

$$A_{vc2} = \frac{gm_{n3,4} + g_{mp3,4}}{g_{dsn3,4} + g_{dsp3,4} + g_{mbn3,4}}$$

3.3 Third stage

In this stage, $M_{5,6}$ are both gate biased and body driving MOS. This stage is the final stage which convert the differential to single ended outputs .Mirror M_{n5} and M_{n6} perform the differential to single ended conversion. In this stage, differential gain of this stage is given as,

$$Av_{d3} = \frac{g_{mbn5,6} + g_{mbp5,6}}{g_{dsn5,6} + g_{dsp5,6}} \frac{1}{1 + s \frac{C_L + C_{o3}}{g_{dsn5,6} + g_{dsp5,6}}}$$

The capacitance C_{o3} is given by

$$C_{o3} = C_{gdn,56} + C_{gdp5,6} + C_{bdn5,6} + C_{bdp5,6}$$

Also, the common mode gain of the third stage is given as,

$$A_{vc3} = \frac{g_{mbn5,6} + g_{mbp5,6}}{g_{dsn5,6} + g_{dsp5,6}} \frac{g_{dsn5,6} + g_{dsp5,6}}{g_{dsn5,6} + g_{dsp5,6} + g_{mn5,6}}$$

Chapter 4

Comparison of FOMs

In this section, the figure of merits mainly the gain and phase plot is presented as figure 4.1 and figure 4.2.

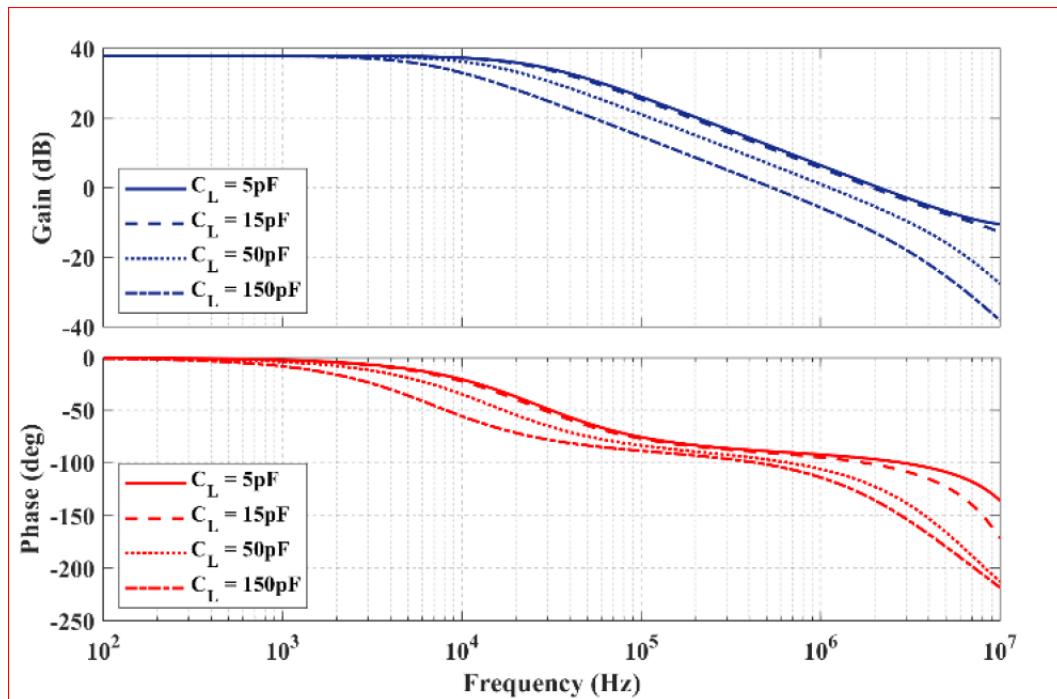


Figure 4.1: Gain and phase results from design 1 [1]

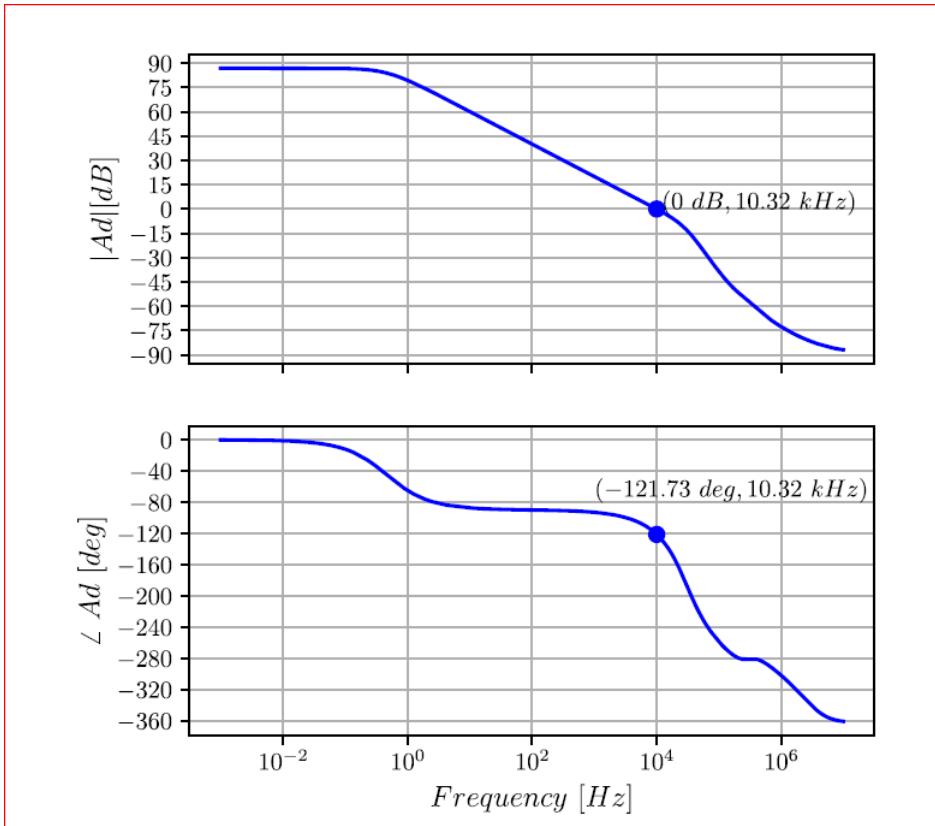


Figure 4.2: Gain and phase results from Design 2 [2]

The two figures represent the two comparing architectures from [1] and [2]. From Figure 4.1 and Figure 4.2 we can see that the gain in the second design have a higher gain of almost 90dB whereas the first design have a gain of about 40dB. Also the phase vs freq plot tell us some insights about the stability response of the two comparing amplifier. Further comparison about two architecture is presented in the following section.

Chapter 5

Table of Comparison

Comparison table for different design techniques			
Parameters	This analysis [1]	This analysis [2]	[3]
Year	2023	2023	2013
Tech	65nm	130nm	0.35nm
VDD[V]	0.3V	0.3V	5V
A_d [dB]	38.1dB	86.83dB	88.3dB
C_L [pF]	50pF	35pF	15pF
GBW	1.06Mhz	10.32kHz	1.93Mhz
PM(°)	70.3	58.27	66.1
CMRR	39.8	57.8	40
PSRR	44.7	46.59	40
Area (μm^2)	1060	2340	525.3

Table 5.1: Different parameters and results of OTAs under study

Chapter 6

Conclusion

In this analysis of body driven OTA, different types of architectures are studied as presented in the previous sections. The designs are also analysed for their gains and their phase margins. As per the comparison table, we can also observe a clear trade-off between gain and phase margin. In [1], the gains is 38dB and the PM is 70° . However, with the increase in gain of the second design [2] the gain almost doubled but the PM drops to 58° . Similar case has been observed in [3].Overall performance in stability can also be observed from the phase margin(higher PM being higher stability).Also due to the small usage of power by the circuit, we can conclude that the sectional area of the Designs are exceptionally small(i.e in order of micrometre) which allows its application in the field of various modern electronics.

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