UltraScale Architecture and Product Overview

DS890 (v2.1) April 27, 2015 **Preliminary Product Specification**

General Description

Xilinx® UltraScale™ architecture comprises high-performance FPGA and MPSoC families that address a vast spectrum of system requirements with a focus on lowering total power consumption through numerous innovative technological advancements.

Kintex® UltraScale FPGAs: High-performance FPGAs with a focus on price/performance, using both monolithic and next-generation stacked silicon interconnect (SSI) technology. High DSP and block RAM-to-logic ratios and next-generation transceivers, combined with low-cost packaging, enable an optimum blend of capability and cost.

Kintex UltraScale+™ FPGAs: Based on the UltraScale architecture, these devices have increased performance and on-chip UltraRAM memory to reduce BOM cost, providing the ideal mix of high-performance peripherals and cost-effective system implementation. In addition, Kintex UltraScale+ FPGAs have numerous power options that deliver the optimal balance between the required system performance and the smallest power envelope.

Virtex® UltraScale FPGAs: The industry's most capable high-performance FPGAs enabled using both monolithic and next-generation SSI technology to achieve the highest system capacity, bandwidth, and performance. Variants of the Virtex UltraScale family are optimized to address key market and application requirements through integration of various system-level functions, delivering unprecedented embedded memory and serial connectivity capabilities.

Virtex UltraScale+ FPGAs: Based on the UltraScale architecture, these devices have the highest transceiver bandwidth, highest DSP count, and highest on-chip memory available in the industry for the ultimate in system performance. In addition, Virtex UltraScale+ FPGAs also provide numerous power options that deliver the optimal balance between the required system performance and the smallest power envelope.

Zynq® UltraScale+ MPSoCs: Combine the ARM® v8-based Cortex®-A53 high-performance energy-efficient 64-bit application processor with the ARM Cortex-R5 real-time processor and the UltraScale architecture to create the industry's first All Programmable MPSoCs. With next-generation programmable engines, security, safety, reliability, and scalability from 32 to 64 bits, the Zynq UltraScale+ MPSoCs provide unprecedented power savings, processing, programmable acceleration, I/O, and memory bandwidth ideal for applications that require heterogeneous processing.

Family Comparisons

Table 1: **Device Resources**

	Kintex UltraScale	Kintex UltraScale+	Virtex UltraScale	Virtex UltraScale+	Zynq UltraScale+
MPSoC Processing System					✓
Logic Cells (K)	355–1,160	205–915	627–4,433	690–2,863	83–915
Block Memory (Mb)	19.0–75.9	5.1–34.6	44.3–132.9	25.3–94.5	4.5–34.6
UltraRAM (Mb)		0–36		90–432	0–36
DSP (Slices)	768–5,520	1,056–3,528	600–2,880	2,280–11,904	240–3,528
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,213	6,287
Transceivers	16–64	16–76	36–120	40–128	0–72
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268
Integrated Blocks for PCIe®	2–6	0–5	2–6	2–6	0–5
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	416–832	76–668
I/O Voltage (V)	1.0–3.3	1.0–3.3	1.0–3.3	1.0–1.8	1.0–3.3

Summary of Features

Processing System

UltraScale+ MPSoCs are built around a feature-rich quad-core ARM Cortex A53 and dual-core ARM Cortex R5 processing system (PS). In addition to the 32-bit/64-bit application processing unit (APU) and 32-bit real-time processing unit (RPU), the PS contains a dedicated ARM Mali™-400 MP2 graphics processing unit (GPU).

To support the processors' functionality, a number of peripherals with dedicated functions are included in the PS. For interfacing to external memories for data or configuration storage, the PS includes a multi-protocol dynamic memory controller, a DMA controller, a NAND controller, an SD/eMMC controller and a Quad SPI controller. In addition to interfacing to external memories, the processing units also contain their level 1 and/or level 2 caches and 256KB of on-chip memory.

For high-speed interfacing, the PS includes 4 channels of transmit (TX) and receive (RX) pairs of transceivers, called PS-GTR transceivers, supporting data rates of up to 6.0Gb/s. These transceivers can interface to the high-speed peripheral blocks to support PCIe Gen2 root complex or end point in x1, x2, or x4 configurations; Serial-ATA (SATA) at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s data rates; and up to two lanes of Display Port at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s data rates. The PS-GTR transceivers can also interface to components over USB 3.0 and Serial Gigabit Media Independent Interface (SGMII).

For general connectivity, the PS includes: a pair of USB 2.0 controllers, which can be configured as host, device, or On-The-Go (OTG); an I2C controller; a UART; and a CAN2.0B controller that conforms to ISO11898-1. There are also four triple speed Ethernet MACs and 128 bits of GPIO, of which 78 bits are available through the MIO and 96 through the EMIO.

High-bandwidth connectivity based on the ARM AMBA® AXI4 protocol connects the processing units with the peripherals and provides interface between the PS and the programmable logic (PL).

I/O, Transceiver, PCIe, 100G Ethernet, and 150G Interlaken

Data is transported on and off chip through a combination of the high-performance parallel SelectIO™ interface and high-speed serial transceiver connectivity. I/O blocks provide support for cutting-edge memory interface and network protocols through flexible I/O standard and voltage support. The serial transceivers in the UltraScale architecture-based devices transfer data up to 32.75Gb/s, enabling 25G+ backplane designs with dramatically lower power per bit than previous generation transceivers. All transceivers, except the PS-GTR, support the required data rates for PCIe Gen3, and Gen4 (rev 0.5), and integrated blocks for PCIe enable UltraScale devices to support up to Gen4 x8 and Gen3 x16 Endpoint and Root Port designs. Integrated blocks for 150Gb/s Interlaken and 100Gb/s Ethernet (100G MAC/PCS) extend the capabilities of UltraScale devices, enabling simple, reliable support for Nx100G switch and bridge applications.

Clocks and Memory Interfaces

UltraScale devices contain powerful clock management circuitry, including clock synthesis, buffering, and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks to minimize the skew, power consumption, and delay associated with clock signals. The clock management technology is tightly integrated with dedicated memory interface circuitry to enable support for high-performance external memories, including DDR4. In addition to parallel memory interfaces, UltraScale devices support serial memories, such as Hybrid Memory Cube (HMC).

Routing, SSI, Logic, Storage, and Signal Processing

Configurable Logic Blocks (CLBs) containing 6-input look-up tables (LUTs) and flip-flops, DSP slices with 27x18 multipliers, 36Kb block RAMs with built-in FIFO and ECC support, and 4Kx72 UltraRAM blocks (in UltraScale+ devices) are all connected with an abundance of high-performance, low-latency interconnect. In addition to logical functions, the CLB provides shift register, multiplexer, and carry logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable block RAMs. The DSP slice, with its 96-bit-wide XOR functionality, 27-bit pre-adder, and 30-bit A input, performs numerous independent functions including multiply accumulate, multiply add, and pattern detect. In addition to the device interconnect, in devices using SSI technology, signals can cross between super-logic regions (SLRs) using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation bus data widths.

Configuration, Encryption, and System Monitoring

The configuration and encryption block performs numerous device-level functions critical to the successful operation of the FPGA or MPSoC. This high-performance configuration block enables device configuration from external media through various protocols, including PCIe, often with no requirement to use multi-function I/O pins during configuration. The configuration block also provides 256-bit AES-GCM decryption capability at the same performance as unencrypted configuration. Additional features include SEU detection and correction, partial reconfiguration support, and battery-backed RAM or eFUSE technology for AES key storage to provide additional security. The System Monitor enables the monitoring of the physical environment via on-chip temperature and supply sensors and can also monitor up to 17 external analog inputs. With UltraScale+ MPSoCs, the device is booted via the Configuration and Security Unit (CSU), which supports secure boot via the 256-bit AES-GCM and SHA/384 blocks. The CSU can be used in the MPSoC after boot for user encryption.

Kintex UltraScale FPGA Feature Summary

Table 2: **Kintex UltraScale FPGA Feature Summary**

	KU035	KU040	KU060	KU085	KU095	KU115
Logic Cells	355,474	424,200	580,440	870,660	940,800	1,160,880
CLB Flip-Flops	406,256	484,800	663,360	995,040	1,075,200	1,326,720
CLB LUTs	203,128	242,400	331,680	497,520	537,600	663,360
Maximum Distributed RAM (Mb)	5.9	7.0	9.1	13.4	4.7	18.3
Block RAM/FIFO w/ECC (36Kb each)	540	600	1,080	1,620	1,680	2,160
Total Block RAM (Mb)	19.0	21.1	38.0	56.9	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	10	10	12	18	16	24
I/O DLLs	40	40	48	56	64	64
Maximum HP I/Os(1)	416	416	520	572	650	676
Maximum HR I/Os(2)	104	104	104	104	52	156
DSP Slices	1,700	1,920	2,760	4,100	768	5,520
System Monitor	1	1	1	2	1	2
PCIe Gen3 x8	2	3	3	4	4	6
150G Interlaken	0	0	0	0	2	0
100G Ethernet	0	0	0	0	2	0
GTH 16.3Gb/s Transceivers(3)	16	20	32	56	32	64
GTY 16.3Gb/s Transceivers(4)	0	0	0	0	32	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in SF/FB packages support data rates up to 12.5Gb/s. See Table 3.
4. GTY transceivers in Kintex UltraScale devices support data rates up to 16.3Gb/s.

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 3: **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP, GTH	HR, HP, GTH	HR, HP, GTH	HR, HP, GTH	HR, HP, GTH, GTY	HR, HP, GTH
SFVA784	23x23	104, 364, 8	104, 364, 8				
FBVA676	27x27	104, 208, 16	104, 208, 16				
FBVA900	31x31	104, 364, 16	104, 364, 16				
FFVA1156	35x35	104, 416, 16	104, 416, 20	104, 416, 28			
FFVA1517	40x40			104, 520, 32			
FLVA1517	40x40				104, 520, 48		104, 520, 48
FFVC1517	40x40					52, 468, 20, 20	
FLVD1517	40x40						104, 234, 64
FFVB1760	42.5x42.5					52, 650, 32, 16	
FLVB1760	42.5x42.5				104, 572, 44		104, 598, 52
FLVD1924	45x45						156, 676, 52
FLVF1924	45x45				104, 520, 56		104, 624, 64
FLVA2104	47.5x47.5						156, 676, 52
FFVB2104	47.5x47.5					52, 650, 32, 32	
FLVB2104	47.5x47.5						104, 598, 64

Notes:
1. Go to Ordering Information for package designation details.
2. FB/FF/FL packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.

Kintex UltraScale+ FPGA Feature Summary

Table 4: **Kintex UltraScale+ FPGA Feature Summary**

	KU3P	KU7P	KU11P	KU15P	KU5P	KU9P	KU13P
Logic Cells	204,960	403,200	522,480	914,760	379,680	479,640	597,240
CLB Flip-Flops	234,240	460,800	597,120	1,045,440	433,920	548,160	682,560
CLB LUTs	117,120	230,400	298,560	522,720	216,960	274,080	341,280
Max. Distributed RAM (Mb)	3.6	6.2	8.9	9.6	6.3	8.8	11.0
Block RAM/FIFO w/ECC (36Kb each)	144	312	600	984	480	912	744
Block RAM (Mb)	5.1	11.0	21.1	34.6	16.9	32.1	26.2
UltraRAM Blocks	64	96	80	128	64	0	112
UltraRAM (Mb)	18.0	27.0	22.5	36.0	18.0	0	31.5
CMTs (1 MMCM and 2 PLLs)	4	8	8	11	4	4	4
Max. HP I/O(1)	208	416	416	572	208	208	208
Max. HD I/O(2)	96	96	96	96	72	96	96
DSP Slices	1,056	1,728	2,928	1,968	1,824	2,520	3,528
System Monitor	1	1	1	1	1	1	1
GTH Transceiver 16.3Gb/s(3)	16	24	32	44	0	28	28
GTY Transceivers 32.75Gb/s	0	0	20	32	16	0	0
PCIe Gen3 x16 and Gen4 x8	2	1	4	5	1	0	0
150G Interlaken	0	0	2	4	0	0	0
100G Ethernet w/RS-FEC	0	0	1	4	1	0	0
Video Codec Blocks	1	1	0	0	0	0	0

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in SF packages support data rates up to 12.5Gb/s. See Table 5.

Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 5: **Kintex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)	Package Dimensions (mm)	KU3P	KU7P	KU11P	KU15P	KU5P	KU9P	KU13P
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
SFVB784	23x23	96, 208 16, 0						
FFVB676	27x27					72, 208 0, 16		
FFVC676	27x27	96, 208 16, 0	96, 208 16, 0					
FBVD900	31x31		96, 312 16, 0					
FFVD900	31x31			96, 312 16, 0				
FFVE900	31x31						96, 208 28, 0	96, 208 28, 0
FFVD1156	35x35			96, 416 16, 0	96, 520 16, 0			
FFVE1156	35x35		96, 416 24, 0	96, 416 24, 0				
FFVE1517	40x40			96, 416 32, 20	96, 416 32, 24			
FFVA1760	42.5x42.5				96, 416 44, 32			
FFVE1760	42.5x42.5				96, 572 32, 24			

Notes:

1. Go to Ordering Information for package designation details.
2. FF packages have 1.0mm ball pitch. SF packages have 0.8mm ball pitch.

Virtex UltraScale FPGA Feature Summary

Table 6: **Virtex UltraScale FPGA Feature Summary**

	VU065	VU080	VU095	VU125	VU160	VU190	VU440
Logic Cells	626,640	780,000	940,800	1,253,280	1,621,200	1,879,920	4,432,680
CLB Flip-Flops	716,160	891,424	1,075,200	1,432,320	1,852,800	2,148,480	5,065,920
CLB LUTs	358,080	445,712	537,600	716,160	926,400	1,074,240	2,532,960
Maximum Distributed RAM (Mb)	4.8	3.9	4.8	9.7	12.7	14.5	28.7
Block RAM/FIFO w/ECC (36Kb each)	1,260	1,421	1,728	2,520	3,276	3,780	2,520
Total Block RAM (Mb)	44.3	50.0	60.8	88.6	115.2	132.9	88.6
CMT (1 MMCM, 2 PLLs)	10	16	16	20	30	30	30
I/O DLLs	40	64	64	80	120	120	120
Fractional PLLs	5	8	8	10	15	15	0
Maximum HP I/Os(1)	468	780	780	780	650	650	1,404
Maximum HR I/Os(2)	52	52	52	104	52	52	52
DSP Slices	600	672	768	1,200	1,560	1,800	2,880
System Monitor	1	1	1	2	3	3	3
PCIe Gen3 x8	2	4	4	4	5	6	6
150G Interlaken	3	6	6	6	8	9	0
100G Ethernet	3	4	4	6	9	9	3
GTH 16.3Gb/s Transceivers	20	32	32	40	52	60	48
GTY 30.5Gb/s Transceivers	20	32	32	40	52	60	0

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Virtex UltraScale Device-Package Combinations and Maximum I/Os

Table 7: **Virtex UltraScale Device-Package Combinations and Maximum I/Os**

Package[1][2][3]	Package Dimensions (mm)	VU065	VU080	VU095	VU125	VU160	VU190	VU440
		HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY	HR, HP GTH, GTY
FFVC1517	40x40	52, 468 20, 20	52, 468 20, 20	52, 468 20, 20				
FFVD1517	40x40		52, 286 32, 32	52, 286 32, 32				
FLVD1517	40x40				52, 286 40, 32			
FFVB1760	42.5x42.5		52, 650 32, 16	52, 650 32, 16				
FLVB1760	42.5x42.5				52, 650 36, 16			
FFVA2104	47.5x47.5		52, 780 28, 24	52, 780 28, 24				
FLVA2104	47.5x47.5				52, 780 28, 24			
FFVB2104	47.5x47.5		52, 650 32, 32	52, 650 32, 32				
FLVB2104	47.5x47.5				52, 650 40, 36			
FLGB2104	47.5x47.5					52, 650 40, 36	52, 650 40, 36	
FFVC2104	47.5x47.5			52, 364 32, 32				
FLVC2104	47.5x47.5				52, 364 40, 40			
FLGC2104	47.5x47.5					52, 364 52, 52	52, 364 52, 52	
FLGB2377	50x50							52, 1248 36, 0
FLGA2577	52.5x52.5						0, 448 60, 60	
FLGA2892	55x55							52, 1404 48, 0

Notes:

1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale architecture-based devices with the same sequence. The footprint compatible devices within this family are outlined. See the UltraScale Architecture Product Selection Guide for details on inter-family migration.

Virtex UltraScale+ FPGA Feature Summary

Table 8: **Virtex UltraScale+ FPGA Feature Summary**

	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P
Logic Cells	689,640	1,051,010	1,379,280	2,068,920	2,147,040	2,862,720
CLB Flip-Flops	788,160	1,201,154	1,576,320	2,364,480	2,453,760	3,271,680
CLB LUTs	394,080	600,577	788,160	1,182,240	1,226,880	1,635,840
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	34.8	46.4
Block RAM/FIFO w/ECC (36Kb each)	720	1,024	1,440	2,160	2,016	2,688
Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5
UltraRAM Blocks	320	470	640	960	1,152	1,536
UltraRAM (Mb)	90.0	132.2	180.0	270.0	324.0	432.0
CMTs (1 MMCM and 2 PLLs)	10	20	20	30	12	16
Max. HP I/O(1)	520	832	832	832	624	832
DSP Slices	2,280	3,474	4,560	6,840	8,928	11,904
System Monitor	1	2	2	3	3	4
GTY Transceivers 32.75Gb/s	40	80	80	120	96	128
PCIe Gen3 x16 and Gen4 x8	2	4	4	6	3	4
150G Interlaken	3	4	6	9	9	12
100G Ethernet w/RS-FEC	3	4	6	9	6	8

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.

Virtex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 9: **Virtex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P
		HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY	HP, GTY
FFVC1517	40x40	520, 40					
FLVF1924	45x45					624, 64	
FLVA2104	47.5x47.5		832, 52	832, 52	832, 52		
FHVA2104	52.5x52.5(4)						832, 52
FLVB2104	47.5x47.5		702, 76	702, 76	702, 76	624, 76	
FHVB2104	52.5x52.5(4)						702, 76
FLVC2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96	
FHVC2104	52.5x52.5(4)						416, 104
FLVA2577	52.5x52.5				448, 120	448, 96	448, 128

Notes:
1. Go to Ordering Information for package designation details.
2. All packages have 1.0mm ball pitch.
3. Packages with the same last letter and number sequence, e.g., A2104, are footprint compatible with all other UltraScale devices with the same sequence. The footprint compatible devices within this family are outlined.
4. These 52.5x52.5mm overhang packages have the same PCB ball footprint as the corresponding 47.5x47.5mm packages (i.e., the same last letter and number sequence) and are footprint compatible.

Zynq UltraScale+ MPSoC Feature Summary

Table 10: **Zynq UltraScale+ MPSoC Feature Summary**

	ZU2EG	ZU3EG	ZU4EV	ZU5EV	ZU6EG	ZU7EV	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Application Processing Unit	Quad ARM Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache										
Real-Time Processing Unit	Dual ARM Cortex-R5 MPCore with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM										
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3; External Quad-SPI; NAND; eMMC										
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters										
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.0; DisplayPort 1.2a; USB 3.0; SGMII										
Graphic Processing Unit	ARM Mali™-400 MP2; 64KB L2 Cache										
Video Codec	0	0	1	1	0	1	0	0	0	0	0
Logic Cells	82,656	123,480	153,720	204,960	375,557	403,200	479,640	522,480	597,240	740,955	914,760
CLB Flip-Flops	94,464	141,120	175,680	234,240	429,208	460,800	548,160	597,120	682,560	846,806	1,045,440
CLB LUTs	47,232	70,560	87,840	117,120	214,604	230,400	274,080	298,560	341,280	423,403	522,720
Distributed RAM (Mb)	1.3	1.8	2.7	3.6	6.9	6.2	8.8	8.9	11.0	7.8	9.6
Block RAM Blocks	150	216	128	144	714	312	912	600	744	796	984
Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
UltraRAM Blocks	0	0	48	64	0	96	0	80	112	102	128
UltraRAM (Mb)	0	0	14.0	18.0	0	27.0	0	22.5	31.5	28.7	36.0
DSP Slices	240	360	728	1,056	1,973	1,728	2,520	2,928	3,528	1,590	1,968
CMTs	3	3	4	4	4	8	4	8	4	11	11
Max. HP I/O(1)	156	156	208	208	208	416	208	416	208	572	572
Max. HD I/O(2)	96	96	96	96	120	96	120	120	120	96	96
System Monitor	2	2	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s(3)	0	0	16	16	24	24	24	32	24	44	44
GTY Transceivers 32.75Gb/s	0	0	0	0	0	0	0	16	0	28	28
PCIe Gen3 x16 and Gen4 x8	0	0	2	2	0	2	0	4	0	4	5
150G Interlaken	0	0	0	0	0	0	0	2	0	2	4
100G Ethernet w/ RS-FEC	0	0	0	0	0	0	0	1	0	2	4

Notes:
1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.
3. GTH transceivers in SB/SF/FB packages support data rates up to 12.5Gb/s.