Advanced mathematical strategies to speed up energy-efficient microelectronic device modeling

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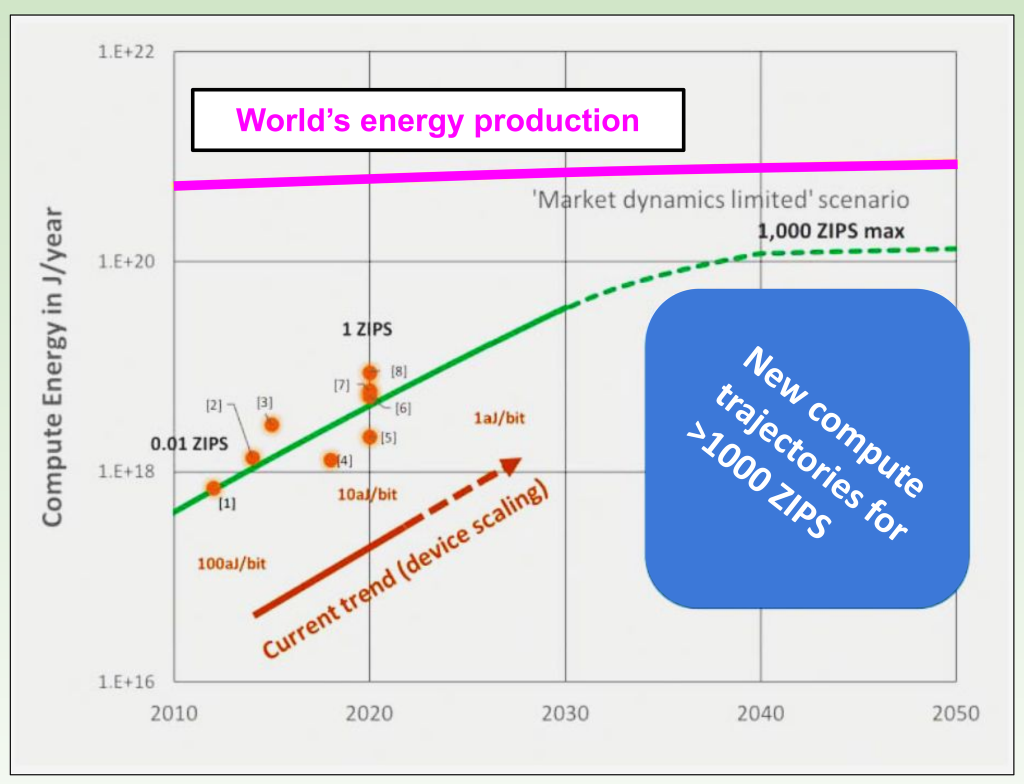
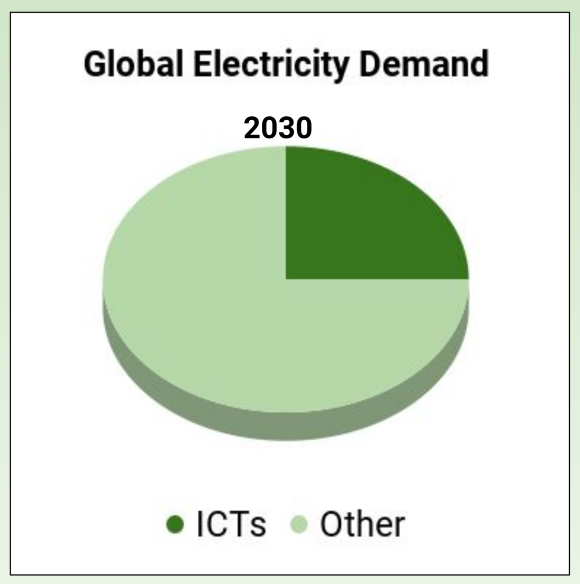
ABSTRACT

Ferroelectric-based transistors can exhibit negative capacitance, a property that allows for lower operating voltages. FerroX is a 3D simulation framework that enables investigation of the energy dynamics within ferroelectric heterostructures. FerroX performs differential-equation based calculations, and is *currently limited by inadequate time integration capabilities*. A successful implementation of the *SUite of Nonlinear and DIfferential/ALgebraic equation Solvers* (SUNDIALS) support doubled the time step length, and helps overcome this restriction.



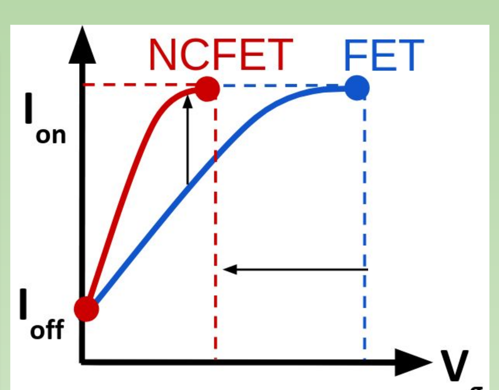
Energy inefficiency of computers is the limiting factor in future global computing capacity. Image credit: Semiconductor Research Corporation, Semiconductor Industry Association.

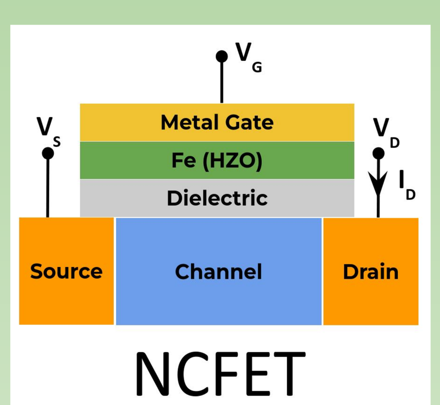


With the current structure of transistors, Information and Communication Technology (ICT) is predicted to account for nearly one quarter of all energy consumption by in 2030.

BACKGROUND

Microelectronic devices function due to the presence of billions of transistors. However, the operating voltage of modern transistors is *unsustainably high*.





Transistor structure shows the gate stack, semiconductor channel, source, and drain. Image credit: Kumar et al. 2024.

Negative Capacitance Field Effect Transistor (NCFET) requires lower voltage than Field Effect Transistor (FET) to overcome off-on threshold. Image credit: P. Kumar, CSA Postdoc Symposium 2023

$$\rho(\mathbf{r}) = e\left[n_p - n_e + N_d^+ - N_a^-\right]$$

Charge equation for the free charge density of semiconductor

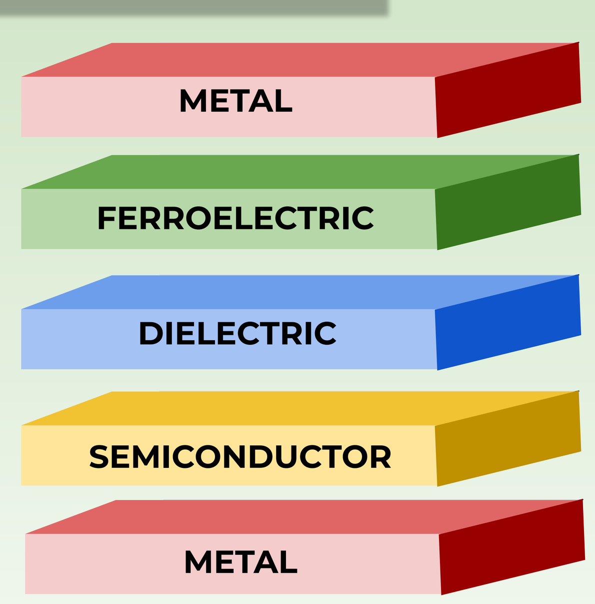
$$\frac{\partial \mathbf{P}(\mathbf{r},t)}{\partial t} = -\Gamma \frac{\delta F}{\delta \mathbf{P}(\mathbf{r},t)}$$

Time-Dependent Ginzburg-Landau equation for ferroelectric polarization

$$\nabla \cdot \varepsilon \nabla \Phi = \nabla \cdot \mathbf{P} - \rho$$

Poisson's equation for electric potential

Δt

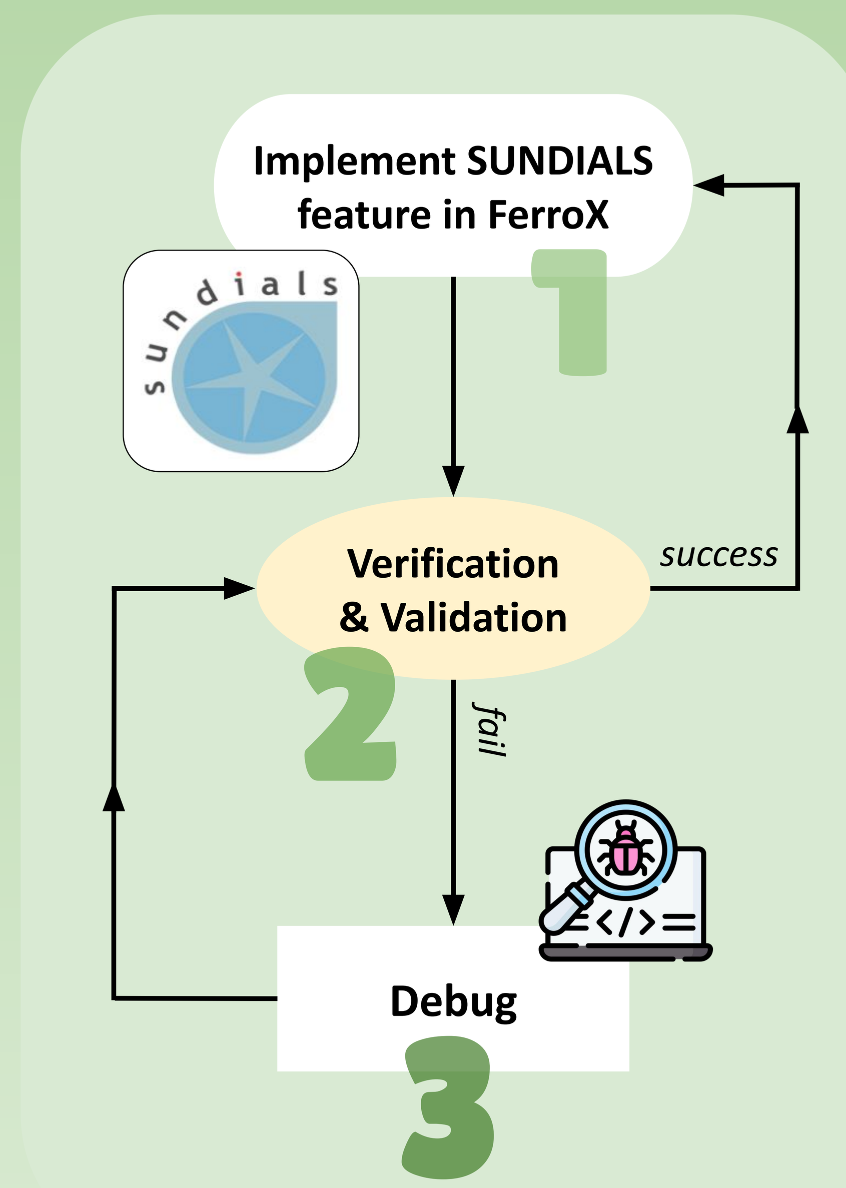


The scalable, massively parallel, 3D simulation program FerroX models the complex physical properties of multi-material stacks (illustrated above) by self-consistently solving coupled differential equations (left).

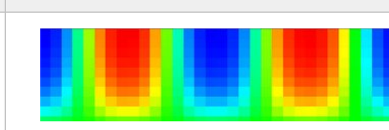
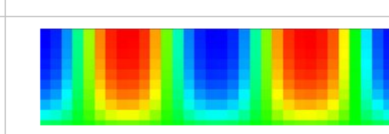
OUR QUESTION

How can we improve the performance and accuracy of FerroX to simulate ferroelectric-material-based microelectronic devices?

PROCEDURE



Establishing Baseline FerroX Performance

Internal FerroX Method	Max Supported Timestep	VisIt Output
First Order	4.0e-13	
Second Order	4.0e-13	

Data from stability testing to determine largest allowable time step length without the support of external math libraries. The right-most column depicts stable simulation output as visualized through the VisIt software.

Verification and Validation of SUNDIALS

Native Runge Kutta	Explicit Runge Kutta (ERK)	Order of Accuracy
Forward Euler	ARKODE_FORWARD_EULER_1_1	1.00
Trapezoid	ARKODE_HEUN_EULER_2_1_2	2.11
SSPRK3	ARKODE_ARK324L2SA_ERK_4_2_3*	3.05
RK4	ARKODE_ARK436L2SA_ERK_6_3_4*	4.07

The convergence rates for SUNDIALS ERK methods correspond to the order of accuracy of each respective Native Runge Kutta method, effectively validating the SUNDIALS implementation.

EXPLORING ADVANCED METHODS

Diagonally Implicit Runge Kutta (DIRK)	Time step	Runtime
ARKODE_IMPLICIT_TRAPEZOID_2_2	6.0e-13	~700 sec
ARKODE_BILLINGTON_3_3_2	9.0e-13	~630 sec
ARKODE_IMPLICIT_MIDPOINT_1_2	6.0e-13	~600 sec

SUNDIALS offers a different types of time integration methods. The table above shows a few examples of Diagonally Implicit Runge-Kutta (DIRK) methods with their maximum time step. We observe a doubling of the allowable time step.

CONCLUSIONS

Time Integration Method	Time step		
	Order	Stable	Unstable
Forward Euler	1	4.0e-13	5.0e-13
Trapezoid	2	4.0e-13	5.0e-13
SSPRK3	3	5.0e-13	6.0e-13
RK4	4	5.0e-13	6.0e-13
ARKODE_BILLINGTON_3_3_2	2	9.0e-13	10.0e-13

Having validated the SUNDIALS library implementation with convergence tests, we determined the maximum time step supported by several methods.

FUTURE STEPS

1. **Refactor source code**
2. **Implement multi-rate functions**
3. **Reduce simulation runtime**

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