

**JOMO KENYATTA UNIVERSITY OF AGRICULTURE AND TECHNOLOGY**

**SCHOOL OF COMPUTING**

**DEPARTMENT:** COLLEGE OF PURE AND APPLIED SCIENCE

**UNIT NAME:** COMPUTER ARCHITECTURE

**UNIT CODE:** BCT 2408

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**TASK:** LAB2

**Use the following code fragment:**

**loop:** **LD R1,0(R2)**

**DADDI R1,R1,1**

**SD 0(R2),R1**

**DADDI R2,R2,4**

**DSUB R4,R3,R2**

**BNEZ R4,loop**

**Assume that the initial value of R3 is R2+396. Throughout this exercise use the classic RISC five-stage integer pipeline in H&P. Specifically, assume that: 1) branches are resolved in the second stage of the pipeline; 2) there are separate instruction and data memories; 3) all memory accesses take 1 clock cycle.**

R3 = R2+396 loop runs 99 times (396/4 = 99 iterations)

Pipeline Assumptions:

1. 5-stage MIPS pipeline: IF, ID, EX, MEM, WB.
2. Branches resolved in ID stage (no dynamic prediction unless specified).
3. No forwarding/bypassing in part (a); forwarding in parts (b) and (c).
4. Register read/write in the same cycle forwards data.

**a. Show the timing of this instruction sequence for the RISC pipeline without any forwarding or bypassing hardware but assuming a register read and a write in the same clock cycle “forwards” through the register file. Assume that the branch is handled by flushing the pipeline. If all memory references take 1 cycle, how many cycles does this loop take to execute?**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Cycle** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** |
| LD | IF | ID | EX | MEM | WB |  |  |  |  |  |
| DADDI |  | IF | ID | STALL | EX | MEM |  |  |  |  |
| SD |  |  | IF | ID | STALL | EX | MEM | WB |  |  |
| DADDI |  |  |  | IF | ID | EX | MEM | WB |  |  |
| DSUB |  |  |  |  | IF | ID | STALL | EX | MEM | WB |
| BNEZ |  |  |  |  |  | IF | FLUSH | FLUSH | FLUSH | IF |

Total cycles:

* per iteration: 10 cycles
* Total (99 iterations): (99 10 = 990 cycles)

**b. Show the timing of this instruction sequence for the RISC pipeline with normal forwarding, and bypassing hardware. Assume that the branch is handled by predicting it as not taken. If all memory references take 1 cycle, how many cycles does this loop take to execute?**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Cycle** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| LD | IF | ID | EX | MEM | WB |  |  |  |  |
| DADDI |  | IF | ID | EX | MEM | WB |  |  |  |
| SD |  |  | IF | ID | EX | MEM | WB |  |  |
| DADDI |  |  |  | IF | ID | EX | MEM | WB |  |
| DSUB |  |  |  |  | IF | ID | EX | MEM | WB |
| BNEZ |  |  |  |  |  | IF | ID | FLUSH | IF |

Total cycles:

* per iteration: 8 cycles
* Total (99 iterations): (998 = 792 cycles)

**c. Assume the RISC pipeline with a single-cycle delayed branch and normal forwarding and bypassing hardware. Schedule the instructions in the loop including the branch delay slot. You may reorder instructions and modify the individual instructions operands, but do not undertake other loop transformations that change the number or opcode of the instructions in the loops. Show a pipeline timing diagram and compute the number of cycles needed to execute the entire loop.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Cycle** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| LD | IF | ID | EX | MEM | WB |  |  |
| DADDI |  | IF | ID | EX | MEM | WB |  |
| DADDI |  |  | IF | ID | EX | MEM | WB |
| SD |  |  |  | IF | ID | EX | MEM |
| DSUB |  |  |  |  | IF | ID | EX |
| BNEZ |  |  |  |  |  | IF | ID |

Total cycles:

* per iteration: 7 cycles
* Total (99 iterations): (997 = 693 cycles)