

**JOMO KENYATTA UNIVERSITY OF AGRICULTURE AND TECHNOLOGY**

**SCHOOL OF COMPUTING**

**DEPARTMENT:** COLLEGE OF PURE AND APPLIED SCIENCE

**UNIT NAME:** COMPUTER ARCHITECTURE

**UNIT CODE:** BCT 2408

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**TASK:** LAB4

**1. Assume we have a computer where the CPI is 1.0 when all memory accesses (including data and instruction accesses) hit in the cache. The cache is a unified (data + instruction) cache of size 256 KB, 4-way set associative, with a block size of 64 bytes. The data accesses (loads and stores) constitute 50% of the instructions. The unified cache has a miss penalty of 25 clock cycles and a miss rate of 2%. Assume 32-bit instruction and data addresses.**

**a. What is the tag size for the cache?**

Cache size:

Block size:

Number of blocks:

4-way set associative: Number of sets =

Address bits: 32 bits.

Offset bits:

Index bits:

Tag bits:

The tag size is 16 bits.

**b. How much faster would the computer be if all memory accesses were cache hits?**

Base CPI: 1.0 (all hits)  
Miss penalty: 25 cycles, miss rate 2%.  
Effective CPI:

Speedup:

The computer would be 1.5 times faster.

**2. You purchased an Acme computer with the following features:**

**• 95% of all memory accesses are found in the cache.**

**• Each cache block is two words, and the whole block is read on any miss.**

**• The processor sends references to its cache at the rate of 109 words per second.**

**• 25% of those references are writes.**

**• Assume that the memory system can support 109 words per second, reads or writes.**

**• The bus reads or writes a single word at a time (the memory system cannot read or write two words at once).**

**• Assume at any one time, 30% of the blocks in the cache have been modified.**

**• The cache uses write allocate on a write miss.**

**You are considering adding a peripheral to the system, and you want to know how much of the memory system bandwidth is already used. Calculate the percentage of memory system bandwidth used on the average in the two cases below. Be sure to state your assumptions.**

**a. The cache is write through.**

Read bandwidth:

Write bandwidth: Total bandwidth:

Percentage used:

28.75% of memory bandwidth is used.

**b. The cache is write back.**

Read bandwidth: same as above:

Write bandwidth:   
 Misses:

Dirty block evictions:

Total write bandwidth:

Total bandwidth:

Percentage used:

8% of memory bandwidth is used.

**3. One difference between a write-through cache and a write-back cache can be in the time it takes to write. During the first cycle, we detect whether a hit will occur, and during the second (assuming a hit) we actually write the data. Let’s assume that 50% of the blocks are dirty for a write-back cache. For this question, assume that the write buffer for the write through will never stall the CPU (no penalty). Assume a cache read hit takes 1 clock cycle, the cache miss penalty is 50 clock cycles, and a block write from the cache to main memory takes 50 clock cycles. Finally, assume the instruction cache miss rate is 0.5% and the data cache miss rate is 1%. Assuming that on average 26% and 9% of instructions in the workload are loads and stores, respectively, estimate the performance of a write-through cache with a two-cycle write versus a write-back cache with a two-cycle write.**

Write through cache:

Read stalls:

Write stalls:

Total CPI:

Write-back cache:

Read stalls: same as write-through: 0.38 cycles/instruction

Write stalls:  
 Hit:

Miss:

Dirty block write-back:

Total CPI:

Comparison: write-through (CPI=1.425) performs better than write-back (CPI = 1.5375 )