

**JOMO KENYATTA UNIVERSITY OF AGRICULTURE AND TECHNOLOGY**

**SCHOOL OF COMPUTING**

**DEPARTMENT:** COLLEGE OF PURE AND APPLIED SCIENCE

**UNIT NAME:** COMPUTER ARCHITECTURE

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**TASK:** LAB5

**Consider a computer system with a first-level data cache with the following characteristics: size: 16KBytes; associativity: direct-mapped; line size: 64Bytes; addressing: physical.**

**The system has a separate instruction cache and you can ignore instruction misses in this problem. This system is used to run the following code:**

**for (i=0; i<4096; i++)**

**X[i] = X[i] \* Y[i] + C**

**Assume that both X and Y have 4096 elements, each consisting of 4 bytes (single precision floating point). These arrays are allocated consecutively in physical memory. The assembly code generated by a naive compiler is the following:**

**loop: lw f2, 0(r1) # load X[i]**

**lw f4, 0(r2) # load Y[i]**

**multd f2, f2, f4 # perform the multiplication**

**addd f2, f2, f0 # add C (in f0)**

**sw 0(r1), f2 # store the new value of X[i]**

**addi r1, r1, 4 # update address of X**

**addi r2, r2, 4 # update address of Y**

**addi r3, r3, 1 # increment loop counter**

**bne r3, 4096, loop # branch back if not done**

**a. How many data cache misses will this code generate? Breakdown your answer into the three types of misses. What is the data cache miss rate?**

Cache parameters:

Size: 16KB, direct-mapped, line size: 64 bytes

Number of cache lines: 16KB/64B = 256 lines

Offset bits:

Index bits:

Tag bits:

Memory Access pattern:

Arrays X and Y each have 4096 elements of 4 bytes, allocated consecutively  
 Total size of X and Y:

Each iteration accesses X[i] (read+Write) and Y[i] (read)

Cache Behavior:

Compulsory Misses: First access to each cache line (64B line = 16 elements

For X and Y: misses each (total 512).

Capacity Misses: The working set (32KB) exceeds cache size (16KB), causing thrashing.

After filling half the cache, new lines evict old ones, leading to additional misses.

Total capacity misses: Approximately equal to compulsory misses (512).

Conflict Misses: Direct-mapped cache causes conflicts when X and Y lines map to the same index.

For every pair X[i] and Y[i], they may conflict, doubling misses.

Total conflict misses: Roughly equal to compulsory misses (512).

Total misses:  
 Compulsory: 512.

Capacity: 512.

Conflict: 512.

Total: 1536 misses.

Miss rate:

Total accesses:

Miss rate:

Answers:

* Compulsory misses: 512, capacity misses: 512, conflict misses: 512.
* Total misses: 1536.
* Miss rate: 12.5%.

**b. Provide a software solution that significantly reduces the number of data cache misses. How many data cache misses will your code generate? Breakdown the cache misses into the three types of misses. What is the data cache miss rate?**

Loop blocking (tiling).

Break the loop into smaller blocks that fit in the cache.

Example: Process 256 elements at a time (16KB / (3 arrays × 4B) ≈ 1365, but 256 is simpler).

Miss Reduction:

Compulsory misses: Same (512).

Capacity misses: Eliminated (working set fits in cache).

Conflict misses: Reduced (fewer conflicts due to smaller working set).

Total misses: ~512 (only compulsory).

Miss Rate:

Total accesses: 12288.

Miss rate:

**Answers**:

* Compulsory misses: 512, capacity misses: 0, conflict misses: 0.
* Total misses: 512.
* Miss rate: ~4.17%.

**c. Provide a hardware solution that significantly reduces the number of data cache misses. You are free to alter the cache organization and/or the processor. How many data cache misses will your code generate? Breakdown the cache misses into the three types of misses. What is the data cache miss rate?**

Solution:

Increase associativity (e.g., 4-way set-associative).

Reduces conflict misses by allowing more flexible placement.

Miss Reduction:

Compulsory misses: Same (512).

Capacity misses: Same (512, working set still exceeds cache size).

Conflict misses: Eliminated (no thrashing due to associativity).

Total misses: 1024.

Miss Rate:

Total accesses: 12288.

Miss rate:

**Answer**:

* Compulsory misses: 512, capacity misses: 512, conflict misses: 0.
* Total misses: 1024.
* Miss rate: ~8.33%.